

Description

The **SiT9501** is a differential MEMS oscillator that is engineered for low-jitter applications requiring standard networking frequencies from 25 MHz to 644.53125 MHz.

A unique FlexSwing™ output-driver performs like LVPECL but provides independent control of voltage swing and DC offset to simplify interfacing with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. The device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT9501 can be factory programmed for specific combinations of frequency, stability, voltage, output signaling, and pin 1 functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The wide frequency range and programmability makes this device ideal for communications, enterprise, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to [Manufacturing Notes](#) for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- 14 Standard networking frequencies from 25 MHz to 644.53125 MHz
- 70 fs RMS typical phase jitter, 12 kHz to 20 MHz
- Excellent power-supply noise rejection
- LVPECL, LVDS, HCSL, Low-power HCSL, and FlexSwing signaling options
- ±20, ±25, ±30, and ±50 ppm frequency stabilities
- Wide temperature support up to -40°C to 105°C
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous range power supply voltage
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm package ([Contact SiTime](#) for 7 x 5, and 5 x 3.2 mm x mm packages)

Applications

- 400G/800G network equipment
- Optical modules
- Coherent optics
- Network switches, routers
- Industrial networking equipment

Block Diagram

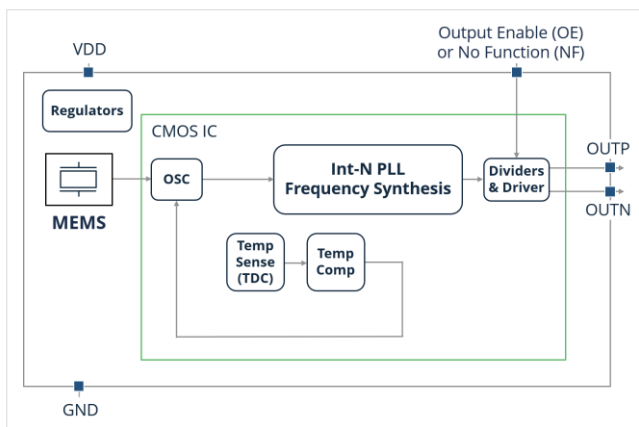


Figure 1. SiT9501 Block Diagram

Package Pinout

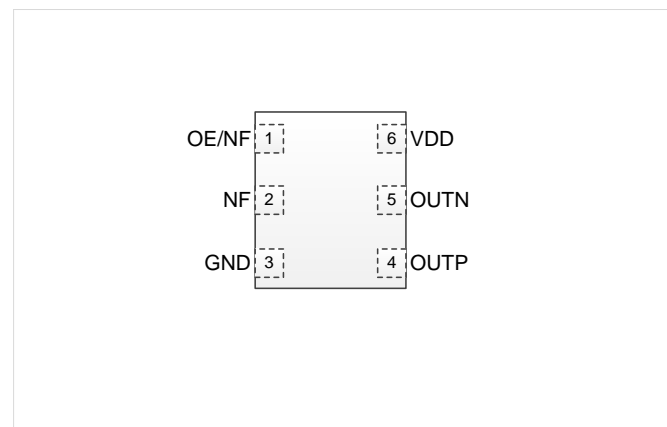


Figure 2. Pin Assignments (Top view)
(Refer to [Table 18](#) for Pin Descriptions)

Typical Phase Jitter (70 fs RMS) and Phase Noise Data

Table 1. Phase Noise for 3.3 V 156.25 MHz LVPECL Device at 25°C

Offset Frequency (Hz)	Phase Noise (dBc/Hz)
100	-87
1k	-114
10k	-141
100k	-151
1M	-152
10M	-165
40M	-170

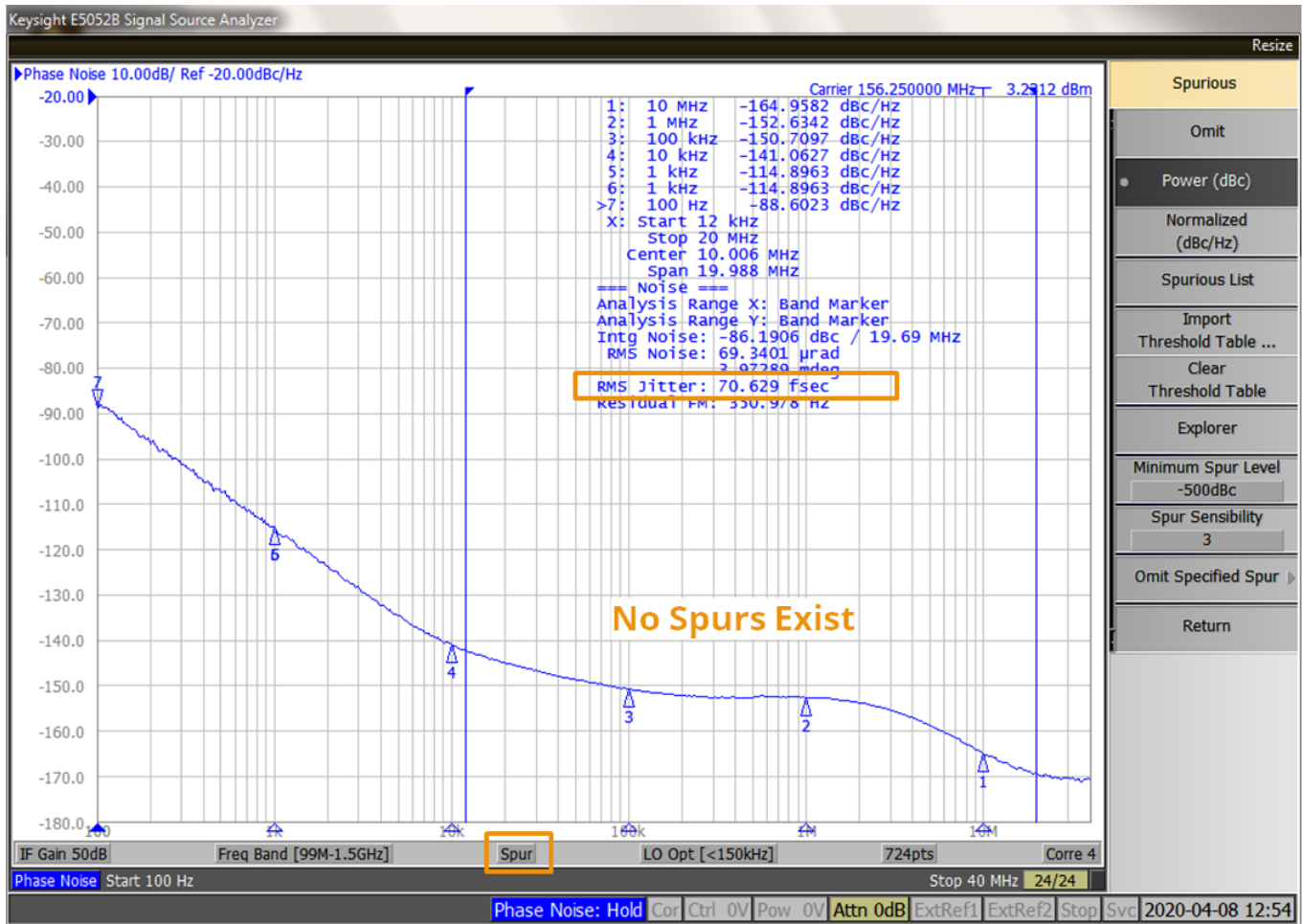


Figure 3. Phase Noise Plot of 3.3 V 156.25 MHz LVPECL Device at 25°C

Ordering Information

SiT9501AC-01B2-3310-125.000000T

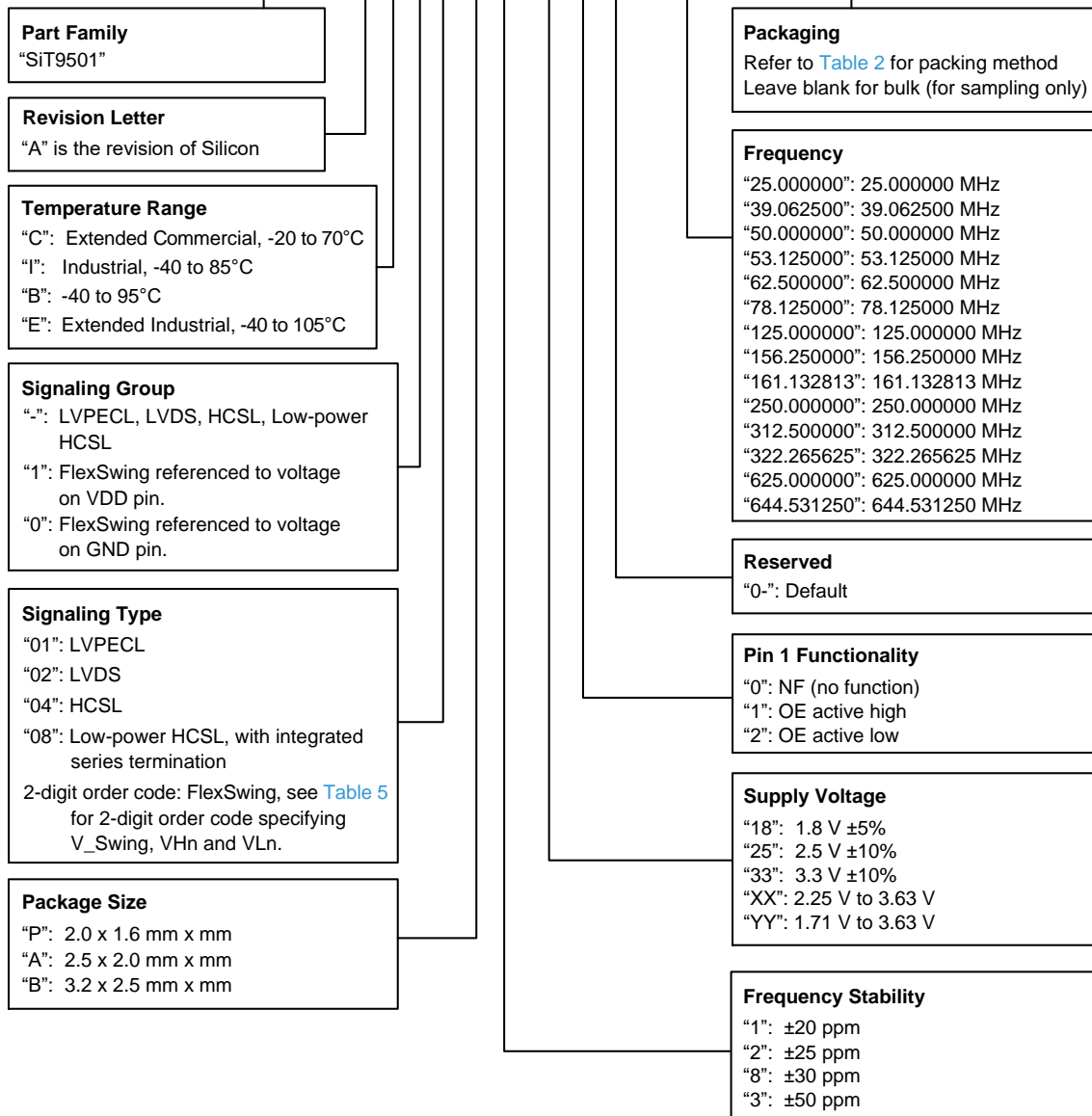


Table 2. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)
2.0 x 1.6	D	E	G
2.5 x 2.0	D	E	G
3.2 x 2.5	D	E	G

TABLE OF CONTENTS

Description 1

Features 1

Applications 1

Block Diagram 1

Package Pinout 1

Typical Phase Jitter (70 fs RMS) and Phase Noise Data 2

Ordering Information 3

Electrical Characteristics 5

Pin Description 14

FlexSwing Configurations 15

Waveform Diagrams 17

Termination Diagrams 20

 LVPECL and FlexSwing Termination 20

 LVDS, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 21

 HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 21

 Low-power HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 21

Dimensions and Patterns — 2.0 x 1.6 mm x mm 22

Dimensions and Patterns — 2.5 x 2.0 mm x mm 23

Dimensions and Patterns — 3.2 x 2.5 mm x mm 24

Additional Information 25

Revision History 25

Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 3. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	Standard frequencies			MHz	Refer to frequencies listed in Ordering Information section.
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and 10 years aging at 25°C
		–	–	±25	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and first year aging at 25°C
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±1	–	ppm	Ambient temperature of 25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code "YY"
		2.25	–	3.63	V	Voltage-supply order code "XX"
		1.71	1.80	1.89	V	Voltage-supply order code "18". Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code "25"
		2.97	3.30	3.63	V	Voltage-supply order code "33"
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Voltage Low	VIL	–	–	30%	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Pull-up Impedance	Z_in	–	100	–	kΩ	Pins 1 and 2 for OE and SE, respectively
Output Characteristics						
Duty Cycle	DC	45	–	55	%	See Figure 6 and Figure 8
Startup, OE and SE Timing						
Startup Time	T_start	–	1	5	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time	T_oe	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of swing. See Figure 13
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 14
Jitter and Phase Noise, f = 156.25 MHz						
RMS Phase Jitter (random)	T_phj	–	70	100	fs	12 kHz to 20 MHz offset frequency integration bandwidth
Spurious Phase Noise	T_spn	–	-110	–	dBc	12 kHz to 20 MHz offset frequency range
RMS Period Jitter^[1]	T_jitt_per	–	1	–	ps	
Peak Cycle-to-cycle Jitter^[1]	T_jitt_cc	–	6	–	ps	

Note:

1. Measured according to JESD65B.

Table 4. Electrical Characteristics – LVPECL | Supply voltage (“order code”): 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	34	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	47	–	mA	Including load termination current as shown in Figure 18 for Vdd = 3.3 V \pm 10%, Vdd = 2.25 V to 3.63 V and R3 = 220 Ohms.
		–	45.5	–	mA	Including load termination current as shown in Figure 18 for Vdd = 2.5 V \pm 10% and R3 = 220 Ohms.
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	62	–	mA	Including load termination current. See Figure 19 for termination
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	56	–	mA	Including load termination current as shown in Figure 18 for Vdd = 3.3 V \pm 10%, Vdd = 2.25 V to 3.63 V and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
		–	54.5	–	mA	Including load termination current as shown in Figure 18 for Vdd = 2.5 V \pm 10% and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	71	–	mA	Including load termination current. See Figure 19 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.025	Vdd-0.95	Vdd-0.88	V	See Figure 5
Output Low Voltage	VOL	Vdd-1.81	Vdd-1.7	Vdd-1.62	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.2	1.5	1.9	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 5. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to VDD only: 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	34	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	41.5	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 18 for Vdd = 3.3 V \pm 10%, Vdd = 2.25 V to 3.63 V, and R3 = 220 Ohms.
		–	40	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 18 for Vdd = 2.5 V \pm 10%, and R3 = 220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	50.5	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 18 for Vdd = 3.3 V \pm 10%, Vdd = 2.25 V to 3.63 V, and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
		–	49	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 18 for Vdd = 2.5 V \pm 10%, and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 5 , Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values.
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 5 , Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 6
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ⁽²⁾	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 6. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 1.8 V \pm 5% (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	34	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 18 for Vdd = 1.8 V \pm 5% and R3 = 220 Ohms.
		–	44	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 18 for Vdd = 1.71 V to 3.63 V and R3 = 220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	53	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 18 for Vdd = 1.8 V \pm 5% and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
		–	53	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 18 for Vdd = 1.71 V to 3.63 V and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 5 , Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 5 , Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 6
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 7. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	34	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44	–	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 18 for Vdd = 3.3 V \pm 10% and R3 = 220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	53	–	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 18 for Vdd = 3.3 V \pm 10% and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 5 , Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 5 , Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 6
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 8. Electrical Characteristics – LVDS | Supply voltage (“order code”): 2.5 V ±10% (“25”), 3.3 V ±10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	36	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	40	–	mA	Including load termination current. See Figure 22 for termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	49	–	mA	Including load termination current. See Figure 22 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 7
Delta VOD	ΔVOD	–	–	50	mV	See Figure 7
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 7
Delta VOS	ΔVOS	–	–	50	mV	See Figure 7
Rise/Fall Time	Tr, Tf	–	290	–	ps	Measured 20% to 80% using Figure 22 for termination. See Figure 8
Differential Asymmetry, peak-peak	V_da	–	50	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of VOD; see Figure 12
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 9. Electrical Characteristics – LVDS | Supply voltage (“order code”): 1.8 V ±5% (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	36	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	40	–	mA	Including load termination current. See Figure 21 and Figure 22 for termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	49	–	mA	Including load termination current. See Figure 21 and Figure 22 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 7
Delta VOD	ΔVOD	–	–	50	mV	See Figure 7
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 7
Delta VOS	ΔVOS	–	–	50	mV	See Figure 7
Rise/Fall Time	Tr, Tf	–	290	–	ps	Measured 20% to 80% using Figure 22 for termination. See Figure 8
Differential Asymmetry, peak-peak	V_da	–	50	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of VOD; see Figure 12
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 10. Electrical Characteristics – HCSL | Supply voltage (“order code”): 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	47	–	mA	Including load termination current. See Figure 23 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	55	–	mA	Including load termination current. See Figure 23 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 5
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1	1.4	1.6	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	400	–	ps	Measured 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 11. Electrical Characteristics – HCSL | Supply voltage (“order code”): 1.8 V \pm 5% (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	47	–	mA	Including load termination current. See Figure 23 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	55	–	mA	Including load termination current. See Figure 23 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 5
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1	1.4	1.6	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	400	–	ps	Measured 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 12. Electrical Characteristics – Low Power HCSL | Supply voltage (“order code”): 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	35	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	37	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 24 for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	39	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 24 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 5
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.55	1.65	1.9	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	520	–	ps	Measured 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	550	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 30	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 13. Electrical Characteristics – Low Power HCSL | Supply voltage (“order code”): 1.8 V \pm 5% (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	35	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	37	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 24 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	39	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 24 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 5
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.55	1.65	1.9	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	520	–	ps	Measured 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	550	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	\pm 30	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Note:

- Terminology chosen for clarity; referred to historically as power-supply noise rejection (PSNR).

Table 14. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		–	260	°C

Table 15. Thermal Considerations^[3]

Package	θ_{JA} , 4 Layer Board (°C/W)	θ_{JC} , Bottom (°C/W)
3225, 6-pin	TBD	TBD

Notes:

3. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 16. Maximum Operating Junction Temperature^[4]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	TBD
85°C	TBD
95°C	TBD
105°C	TBD

Notes:

4. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 17. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Pin Description

Table 18. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H ^[5] Specified frequency output L: OOTP (OUTN) held at logic high (low)
		No Function (NF)	H or L or Open: No effect on output frequency or other device functions.
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions
3	GND	Power	VDD Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage ^[6]

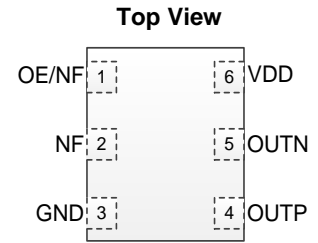


Figure 4. Pin Assignments

Notes:

- 5. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noise environments, OE pin that is active high or active low are recommended to include an external pull-up or pull-down resistor, respectively, of 10 kΩ when the pin is not externally driven.
- 6. A capacitor of value 0.1 μF or higher between VDD and GND pins is required.

FlexSwing Configurations

A FlexSwing output-driver performs like LVPECL but provides independent control of voltage swing and DC offset voltage levels. This simplifies interfacing with chipsets having non-standard input voltage requirements

and can eliminate all external source-bias resistors. FlexSwing supports power supply voltages from 1.71 V to 3.63 V, and the programmable VOH and VOL levels may be referenced to the voltage on either VDD or GND pins.

Table 19. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on VDD pin

Order Code V_Swing (V)	VLn																													
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X								
Vdd-2.32V										AJ	AK	AL	AM	AN	AP	AQ	AR	AS	AT	AU	AV	AW	AX							
Vdd-2.27V										1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85							
Vdd-2.22V									BH	BJ	BK	BL	BM	BN	BP	BQ	BR	BS	BT	BU	BV	BW	BX							
Vdd-2.17V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76							
Vdd-2.12V									CG	CH	CJ	CK	CL	CM	CN	CP	CQ	CR	CS	CT	CU	CV	CW	CX						
Vdd-2.07V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.68							
Vdd-2.02V									DF	DG	DH	DJ	DK	DL	DM	DN	DP	DQ	DR	DS	DT	DU	DV	DW	DX					
Vdd-1.97V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.59						
Vdd-1.92V									EE	EF	EG	EH	EJ	EK	EL	EM	EN	EP	EQ	ER	ES	ET	EU	EV	EW	EX				
Vdd-1.87V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.59	0.51					
Vdd-1.82V									FE	FF	FG	FH	FJ	FK	FL	FM	FN	FP	FQ	FR	FS	FT	FU	FV	FX					
Vdd-1.78V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.42				
Vdd-1.73V									GC	GD	GE	GF	GG	GH	GJ	GK	GL	GM	GN	GP	GQ	GR	GS	GT	GU	GV	GW	GX		
Vdd-1.68V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34		
Vdd-1.63V									HB	HC	HD	HE	HF	HG	HJ	HK	HL	HM	HN	HP	HQ	HR	HS	HT	HU	HV	HW	HX		
Vdd-1.58V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25	
Vdd-1.53V									JA	JB	JC	JD	JE	JF	JG	JH	JJ	JK	JL	JM	JN	JP	JQ	JR	JS	JT	JU	JV	JW	
Vdd-1.48V									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25	
Vdd-1.43V									KA	KB	KC	KE	KF	KG	KH	KJ	KK	KL	KM	KN	KP	KQ	KR	KS	KT	KU	KV			
Vdd-1.38V									1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25		
Vdd-1.33V									LA	LB	LC	LD	LE	LF	LG	LH	LJ	LK	LL	LM	LN	LP	LQ	LR	LS	LT	LU			
Vdd-1.28V									1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25			
									MA	MB	MC	MD	ME	MF	MG	MH	MJ	MK	ML	MM	MN	MP	MQ	MR	MS	MT				
									1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25				
									NA	NB	NC	ND	NE	NF	NG	NH	NJ	NK	NL	NM	NN	NP	NQ	NR	NS					
									1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25					
									PA	PB	PC	PD	PE	PF	PG	PH	PJ	PK	PL	PM	PN	PP	PQ	PR						
									1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25						
									QA	QB	QC	QD	QE	QF	QG	QH	QJ	QK	QL	QM	QN	QP	QQ							
									1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25							
									RA	RB	RC	RD	RE	RF	RG	RH	RJ	RK	RL	RM	RN	RP								
									1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25								
									SA	SB	SC	SD	SE	SF	SG	SH	SJ	SK	SL	SM	SN									
									1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25									
									TA	TB	TC	TD	TE	TF	TG	TH	TJ	TK	TL	TM										
									1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25										
									UA	UB	UC	UD	UE	UF	UG	UH	UJ	UK	UL											
									1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25											
									VA	VB	VC	VD	VE	VF	VG	VH	VJ	VK												
									1.01	0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25												
									WA	WB	WC	WD	WE	WF	WG	WH	WJ													
									0.93	0.85	0.76	0.68	0.59	0.51	0.42	0.34	0.25													

Supply Voltage	Available Colors
1.8V±5%	Not Supported
1.71V to 3.63V	Not Supported
2.5V±10%	Blue
3.3V±10%	Blue Red
2.25V to 3.63V	Blue

The above table identifies supported combinations of nominal VOH (i.e. VHn) and nominal VOL (i.e. VLn) in colored boxes. The two-character code in each box corresponds to the VHn and VLn codes specified in the 2nd column and 2nd row in the table, respectively. The number in each box indicates the nominal differential swing or 2(VHn – VLn).

X = 0.95 V, we obtain X = 1.55 V, whose closest match is 1.53 V, or column “S” in Table 19. The differential swing in Row D (i.e. 1.01 Vpp) is the closest match to V_Swing = 1 Vpp. Thus, the FlexSwing order code is “DS”. The value for VHn may be computed as VLn + V_Swing/2 = 0.95 V + (1.01 Vpp)/2 = 1.455 V. The common mode voltage is VLn + V_Swing/4 = 0.97 V + 1.01V/4 = 1.2225 V.

Example 1 – Suppose a design requires a differential swing (V_Swing) of 1 Vpp with a common-mode voltage of Vdd-1.3 V. If VDD is 2.5 V, and using Table 19, then VOL = Vdd – 1.3 V – (1 Vpp)/4 = 0.95 V. Solving for X in VLn = 2.5 V –

Waveform Diagrams

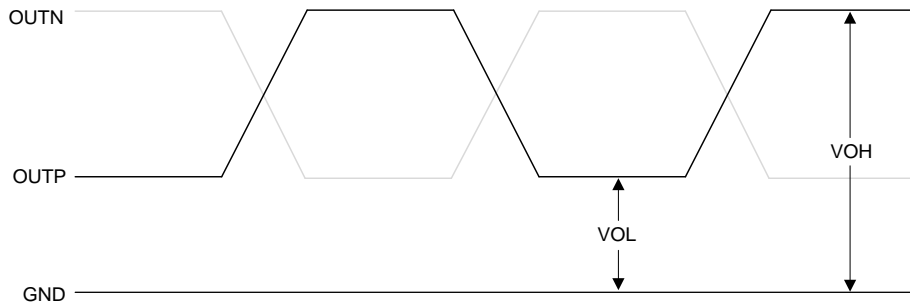


Figure 5. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

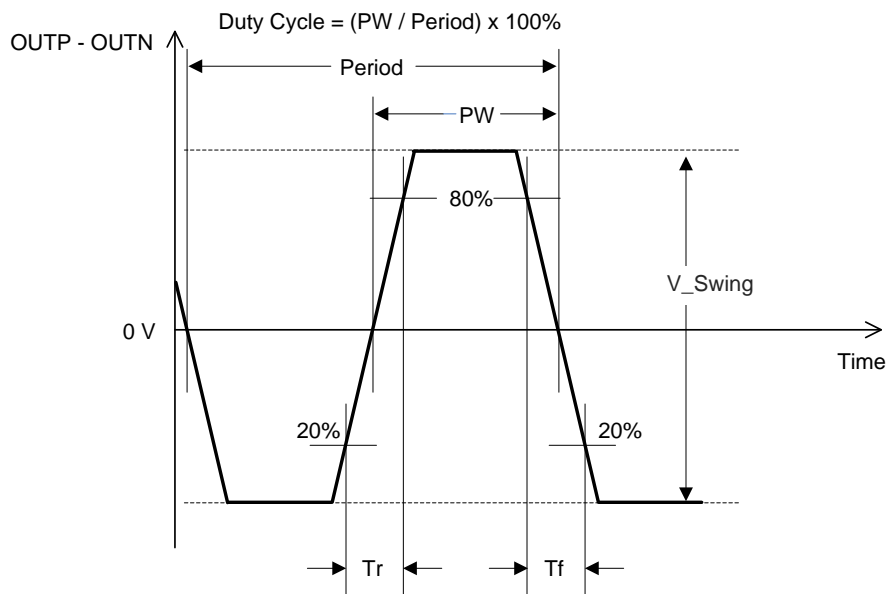


Figure 6. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

Waveform Diagrams (continued)

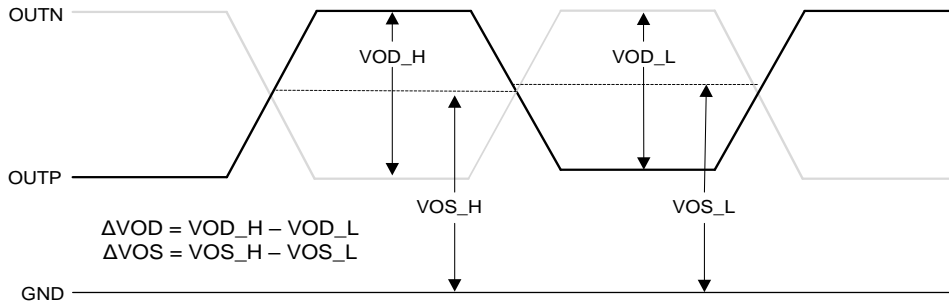


Figure 7. LVDS Voltage Levels per Differential Pin

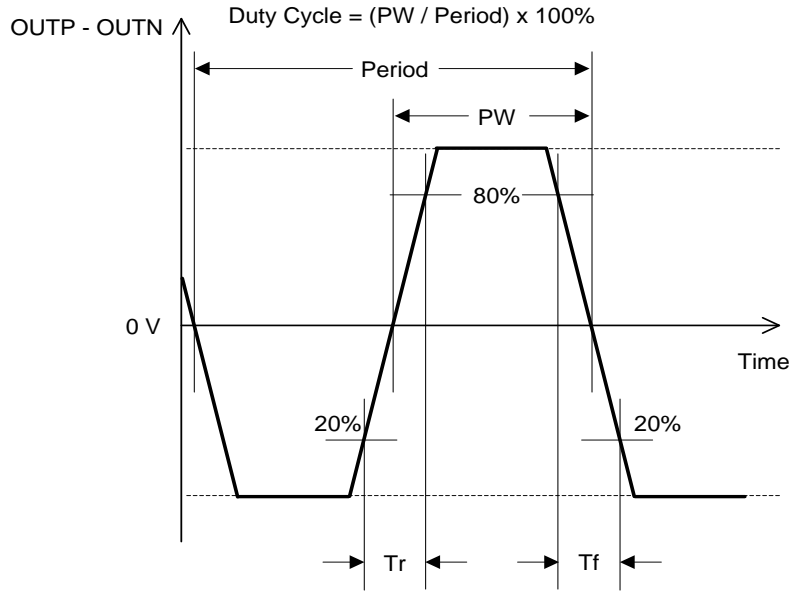


Figure 8. LVDS Differential Waveform

Waveform Diagrams (continued)

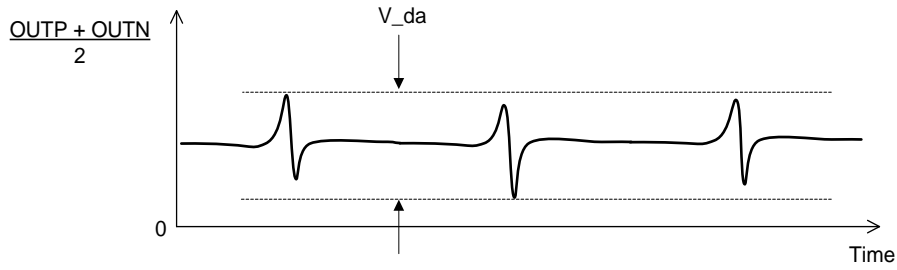


Figure 9. Differential Asymmetry (V_{da})

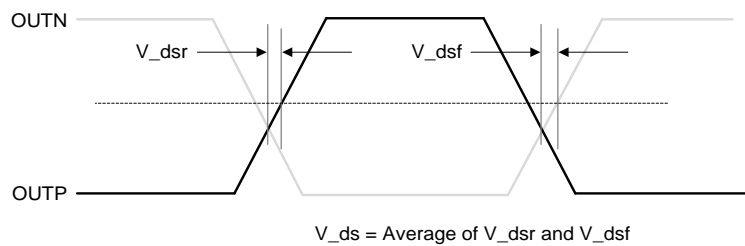


Figure 10. Differential Skew (V_{ds}) is measured as the Time between the Average Voltage Level and Crossing Voltage

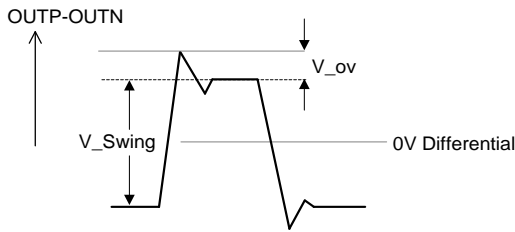


Figure 11. Overshoot Voltage (V_{ov}) for LVPECL, FlexSwing, HCSL, Low-power HCSL

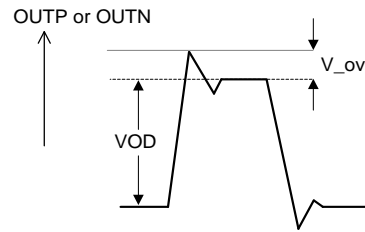


Figure 12. Overshoot Voltage (V_{ov}) for LVDS Output

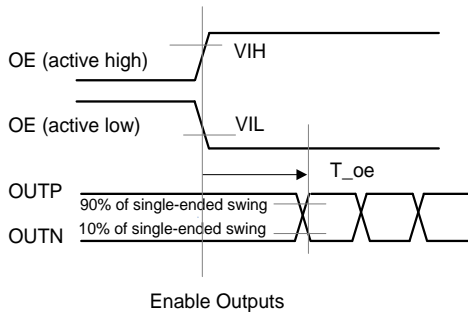


Figure 13. OE Pin Enable Timing (T_{oe})

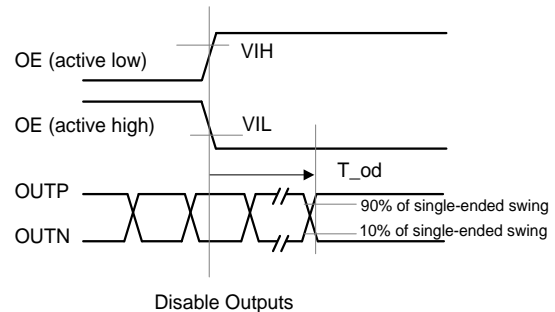


Figure 14. OE Pin Disable Timing (T_{od})

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9501 FlexSwing output drivers support low power without sacrificing signal integrity via simple terminations as shown in Figure 16 and Figure 18, compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are

voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_{load}) into the load termination.

Table 21. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage Order Codes	Termination Options					
		Figure 15	Figure 16	Figure 17	Figure 18	Figure 19	Figure 20
LVPECL referenced to Vdd	"25", "33", "XX"	OK to use $I_{load} = 40$ mA with 100Ω near-end bias resistor	Do Not Use	OK to use $I_{load} = 28$ mA	OK to use	OK to use $I_{load} = 28$ mA	Do Not Use
FlexSwing referenced to Vdd			OK to use (see Figure 16 for frequency ranges and voltage swings)	OK to use ⁷	OK to use	OK to use	Do Not Use
FlexSwing referenced to Gnd	"25", "33", "XX", "YY"	OK to use ⁷	OK to use (see Figure 16 for frequency ranges and voltage swings)	Do Not Use	OK to use	Do Not Use	Do Not Use
	"18"			Do Not Use	OK to use	Do Not Use	OK to use

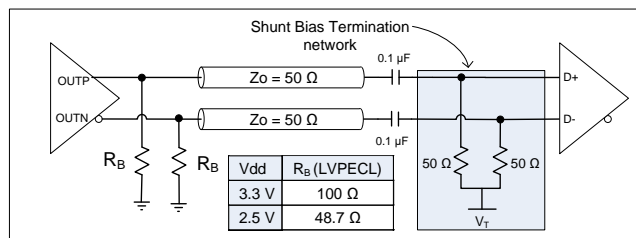


Figure 15. Recommended LVPECL and FlexSwing⁸ Termination when AC-coupled

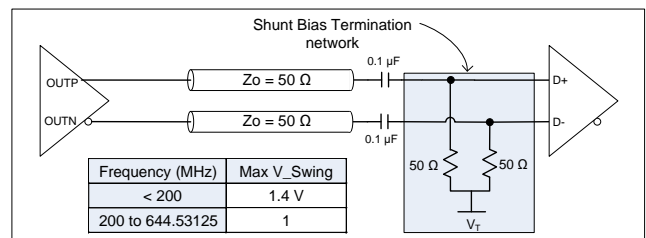


Figure 16. Recommended FlexSwing Termination when AC-coupled

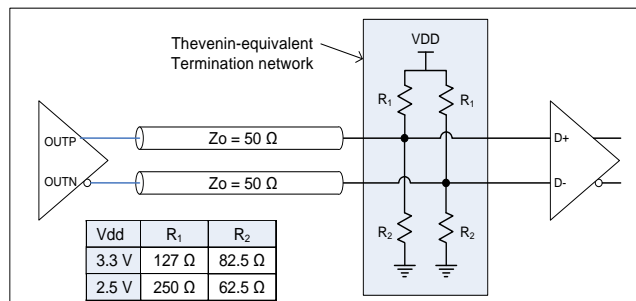


Figure 17. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network

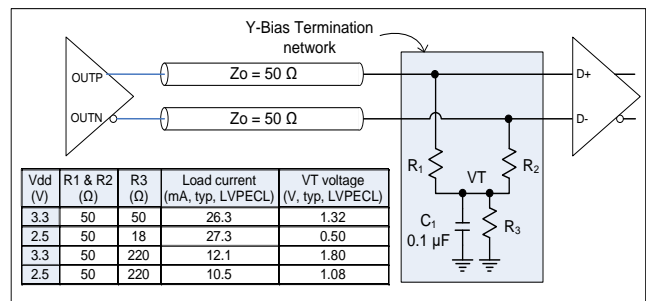


Figure 18. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

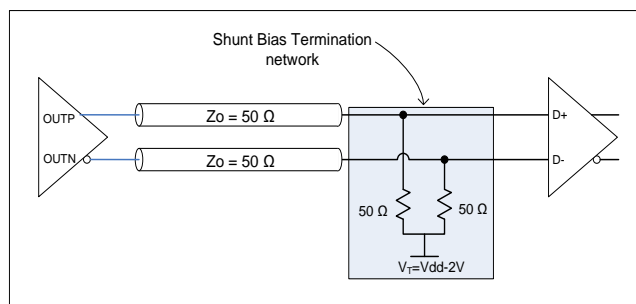


Figure 19. LVPECL and FlexSwing with Y-Bias Termination

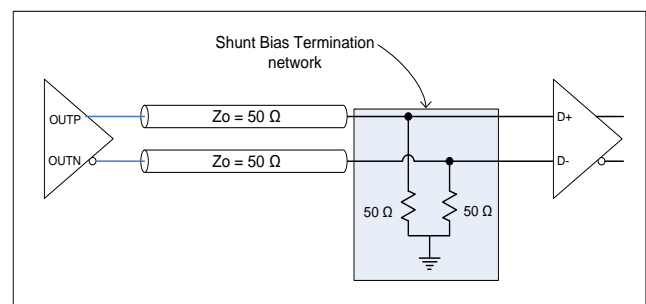


Figure 20. FlexSwing Termination - Only for use with Supply Voltage Order Code "18"

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

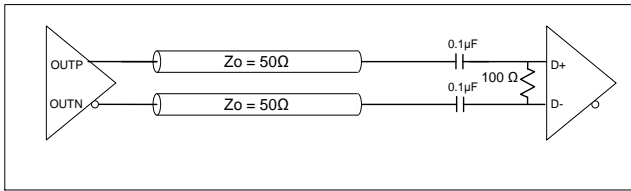


Figure 21. LVDS AC Termination

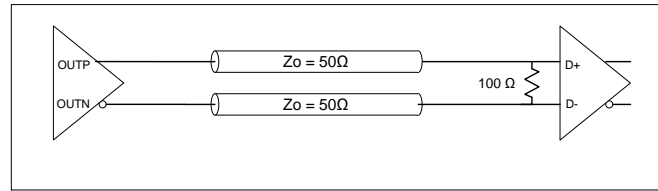


Figure 22. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

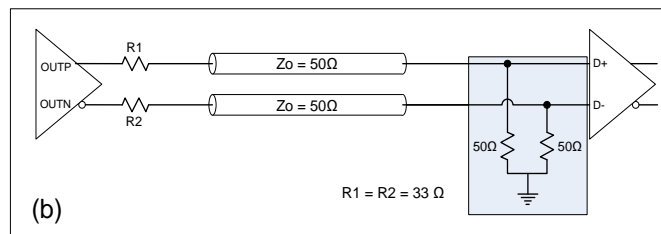
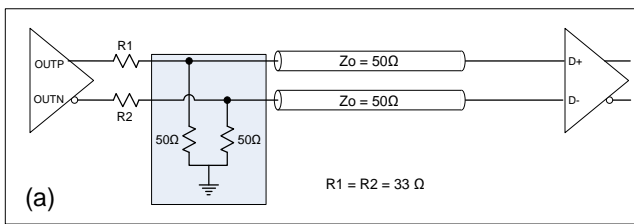


Figure 23. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

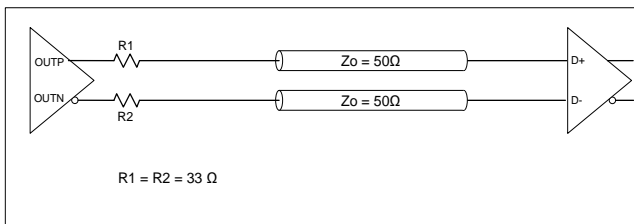


Figure 24. Low-power HCSL Termination

Notes:

- 7. Contact [SiTime](http://www.sitime.com) for optimum R1 and R2 values for FlexSwing options.
- 8. Contact [SiTime](http://www.sitime.com) for optimum Rs values for FlexSwing options.

Dimensions and Patterns — 2.0 x 1.6 mm x mm

Package Size – Dimensions (Unit: mm)^[9]

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.700	0.750	0.800
STAND OFF	A1	0.000	0.035	0.050
BODY SIZE	X	D		
	Y	E		
LEAD WIDTH	b	0.225	0.275	0.325
LEAD LENGTH	L	0.324 REF		
	L1	0.300	0.400	0.500
LEAD PITCH	e	0.730 BSC		
PACKAGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	bbb	0.100		
COPLANARITY	ccc	0.080		

NOTE

1. ALL DIMENSION IN MM

PKG INFO		DRAWING NO.	
6L PQFD		POD-077-PQFN-006-C02016	
2.000x1.600X0.750 mm		REV	SHEET
DATE	2020/6/1	A01	01

Recommended Land Pattern (Unit: mm)^[10]

Note : All units in mm.

PKG INFO		SPL DRAWING NO.	
6L PQFN		SPL-077-PQFN-006-C02016	
2.000x1.600 mm		REV	SHEET
DATE	2020/04/20	A00	01

Notes:

9. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
10. A capacitor of value 0.1 μ F or higher between VDD and GND is required.

Dimensions and Patterns — 2.5 x 2.0 mm x mm

Package Size – Dimensions (Unit: mm)^[9]

(TOP VIEW)

(BOTTOM VIEW)

(SIDE VIEW)

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.800	0.850	0.900
STAND OFF	A1	0.000	0.035	0.050
BODY SIZE	X	D		
	Y	E		
LEAD WIDTH	b	0.330	0.380	0.430
LEAD LENGTH	L	0.572 REF		
	L1	0.550	0.650	0.750
LEAD PITCH	e	0.900 BSC		
PACKAGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	bbb	0.100		
COPLANARITY	ccc	0.080		
HALF CUT WIDTH	R	0.075	---	---
HALF CUT DEPTH	A3	---	---	0.075
NOTE				
1. ALL DIMENSION IN MM				

SiTime			
PKG INFO		DRAWING NO.	
6L PQFD 2.500x2.000X0.850 mm		POD-078-PQFW-006-C02520	
		REV	SHEET
DATE	2020/6/1	A01	01

Recommended Land Pattern (Unit: mm)^[10]

Note : All units in mm.

SiTime	PKG INFO		SPL DRAWING NO.	
	6L PQFW 2.500x2.000 mm		SPL-078-PQFW-006-C02520	
DATE		REV	SHEET	
2020/04/20		A00	01	

Dimensions and Patterns — 3.2 x 2.5 mm x mm

Package Size – Dimensions (Unit: mm)^[9]

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.800	0.850	0.900
STAND OFF	A1	0.000	0.035	0.050
BODY SIZE	X	D		
	Y	E		
LEAD WIDTH	b	0.550	0.600	0.650
LEAD LENGTH	L	0.650	0.700	0.750
	L1	0.800 REF		
LEAD PITCH	e	1.100 BSC		
PACKAGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	bbb	0.100		
COPLANARITY	ccc	0.080		
DIMPLE WIDTH	T	0.150 REF		
DIMPLE LENGTH	P	0.150 REF		
DIMPLE DEPTH	A2	0.100 REF		
NOTE				
1. ALL DIMENSION IN MM				
PKG INFO		DRAWING NO.		
6L PQFD 3.200x2.500X0.850 mm		POD-076-PQFD-006-C03225		
		REV	SHEET	
DATE	2020/6/1	A02	01	

Recommended Land Pattern (Unit: mm)^[10]

Note : All units in mm.

	PKG INFO	SPL DRAWING NO.	
	6L PQFD 3.200x2.500 mm	SPL-076-PQFD-006-C03225	
DATE		REV	SHEET
2020/04/20		A01	01

Additional Information

Table 22. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	TBD

Revision History

Table 23. Revision History

Revision	Release Date	Change Summary
0.5	27-Apr-2020	Advanced datasheet
0.51	18-May-2020	Formatting changes Fixed typos Added 2016 and 2520 packages
0.52	1-Jun-2020	Formatting changes Updated package drawings
0.53	2-Aug-2020	Modified Termination Diagrams section
0.54	23-Sep-2020	Modified LVPECL, FlexSwing, LVDS current consumption specifications Modified phase jitter specification Added FlexSwing order codes Added 250u T&R order code Changed rev table date format
0.55	23-Oct-2020	Trademarks update Modified termination for HCSL and low-power HCSL rise/fall time specs
0.56	15-Dec-2020	Updated current consumption
0.57	5-Jan-2021	Updated FlexSwing Electrical Characteristics tables and description Formatting updates
0.58	23-Mar-2021	Pg 12 Note 11 update, Provide Flexswing use case example Updated hyperlinks; Changed date format

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | Phone: +1-408-328-4400 | Fax: +1-408-328-4439

© SiTime Corporation 2016-2021. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. Products sold by SiTime are not suitable or intended to be used in a life support application or component, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY

BUYER AGREES NOT TO USE SITIME'S PRODUCTS FOR ANY APPLICATION OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.

单击下面可查看定价，库存，交付和生命周期等信息

[>>SiTime\(赛特时脉\)](#)