
CH7025/CH7026 TV/VGA Encoder

Features

- TV encoder targets the handheld devices and other appropriate display devices used in consumer products. (i.e. automobile)
- Support multiple output formats. Such as SDTV format (NTSC and PAL), HDTV format for 480p,576p,720p and 1080i, analog RGB output for VGA. Sync signals can be provided in separated or composite manner (programmable composite sync generation).
- Three on-chip 10-bit high speed DACs providing flexible output capabilities. Such as single, double or triple CVBS outputs, YPbPr output, RGB output and simultaneous CVBS and S-video outputs.
- 16Mbits SDRAM is used as frame buffer. Supporting for frame rate conversion.
- Flexible up and down scaling engine is embedded including de-flickering capability.
- Programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supports various RGB (RGB888, RGB666, RGB565 and etc), YCbCr (4:4:4 YCbCr, ITU656) and 2x or 3x multiplexed input. CPU interface are also supported.
- Support for flexible input resolution up to 800x800 and 1024x680.
- Pixel by pixel brightness, contrast, hue and saturation adjustment for each kind of output is supported. (For RGB output, only brightness and contrast adjustment is supported).
- Pixel by pixel horizontal position adjustment and line by line vertical position adjustment are supported.
- 90/180/270 degree image rotation and vertical or horizontal flip functions are supported.
- Macrovision 7.1.L1 for SDTV is supported in CH7025. (CH7026 is Non-Macrovision part.)
- Macrovision™ copy protection support for progressive scan TV (480p, 576p CH7025 only)
- CGMS-A support for SDTV and HDTV
- TV/Monitor connection detect capability. DAC can be switched off based on detection result. (Driver support is required)
- Programmable power management.
- Flexible pixel clock frequency from graphics controller is supported. (2.3MHz –120MHz) Flexible input clock from crystal or oscillator is supported. (2.3MHz – 64MHz)
- Only slave mode supported.
- Offered in BGA or QFP package.
- Fully programmable through serial port.
- IO and SPC/SPD voltage supported is from 1.2V to 3.3V.

General Description

The CH7025/CH7026 is a device targeting handheld and similar systems which accept digital input signal, and encodes and transmits data through 10-bit DACs. The device is able to encode the video signals and generate synchronization signals SDTV format for NTSC and PAL standards and HDTV format for 480p,576p,720p and 1080i. Analog RGB output and composite SYNC signal are also supported. The device accepts different data formats including RGB and YCbCr (e.g. RGB565, RGB666, RGB888, ITU656 like YCbCr, etc.). 16Mbit SDRAM is embedded in package. Frame rate conversion and Image rotation are possible.

Note: the above feature list is subject to change without notice. Please contact Chrontel for more information and current updates.

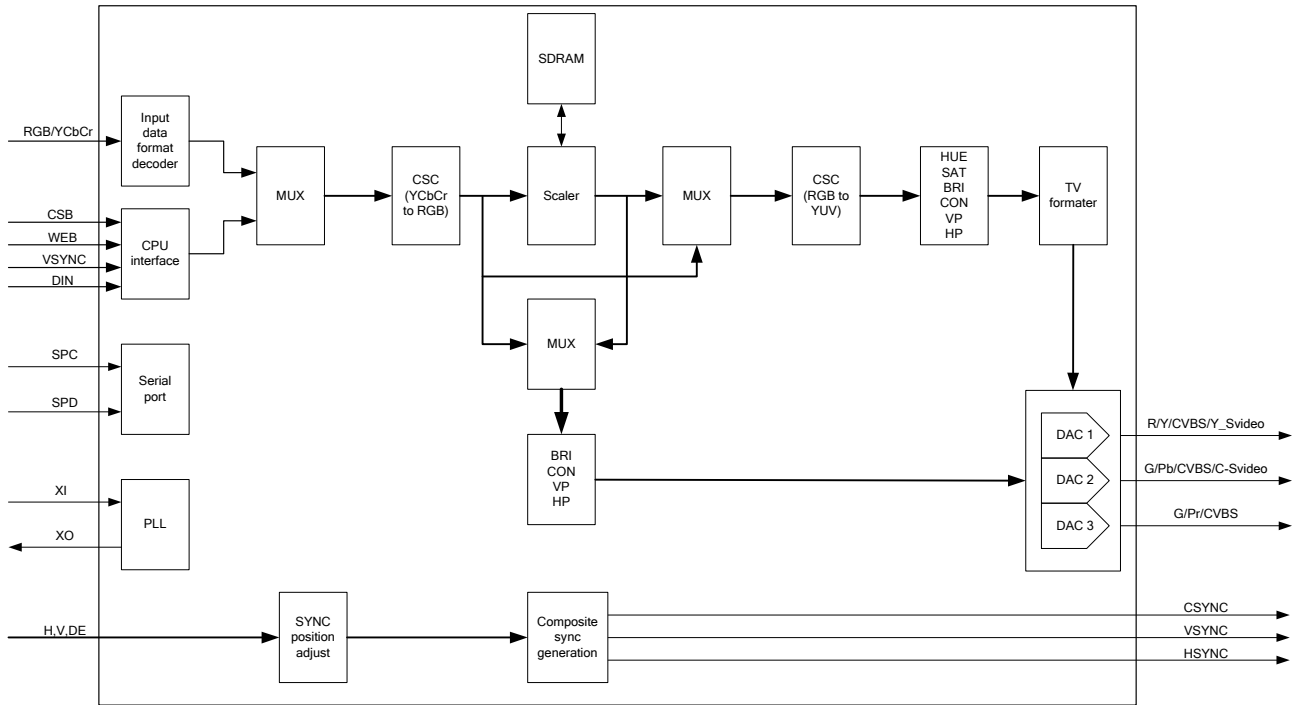


Figure 1: CH7025/CH7026 block diagram

1.0 Pin-out

1.1 Package Diagram

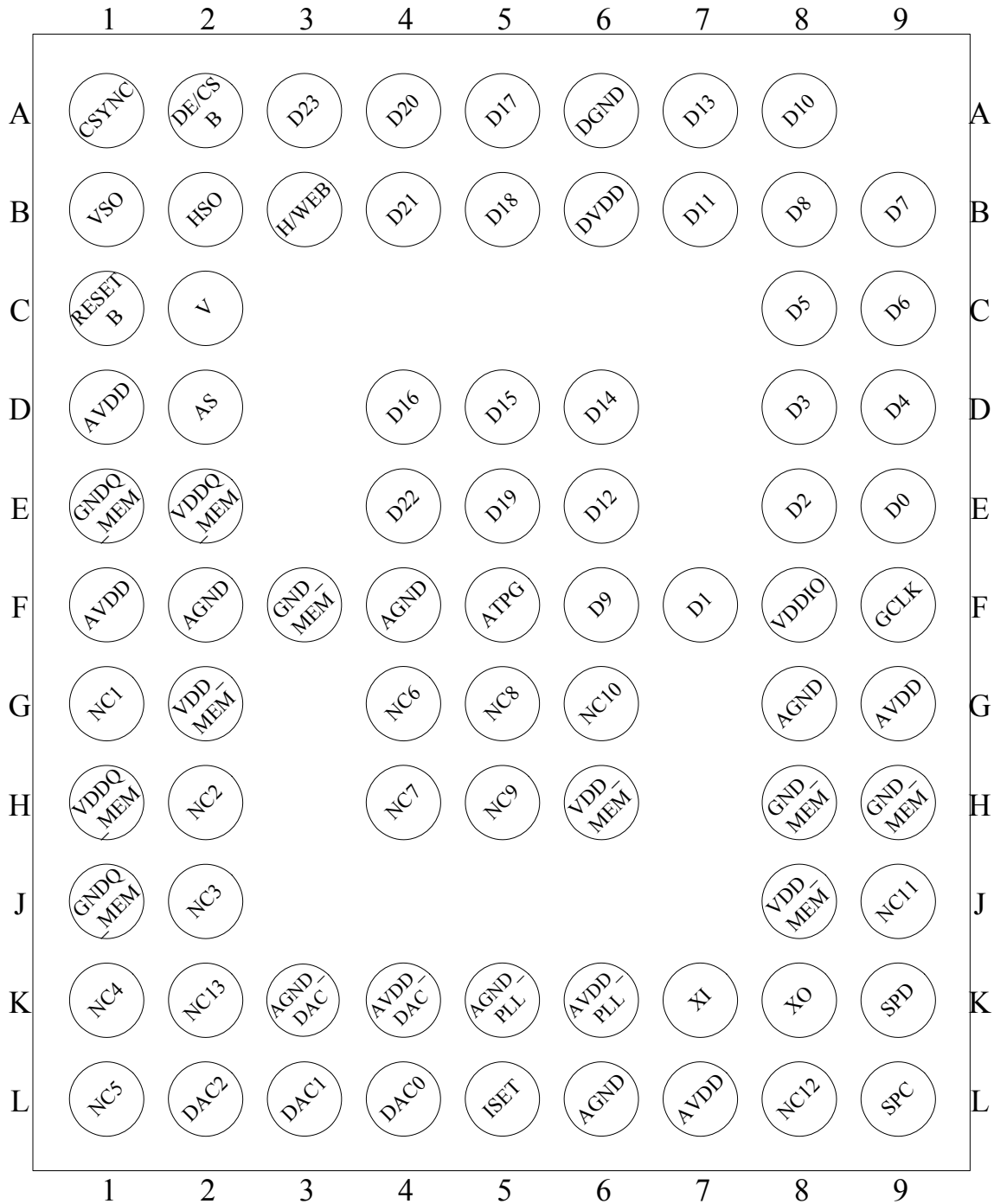


Figure 2: BGA Package

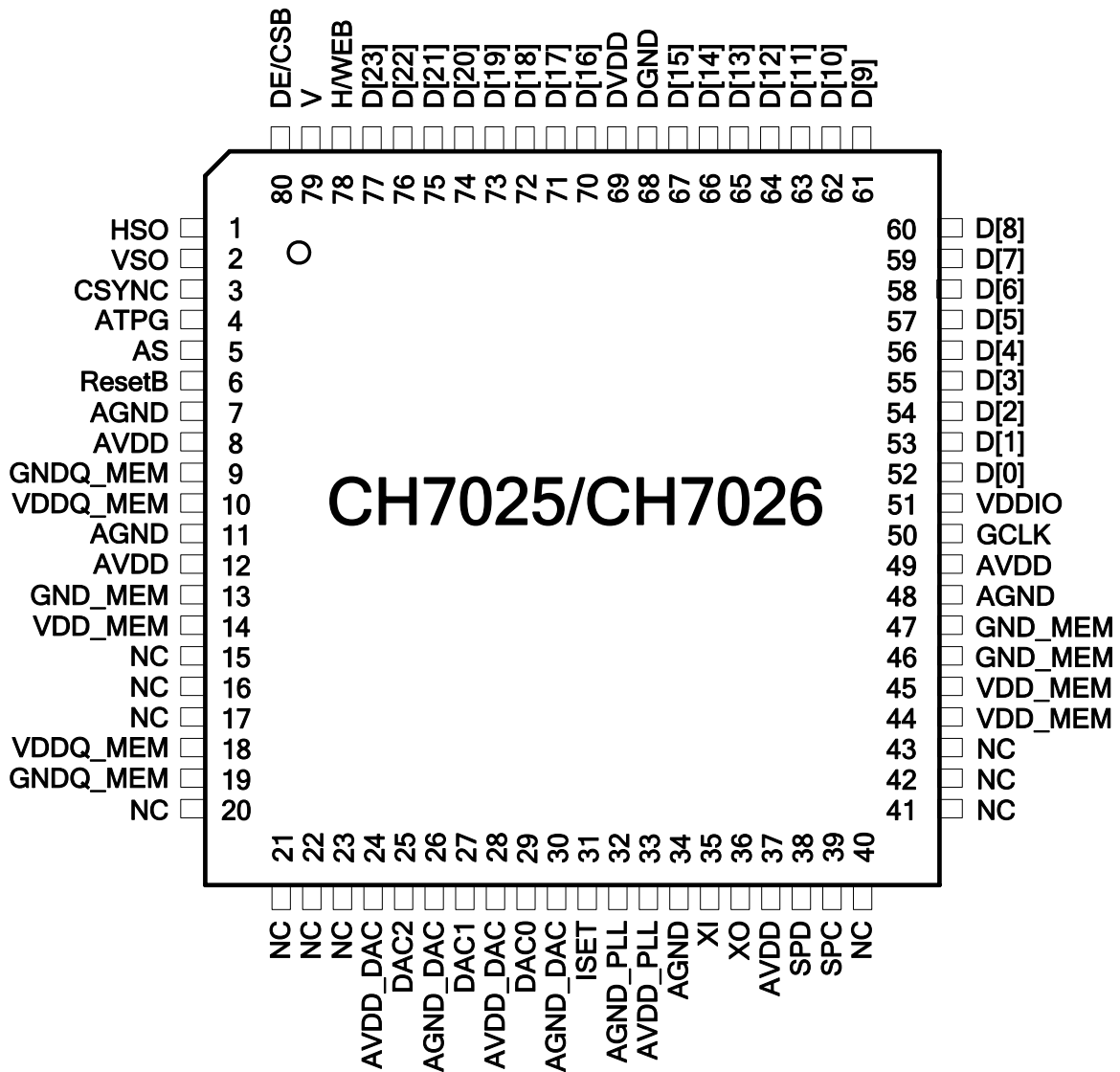


Figure 3: 80 Pin LQFP Package

1.2 Pin Description

Table 1: Pin Name Description (BGA Package)

Pin #	Type	Symbol	Description
A3, E4, B4, A4, E5, B5, A5, D4, D5, D6, A7, E6, B7, A8, F6, B8, B9, C9, C8, D9, D8, E8, F7, E9	In	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
C2	In/Out	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
B3	In/Out	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
A2	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also the CSB signal of CPU interface The amplitude will be 0 to VDDIO.
D2	In	AS	Address select
F5	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V.
C1	In	ResetB	Reset * Input When this pin is low, the device is held in the hardware reset condition. When this pin is high, reset is controlled through the serial port.
K9	In/Out	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resistor is required.
L9	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resistor is required.

Pin #	Type	Symbol	Description
L4	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
L3	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
L2	Out	DAC2	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
L5	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k Ω , 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
K7	In	XI	Crystal Input / External Input For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
K8	Out	XO	Crystal Output For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
F9	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
B1	Out	VSO	Vertical sync signal output
B2	Out	HSO	Horizontal sync signal output
A1	Out	CSYNC	Composite sync output
F8	Power	VDDIO	IO supply voltage (1.2-3.3V)
B6	Power	DVDD	Digital supply voltage (1.8V)
D1, F1, L7, G9	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
K6	Power	AVDD_PLL	PLL supply voltage (1.8V)
K4	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
E2, H1	Power	VDDQ_MEM	SDRAM output buffer supply voltage (2.5V)
G2, J8, H6	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
A6	Power	DGND	Digital supply ground
F4, F2, L6, G8	Power	AGND	Analog supply ground
K5	Power	AGND_PLL	PLL supply ground
K3	Power	AGND_DAC	DAC supply ground
E1, J1	Power	GNDQ_MEM	SDRAM output buffer supply ground
F3, H9, H8	Power	GND_MEM	SDRAM device supply ground

Table 2: Pin Name Descriptions (LQFP80 Package)

Pin #	Type	Symbol	Description
52 - 67 70 - 77	In	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
79	In/Out	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
78	In/Out	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
80	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. CSB signal input of CPU interface The amplitude will be 0 to VDDIO.
5	In	AS	Chip address select 0: 76h 1: 75h
4	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V.
6	In	ResetB	Reset * Input When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
38	In/Out	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resistor is required.
39	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resistor is required.
29	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
27	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
25	Out	DAC2	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
31	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k Ω , 1% tolerance resistor should

Pin #	Type	Symbol	Description
			be connected between this pin and AGND_DAC using short and wide traces.
35	In	XI	Crystal Input / External Input For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
36	Out	XO	Crystal Output For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
50	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
2	Out	VSO	Vertical sync signal output, The amplitude of this pin is from 0 to AVDD
1	Out	HSO	Horizontal sync signal output, The amplitude of this pin is from 0 to AVDD
3	Out	CSYNC	Composite sync output, The amplitude of this pin is from 0 to AVDD
51	Power	VDDIO	IO supply voltage (1.2 – 3.3V)
69	Power	DVDD	Digital supply voltage (1.8V)
8, 12 37, 49	Power	AVDD	Analog supply voltage(2.5 – 3.3V)
33	Power	AVDD_PLL	PLL supply voltage(1.8V)
24, 28	Power	AVDD_DAC	DAC power supply(2.5 – 3.3V)
10 18	Power	VDDQ_MEM	SDRAM output buffer supply voltage(2.5V)
14, 44 45	Power	VDD_MEM	SDRAM device supply voltage(2.5V)
68	Power	DGND	Digital supply ground
7, 11, 34 48	Power	AGND	Analog supply ground
32	Power	AGND_PLL	PLL supply ground
26, 30	Power	AGND_DAC	DAC supply ground
9, 19	Power	GNDQ_MEM	SDRAM output buffer supply ground
13, 46, 47	Power	GND_MEM	SDRAM device supply ground

2.0 Package Dimensions

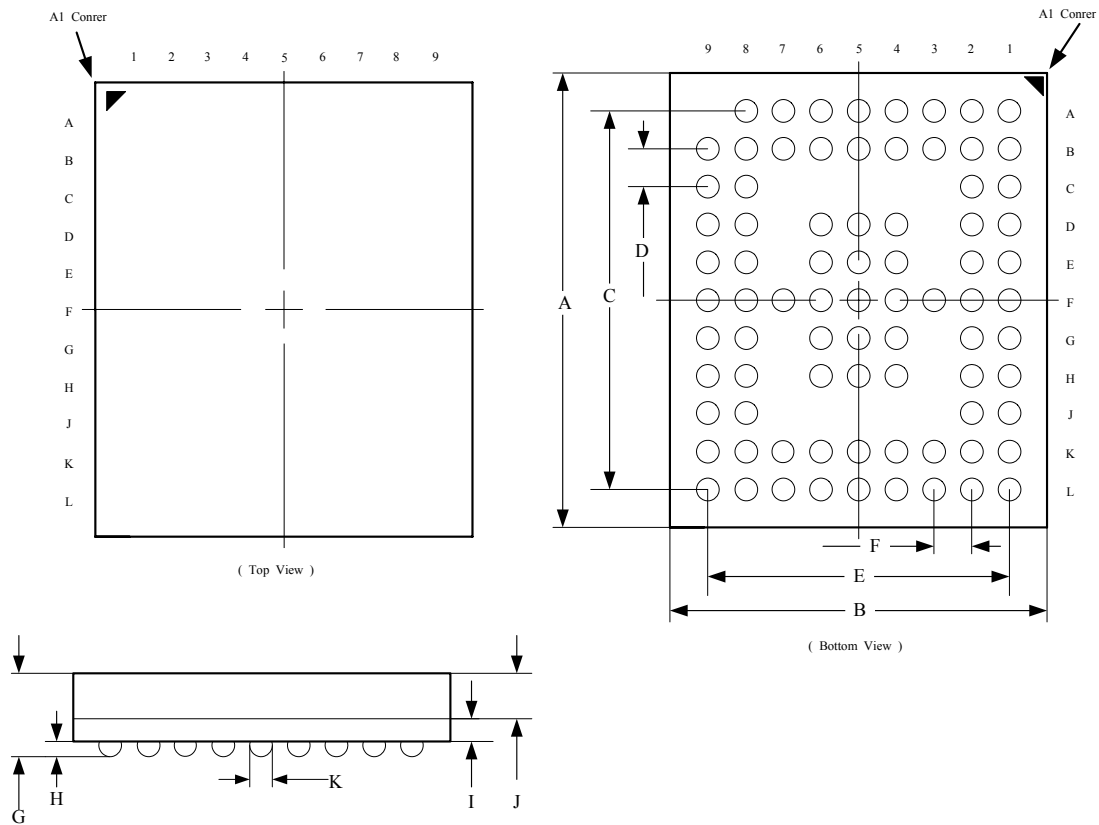


Figure 4: 80 Pin BGA Package

Table of Dimensions

No. of Leads		SYMBOL										
80 (5 X 6 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli- meters	Min	6.00	5.00	5.00	0.50	4.00	0.50		0.22	0.30	0.60	0.30
	Max							1.20	0.30			

Notes:

- All dimensions conform to JEDEC standard MO-216.

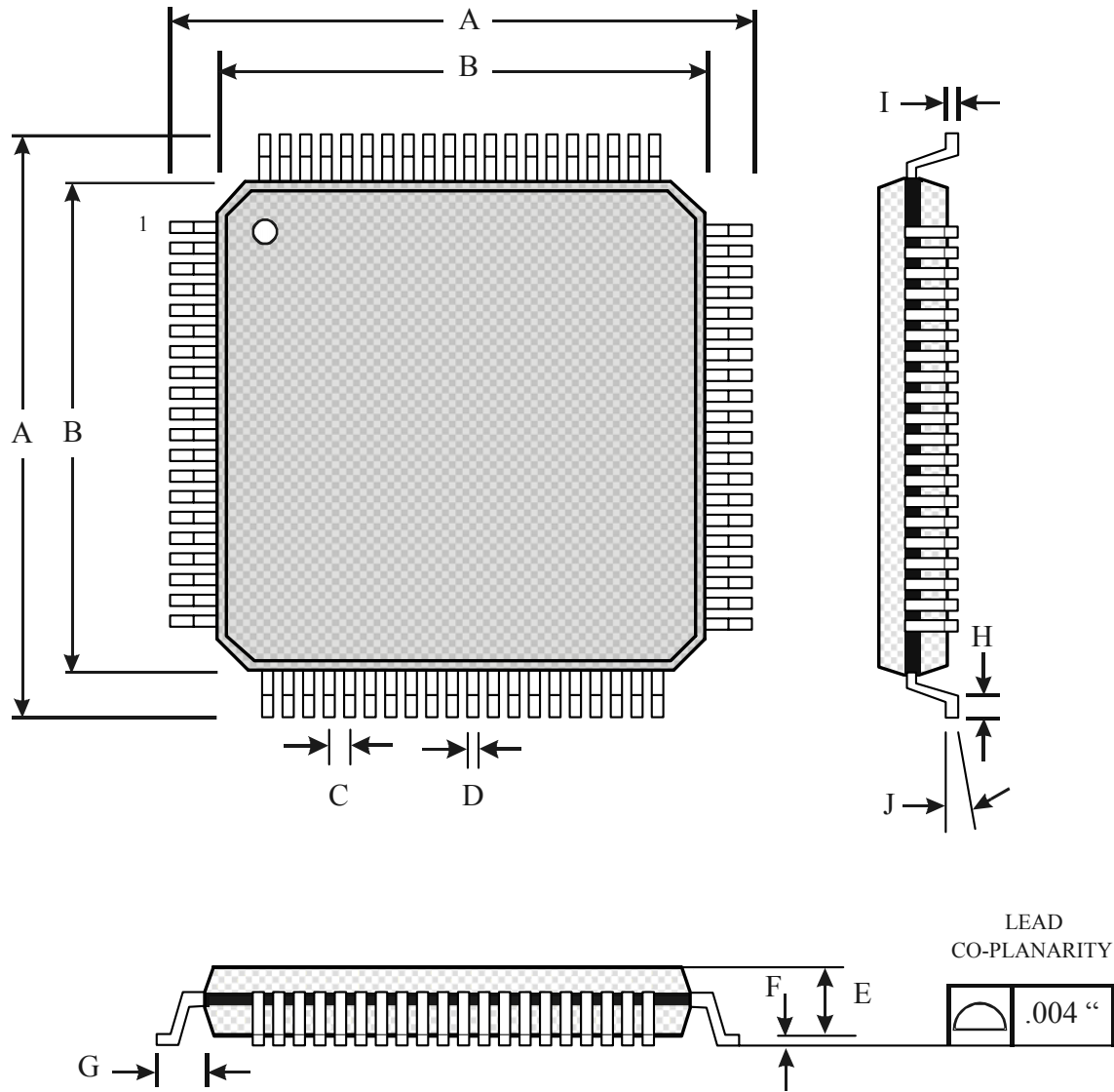


Figure 5: 80 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
80 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	11.90	9.90	0.40	0.13	1.35	0.05	1.00	0.45	0.09	0°
	MAX	12.10	10.10		0.23	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

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ORDERING INFORMATION			
Part Number	Package Type	Copy Protection	Operating Temperature Range
CH7025B-GF	80TFBGA, Lead-free	Macrovision™	Commercial : -20 to 70°C
CH7025B-GFI	80TFBGA, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7025B-TF	80LQFP, Lead-free	Macrovision™	Commercial : -20 to 70°C
CH7025B-TFI	80LQFP, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7026B-GF	80TFBGA, Lead-free	None	Commercial : -20 to 70°C
CH7026B-GFI	80TFBGA, Lead-free	None	Industrial : -40 to 85°C
CH7026B-TF	80LQFP, Lead-free	None	Commercial : -20 to 70°C
CH7026B-TFI	80LQFP, Lead-free	None	Industrial : -40 to 85°C

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