Synaptics®

ADVANCING THE HUMAN INTERFACE

VMM5320 Datasheet

DisplayPort 1.4 Multi-Stream Hub Controller

PN: 505-000736-01 Rev 4

Introduction

VMM5320 is a VESA DisplayPort™ v1.4/v1.1a, HDMI™ v2.0b/v1.4b, DVI and VESA DDM standard compliant multi-stream hub controller. All members of the VMM5000 family include one DP v1.4 input port and support multiple video/audio streams. VMM5320 has one HDMI output port and two DP1.4 output ports.

After initialization, VMM5320 will detect downstream monitors, retrieve those monitors' EDID, and alert the upstream device. When the upstream device is DisplayPort v1.4 MST capable, it will see all the monitors connected to VMM5320. When the upstream device is DisplayPort v1.1a capable, VMM5320 can enable the patented ViewXpand™ technology and present an aggregated EDID, allowing all downstream monitors to act as a single large display.

All of the VMM5xxx product family DP and HDMI ports are protected with the highest security built-in circuitry fully compliant with the industry standard HDCP v2.2.

Features and benefits

- Standards compliance/support: DisplayPort™ v1.4, DisplayPort™ v1.1a, HDMI™ Standard v2.0b, VESA DDM Standard, HDCP v2.2, DisplayID, and EDID v1.4
- VMM5320 supports 1 HDMI v2.0b output port, 2 DP1.4/DP++ output ports
- Supports dual 4k @ 60Hz/24bpp without compression
- Input interfaces
  - One receiver capable of DP1.4 operation
  - ViewXpand SST horizontal splitting
  - Hot Plug Detect (HPD)
  - HDCP v1.4/v2.2 compliant
  - EDID, MCCS support
  - Interlaced and 3D video
  - RGB, YCC444, YCC422, YCC420
  - 1-32 channels of LPCM audio including HBR audio rates
  - IEC 61937 compressed audio
  - 1.0V main-link operation
  - Manchester AUX (I^2C, Native)
  - 1, 2, or 4 lane configurations
  - 8.1, 5.4, 2.7, or 1.62 Gbps per lane
  - Forward Error Correction
  - SST or up to 12 stream MST
  - 6, 8, 10, 12 bpc video
  - 1280 Mpps max stream clock
  - Sideband messaging
  - DSC1.2 transport and up to 4-slice decompression
  - High Dynamic Range (HDR) video
- Output Interfaces
  - 1 HDMI Transmitter Port (Tx0) capable of HDMI2.0b/DVI mode operation
  - 2 DP++ Transmitter Ports (Tx1, Tx2)
- All output modes (DP/HDMI/DP++) features
  - Hot Plug Detect (HPD)
  - HDCP v2.2 compliant
  - EDID, MCCS support
  - High Dynamic Range (HDR) video
  - Interlaced and 3d video
  - RGB, YCC444, YCC422, YCC420
  - 1-32 channels of LPCM audio including HBR audio rates
  - IEC 61937 compressed audio
  - Internal video pattern generator

- DP output mode features
  - 1.0V main-link operation
  - Manchester AUX (I^2C, Native)
  - 1, 2, or 4 lane configurations
  - 8.1, 5.4, 2.7, or 1.62 Gbps per lane
  - Forward Error Correction
  - SST or up to 4 stream MST
  - 6, 8, 10, 12 bpc video
  - 1280 Mpps max stream clock
  - Sideband messaging
  - DSC1.2 compressed video transport
- HDMI/DP++ mode features
  - HDMI output ports are 3.3V, DP++ are 1.0V
  - HDMI 2.0b compliance
  - Single DVI output
  - 8, 10, 12 bit per pixel video
  - 600 Mpps max stream/TMDS clock
  - DDC inouts
- Dedicated I^2C slave for main processor to access the VMM5320
- Swappable input and output lanes for flexible PCB Layout
- Built-in 80251 MCU
- "Flash-over-AUX" capability enabling firmware upgradable in the field
- AC coupled for low voltage chipset operation
- 168 Pin BGA RoHS compliant green packages
- Halogen-free according to IEC 61249-2-21 definition

Applications

- PC/Laptop motherboard
- Laptop / Ultra book / Tablet dock
- DisplayPort multi video/audio stream hub
- DisplayPort to DP++ / HDMI / DVI active adapter / protocol converter
- Multi Monitor / Digital signage

Contents

Architecture

Functional Block Diagram

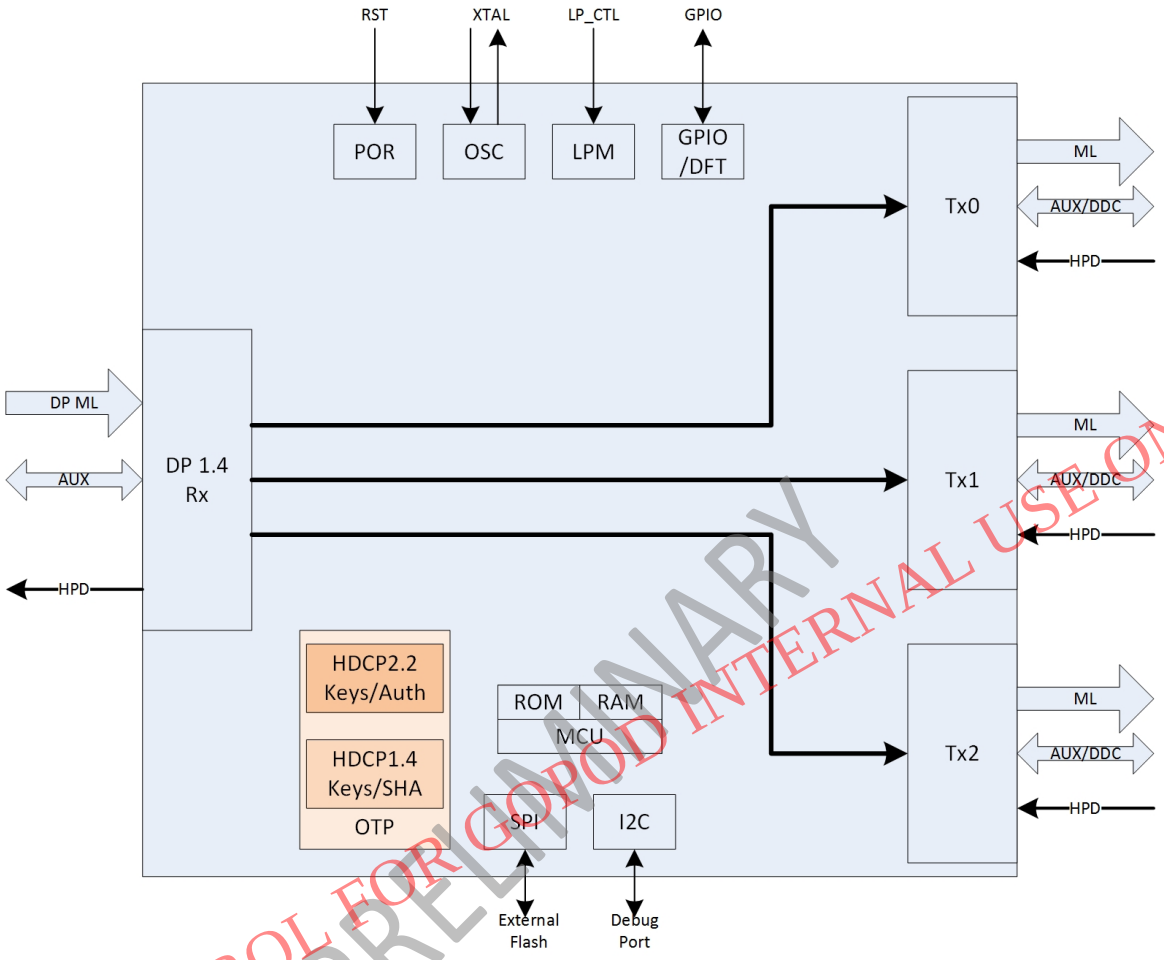


Figure 1. VMM53xx functional block diagram

Rx Operation Modes

- DPRx Single SST Mode
  - DP1.4 or 1.1a single stream (SST) operation
  - One input stream with audio and/or video
  - Audio and/or video stream may be sent out to one of the three Tx outputs or to multiple Tx outputs

- DPRx MST Mode
  - DP1.4 multi-stream (MST) operation
  - One to twelve independent input streams each with video and/or audio
  - Up to three audio and/or video streams may be decoded and each be sent to one of the two (DP/HDMI) Tx outputs (Tx in SST mode)
  - Clone mode operation or downstream ViewXpand SST also permitted
  - Downstream MST mode supported for transmission of up to 12 MST streams to the DP Tx port in MST mode
  - Decoding/transmitting some MST streams into HDMI Tx port can be done while simultaneously passing through other MST streams to DP TX port

DP++ TX port operation modes

- DPTx SST Mode
  - DP1.4 or 1.1a single stream (SST) operation
  - Supports transport of a single audio and video stream to DPTx outputs
- DPTx MST Mode
  - DP1.4 multi stream (MST) operation
  - Supports transport of a up to 4 streams, each containing audio and/or video to DPTx outputs
- DP++ Tx HDMI Mode
  - HDMI stream transmission at DP voltages, to be converted to HDMI with external level-shifter
  - Supports transport of a single audio and/or video stream in each of the Tx output
- DP++ Tx Single DVI Mode
  - Single DVI video transmission at DP voltages, to be converted to DVI with external level-shifter
  - Supports transport of a single video stream in the Tx output

HDMI TX port operation modes

- HDMI/DVI Tx Mode
  - HDMI/DVI stream transmission at HDMI voltages, NO external level-shifter required
  - Supports transport of a single audio and/or video stream

Pin assignments

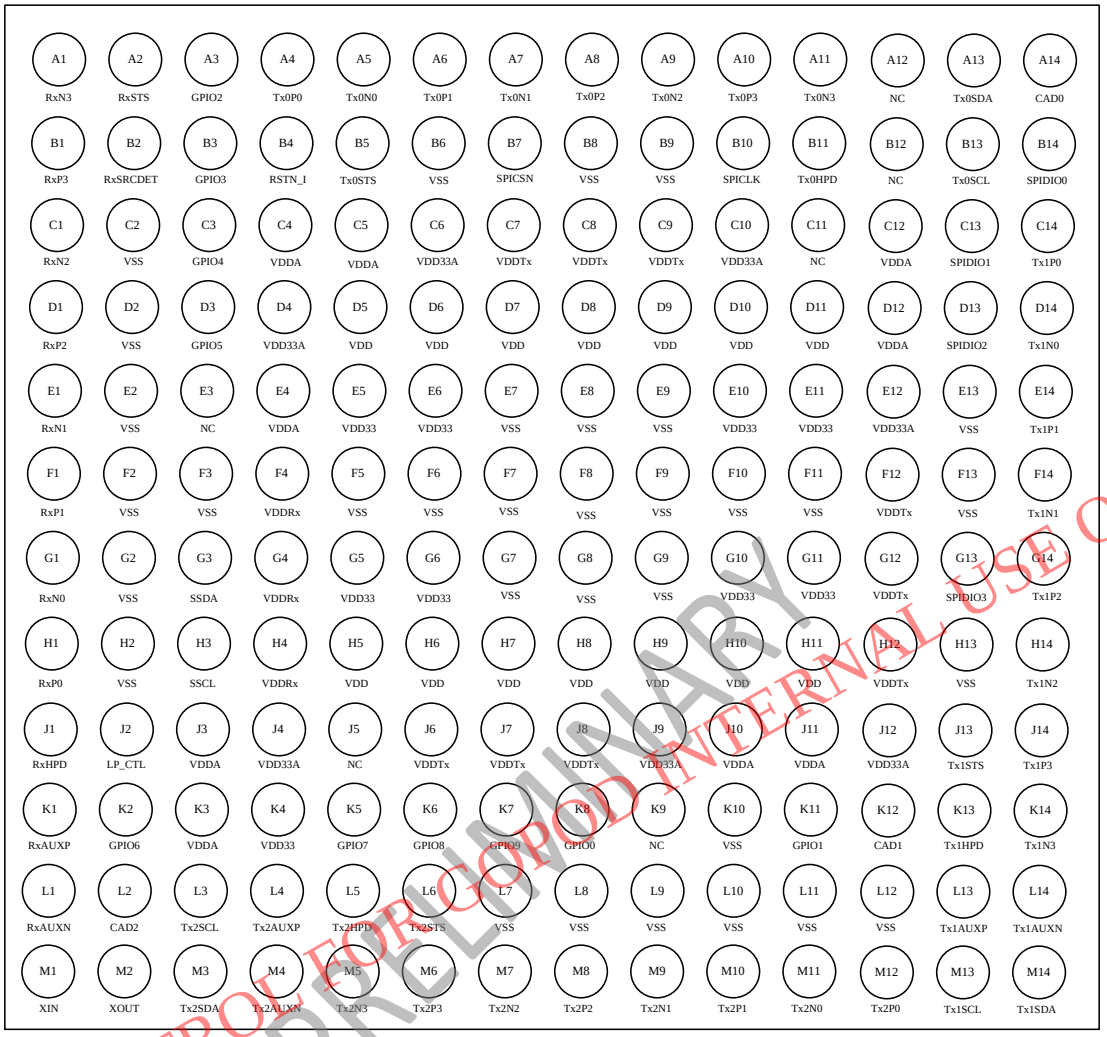


Figure 2. VMM5320 pin assignments (top view)

Pin definitions

Table 1. RX Pins

Pin Location(s)	Signal	Pin Type	Description
A1	RxN3	Input	DP RX Lane3 -
B1	RxP3	Input	DP RX Lane3 +
C1	RxN2	Input	DP RX Lane2 -
D1	RxP2	Input	DP RX Lane2 +
E1	RxN1	Input	DP RX Lane1 -
F1	RxP1	Input	DP RX Lane1 +
G1	RxN0	Input	DP RX Lane0 -
H1	RxP0	Input	DP RX Lane0 +
K1	RxAUXP	Bidirectional	DP RX AUX +
L1	RxAUXN	Bidirectional	DP RX AUX -
B2	RxSRCDET	Input	DP RX Source Detect
J1	RxHPD	Output	DP RX HPD (internal pull-down resistor, 5V tolerant)

Table 2. TX0 Pins - HDMI

Pin Location(s)	Signal	Pin Type	Description
A4	Tx0P0	Output	TMDS TX D2+
A5	Tx0N0	Output	TMDS TX D2-
A6	Tx0P1	Output	TMDS TX D1+
A7	Tx0N1	Output	TMDS TX D1-
A8	Tx0P2	Output	TMDS TX D0+
A9	Tx0N2	Output	TMDS TX D0-
A10	Tx0P3	Output	TMDS TX CLK+
A11	Tx0N3	Output	TMDS TX CLK-
A14	CAD0	Input	Tx0 cable adaptor detect. External resistor needed: see notes below
B13	Tx0SCL	Output	HDMI TX DDC clock (open drain, 5V tolerant)
A13	Tx0SDA	Bidirectional	HDMI TX DDC data (open drain, 5V tolerant)
B11	Tx0HPD	Input	HDMI TX HPD (internal pull-down, 5V tolerant)

Table 3. TX1 Pins - DP

Pin Location(s)	Signal	Pin Type	Description
C14	Tx1P0	Output	TX1 Lane0 +
D14	Tx1N0	Output	TX1 Lane0 -
E14	Tx1P1	Output	TX1 Lane1 +
F14	Tx1N1	Output	TX1 Lane1 -
G14	Tx1P2	Output	TX1 Lane2 +
H14	Tx1N2	Output	TX1 Lane2 -
J14	Tx1P3	Output	TX1 Lane3 +
K14	Tx1N3	Output	TX1 Lane3 -
K12	CAD1	Input	Tx1 cable adaptor detect. External resistor needed: see notes below
L13	Tx1AUXP	Bidirectional	TX1 AUX +
L14	Tx1AUXN	Bidirectional	TX1 AUX -
M13	Tx1SCL	Output	TX1 DDC clock (open drain, 5V tolerant)
M14	Tx1SDA	Bidirectional	TX1 DDC data (open drain, 5V tolerant)
K13	Tx1HPD	Input	TX1 HPD (internal pull-down, 5V tolerant)

Table 4. TX2 Pins - DP

Pin Location(s)	Signal	Pin Type	Description
M12	Tx2P0	Output	TX2 Lane0 +
M11	Tx2N0	Output	TX2 Lane0 -
M10	Tx2P1	Output	TX2 Lane1 +
M9	Tx2N1	Output	TX2 Lane1 -
M8	Tx2P2	Output	TX2 Lane2 +
M7	Tx2N2	Output	TX2 Lane2 -
M6	Tx2P3	Output	TX2 Lane3 +
M5	Tx2N3	Output	TX2 Lane3 -
L2	CAD2	Input	Tx2 cable adaptor detect. External resistor needed: see notes below
L4	Tx2AUXP	Bidirectional	TX2 AUX +
M4	Tx2AUXN	Bidirectional	TX2 AUX -
L3	Tx2SCL	Output	TX2 DDC clock (open drain, 5V tolerant)
M3	Tx2SDA	Bidirectional	TX2 DDC data (open drain, 5V tolerant)
L5	Tx2HPD	Input	TX2 HPD (internal pull-down, 5V tolerant)

Table 5. Control Pins

Pin Location(s)	Signal	Pin Type	Description
B4	RSTN_I	Input	External reset (internal pull-up, Schmitt trigger)
M1	XIN	Input	External crystal clock input (27 MHz)
M2	XOUT	Output	Reference crystal clock output
H3	SSCL	Bidirectional	Debug port I^2C slave clock (open drain)
G3	SSDA	Bidirectional	Debug port I^2C slave data (open drain)
B7	SPICSN	Output	External firmware SPI chip select
B10	SPICLK	Output	External firmware SPI master clock
B14	SPIDIO0	Bidirectional	External firmware SPI master data0
C13	SPIDIO1	Bidirectional	External firmware SPI master data1
D13	SPIDIO2	Bidirectional	External firmware SPI master data2
G13	SPIDIO3	Bidirectional	External firmware SPI master data3
K8	GPIO0	Bidirectional	General purpose IO0 (internal pull-down)
K11	GPIO1	Bidirectional	General purpose IO1 (internal pull-down)
A3	GPIO2	Bidirectional	General purpose IO2 (internal pull-down)
B3	GPIO3	Bidirectional	General purpose IO3 (internal pull-down)
C3	GPIO4	Bidirectional	General purpose IO4 (internal pull-down)
D3	GPIO5	Bidirectional	General purpose IO5 (internal pull-down)
K2	GPIO6	Bidirectional	General purpose IO6 (internal pull-down)
K5	GPIO7	Bidirectional	General purpose IO7 (internal pull-down)
K6	GPIO8	Bidirectional	General purpose IO8 (internal pull-down)
K7	GPIO9	Bidirectional	General purpose IO9 (internal pull-down)
J2	LP_CTL	Input	Low-power mode control (internal pull-down, Schmitt trigger). Drive low to enable. Drive high to disable.
A2	RX_STS	Output	RX port status (internal pull-down)
B5	TX0_STS	Output	TX0 port status (internal pull-down)
J13	TX1_STS	Output	TX1 port status (internal pull-down)
L6	TX2_STS	Output	TX2 port status (internal pull-down)

Table 6. Power - 1.0V

Pin Location(s)	Signal	Pin Type	Description
D5, D6, D7, D8, D9, D10, D11, H5, H6, H7, H8, H9, H10, H11	VDD	Power	1.0V digital core supply
F4, G4, H4	VDDRx	Power	1.0V Rx supply
C7, C8, C9, F12, G12, H12, J6, J7, J8	VDDTx	Power	1.0V Tx supply
J3, K3, E4, C4, C5, C12, D12, J10, J11	VDDA	Power	1.0V analog supply

Table 7. Power - 3.3V

Pin Location(s)	Signal	Pin Type	Description
E5, E6, E10, E11, G5, G6, G10, G11, K4	VDD33	Power	3.3V digital supply
C6, C10, D4, E12, J4, J9, J12	VDD33A	Power	3.3V analog supply

Table 8. Ground

Pin Location(s)	Signal	Pin Type	Description
B6, B8, B9, C2, D2, E2, E7, E8, E9, E13, F2, F3, F5, F6, F7, F8, F9, F10, F11, F13, G2, G7, G8, G9, H2, H13, K10, L7, L8, L9, L10, L11, L12	VSS	Power	Ground

Table 9. NC

Pin Location(s)	Signal	Pin Type	Description
A12, B12, E3, C11, K9, J5	NC	-	Do not connect

Notes:

- Internal pull-up resistor is 27~59kΩ (38kΩ nominal)
- Internal pull-down resistor is 31~80kΩ (46kΩ nominal)
- If using TXn (n=0, 1, 2) port as DP++ mode, add 1MΩ pull-down resistor on CADn
- If using TXn (n=0, 1, 2) port as HDMI mode, add 100kΩ pull-up resistor on CADn

Power Management

Low Power Mode

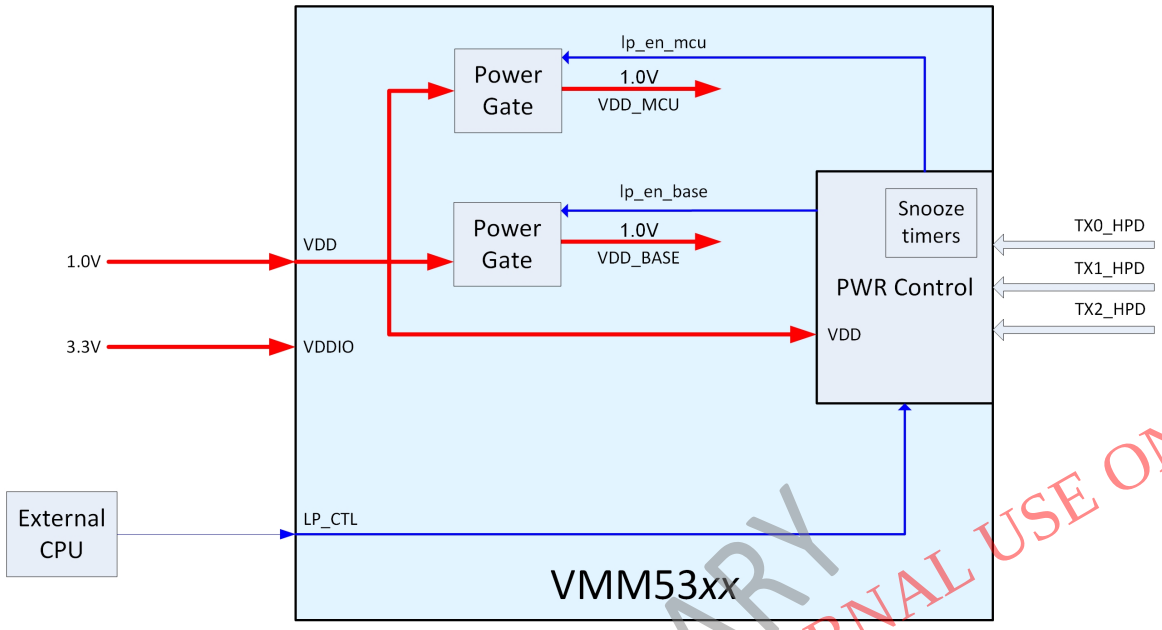


Figure 3. VMM5000 series low power mode system diagram

VMM5000 series products include internal power gating to shut down various parts of the chip in different modes to reduce the power consumption of the device. It contains multiple power domains which may be switched based on the activity of the device.

Power States

- Deep sleep - Minimal power state which may be entered when no monitors are connected. Only the minimal always-on logic remains powered, and device can be awakened by pin inputs (Tx HPDs and LP_CTL) or via an internal timer.
- Standby - Reduced power state where the datapath logic is powered down but the internal MCU remains on, running from an internal low-power oscillator. This is typically used when the DP source sends a D3 standby command to power down the hub and attached monitors. The source can wake the VMM5000 Series device from standby by issuing an AUX command, which will be responded to and initiates wakeup.
- Normal - Fully powered-on state, which is used during initial boot, active standby (monitors attached but no traffic from source), and normal operation (Rx/Tx activity).

Power Domains

- VDD - Always on. This domain is not switched internal to the device.
- VDD_MCU - Switched on chip. This contains the MCU and all associated logic needed to reply to DP Rx AUX transactions.
- VDD_BASE - Switched on chip. This includes datapath logic including Rx/Tx0/Tx1/Tx2/DSC/HDCP2.2. It is never powered up without VDD_MCU also being powered up.

Table 10. VMM5320 power states and domains

State/domain	VDD (always-on)	VDD_MCU (MCU + RxAUX)	VDD_BASE (Rx, Tx0, Tx1, Tx2)
Deep sleep	On	Off	Off
Standby	On	On	Off
Normal	On	On	On

State Transitions

The following diagram shows the flow chart and events for VMM5320 switching between power modes.

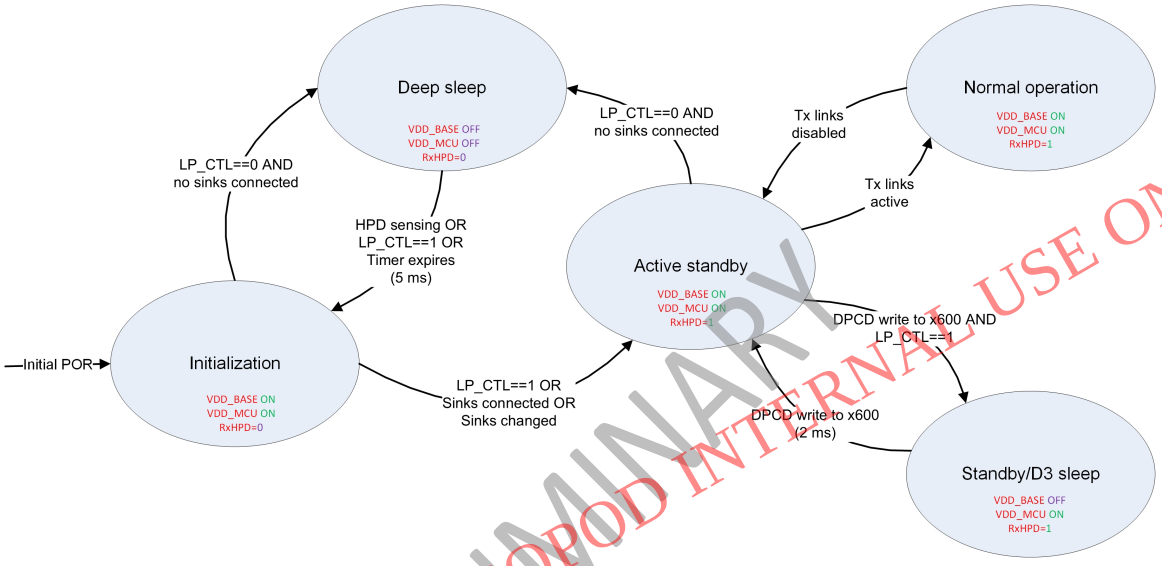


Figure 4. VMM5000 Series low power state diagram

Application Configurations

DP 1.4 Multi-Monitor Hub

Figure 5 shows the typical output configuration for the VMM5320 application.

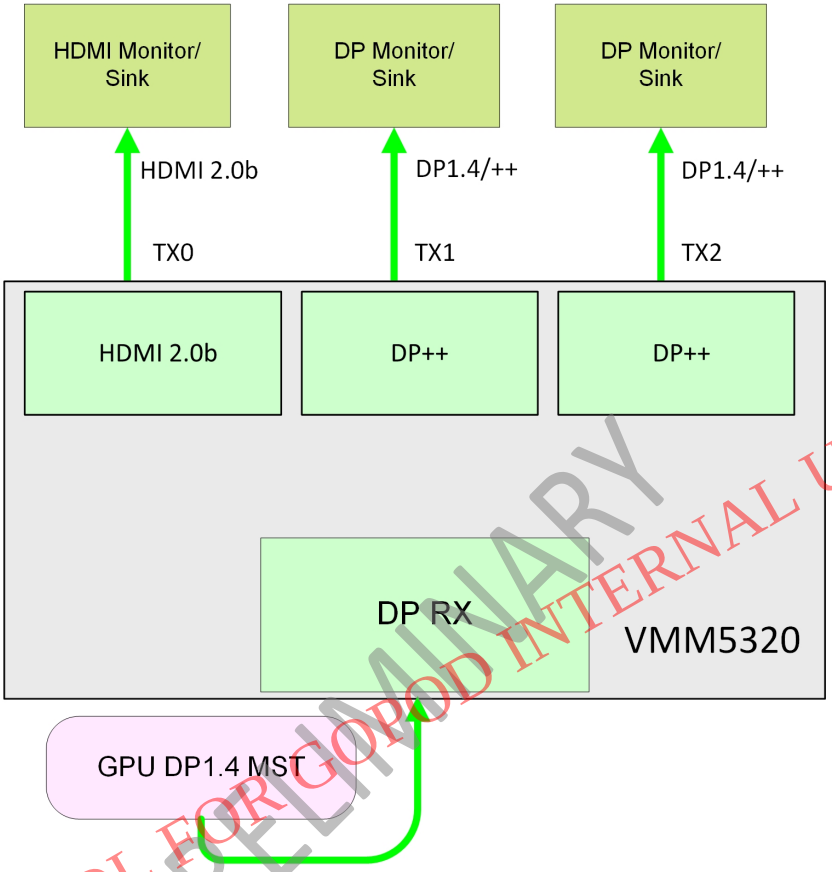


Figure 5. VMM5320 typical output configuration

When the source is DP 1.4, the hub takes DP 1.4 multi-stream input and outputs in the following format:

- 1 x HDMI outputs
- 2 x DP SST or MST output

When the source is DP 1.1, the hub enables View-Xpand multi-monitor. It eases the transition from DP 1.1 to DP 1.4.

Bootstrap Configurations

Table 11. VMM5000 Series bootstrap configurations

GPIO #	Function Mode	Function Description	Default Value
0	Firmware auto-load source	0: Normal mode 1: Test mode	0
2:1	CPU speed and SPI speed	00: Reserved 01: 270 MHz MCU, 33.75 MHz SPI 10: 270 MHz MCU, 27 MHz SPI 11: 27 MHz MCU, 6.75 MHz SPI	0
3	Bootloader service mode	0: Normal mode 1: Bootloader mode	0

Notes:

- Minimum storage size requirement is 512 kbytes (4 Mbits).

Electrical specifications

Absolute maximum ratings

Table 12. VMM5320 absolute maximum ratings

Parameter	Min	Max	Units
1.0V supply voltage	-0.15	1.15	V
3.3V supply voltage	-0.3	3.79	V
Storage temperature, unbiased	-55	150	°C
Operating temperature	0	70	°C
Lead soldering temperature (10 seconds)	-	260	°C
Input current at any pin (EIA/JESD78 latch-up)	-	100	mA
ESD rating, HBM	-	±2	kV
ESD rating, CDM	-	±500	V

Notes:

- Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Specification

Table 13. VMM5320 DC Specification

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	5.5	V
V_T	Threshold point	1.36	1.43	1.51	V
V_{T+}	Schmitt trigger low to high threshold point	1.61	1.69	1.77	V
V_{T-}	Schmitt trigger high to low threshold point	1.18	1.27	1.35	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.33	1.4	1.48	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.38	1.45	1.52	V

Symbol	Parameter	Min	Typ	Max	Units
V_{T+PU}	Schmitt trigger low to high threshold point with pull-up resistor enabled	1.58	1.67	1.74	V
V_{T-PU}	Schmitt trigger high to low threshold point with pull-up resistor enabled	1.15	1.23	1.33	V
V_{T+PD}	Schmitt trigger low to high threshold point with pull-down resistor enabled	1.63	1.73	1.80	V
V_{T-PD}	Schmitt trigger high to low threshold point with pull-down resistor enabled	1.20	1.27	1.36	V
I_I	Input leakage current @ V_I = 3.3V or 0V	-	-	±10	uA
I_{OZ}	Tri-state output leakage current @ V_O = 3.3V or 0V	-	-	±10	uA
R_{PU}	Internal pull-up resistor value	27	38	59	kΩ
R_{PD}	Internal pull-down resistor value	31	46	80	kΩ
V_{OL}	Output low voltage	-	-	0.4	V
V_{OH}	Output high voltage	2.4	-	-	V
I_{OL}	Low level output current @ V_{OL} (max)	9.7	15.6	21.5	mA
I_{OH}	High level output current @ V_{OH} (min)	17.0	34.0	56.5	mA

DisplayPort/HDMI Interface DC Specification

The VESA DisplayPort related DC specification is compliant with the VESA DisplayPort Standard v1.1a/v1.2/v1.4.

The HDMI related DC specification is compliant with HDMI Specification version 2.0b.

Power Supply DC Specification

Table 14. Power Supply DC Specification

Parameter	Min	Typ	Max	Units
1.0V power supply	0.95	1.0	1.05	V
3.3V power supply	2.97	3.3	3.63	V

AC Specification

DisplayPort/HDMI Interface AC Specification

The VESA DisplayPort related AC specification is compliant with the VESA DisplayPort Standard v1.1a/v1.2/v1.4.

The HDMI related AC specification is compliant with HDMI Specification version 2.0b.

I^2C SCL/SDA Specification

DDC and I^2C AC/DC specification is compliant with the standard I^2C specification.

SPI specification

SPI interface AC/DC specification is compliant with Standard SPI specification.

Crystal Oscillator Interface AC Specification

Table 15. Crystal Oscillator Interface AC Specification

Symbol	Parameter	Min	Typ	Max	Units
F_C	Clock frequency		27		MHz
T_{CC}	Clock frequency tolerance	-100		+100	ppm

Power consumption

Table 16. Active Mode power consumption

Symbol	Parameter	Typ	Units
One output: 1 x 4k monitor @ 60 Hz			
$P_{T\text{-}1p1.0}$	1V operation	1100	mW
$P_{T\text{-}1p3.3}$	3.3V operation	40	mW
Two outputs: 2 x 4k monitors @ 60 Hz			
$P_{T\text{-}2p1.0}$	1V operation	1350	mW
$P_{T\text{-}2p3.3}$	3.3V operation	50	mW
Three outputs: 1 x 4k monitor @ 60 Hz, 1 x 4k monitor @ 30 Hz, 1 x FHD @ 60 Hz			
$P_{T\text{-}3p1.0}$	1V operation	1450	mW
$P_{T\text{-}3p3.3}$	3.3V operation	56	mW

Notes:

- Typ condition is 1.0V/3.3V supply, room temperature.

Table 17. Low Power Mode power consumption

Symbol	Parameter	Typ	Units
Standby - D3 sleep mode			
$P_{standby-1.0}$	1V operation	35	mW
$P_{standby-3.3}$	3.3V operation	3	mW
Low power - deep sleep, all Tx unplugged			
$P_{L1.0}$	1V operation	16	mW
$P_{L3.3}$	3.3V operation	2	mW

Notes:

- Typ condition is 1.0V/3.3V supply, room temperature.

Layout Guidelines

Layer Stack-up

- Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the hub inputs and from the hub output to the subsequent receiver circuit.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission-line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.
- Routing the fast-edged control signals on the bottom layer prevents cross-talk into the high-speed signal traces and minimizes EMI.

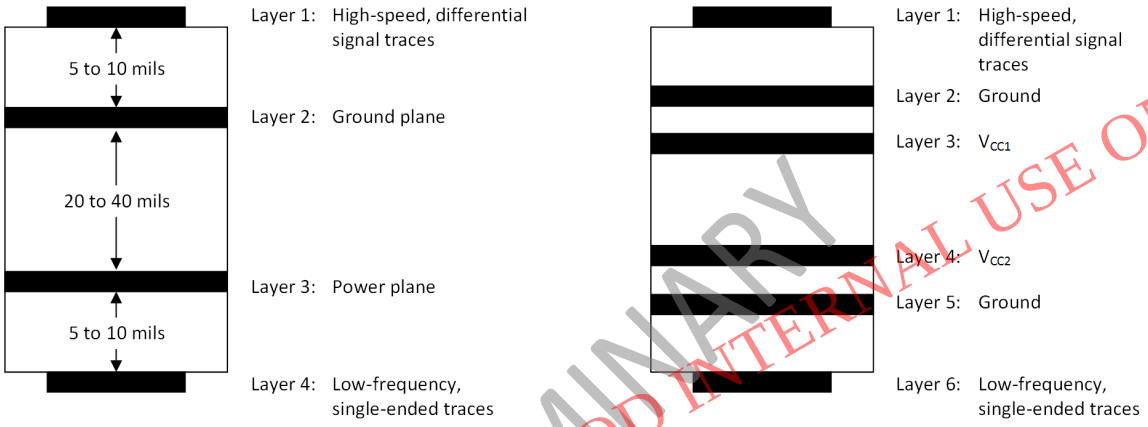


Figure 6. Recommended 4- or 6-Layer (0.062") Stack-up for a Receiver PCB Design

Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and minimize EMI.

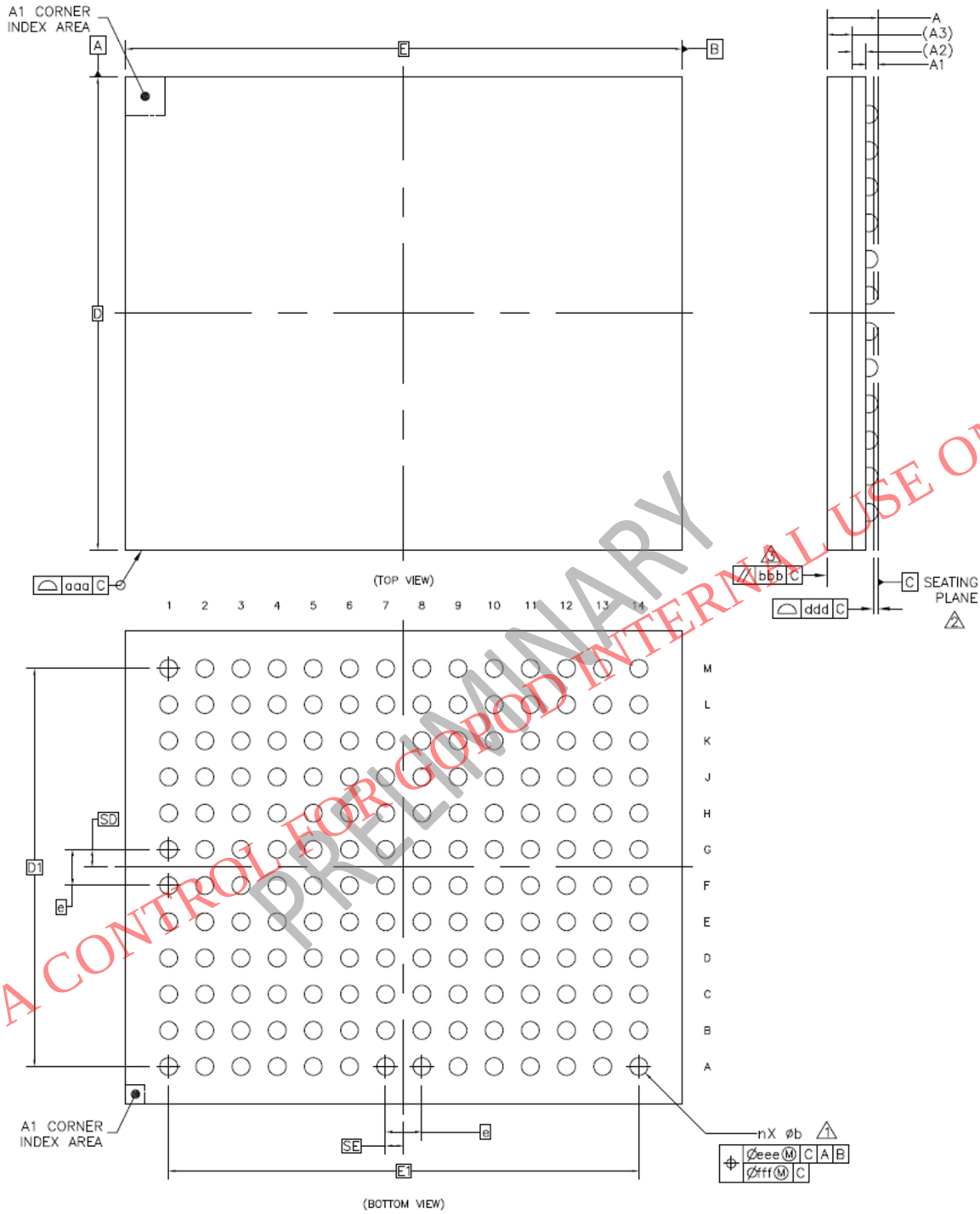
- Select proper PCB stack up and trace width at 90Ω differential transmission line impedance for the high-speed DP/TMDS signals
  - RXP/N and TXP/N pairs should be routed with controlled 90Ω differential impedance (± 15%).
  - For 90Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
  - Route all differential pairs on the same layer.
  - Keep away from other high-speed signals.
- Minimize intra-pair and inter-pair trace lengths within each differential pair.
  - Intra-pair routing should be kept to within 2 mils.
  - Reduce inter-pair skew, caused by component placement and IC pinouts.
  - Each pair should be separated at least by 3 times the signal trace width.
- Use 45 ° bends (chamfered corners), instead of right-angle (90 °) bends.
  - Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities.
  - A 45 ° bend is seen as a smaller discontinuity.

- When routing around an object, route both traces of a pair in parallel.
  - Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.
- Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other.
  - 0402 size is recommended; 0603 size is acceptable; 0805 size is not allowed.
- When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane underneath.
- Avoid metal layers and traces underneath or between the pads of the DisplayPort connectors for better impedance matching, otherwise they will cause the differential impedance to drop below 75Ω and cause the board to fail during TDR testing.
- Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 90Ω differential impedance.
  - Large vias and pads can cause the impedance to drop outside the required range (90Ω ± 15%).
  - The number of vias should be kept to a minimum. It is recommended to keep the via count to two or fewer.
- Use solid power and ground planes for 90Ω impedance control and minimum power noise.
  - Keep traces on layers adjacent to ground plane.
  - Do NOT route differential pairs over any plane split.
- Keep the trace length between the DisplayPort connector and the hub device as short as possible to minimize attenuation.
  - Keep the RX trace length < 4" with IL < 4dB @4.05GHz from DP connector to hub.
  - Keep the TX trace length < 6" with IL < 6dB @4.05GHz from hub to DP connector.
- Use good DisplayPort connectors whose impedances meet the specifications.
- Adding test points will cause impedance discontinuity, and therefore negatively impact signal performance.
  - If test points are used, they should be placed in series and symmetrically.
  - They must not be placed in a manner that causes a stub on the differential pair.

Filtering Capacitors

- Place bulk capacitors (for example, 10 µ F) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
- Place smaller 0.1 µ F or 0.01 µ F capacitors close to the hub device.

Package and Ordering Information



- Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
- Datum C (seating plane) is defined by the spherical crowns of the solder balls.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

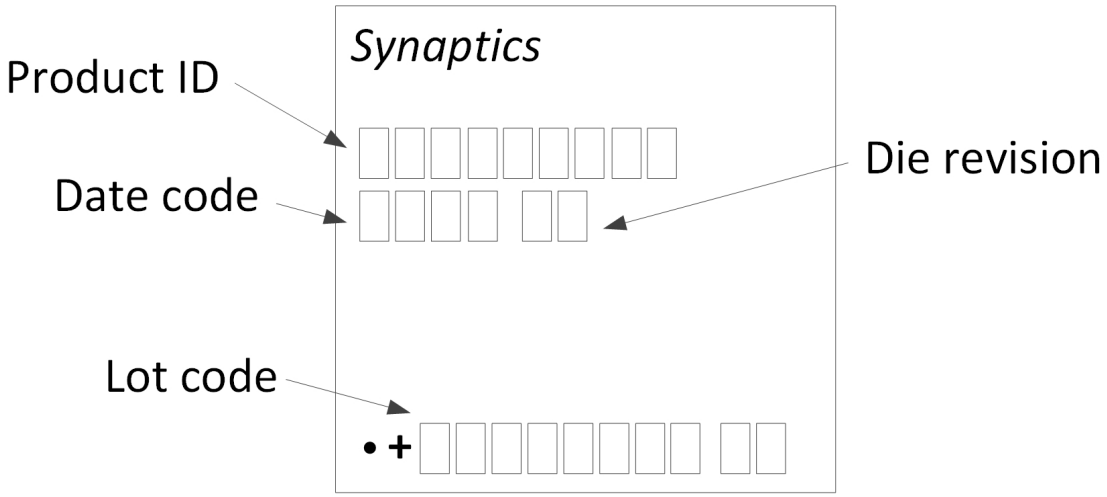
Dimensions

All measurements are in millimeters unless otherwise specified.

Table 18. Package dimensions

Dimension	Symbol	Minimum	Typical	Maximum
Total thickness	A	-	-	1.0
Standoff	A1	0.16	-	0.26
Substrate thickness	A2		0.26 REF	
Mold thickness	A3		0.45 REF	
Body size	D		8.5 BSC	
Body size	E		10 BSC	
Ball diameter		-	0.3	-
Ball opening		-	0.275	-
Ball width	b	0.27	-	0.37
Ball pitch	e		0.65 BSC	
Ball count	n		168	
Edge ball center to center	D1		7.15 BSC	
Edge ball center to center	E1		8.45 BSC	
Body center to contact ball	SD		0.325 BSC	
Body center to contact ball	SE		0.325 BSC	
Package edge tolerance	aaa		0.1	
Mold flatness	bbb		0.1	
Coplanarity	ddd		0.08	
Ball offset (package)	eee		0.15	
Ball offset (ball)	fff		0.08	

Package marking



Ordering information

Table 19. Part numbers for ordering

Ordering code	Package description	Shipping
VMM5320BJG-T	168-contact BGA, 8.5 x 10 mm	Trays
VMM5320BJG-R	168-contact BGA, 8.5 x 10 mm	Tape and reel

Note: Tape and reel only available for volume shipments.

Environmental and regulatory compliance

This Synaptics product is built in compliance with the RoHS directive and the Synaptics Quality Specification: Environmental Conservation Program (PN: 526-000223-01). This Synaptics product is also Halogen-Free (HF) compliant.

Tape and Reel Information

Reel Dimensions

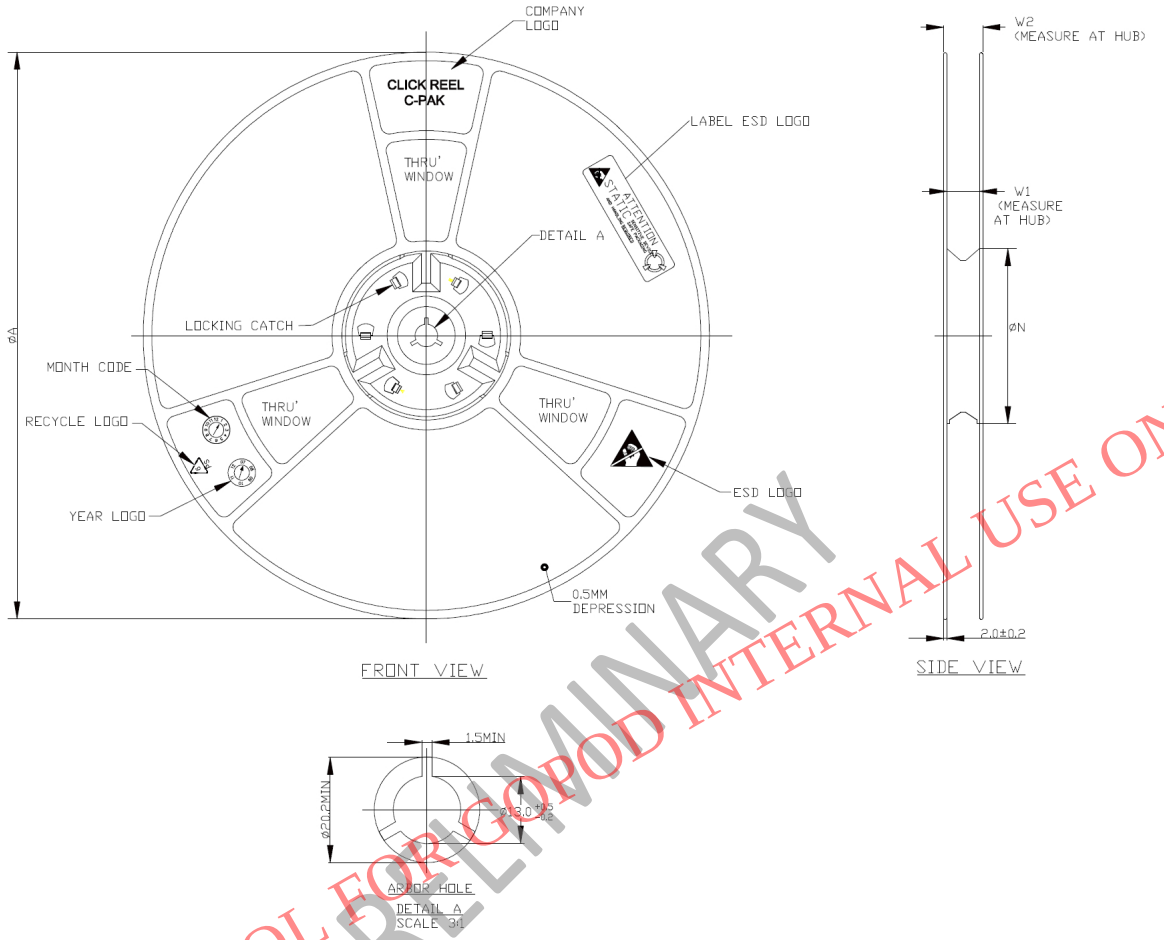


Table 20. Reel dimensions in mm

Tape width	Ø A ± 2.0	Ø N (min)	W1	W2 (max)
24	330.0	100.0	24.4 +2.0/-0.0	30.4

Tape Dimensions

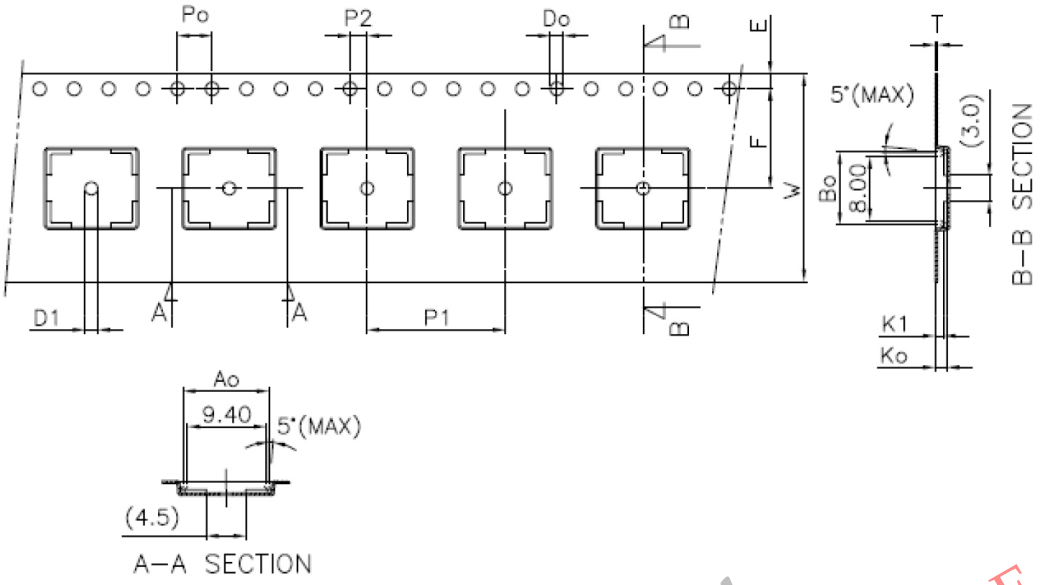


Table 21. Tape dimensions in mm

Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	10.5 ± 0.10	9.00 ± 0.10	1.40 ± 0.10	4.00 ± 0.10	16.0 ± 0.10	2.00 ± 0.10	0.30 ± 0.05

Symbol	E	F	Do	D1	W	10Po	K1
Spec	1.75 ± 0.10	11.50 ± 0.10	1.50 +0.10/-0	1.50 ± 0.10	24.0 +0.30/-0	40.0 ± 0.20	1.00 ± 0.10

Revision history

Revision	Description
1	Initial preliminary release.
2	Added layout guidelines. Added tape & reel information. Updated power consumption.
3	Correction to pinout tables. Added ordering and environmental compliance sections. Changed differential impedance to 90Ω in layout guidelines.
4	Updated typical power consumption data.

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