

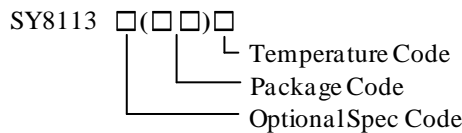
## High Efficiency, 3.0A, 18V Input Synchronous Step Down Regulator

### General Description

The SY8113B1 is a high efficiency, 1.4MHz synchronous step-down DC/DC regulator capable of delivering up to 3A load current. It can operate over a wide input voltage range from 4.5V to 18V and integrate main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

The SY8113B1 adopts the instant PWM architecture to achieve fast transient responses for high step down applications. In addition, it operates at pseudo-constant frequency of 1.4MHz to minimize the size of the inductor and the capacitor.

### Ordering Information



Ordering Number	Package type	Note
SY8113B1ADC	TSOT23-6	----

### Features

- Low  $R_{DS(ON)}$  for Internal Switches (Top/Bottom): 80mΩ/40mΩ
- 4.5~18V Input Voltage Range
- 3A Output Current Capability
- 1.4MHz Switching Frequency Minimize the External Components
- Stable with 10μF  $C_{OUT}$  and 0.68μH Inductor
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Forced PWM Operation
- Cycle-by-cycle Peak/Valley Current Limitation
- Hic-cup Mode Output Short Circuit Protection
- Thermal Shutdown with Auto Recovery
- Output Auto Discharge Function
- Compact Package: TSOT23-6

### Applications

- Set Top Box
- Portable TV
- DSL Modem
- LCD TV
- IP CAM
- Networking

### Typical Application

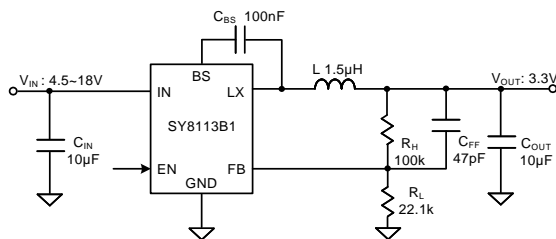


Figure1. Schematic Diagram

Inductor and  $C_{OUT}$  Selection Table

$V_{OUT}$ [V]	$L$ [μH]	$C_{OUT}$ [μF]		
		4.7	10	22
1.2	0.68		√	√
	1.0		☆	√
1.8	1.0		√	√
	1.5		☆	√
3.3	1.5		☆	√
5	2.2		√	√
	3.3		☆	√

Note: '☆' means recommended for most applications.

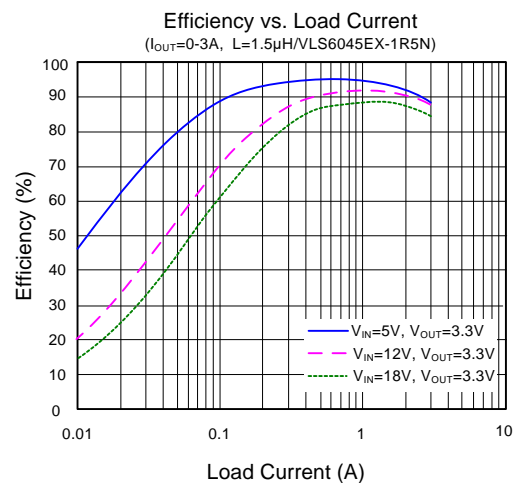
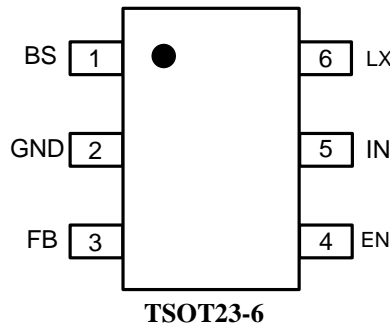


Figure2. Efficiency vs. Output Current

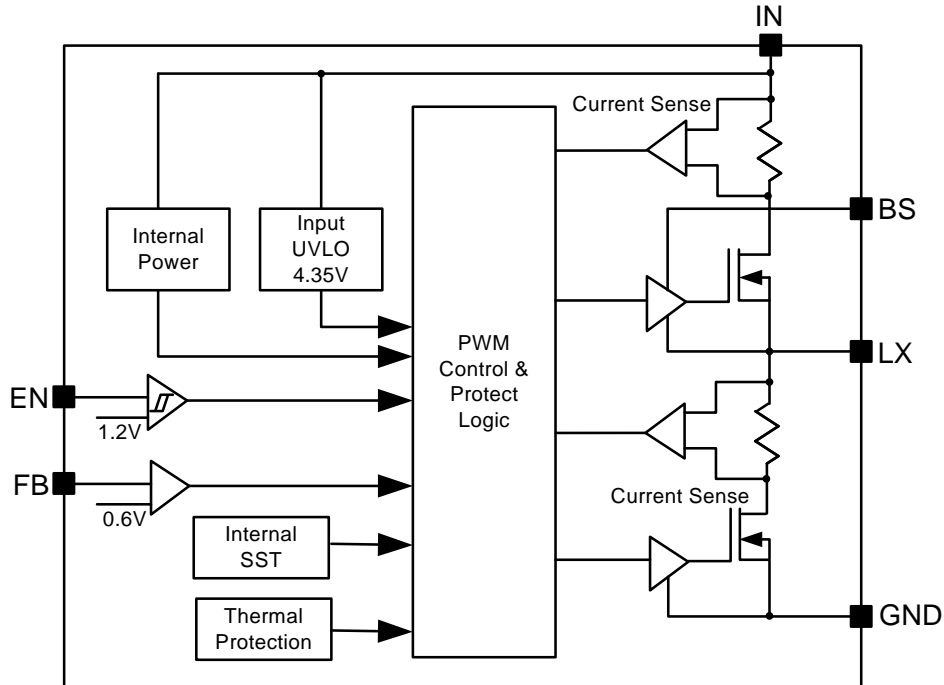
**Pinout (top view)**



Top mark: **L2xyz** (Device code: L2, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1 μF ceramic capacitor between the BS and the LX pins.
GND	2	Power ground pin.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_H/R_L)$ .
EN	4	Enable control. Pull high to turn on. Do not leave this pin floating.
IN	5	Input pin. Decouple this pin to GND pin with at least a 10 μF ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of inductor.

**Block Diagram**



**Figure3. Block Diagram**



**Absolute Maximum Ratings** (Note 1)

Supply Input Voltage	-----	-0.3V to 19V
LX, EN Voltage	-----	-0.3V to V <sub>IN</sub> + 0.3V
FB, BS-LX Voltage	-----	-0.3V to 4V
Power Dissipation, P <sub>D</sub> @ T <sub>A</sub> = 25 °C TSOT23-6,	-----	1.5W
Package Thermal Resistance (Note 2)		
θ <sub>JA</sub>	-----	66 °C/W
θ <sub>JC</sub>	-----	15 °C/W
Junction Temperature Range	-----	-40 °C to 150 °C
Lead Temperature (Soldering, 10 sec.)	-----	260 °C
Storage Temperature Range	-----	-65 °C to 150 °C
Dynamic LX Voltage in 10ns Duration (Note3)	-----	IN+3V to GND-5V

**Recommended Operating Conditions** (Note 3)

Supply Input Voltage	-----	4.5V to 18V
Junction Temperature Range	-----	-40 °C to 125 °C
Ambient Temperature Range	-----	-40 °C to 85 °C

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 1.5\mu H$ ,  $C_{OUT} = 10\mu F$ ,  $T_A = 25^\circ C$ ,  $I_{OUT} = 1A$  unless otherwise specified)

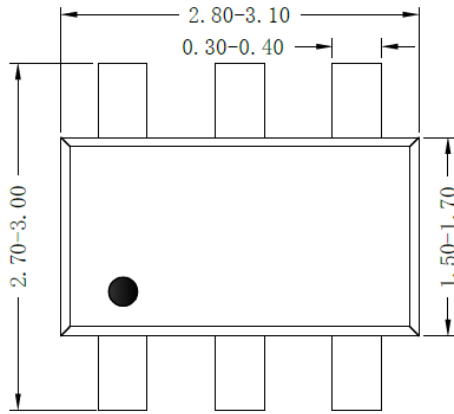
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		4.5		18	V
Input UVLO Threshold	$V_{UVLO}$				4.35	V
Input UVLO Hysteresis	$V_{HYS}$			0.6		V
Shutdown Current	$I_{SHDN}$	EN=0		5	10	$\mu A$
Feedback Reference Voltage	$V_{REF}$		591	600	609	mV
FB Input Current	$I_{FB}$	$V_{FB}=3.3V$	-50		50	nA
Output Discharge Resistance	$R_{DIS}$			40		$\Omega$
Top FET $R_{ON}$	$R_{DS(ON)1}$			80		m $\Omega$
Bottom FET $R_{ON}$	$R_{DS(ON)2}$			40		m $\Omega$
EN Rising Threshold	$V_{EN,R}$		1.08	1.2	1.32	V
EN Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	V
Min ON Time	$t_{ON,MIN}$			50		ns
Min OFF Time	$t_{OFF,MIN}$			200		ns
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		300		$\mu s$
Soft-start Time	$t_{SS}$	$V_{OUT}$ from 0 to 100%		1		ms
Switching Frequency	$f_{SW}$	$V_{OUT}=3.3V$ , CCM		1.4		MHz
Top FET Current Limit	$I_{LIM, TOP}$		4.5			A
Bottom FET Current Limit	$I_{LIM, BOT}$		3			A
Bottom FET Reverse Current Limit	$I_{LIM, RVS}$		1.3			A
Output Under Voltage Protection Threshold	$V_{UVP}$			33%		$V_{REF}$
Output UVP Delay	$t_{UVP, DLY}$			100		$\mu s$
UVP Hiccup On Time	$t_{UVP, ON}$			2		ms
UVP Hiccup Off Time	$t_{UVP, OFF}$			6		ms
Thermal Shutdown Temperature	$T_{SD}$			150		$^\circ C$
Thermal Shutdown Hysteresis	$T_{HYS}$			15		$^\circ C$

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

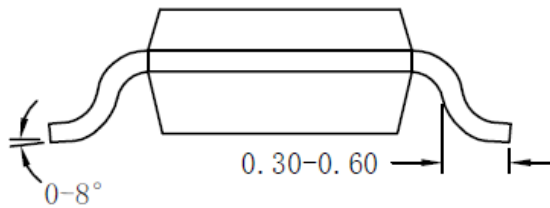
**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a 2-oz two-layer Silergy evaluation board. Paddle of TSOT23-6 package is the case position for SY8113B1  $\theta_{JC}$  measurement.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

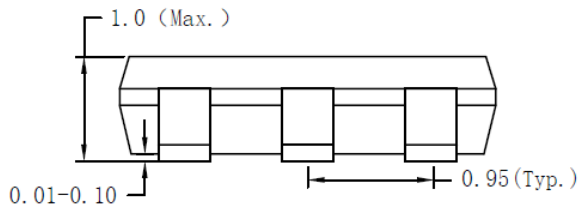
**TSOT23-6 Package Outline & PCB Layout**



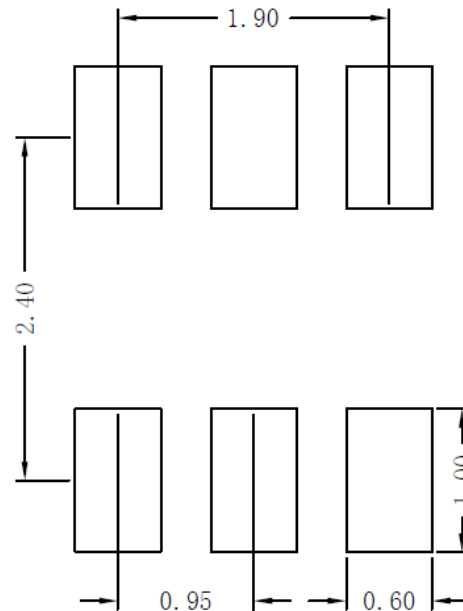
**Top view**



**Side view**



**Front view**



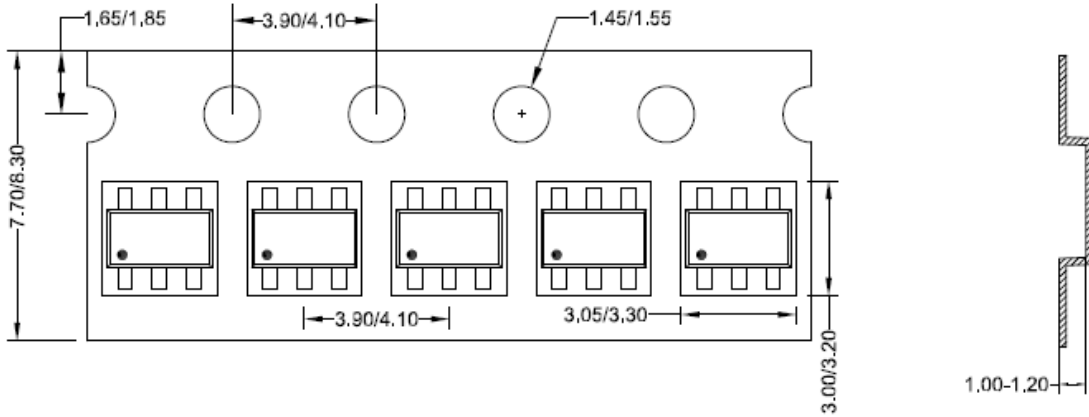
**Recommended Pad Layout**

**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

**Taping & Reel Specification**

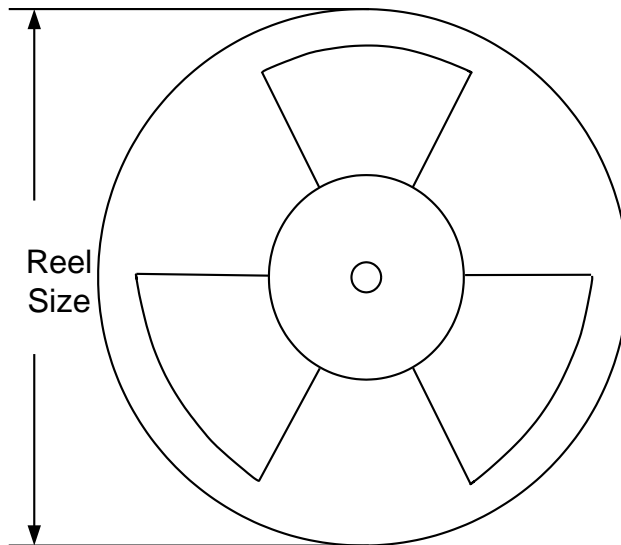
**1. Taping orientation**

**TSOT23-6**



Feeding direction →

**2. Carrier Tape & Reel specification for packages**



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7"	400	160	3000

**3. Others: NA**

单击下面可查看定价，库存，交付和生命周期等信息

[>>SILERGY\(矽力杰\)](#)