MT1001 High Efficiency Synchronous Step-Down Module

2.5V to 6V, 3A Power Module

1. Features

- 2.5V to 6V Input Voltage Range
- 0.8V to V_{IN} Adjustable Output Voltage
- Up to 3A Output Current
- 23μA Low Quiescent Current
- Up to 95% Efficiency
- High Switching Frequency 2.4MHz
- -40°C to 125°C Operating Temperature Range
- Output Auto Discharge Function
- Power Good Output
- Internal Soft-Start Limits the Inrush Current
- 100% Dropout Operation
- Hiccup Mode for Short Circuit Protection
- Auto-Recovery Mode for UVP, UVLO, OTP
- Instant PWM Control Achieve Ultra-Fast Dynamic Response
- 3.0mm x 2.8mm x 1.3mm 8-Pin LGA Package

2. Application

- Optical module
- Computing
- Solid state drive
- Telecom
- Audio/video control system

3. General Description

The MT1001 is a 2.4MHz synchronous step-down power module optimized for small solution size and high efficiency. The power module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area.

MT1001 is capable of delivering up to 3A output currents operating over a wide input voltage range from 2.5V to 6V. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 2.4MHz and automatically enters PFM operation at light load currents. Using the COT-control topology, the device achieves excellent load transient performance and accurate output voltage regulation. The EN and PG pins support sequencing configurations and bring system design flexibility. The integrated soft startup reduces the inrush current from the input supply. The build-in over temperature protection and hiccup short circuit protection deliver a robust and reliable solution.

4. Typical Application

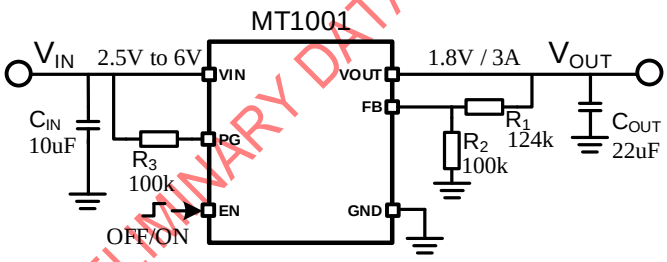
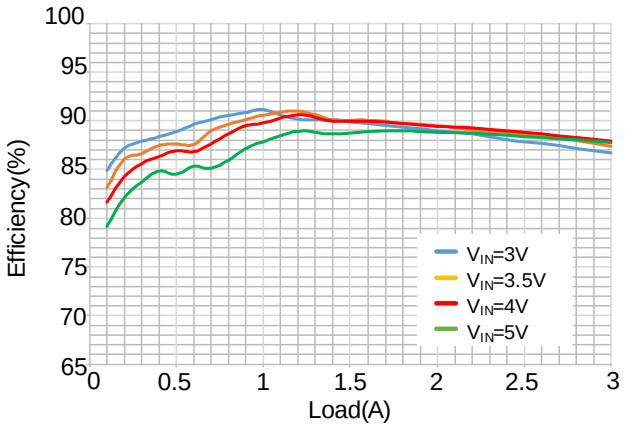


Figure 1. Typical Application



V_{OUT} = 1.8V

Figure 2. Typical Output Efficiency

5. Pin Configuration and Functions

Top View

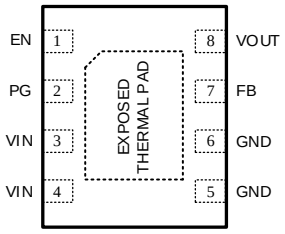


Figure 3. Pin Configuration

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pull-down resistor of typically 400kΩ when the device is disabled.
PG	2	O	Power good open drain output pin. A pull-up resistor can be connected to any voltage less than 6V. Leave it open if it is not used.
V_{IN}	3, 4	PWR	Input voltage pin.
GND	5, 6	PWR	Ground pin.
FB	7	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage. $V_{OUT}=0.8\times(1+R_1/R_2)$.
V_{OUT}	8	PWR	Output voltage pin.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

6. Specifications

6.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
Supply input voltage (2)	V_{IN}	-0.3	7.0	V
Voltage at pins	EN, PG, FB, V_{OUT}	-0.3	V_{IN} +0.3	V
Module operating temperature range		-40	125	°C
Storage temperature range		-40	125	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

		MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Condition (1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	2.5	6	V
I_{OUT}	Output current range	0	3	A
T_J	Module operating temperature range(2)	-40	125	°C

(1) The device is not guaranteed to function outside of its operating conditions.

(2) The module operating temperature range includes module self-temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated.

6.4 Thermal Information

THERMAL METRIC		TYP	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) Thermal Resistance	N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) Thermal Resistance	17.4	°C/W

6.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 3.6V. Typical values are at T_J = 25°C unless otherwise noted. The values are guaranteed by test, design or statistical correlation.

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply						
Input voltage range	V_{IN}		2.5		6	V
Supply current (shutdown)	I_{SHDN}	V_{IN} = 5.5V, V_{EN} = Low, T_J=25°C		0.1	2	μA
Supply current (quiescent)	I_Q	V_{IN} = 5.5V, V_{FB} = 1.05×Vref, T_J=25°C		23	35	μA
Under voltage lock-out threshold	V_{UVLO}	V_{IN} falling	2.1	2.2	2.3	V
		V_{IN} rising		2.4		V
Enable						
EN input voltage high	$V_{EN,H}$		1.0			V
EN input voltage low	$V_{EN,L}$				0.4	V
EN pull down resistance	R_{EN}			400		kΩ
Power Good and Soft Start						
Power good threshold	V_{PG}	V_{FB} falling, referenced to V_{OUT} nominal	87	90	93	%
		V_{FB} rising, referenced to V_{OUT} nominal	93	95	98	
Power good pull low resistor	R_{PG}			10		Ω
Power good output low	$V_{PG,L}$	I_{PG}=2.5mA		0.025		V
Input leakage current into PG pin	$I_{PG,LKG}$	V_{PG} = 6.0 V		0.01	0.1	μA
Soft-start time	t_{SS}	From EN high to 95% of V_{OUT} nominal	0.4	0.8	2	ms
Output						
Feedback reference voltage	V_{REF}	I_{OUT}=1A, CCM	0.788	0.8	0.812	V
Output voltage line regulation	ΔV_{LNR}	V_{IN}=3.0V to 6.0V, I_{OUT}=1.0A		0.02	0.1	%/V
Output voltage load regulation	ΔV_{LDR}	I_{OUT}=0.5A~3A		0.16		%/A
Output discharge resistor	R_{DIS}			260		Ω
Output under voltage protection threshold	V_{UVP}			30		$\%V_{FB}$
Output UVP delay	$t_{UVP,DLY}$			20		μs
Power Switch						
High side FET on-resistance	$R_{DS(ON)1}$			31		mΩ
Low side FET on-resistance	$R_{DS(ON)2}$			23		mΩ
High side FET current limit	I_{LIMIT_HS}		3.8	4.6	6	A
Switching Frequency and Minimum On/Off Time						
Switching frequency	f_{SW}			2.4		MHz
Minimum on-time	t_{ON_MIN}			50		ns
Minimum off-time	t_{OFF_MIN}				100	ns
Maximum duty cycle(1)	D_{MAX}		100			%
Thermal Protection						
Thermal shutdown	T_{SD}	T_J rising		150		°C
Thermal shutdown hysteresis	T_{SD-HYS}	T_J falling		20		°C

(1) When VOUT=3.7V, IOUT=0A (PFM mode), if VIN decreases from high to low and VIN≤4.35V, the IC will enter into FCCM operation; when VOUT=3.7V, IOUT=0A (FCCM mode), if VIN increases from low to high and VIN≥5.2V, the IC will enter into PFM operation.

7. Detail Description

7.1 Overview

The MT1001 is a 2.4MHz synchronous step-down power module optimized for small solution size and high efficiency. The power module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, and the feedback resistors (R1 and R2) need to be selected for the targeted application specifications.

7.2 Block Diagram

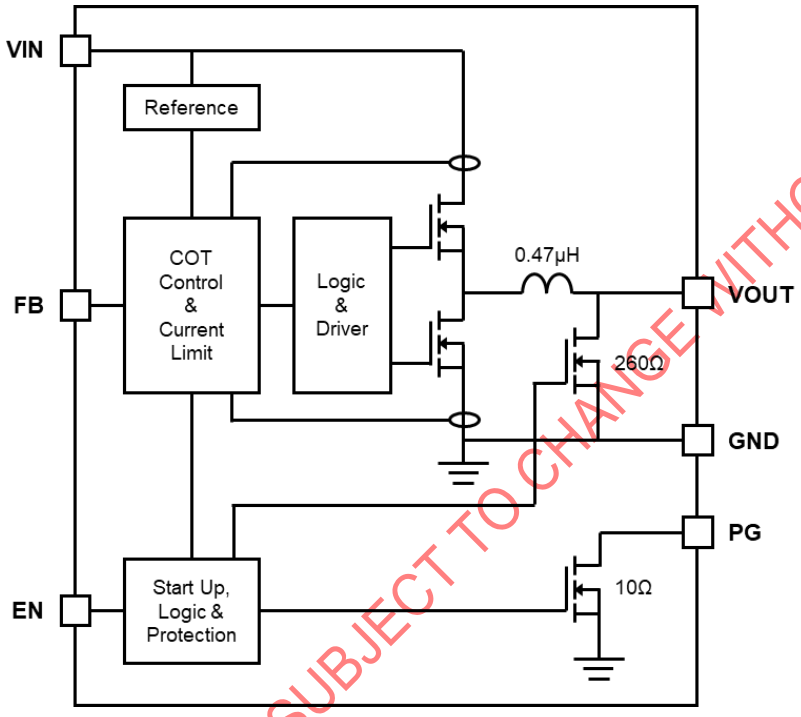


Figure 4. Functional Block Diagram

7.3 Feature Description

7.3.1 Soft Start

The device has an internal soft start circuit which ramps up the output voltage to the nominal voltage during a soft start time of typically 0.8ms. This avoids excessive inrush current and creates a smooth output voltage slope. It also prevents excessive voltage drops of batteries with high internal impedance.

7.3.2 Output Voltage Setting

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. V_{OUT} can be calculated according to the following equation:

$$Vout = 0.8V * (1 + \frac{R1}{R2})$$

7.3.3 Over Voltage Protection

If the DC output voltage is about 3% over the regulation level, both high side power FET and low side power FET will turn off and enter into stand-by mode.

7.3.4 Over Current Protection (OCP)

With load current increasing, as soon as the high side power FET current gets higher than peak current limit threshold, the high side power FET will turn off and the low side power FET will keep turning on until low side power FET current

decrease below the valley current limit threshold. If the load current continues to increase, the output voltage will drop.

7.3.5 Thermal Shutdown

If the junction temperature is higher than the thermal shutdown temperature (typical 150°C), the power module will turn off both high side power FET and low side power FET, and enters thermal shutdown protection mode. It will remain in this state until the junction temperature decreases below 130°C. After exiting this state, the IC auto retries to normal operation.

7.3.6 Enable and Disable

The device is enabled by setting the EN pin to a logic High (higher than 1V). Accordingly, shutdown mode is forced if the EN pin is pulled Low (lower than 0.4V). An internal resistor of 260Ω discharges the output via the V_{OUT} pin smoothly when the device is disabled. The output discharge function also works when thermal shutdown or under voltage lockout are triggered.

An internal pull-down resistor of 400kΩ is connected to the EN pin when the EN pin is Low. The pull-down resistor is disconnected when the EN pin is High.

7.3.7 Power Good Output

The device has a power good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 2.5mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6V.

8. Application Information

The MT1001 is synchronous step-down converter power modules whose output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for typical application as a reference.

The power inductor integrated inside the MT1001 is 0.47μH with approximately +/- 20% tolerance.

8.1 Typical Application:

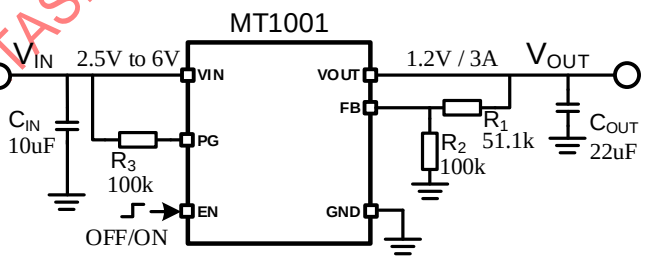


Figure 5. 1.2V Output Application

8.1.1 Design Requirements

Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5V to 6 V
Output voltage	1.2V
Output ripple voltage	<20mV
Output current rating	3A

List of Components

REFERENCE	DESCRIPTION
C_{in}	10μF MLCC
R_1	51.1kΩ, 1% accuracy

R_2	100kΩ, 1% accuracy
R_3	100kΩ, 1% accuracy
C_{out}	22μF MLCC

8.1.2 Detailed Design Procedure

8.1.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equation:

$$Vout = V_{FB} * \left(1 + \frac{R1}{R2}\right) = 0.8V * (1 + \frac{R1}{R2})$$

To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors.

8.1.2.2 Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, to minimize the potential noise problem, please place this ceramic capacitor really close to the V_{IN} and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and V_{IN} / GND pins.

The capacitance can vary significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR. The capacitance value can be calculated with targeted input voltage ripple from the following equation:

$$Cin = \frac{Iout}{\Delta Vin * fs} * \frac{Vout}{Vin} * (1 - \frac{Vout}{Vin})$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$

$$Cin = \frac{Iout}{4 * \Delta Vin * fs}$$

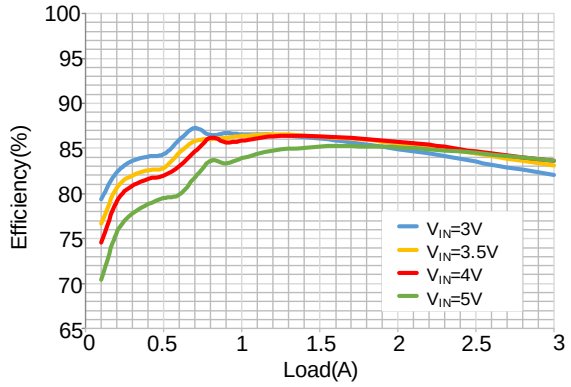
8.1.2.3 Output Capacitor

The output capacitor maintains the DC output voltage. Polar electrolytic capacitor or ceramic capacitors can be used here, and the output voltage ripple can be estimated with the following equation:

$$\Delta Vout = \left(1 - \frac{Vout}{Vin}\right) * \left(\frac{Vout}{0.47uH * fs}\right) * (ESR + \frac{1}{8 * fs * Cout})$$

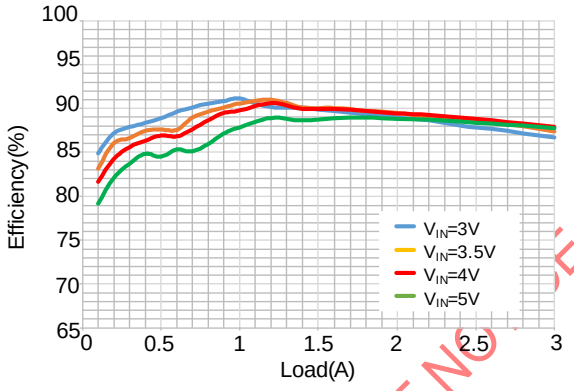
8.2 Application Performance Curves

T_A=25°C, V_{IN}=5V unless otherwise noted



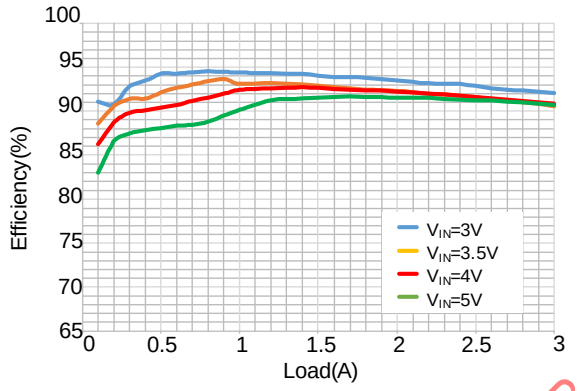
V_{OUT}=1.2V

Figure 6. Efficiency



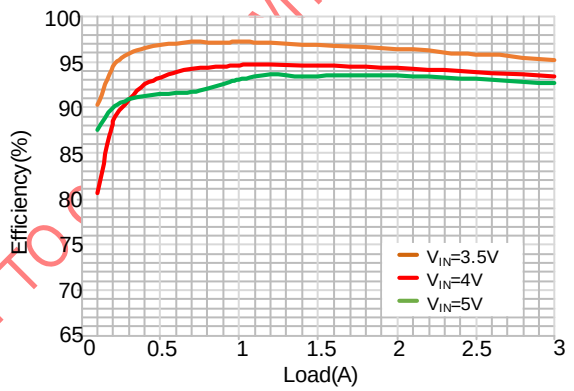
V_{OUT}=1.8V

Figure 7. Efficiency



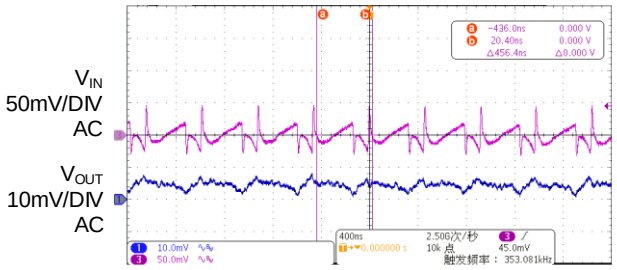
V_{OUT}=2.5V

Figure 8. Efficiency



V_{OUT}=3.3V

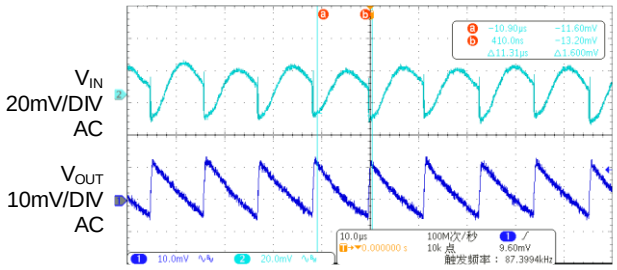
Figure 9. Efficiency



Time - 400ns/DIV

V_{OUT} = 1.2V, I_{OUT} = 2A

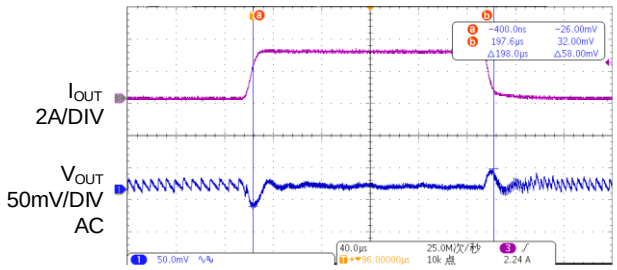
Figure 10. Input and Output Ripple



Time - 10us/DIV

V_{OUT} = 1.2V, I_{OUT} = 25mA

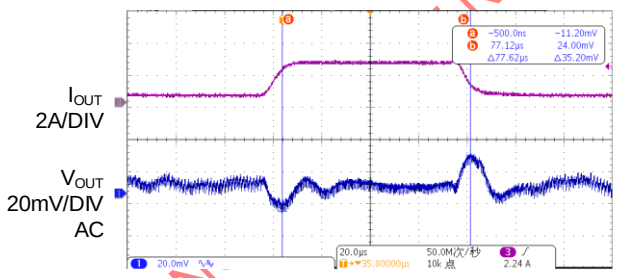
Figure 11. Input and Output Ripple



Time - 40us/DIV

V_{OUT} = 1.2V, I_{OUT} = 25mA to 3A

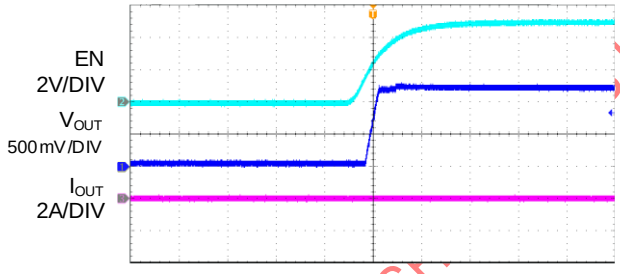
Figure 12. Load Transient



Time - 20us/DIV

V_{OUT} = 1.2V, I_{OUT} = 0.5A to 2.5A

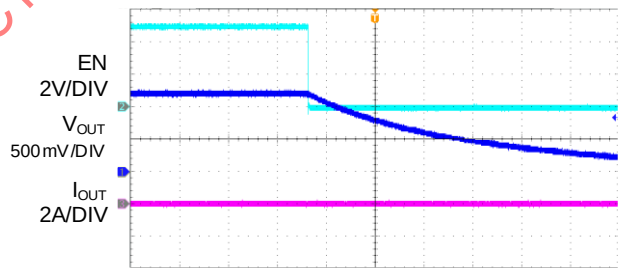
Figure 13. Load Transient



Time - 2ms/DIV

V_{OUT} = 1.2V, No Load

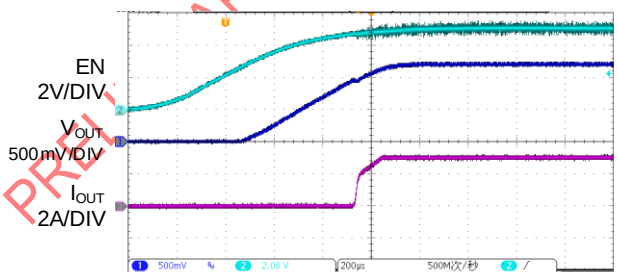
Figure 14. Startup



Time - 2ms/DIV

V_{OUT} = 1.2V, No Load

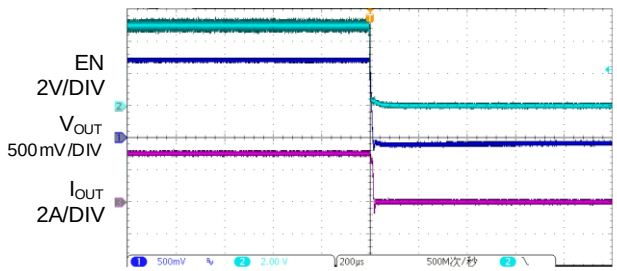
Figure 15. Shutdown



Time – 200us/DIV

V_{OUT} = 1.2V, I_{OUT} = 3A

Figure 16. Startup with CC Load



Time – 200us/DIV

V_{OUT} = 1.2V, I_{OUT} = 3A

Figure 17. Shutdown with CC Load

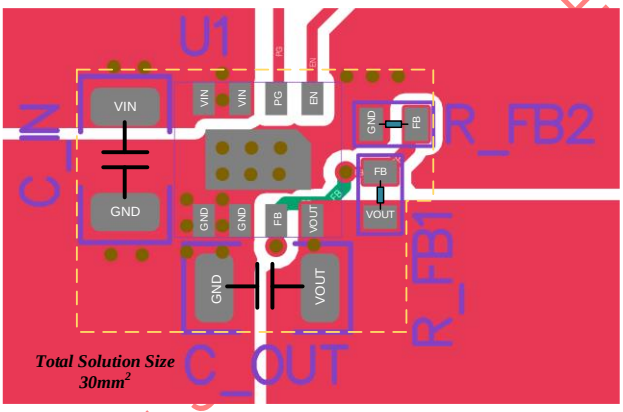
9. Layout

9.1.1 PCB Layout Guidelines

PCB layout is critical for stable operation. For the best results, refer to the guidelines below：

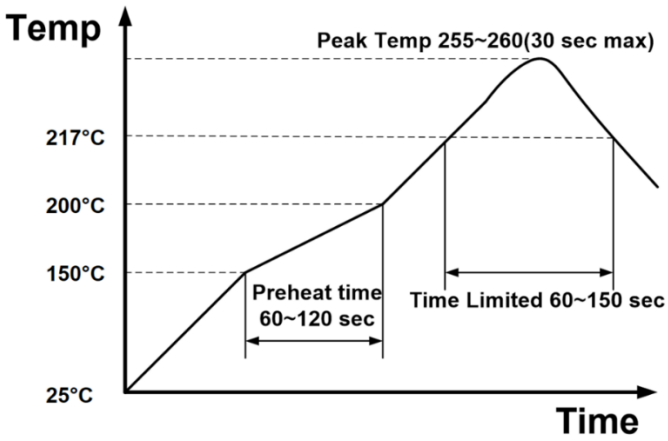
1. Keep the power loop as small as possible.
2. Connect a large ground plane directly to GND. If the bottom layer is a ground plane, add Vias near GND.
3. Ensure the high-current paths at GND and V_{IN} have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor as close to the V_{IN} and GND pins as possible to minimize high-frequency noise.
5. Keep the paths between the input capacitor and V_{IN} as short and wide as possible.
6. Connect V_{IN}, V_{OUT}, and GND to a large copper area to improve thermal performance and long-term reliability.
7. Separate the input GND area from the other GND area at the top layer, and connect them together at the internal layers and bottom layer through multiple Vias.
8. Ensure that there is a complete GND plane at either the internal layer or the bottom layer.
9. A 4-layer layout is recommended to achieve better thermal performance. Use multiple Vias to connect the power planes to internal layers.

9.1.2 Layout Example



10. Reflow Parameter

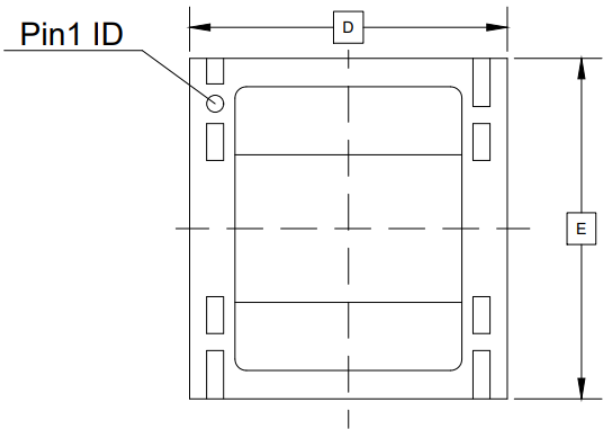
Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. The figure below shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60~150 seconds limit to melt the solder and make the peak temperature at the range from 255°C to 260°C (Do not exceed 30 sec). It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formula.



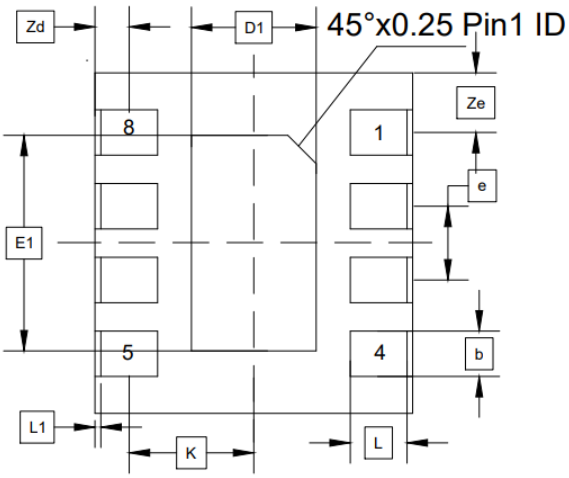
11. Mechanical and Packaging Information

11.1 Package Outline Drawing

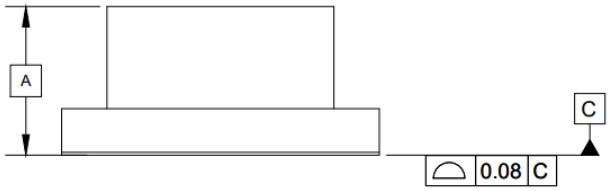
Unit: mm



TOP VIEW



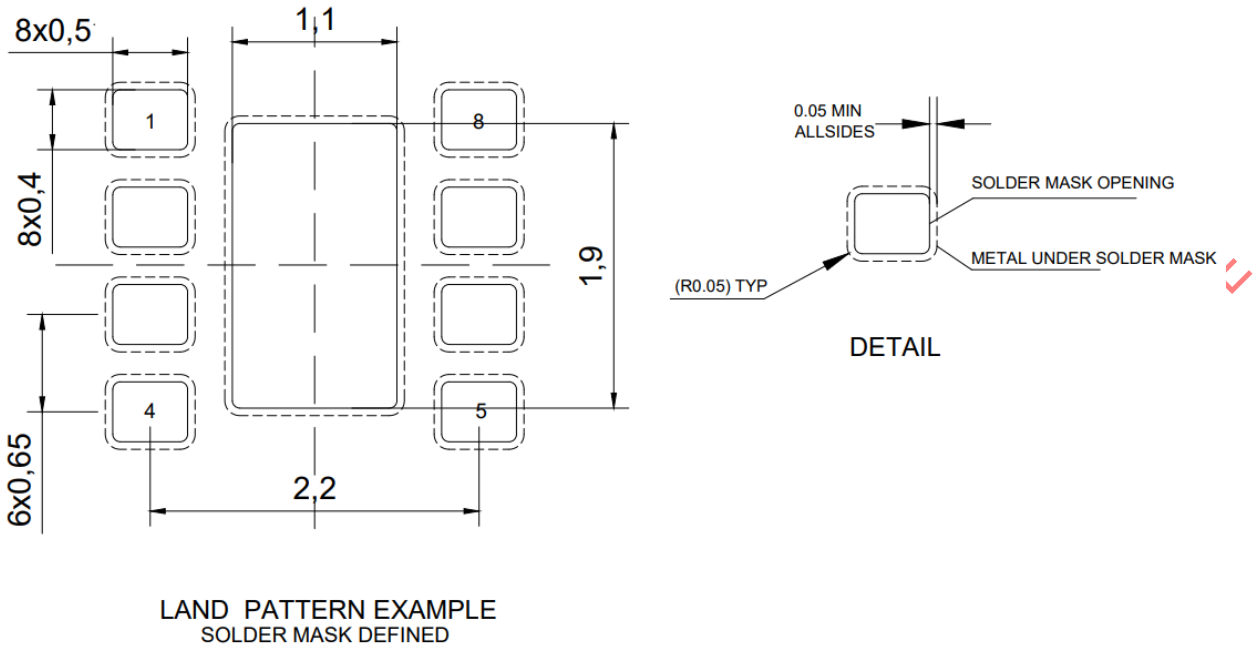
BOTTOM VIEW



SIDE VIEW

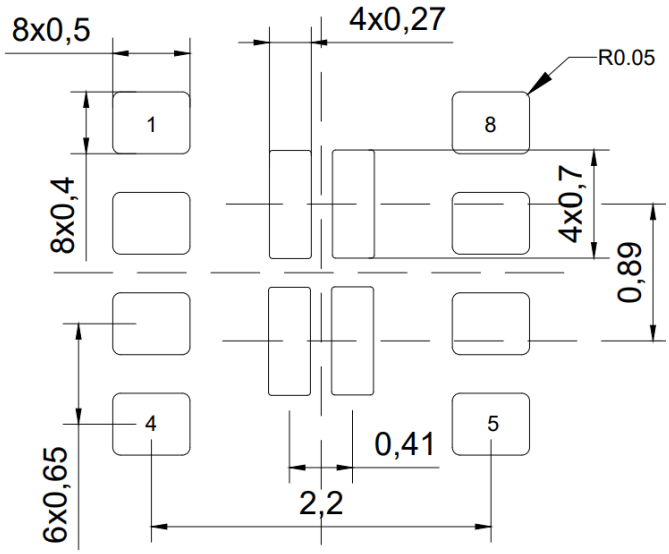
DIM	MIN	NOM	MAX
A	-	1.30	1.39
D	2.70	2.80	2.90
D1	1.00	1.10	1.20
E	2.90	3.00	3.10
E1	1.80	1.90	2.00
K	1.00	1.10	1.20
e	0.55	0.65	0.75
b	0.30	0.40	0.50
L	0.40	0.50	0.60
L1	0.00	0.05	0.15
Zd	0.20	0.30	0.40
Ze	0.425	0.525	0.625

11.2 Example Board Layout **Unit: mm**



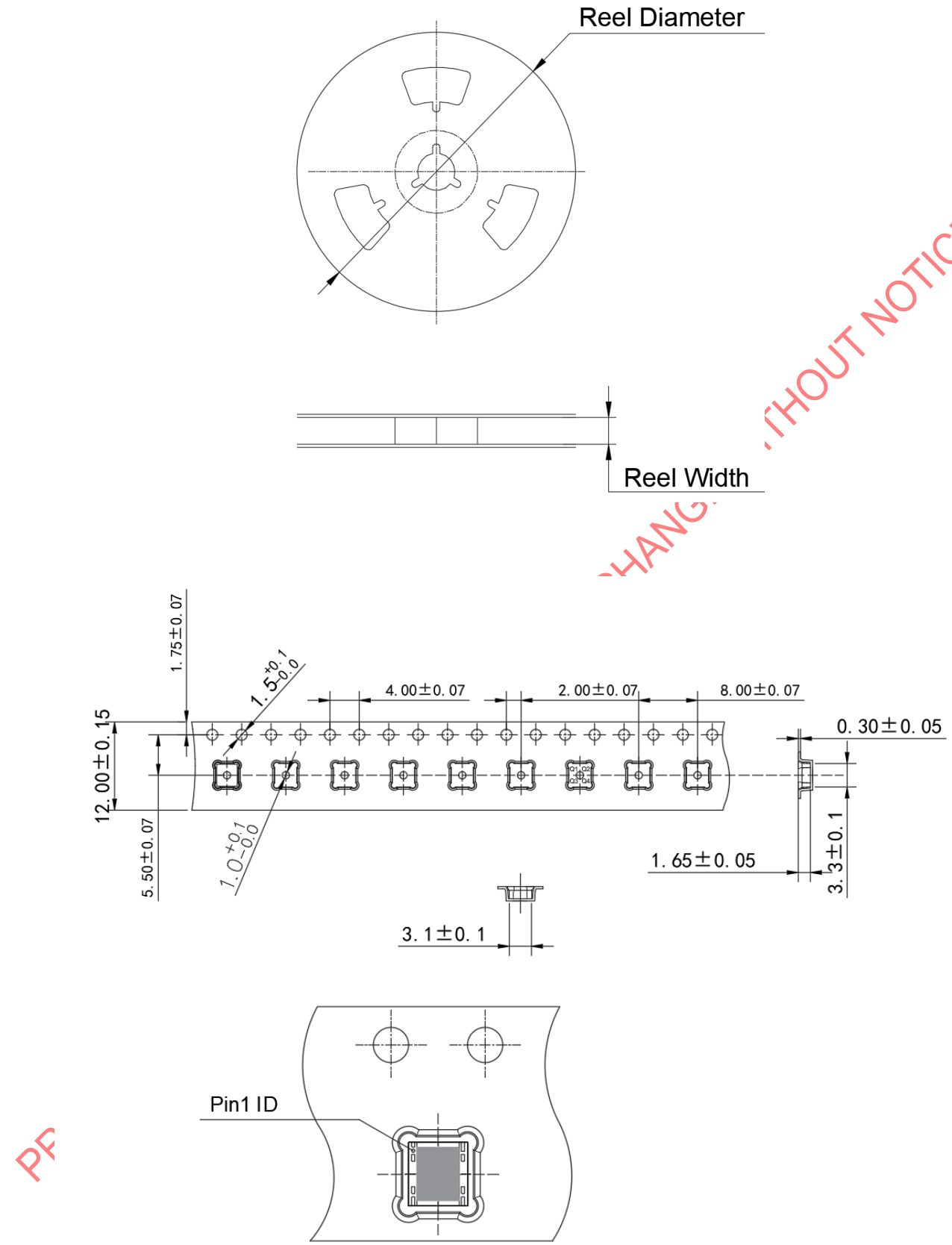
LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

11.3 Example Stencil Design **Unit: mm**

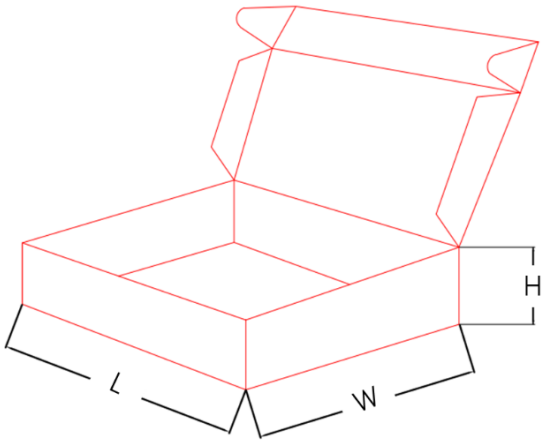


SOLDER PASTE EXAMPLE
BASED ON 0.12mm THICKNESS STENCIL(Reference only)

11.4 Tape & Reel Specification



Tape and Reel Box Dimensions



Orderable Device	Package Type	Reel Diameter(mm)	Reel Width(mm)	QTY/Reel	Box Size(mm)	QTY/Box
MT1001R	uSiP	330	12	3000	355x340x80	6000
MT1001T	uSiP	178	13	250	240x220x50	500

12. Revision History

Rev.	Change list	Date
0.72	Block diagram. T&R drawing. Box size. Orderable Device.	2022.11.01
1.0	Initial release.	TBD

单击下面可查看定价，库存，交付和生命周期等信息

>>METAPWR(沛塬)