XC9145 Series

ETR04032-001a

400nA Ultra-Low Quiescent, 0.8A, PWM/PFM Step-up DC/DC Converters

☆Green Operation compatible

■GENERAL DESCRIPTION

XC9145 series are synchronous step-up DC/DC converters with a 200mΩ N-channel driver FET and a 270mΩ synchronous P-channel switching FET built-in.

The ultra-low current consumption of 400nA and PWM/PFM auto-switching control have dramatically improved the efficiency of the output current of 10μA or less, which was difficult to achieve in the past. (89.9%@V_{IN}=2.4V, V_{OUT}=3.3V, I_{OUT}=10μA)

XC9145 series can significantly reduce the power consumption of battery-powered devices which consume a large percentage of power when the system is in standby mode. It contributes to keeping battery life longer and reducing battery size smaller.

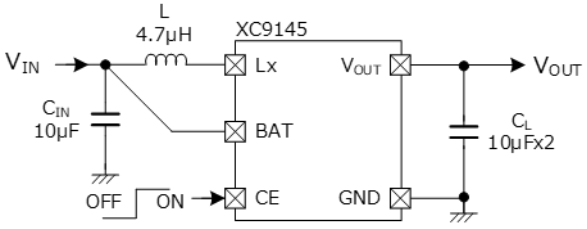
■APPLICATIONS

- ●Low power wireless communication products
- ●Low power IoT module
- ●Battery-powered medical devices / Wearable devices (Health monitoring, Fitness devices)
- ●Remote controls
- ●Primary battery portable systems
- ●Metering devices / Smart meter (Gas / Water / Temperature)
- ●Home Security / Home Automation
- ●Energy Harvest

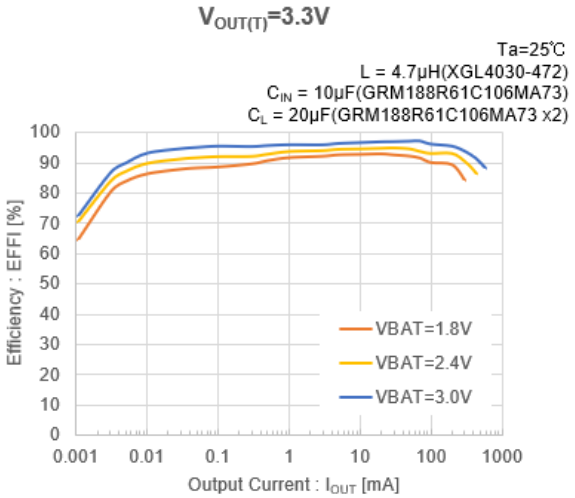
■FEATURES

Input Voltage Range	: 0.65V ~ 5.5V (Operation Start Voltage 1.6V)
Fixed Output Voltage	: 3.0V ~ 5.5V (0.1V increments)
Output Current	: 430mA @V_{OUT}=5.0V, V_{BAT}=3.3V 300mA @V_{OUT}=3.3V, V_{BAT} =1.8V
Oscillation Frequency	: 1.2MHz
Quiescent Current	: 400nA
Efficiency	: 89.9% @V_{IN}=2.4V, V_{OUT}=3.3V, I_{OUT}=10μA 93.2% @V_{IN}=2.4V, V_{OUT}=3.3V, I_{OUT}=100mA
Control Mode	: Auto PWM/PFM
Load transient response	: 300mV @V_{OUT}=3.3V, V_{BAT}=1.8V, I_{OUT}=1mA→200mA
Protection function	: Current Limit
Functions	: Soft start Load Disconnection
Operating Ambient Temperature	: -40℃ ~ 105℃
Package	: USP-6C (1.8x2.0x0.6mm) WLP-6-05 (1.08x1.28x0.4mm)
Environmentally Friendly	: EU RoHS Compliant, Pb Free

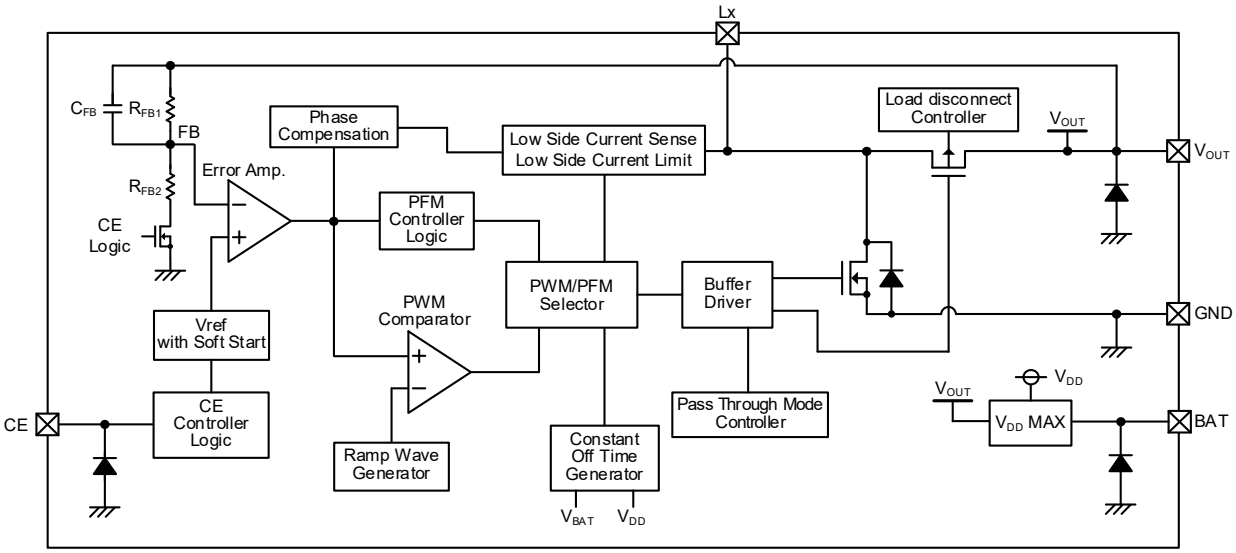
■ TYPICAL APPLICATION



■TYPICAL CHARACTERISTICS



■BLOCK DIAGRAM



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

■PRODUCT CLASSIFICATION

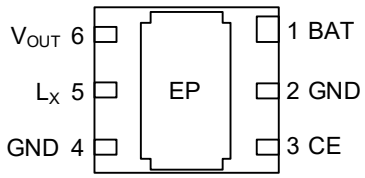
●Ordering Information

XC9145①②③④⑤⑥−⑦

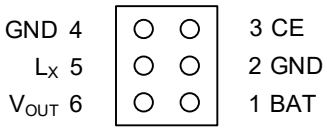
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	-
②③	Output Voltage	30 ~ 55	Output voltage options e.g. 3.0V → ②=3, ③=0
④	Oscillation Frequency	C	1.2MHz
⑤⑥−⑦(*1)	Packages (Order Unit)	ER-G	USP-6C (3,000pcs/Reel)
		0R-G	WLP-6-05 (5,000pcs/Reel)

(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

■PIN CONFIGURATION



USP-6C
(BOTTOM VIEW)



WLP-6-05
(BOTTOM VIEW)

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
USP-6C	WLP-6-05		
3	3	CE	Chip Enable
2,4	2,4	GND	Ground
1	1	BAT	Power Supply Input
6	6	V_{OUT}	Output Voltage
5	5	Lx	Switching
7	-	EP	Exposed thermal pad. The Exposed pad must be connected to GND(Pin2,4).

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
CE	L	Stand-by
	H	Active
	OPEN	Undefined State (*1)

* Do not leave the CE pin open.

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
BAT Pin Voltage		V_{BAT}	-0.3 ~ 6.6	V
Lx Pin Voltage		V_{Lx}	-0.3 ~ 6.6	V
V_{OUT} Pin Voltage		V_{OUT}	-0.3 ~ 6.6	V
CE Pin Voltage		V_{CE}	-0.3 ~ 6.6	V
Power Dissipation (Ta=25℃)	USP-6C	Pd	1250 (JESD51-7 board) (*1)	mW
	WLP-6-05		700 (JESD51-7 board) (*1)	
Junction Temperature		Tj	-40 ~ 125	℃
Storage Temperature		Tstg	-55 ~ 125	℃

* All voltages are described based on the GND pin.

(*1) The power dissipation figure is the one when IC is mounted on PCB and the figure is for reference only. Please refer to PACKAGING INFORMATION for the mounting condition.

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Voltage	V_{BAT}	0.65	-	5.5	V
Lx Pin Current (*1)	I_{LX}	-	-	2.0	A
CE Pin Voltage	V_{CE}	0.0	-	6.0	V
Operating Ambient Temperature	Topr	-40	-	105	℃
Input Capacitor (Effective Value)	C_{IN}	6.0 (*2)	-	1000 (*3)	μF
Output Capacitor (Effective Value)	C_L	8.0 (*2)	-	100 (*4)	μF
Inductor	L	3.76 (*5)	4.70 (*5)	5.64 (*5)	μH

* All voltages are described based on the GND pin.

(*1) Due to the Lx pin current, the junction temperature may cross over the maximum junction temperature. Please use within the range that does not cross over the maximum junction temperature.

(*2) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor considering the DC bias conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*3) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitor, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

(*4) If using a large-capacity capacitor as the output capacitor, it may not start during the soft start period, and the current limiting function may operate during startup.

(*5) Select an inductor with the saturation current (the DC superimposing characteristics) that is equal to or greater than the recommended component. Also, please use a shield type inductor to suppress noise leakage from the inductor.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V_{BAT}		-	-	5.5	V	①
Output Voltage (PFM)	V_{OUT_PFM}	$V_{BAT}=V_{OUT(T)}\times0.7$, $V_{OUT}=V_{OUT(T)}\times1.05\rightarrow V_{OUT(T)}\times0.95$ V_{OUT} Voltage when Lx pin voltage changes from “H” level to “L” level or starting oscillation(*1)	<E-1>	<E-2>	<E-3>	V	④
Output Voltage (PWM)	V_{OUT_PWM}	$V_{BAT}=V_{OUT(T)}\times1.05$, $V_{OUT}=V_{OUT(T)}\times1.03\rightarrow V_{OUT(T)}\times0.97$ V_{OUT} Voltage when Lx pin voltage changes from “H” level to “L” level or starting oscillation(*1)	<E-4>	<E-5>	<E-6>	V	④
Operation Start Voltage	V_{ST}	V_{BAT}=1.6V	-	-	1.6	V	①
Operation Hold Voltage	V_{HLD}	After output voltage stabilizes, V_{BAT}=1.6V→0.65V, I_{OUT}=1mA	-	0.65	-	V	①
Input Pin Current	Iq_bat	$V_{BAT}=V_{OUT(T)}$-1V, $V_{OUT}=V_{OUT(T)}\times1.04$ Lx pin open (No Switching)	-	5.0	100	nA	②
Quiescent Current	Iq		-	400	1300	nA	②
PWM Off Time	t_{OFF}	$V_{BAT}=V_{OUT(T)}\times0.45$, $V_{OUT}=V_{OUT(T)}\times0.9$, V_{Lx}=2.5V The time which Lx pin voltage changes from “L”→“H” level to “H”→”L” level (*1)	292	417	542	ns	⑥
Maximum On Time	t_{ON_MAX}	V_{BAT}=6.0V, $V_{OUT}=V_{OUT(T)}$-1V, V_{Lx}=2.3V The time which Lx pin voltage changes from “H”→“L” level to “L”→”H” level (*1)	2.5	4.8	8.0	μs	⑥
Minimum Duty Cycle	D_{MIN}	$V_{BAT}=V_{OUT(T)}$-1V, $V_{OUT}=V_{OUT(T)}\times1.04$, Lx pin open	-	-	0	%	②
PFM Switching Current	I_{PFM}	$V_{BAT}=V_{OUT(T)}\times0.8$, R_L=1kΩ The peak current flowing through the coil(*2)	-	200	280	mA	⑦
Efficiency	EFFI	V_{BAT}=2.4V, V_{OUT}=3.3V, I_{OUT}=10μA	-	89.9	-	%	①
		V_{BAT}=2.4V, V_{OUT}=3.3V, I_{OUT}=100mA	-	93.2	-		
Stand-by Current	I_{STB}	$V_{BAT}=V_{Lx}$=6.0V, $V_{OUT}=V_{CE}$=0.0V	-	0.0	0.1	μA	⑤
Lx SW "Pch" ON Resistance	R_{LXP}	$V_{BAT}=V_{LX}$=6.0V, I_{OUT}=200mA(*4)	-	270	-	mΩ	③
Lx SW "Nch" ON Resistance	R_{LXN}	V_{BAT}=6.0V	-	200	-	mΩ	-
Lx SW ”H” Leakage Current	I_{LXLH}	$V_{BAT}=V_{Lx}$=6.0V, $V_{OUT}=V_{CE}$=0.0V	-	0.0	0.1	μA	⑤
Lx SW ”L” Leakage Current	I_{LXLL}	$V_{BAT}=V_{CE}=V_{Lx}$=0.0V, V_{OUT}=6.0V	-	0.0	0.1	μA	②

$V_{OUT(T)}$: Target voltage

Test Conditions : unless otherwise stated, V_{CE}=2.0V

(*1) “H” level = V_{BAT} / V_{OUT}, “L” level = GND

(*2) I_{PFM} = Peak potential difference across RLX / 1Ω

(*3) Designed value

(*4) R_{LXP} = (V_{LX} - V_{OUT}) / 200mA

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUIT
Current Limit	I_{LIM}	V_{BAT}=6.0V The peak current flowing through the coil		<E-7>	<E-8>	<E-9>	A	①
Soft-Start Time	t_{SS}	V_{BAT}= $V_{OUT(T)}$×0.6, V_{OUT}=$V_{OUT(T)}$× 0.9, After "H" level (V_{CEH}) is fed to CE pin, the time by when clocks are generated at Lx pin		0.3	0.8	2.0	ms	④
CE "H" Voltage	V_{CEH}	V_{BAT}=$V_{OUT(T)}$×0.6, V_{OUT}=$V_{OUT(T)}$×0.9 V_{CE} Voltage when Lx pin voltage changes from "H" level to starting oscillation(*1)	Ta=25℃	1.50	-	6.00	V	④
			Ta=-40~105℃ (*3)	1.50	-	6.00		
CE "L" Voltage	V_{CEL}	V_{BAT}=$V_{OUT(T)}$×0.6,V_{OUT}=$V_{OUT(T)}$×1.04 V_{CE} Voltage when Input Pin Current (Iq_bat) increases from 0μA up to 0.5μA	Ta=25℃	GND	-	0.30	V	④
			Ta=-40~105℃ (*3)	GND	-	0.30		
CE "H" Current	I_{CEH}	V_{BAT}=V_{OUT}=V_{Lx}=V_{CE}=6.0V		-	0.0	0.1	μA	②
CE "L" Current	I_{CEL}	V_{BAT}=V_{OUT}=V_{Lx}=6.0V, V_{CE}=0.0V		-	0.0	0.1	μA	②

$V_{OUT(T)}$: Target voltage

Test Conditions : unless otherwise stated, V_{CE}=2.0V

(*1) "H" level = V_{BAT} / V_{OUT}, "L" level = GND

(*2) I_{PFM} = Peak potential difference across RLX / 1Ω

(*3) Designed value

(*4) R_{LXP} = (V_{LX} - V_{OUT}) / 200mA

■ELECTRICAL CHARACTERISTICS

SPEC. Table

NOMINAL OUTPUT VOLTAGE	V_{OUT_PFM}			V_{OUT_PWM}			I_{LIM}		
	<E-1>	<E-2>	<E-3>	<E-4>	<E-5>	<E-6>	<E-7>	<E-8>	<E-9>
UNITS	V	V	V	V	V	V	A	A	A
$V_{OUT(T)}$	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
3.0	2.940	3.000	3.090	2.940	3.000	3.060	0.88	1.30	2.00
3.1	3.038	3.100	3.193	3.038	3.100	3.162	0.89	1.30	2.00
3.2	3.136	3.200	3.296	3.136	3.200	3.264	0.89	1.30	2.00
3.3	3.234	3.300	3.399	3.234	3.300	3.366	0.89	1.30	2.00
3.4	3.332	3.400	3.502	3.332	3.400	3.468	0.89	1.30	2.00
3.5	3.430	3.500	3.605	3.430	3.500	3.570	0.90	1.30	2.00
3.6	3.528	3.600	3.708	3.528	3.600	3.672	0.90	1.30	2.00
3.7	3.626	3.700	3.811	3.626	3.700	3.774	0.90	1.30	2.00
3.8	3.724	3.800	3.914	3.724	3.800	3.876	0.91	1.30	2.00
3.9	3.822	3.900	4.017	3.822	3.900	3.978	0.91	1.30	2.00
4.0	3.920	4.000	4.120	3.920	4.000	4.080	0.91	1.30	2.00
4.1	4.018	4.100	4.223	4.018	4.100	4.182	0.91	1.30	2.00
4.2	4.116	4.200	4.326	4.116	4.200	4.284	0.92	1.30	2.00
4.3	4.214	4.300	4.429	4.214	4.300	4.386	0.92	1.30	2.00
4.4	4.312	4.400	4.532	4.312	4.400	4.488	0.92	1.30	2.00
4.5	4.410	4.500	4.635	4.410	4.500	4.590	0.92	1.30	2.00
4.6	4.508	4.600	4.738	4.508	4.600	4.692	0.93	1.30	2.00
4.7	4.606	4.700	4.841	4.606	4.700	4.794	0.93	1.30	2.00
4.8	4.704	4.800	4.944	4.704	4.800	4.896	0.93	1.30	2.00
4.9	4.802	4.900	5.047	4.802	4.900	4.998	0.94	1.30	2.00
5.0	4.900	5.000	5.150	4.900	5.000	5.100	0.94	1.30	2.00
5.1	4.998	5.100	5.253	4.998	5.100	5.202	0.94	1.30	2.00
5.2	5.096	5.200	5.356	5.096	5.200	5.304	0.94	1.30	2.00
5.3	5.194	5.300	5.459	5.194	5.300	5.406	0.95	1.30	2.00
5.4	5.292	5.400	5.562	5.292	5.400	5.508	0.95	1.30	2.00
5.5	5.390	5.500	5.665	5.390	5.500	5.610	0.95	1.30	2.00

■TEST CIRCUITS

※External Components
C_{IN} : 10μF (ceramic)
C_L : 10μF x 2 (ceramic)
L : 4.7μH

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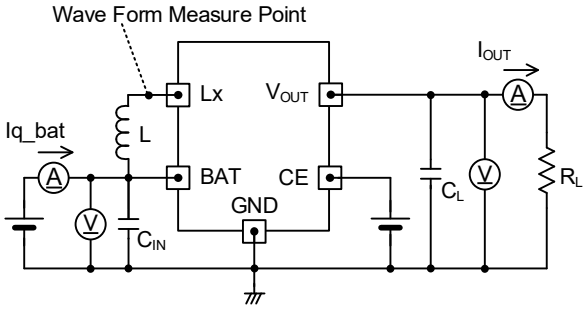

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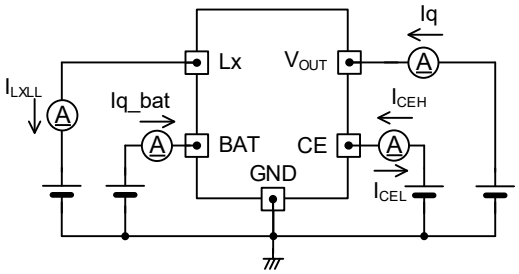

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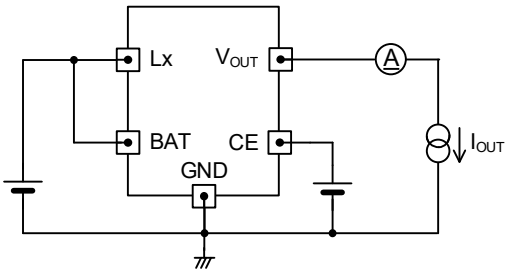

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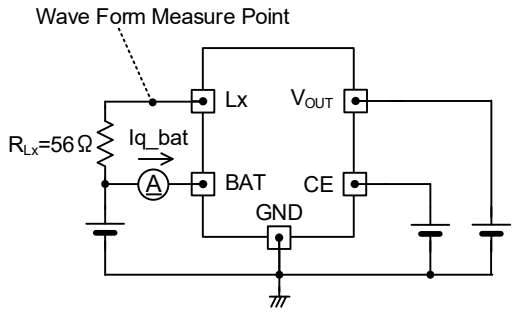

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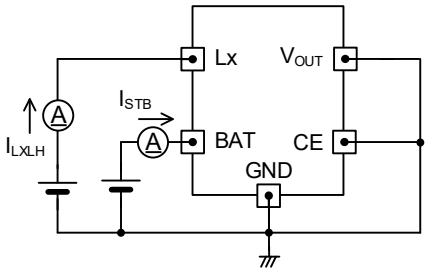

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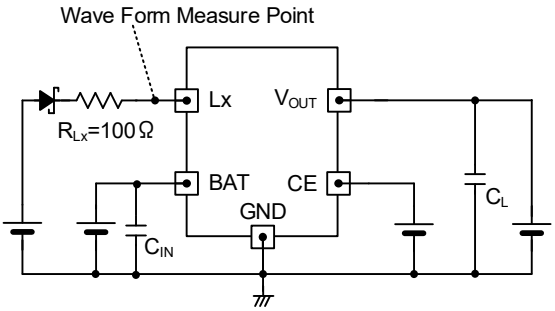

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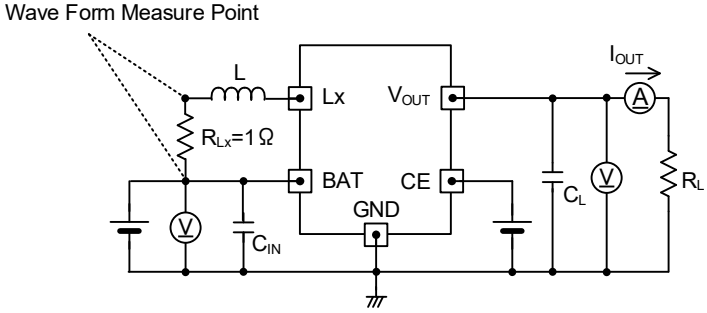
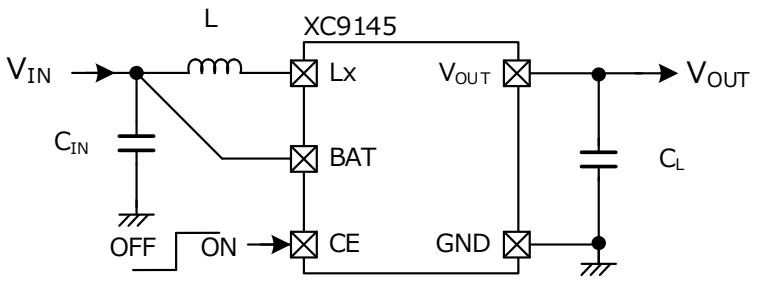


■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION GUIDE



【Typical Examples】

	CONDITIONS	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
L (*5)	-	Murata	DFE201612E-4R7M=P2	4.7μH	2.0x1.6x1.2mm
		Taiyo Yuden	MEKK2520U4R7M	4.7μH	2.5x2.0x1.0mm
		TDK	TMS252012ALM-4R7MTAA	4.7μH	2.5x2.0x1.2mm
		Murata	DFE252012F-4R7M=P2	4.7μH	2.5x2.0x1.2mm
		Würth Elektronik	74438336047	4.7μH	3.0x3.0x2.0mm
		Coilcraft	XGL4030-472	4.7μH	4.0x4.0x3.0mm
CIN (*1,2)	VOUT(T)≦3.3V	Murata	GRM188R61C106MA73	10μF/16V	1.6x0.8x0.8mm
	3.3V<VOUT(T)	Murata	GRM188R61C106MA73	10μF/16V x 2	1.6x0.8x0.8mm
CL (*1,3,4)	-	Murata	GRM188R61C106MA73	10μF/16V x 2	1.6x0.8x0.8mm

(*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor considering the DC bias conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitor, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

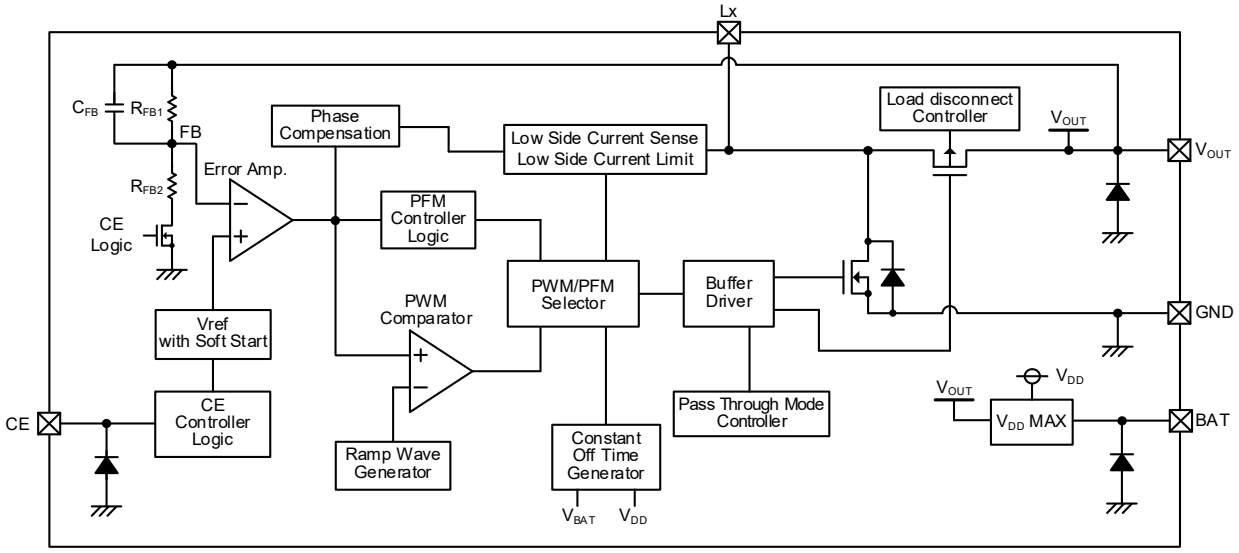
(*3) If a tantalum or low ESR electrolytic capacitor is used for the C_L, the ripple voltage will increase.
When an electrolytic capacitor is used for the C_L, connect a ceramic capacitor in parallel.
In addition, when a large-capacity ceramic capacitor, tantalum, low ESR electrolytic capacitor, etc. are used for the C_L, the output voltage may become unstable under heavy load.

(*4) If using a large-capacity capacitor as the output capacitor, it may not start during the soft start period, and the current limiting function may operate during startup.

(*5) Select an inductor with the saturation current (the DC superimposing characteristics) that is equal to or greater than the recommended component. Also, please use a shield type inductor to suppress noise leakage from the inductor.

■OPERATIONAL EXPLANATION

The XC9145 series consists of a reference voltage source, ramp wave circuit, error amplifier, PFM control circuit, PWM comparator, phase compensation circuit, constant off-time generation circuit, N-channel driver FET, P-channel synchronous rectification switching FET and current limiter circuit.



The phase compensation circuit optimizes the frequency feature of the error amplifier and it also modulates the output signal from the ramp wave generator monitoring the switching current of Nch driver FET during the on period. This provides a stable feedback system even when using low ESR capacitors such as ceramic capacitors and stabilizes the output voltage.

<Driver configuration / Load disconnect control (parasitic diode control).>

The built-in driver FET is a P-channel FET on the high side and an N-channel FET on the low side.

There is a parasitic diode whose source is the cathode, and the drain is the anode in general P-channel FET.

The internal circuit controls the polarity of the parasitic diode of P-channel FET on the High Side of the XC9145 series.

This parasitic diode control circuit compares the input voltage and the output voltage then it will select higher side as the cathode of the parasitic diode. This action prevents current from flowing through the parasitic diode during active and standby mode.

<V_{DD} MAX>

V_{DD} MAX circuit compares the input voltage and the output voltage then it will select the higher one as the power supply for the IC.

■OPERATIONAL EXPLANATION

＜Normal operation＞

The error amplifier compares the internal reference voltage and output feedback voltage through R_{FB1} and R_{FB2}. The phase compensation is applied to the output signal of the error amplifier, and the signal is input to the PFM controller and PWM comparator.

The PFM controller and PWM comparator determine the on-time of the N-channel driver FETs as follows.

PFM controller	: The time until the inductor current reaches the PFM current (I_{PFM}) is used as the ON time of the Nch driver FET.
PWM comparator	: Compares the output signal of the error amplifier and the ramp wave, which determine the ON time of the Nch driver FET.

In the PWM/PFM selection circuit, the on-time output by the PFM controller and PWM comparator is compared, and the pulse with the longer on-time is output.

In actual operation, when the output current is light load, it operates under PFM control.
PFM control keeps Low side Nch driver FET turning on until when the coil current reaches the PFM current (I_{PFM}). As a result, PFM control makes the switching frequency lower for the light load current condition compared to PWM control.

This operation reduces the loss under light load and makes it possible to achieve high efficiency from light load to heavy load. As the output current increases, the switching frequency increases proportionally.

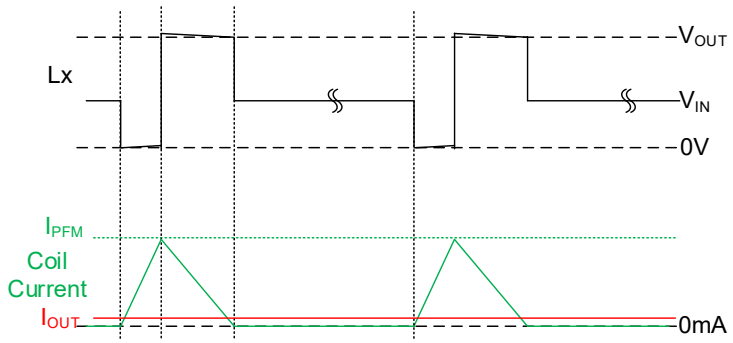
When the output current becomes larger, the peak current of the coil current becomes higher than I_{PFM}, and the PFM control shifts to the PWM control.
In PWM control, the PWM comparator compares the output signal of the error amplifier with the ramp wave to determine the on-time of the Nch driver FET.
The off time (t_{OFF}) is determined by the input voltage and output voltage and turns off the Nch driver FET for a certain period of time. The output voltage is stabilized by performing these controls continuously.

The off time is set as follows.

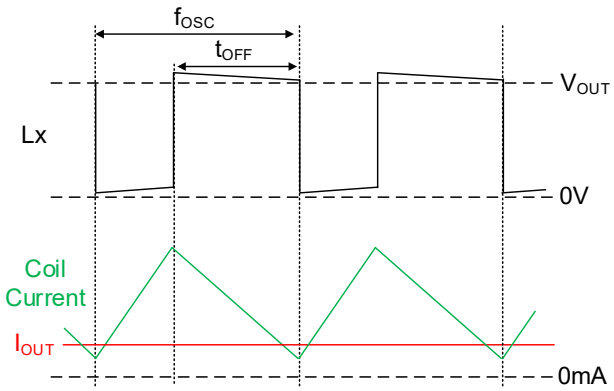
$$t_{OFF} = (V_{IN} / V_{OUT}) \times 833ns$$

In PWM control, it operates in continuous mode.
Since the off time is constant in continuous mode, the ideal oscillation frequency can be calculated by the following equation. However, in reality, the oscillation frequency deviates from the following equation due to the influence of on-resistance and loss of the driver FET.

$$f_{OSC} = (V_{IN} / V_{OUT}) \times (1 / t_{OFF})$$



Example of light load operation (PFM control)



Example of heavy load operation(PWM control)

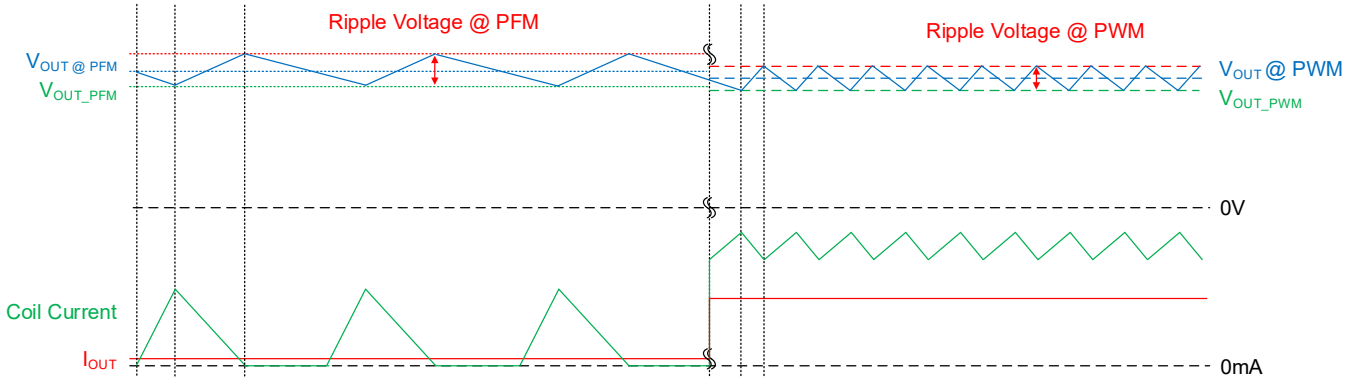
■OPERATIONAL EXPLANATION

＜Normal operation＞

The average output voltage V_{OUT} in actual operation depends on V_{OUT_PFM} and V_{OUT_PWM} and the ripple voltage. It can be calculated as follows.

Therefore, if the ripple voltage fluctuates due to the influence of input voltage, output voltage, peripheral parts, etc., the average value of the output voltage will fluctuate.

PFM control : $V_{OUT} = V_{OUT\_PFM}$ + Ripple Voltage x 1/2
PWM control : $V_{OUT} = V_{OUT\_PWM}$ + Ripple Voltage x 1/2



Example of output voltage operation waveform

$V_{OUT(T)} < V_{BAT}$

When the input voltage is higher than the set output voltage ($V_{OUT(T)} < V_{BAT}$), the Pch synchronous rectifier switch FET is turned on. The output voltage can be calculated by the input voltage minus the voltage drop which is based on the on-resistance of the Pch synchronous rectifier switch FET and the output current.

The current consumption is 6.5μA (TYP.).

■OPERATIONAL EXPLANATION

＜CE function / load disconnection function＞

When a "H" voltage (V_{CEH}) is input to the CE pin, the output voltage is raised by the start-up mode, and then normal operation starts.

When a "L" voltage (V_{CEL}) is input to the CE pin, the IC enters the standby mode, and the current consumption is reduced to the standby current I_{STB} (TYP. 0.0μA), and the Nch driver FET and Pch synchronous rectifier switch FET are turned off.

The load disconnection function operates in the standby mode. The load disconnection function compares the input voltage V_{BAT} and the output voltage V_{OUT}, and optimally controls the polarity of the parasitic diode for the Pch synchronous rectifier switch FET.

This control prevents the current from flowing into the parasitic diode of the Pch synchronous rectifier switch FET and cuts off the connection between the Lx and V_{OUT}.

＜Startup Mode / Soft Start＞

This function gradually boosts the V_{OUT} voltage from standby voltage to suppress the inrush current. When the "H" voltage is input to the CE pin and the IC is changed from the standby state to the active state, the start mode is started.

The detailed operation of the startup mode is as follows.

①$V_{OUT} \leqq V_{BAT}$

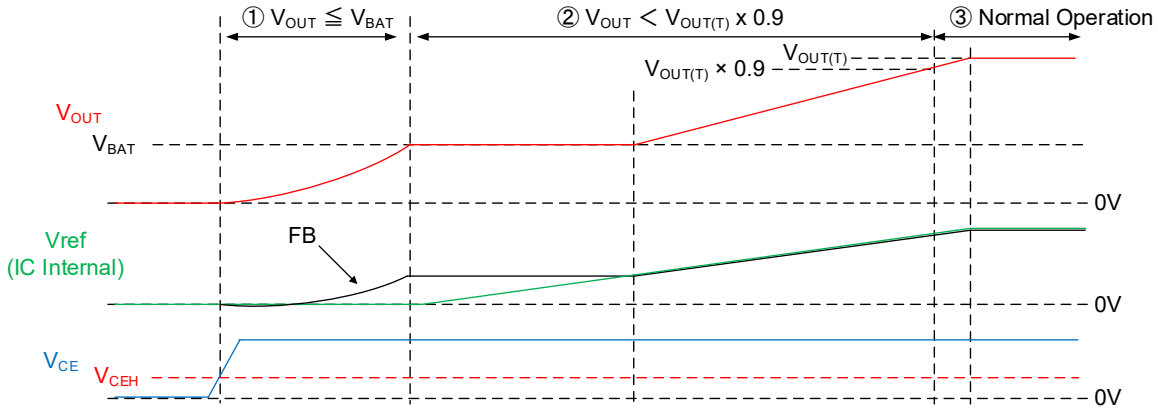
The current is supplied to the output side via Pch synchronous switching FET. Since the Pch synchronous switching FET supplies current to the output side while the current is limited, the V_{OUT} is gradually increased to V_{BAT}.

②$V_{OUT} < V_{OUT(T)} \times 0.9$

After the V_{OUT} voltage reaches to V_{BAT}, the internal reference voltage of the IC is raised slowly. When the FB voltage, which is the voltage divided by the V_{OUT} voltage with R_{FB1} and R_{FB2}, becomes lower than the internal reference voltage of the IC, the switching operation starts. The slope of the V_{OUT} voltage rise is proportional to the slope of the internal reference voltage of the IC.

③Normal operation

When the V_{OUT} voltage reaches $V_{OUT(T)} \times 0.9$, the start-up mode is terminated, and the device shifts to normal operation. However, under the condition of heavy load and large output capacitance, it may not be able to rise to $V_{OUT(T)} \times 0.9$ within the start-up period of the reference voltage. In this case, even if the V_{OUT} voltage is not reached to $V_{OUT(T)} \times 0.9$, the IC will shift from the start-up mode to normal operation after the completion of the start-up of the reference voltage.



Example of startup mode operation waveform

■OPERATIONAL EXPLANATION

＜Current Limit function＞

The current limit function of this IC monitors the current flowing in the Nch driver (=coil current) for each switching cycle, and when the current flowing through the Nch driver FET reached the current limit value I_{LIM} (TYP. 1.3A), it will be in the overcurrent detection state.

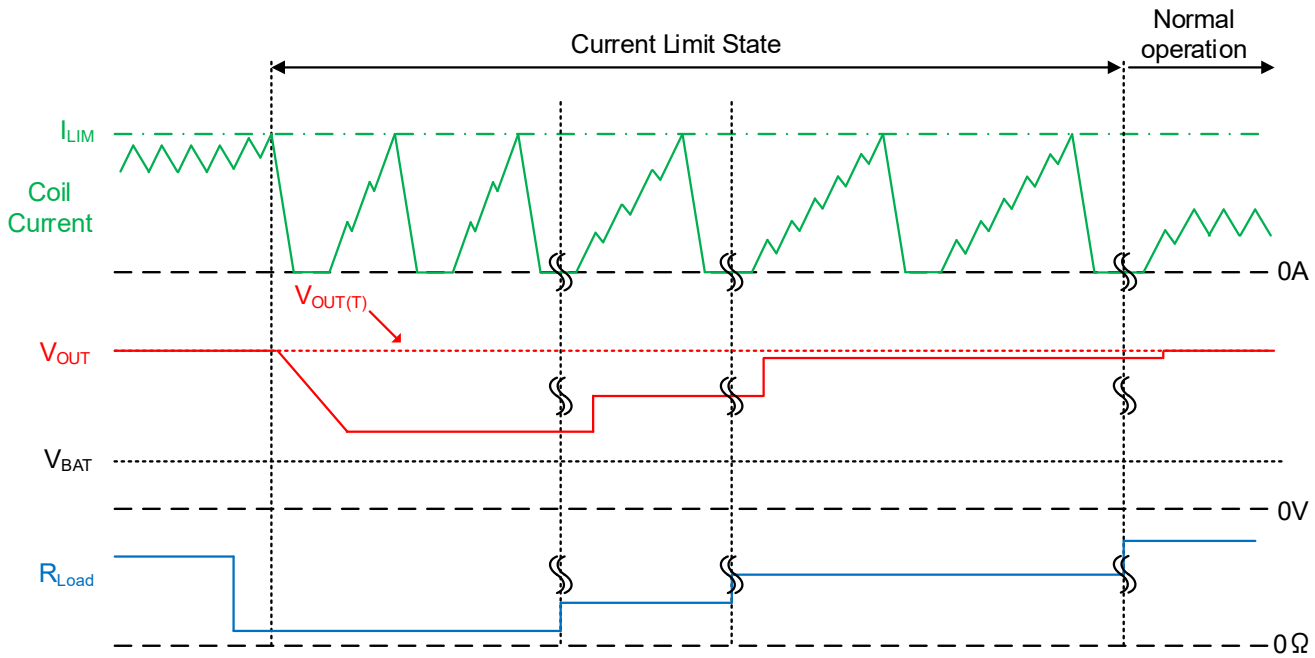
The overcurrent detection status and the operation after the overcurrent detection are as follows.

①If the current flowing in the Nch driver FET reaches the current limit value I_{LIM}, it will be in the overcurrent detection state. The internal circuit turns off Nch driver FET and it also lowers the output signal of the error amplifier.

②By lowering the output signal of the error amplifier, the Nch driver FET remains to turn off. The coil current keeps low level until the off time (t_{OFF}) has elapsed, the output signal of the error amplifier goes up and the boost operation resumes.

③When the output signal of the error amplifier goes up, the boost operation is restarted, and the current flowing in the Nch driver FET reaches the current limit value again, the Nch driver FET is turned off again and the output signal of the error amplifier is lowered.

④If overcurrent state continues, ① to ③ are repeated.



Example of current limiting operation waveform

■NOTES ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute maximum ratings.
Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

2) Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3) The DC/DC converter performance is greatly influenced by not only the ICs' characteristics, but also by those of the external components. Care must be taken when selecting the external components. Especially for capacitor, it is strongly recommended to use an appropriate capacitor according to the DC bias characteristics and temperature characteristics so that the effective capacitance value is equal to or greater than the recommended components under the actual usage conditions.

4) This IC is equipped with a control circuit that suppresses ringing of the Lx terminal voltage in discontinuous conduction mode to reduce conduction noise and radiation noise.
However, if the input voltage is 1V or less, the circuit that suppresses the ringing of the Lx terminal voltage may not operate and the ringing of the Lx terminal voltage may increase.
When using under these conditions, please make sure that there is no malfunction due to noise before using.

5) During PFM operation, when the operation state shifts from the boost operation to the condition of $V_{OUT(T)} < V_{BAT}$ where the boost operation is forcibly stopped and the Pch synchronous rectifier switch FET is continuously on, the operation may not shift smoothly and the output ripple voltage may increase to 500mV or more.
When used under these conditions, in order to transit the operation mode smoothly, please use ceramic capacitor as the output capacitor whose effective capacity is equivalent to "GRM188R61C106MA73" x3 or more.

6) When the voltage difference between the input voltage and the target output voltage is 0.3V or lower, the output ripple voltage increases.
Under this condition, if the lower output ripple voltage is required, use a ceramic capacitor which has the effective capacity of "GRM188R61C106MA73" x 3 or more as the output capacitor. In case when more lower output ripple voltage is required, take measures by increasing the output capacitance value.

7) Depending on the propagation delay time of the current limit circuit, a coil current exceeding the limit current value I_{LIM} may flow.

8) Under the following conditions, the current limit function may not operate.

The boost ratio is small
When the boost ratio is small, the required duty is low and the on-time of the Nch driver FET on the low side is short. If this on-time is shorter than the propagation delay of the current limit circuit, the current limit function may not operate.

The boost ratio is high
When the boost ratio is high, the coil current may be limited below the current limit value due to the maximum duty ratio, on resistance, and DCR of the coil, and the current limit function may not operate.

9) The current limit function is a function that limits the current flowing through the Nch driver FET, and does not limit the current flowing through the Pch synchronous switching FET.
Therefore, an overcurrent may flow in the parasitic diode of the Pch synchronous switching FET and the Pch synchronous switching FET, and the IC may be destroyed.
In particular, it is highly possible that the IC will be destroyed in an overloaded or short-circuited state, so it is recommended to protect the IC from overcurrent by using peripheral circuits.

■NOTES ON USE

10) If a power supply voltage is applied to the output from the outside, the IC may be damaged. Refer to the table below for whether or not an external voltage can be applied to the output under each operating condition.

Condition		Availability of applied voltage at V_{OUT} pin (Condition : $V_{OUT(T)}$ < Applied voltage)
V_{BAT}	CE	
V_{BAT}＜0.65V	L	Unusable
	H	
0.65V≦V_{BAT}＜$V_{OUT(T)}$	L	Available
	H	
$V_{OUT(T)}$≦V_{BAT}	L	Available
	H	Unusable (Reverse Flow toward the input)

11) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.

12) Note on mounting (WLP-6-05)

(a) Mount pad design should be optimized for user's conditions.

(b) Sn-AG-Cu is used for the package terminals. If eutectic solder is used, mounting reliability is decreased. Please do not use eutectic solder paste.

(c) When underfill agent is used to increase interfacial bonding strength, please take enough evaluation for selection. Some underfill materials and applied conditions may decrease bonding reliability.

(d) The IC has exposed surface of silicon material in the top marking face and sides so that it is weak against mechanical damages. Please take care of handling to avoid cracks and breaks.

(e) The IC has exposed surface of silicon material in the top marking face and sides. Please use the IC with keeping the circuit open (avoiding short-circuit from the out).

(f) Semi-transparent resin is coated on the circuit face of the package. Please be noted that the usage under strong lights may affects device performance.

■NOTES ON USE

●Instructions of pattern layouts

Especially noted in the pattern layout are as follows.
Please refer to the reference pattern layout on the next page.

(a) Wire the large current line using thick, short connecting traces.
This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation.
If the wire impedance of the large current line is large, it may cause noise or the IC may not operate normally.

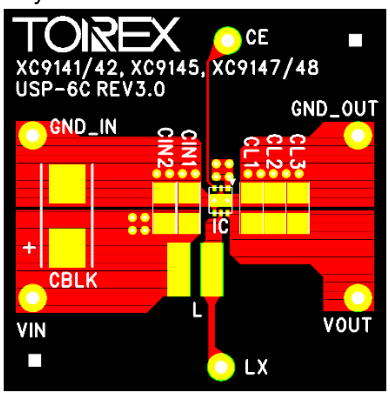
(b) Place the input capacitance C_{IN}, output capacitance C_L, inductor L and IC which the large current flows on the same surface. If they are placed on both sides, a large current will flow through Via, which has high impedance, it may cause noise and the IC may not operate normally.

(c) Please populate each external component as close to the IC as possible.
Especially place the output capacitance C_L near the IC and connect it with as low impedance as possible.
If the output capacity C_L and IC are too far apart, it may cause noise or the IC may not operate normally.

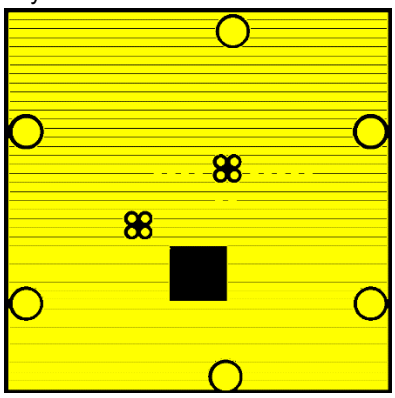
<Pattern layout>

USP-6C

Layer 1



Layer 2



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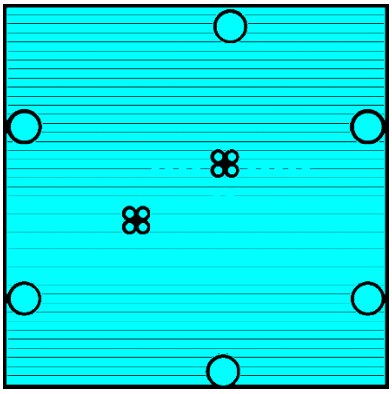

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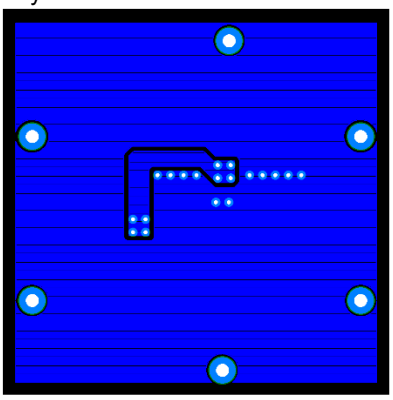
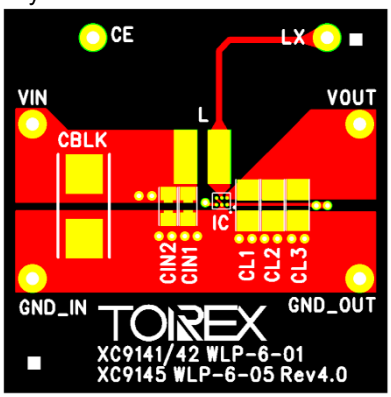


WLP-6-05

Layer 1



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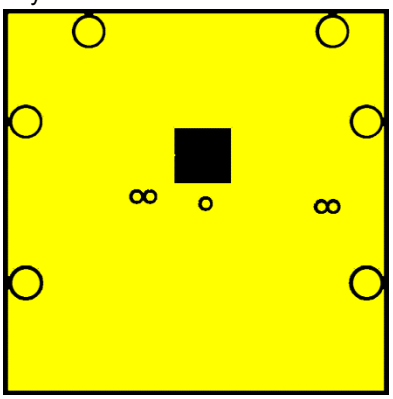

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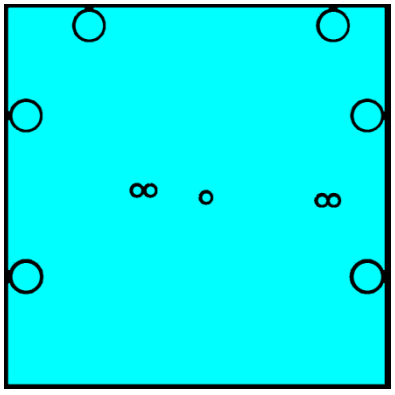

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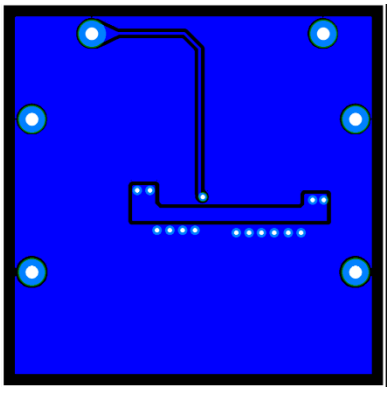
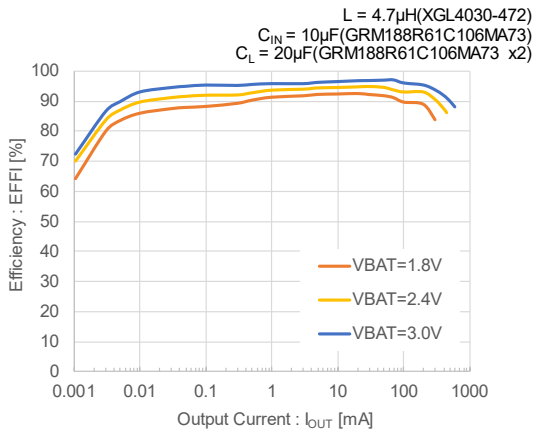


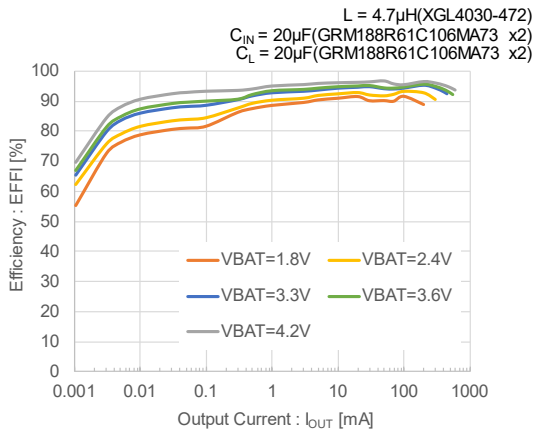
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

$V_{OUT(T)}$=3.3V

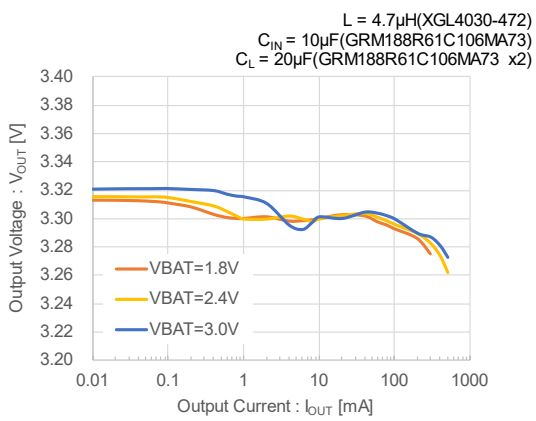


$V_{OUT(T)}$=5.0V

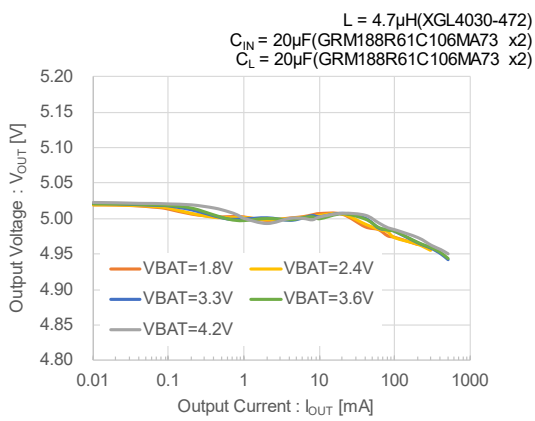


(2) Output Voltage vs. Output Current

$V_{OUT(T)}$=3.3V

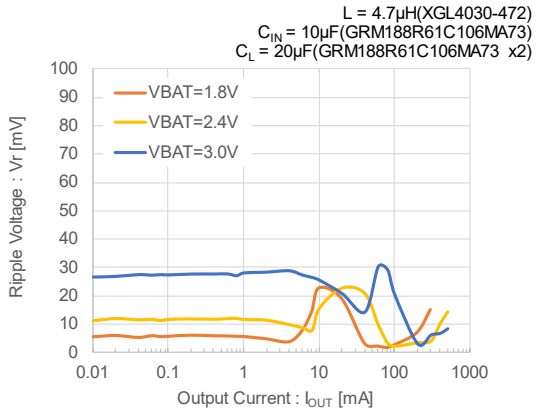


$V_{OUT(T)}$=5.0V

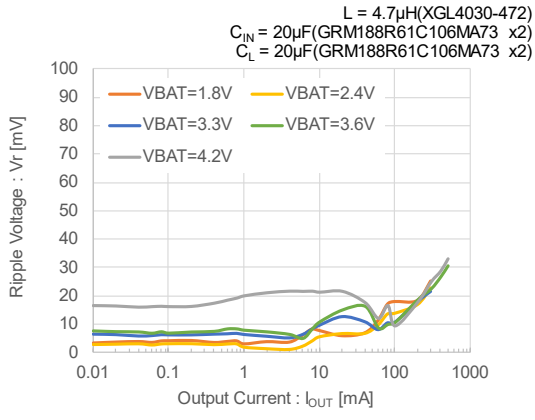


(3) Ripple Voltage vs. Output Current

$V_{OUT(T)}$=3.3V



$V_{OUT(T)}$=5.0V

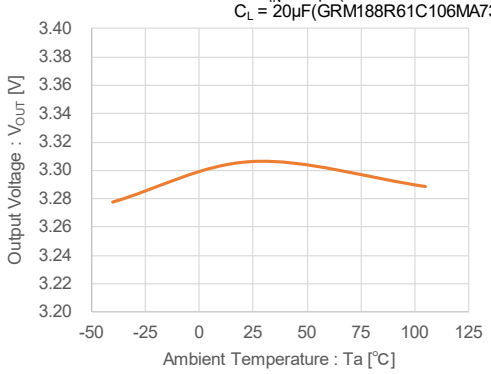


■TYPICAL PERFORMANCE CHARACTERISTICS

(4) Output Voltage vs. Ambient Temperature

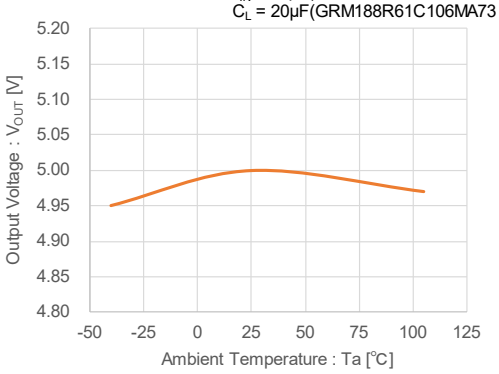
$V_{OUT(T)}$=3.3V

V_{BAT} = 2.5V, I_{OUT} = 100mA
L = 4.7μH(XGL4030-472)
C_{IN} = 10μF(GRM188R61C106MA73)
C_L = 20μF(GRM188R61C106MA73 x2)

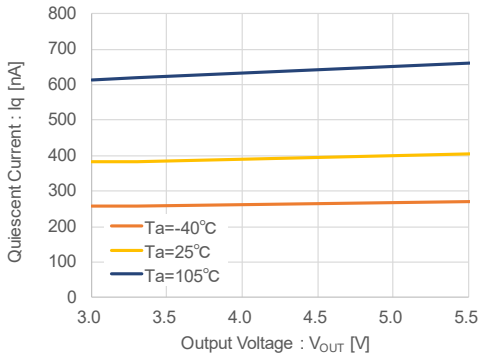


$V_{OUT(T)}$=5.0V

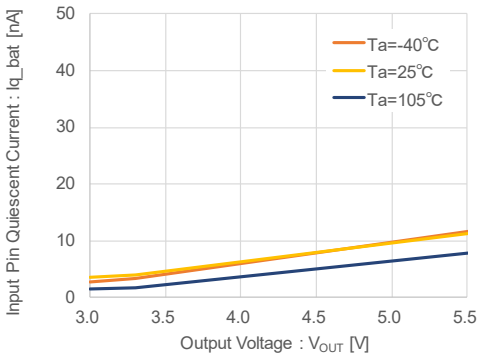
V_{BAT} = 3.7V, I_{OUT} = 100mA
L = 4.7μH(XGL4030-472)
C_{IN} = 20μF(GRM188R61C106MA73 x2)
C_L = 20μF(GRM188R61C106MA73 x2)



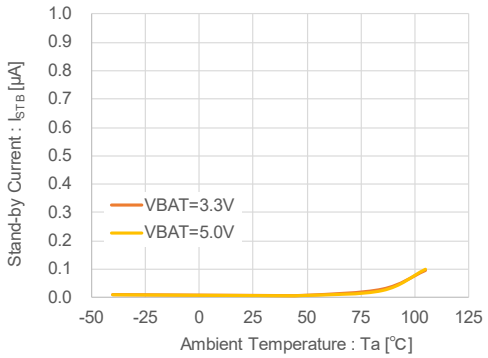
(5) Quiescent Current vs. Output Voltage



(6) Input Pin Qulescent Current vs. Output Voltage



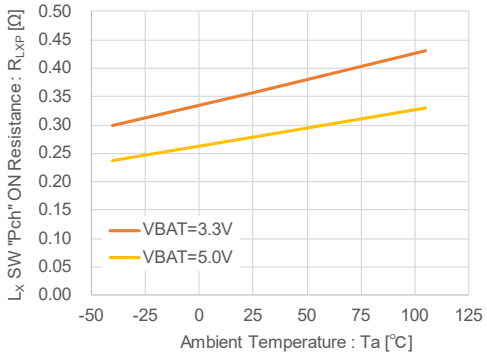
(7) Stand-by Current vs. Ambient Temperature



■TYPICAL PERFORMANCE CHARACTERISTICS

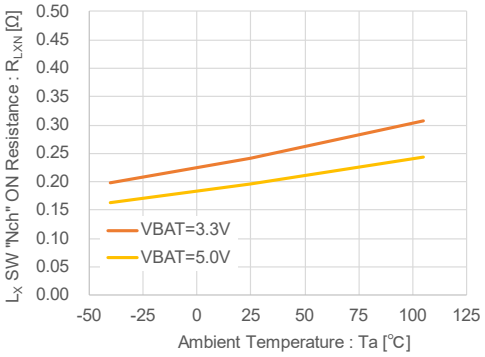
(8) Lx SW "Pch" ON Resistance vs. Ambient Temperature

XC9145BxxCER-G

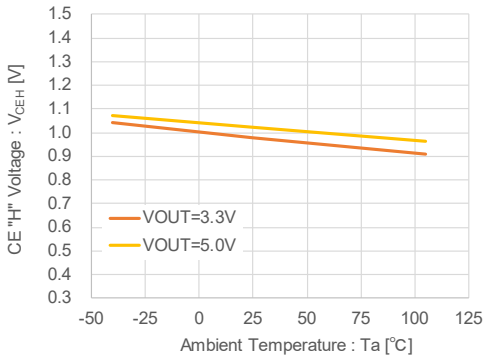


(9) Lx SW "Nch" ON Resistance vs. Output Voltage

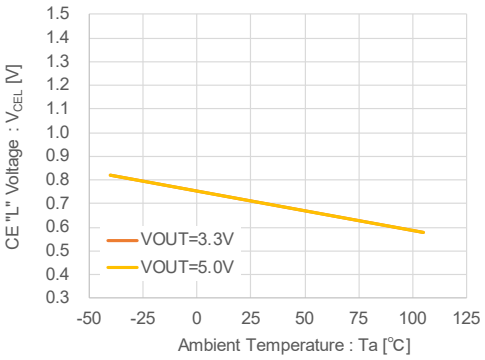
XC9145BxxCER-G



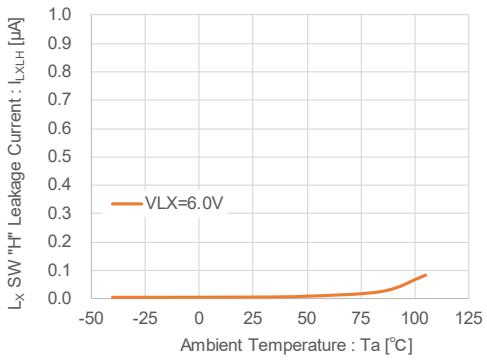
(10) CE "H" Voltage vs. Ambient Temperature



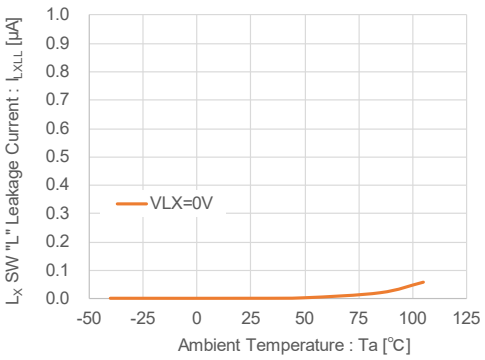
(11) CE "L" Voltage vs. Ambient Temperature



(12) Lx SW "H" Leakage Current vs. Ambient temperture



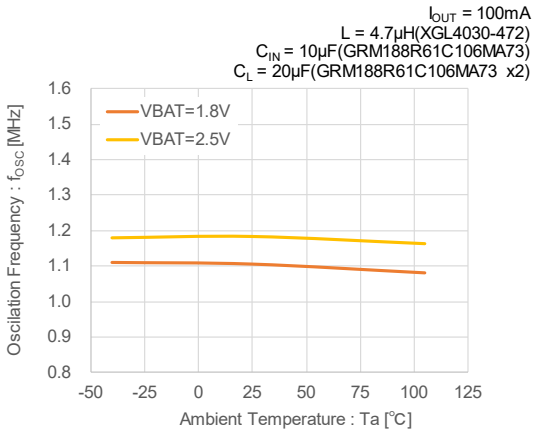
(13) Lx SW "L" Leakage Current vs. Ambient temperture



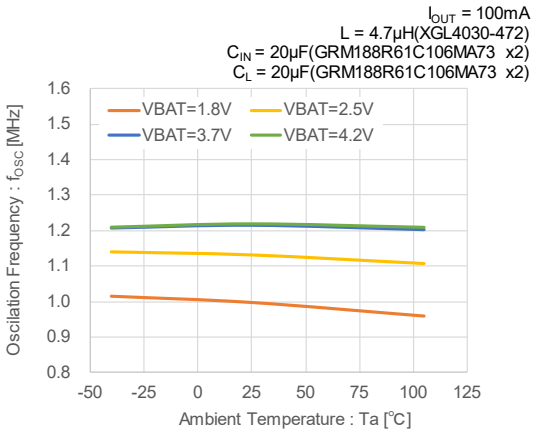
■TYPICAL PERFORMANCE CHARACTERISTICS

(14) Oscillation Frequency vs. Ambient temperture

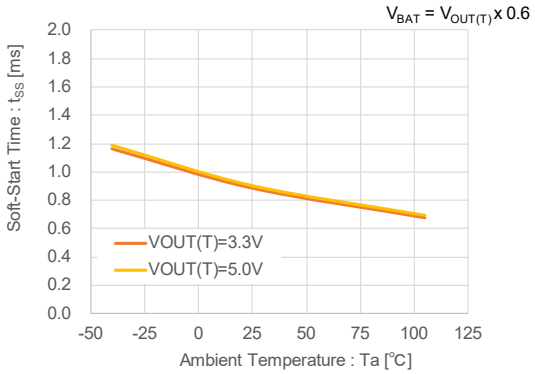
$V_{OUT(T)}$=3.3V



$V_{OUT(T)}$=5.0V

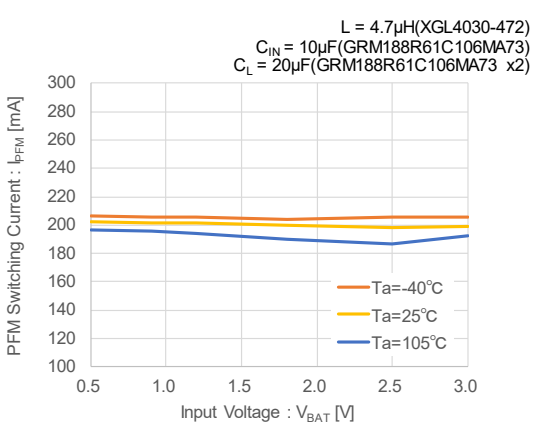


(15) Soft-Start Time vs. Ambient temperature

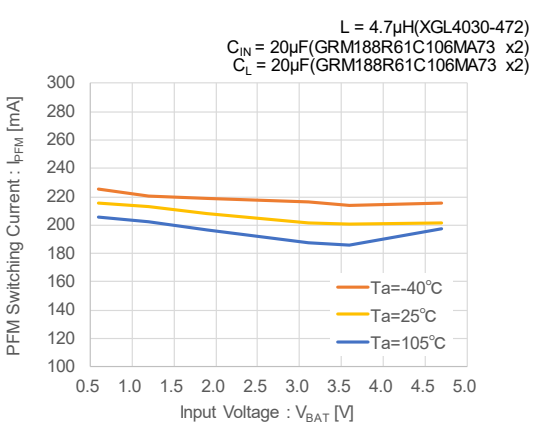


(16) PFM Switching Current vs. Input Voltage

$V_{OUT(T)}$=3.3V

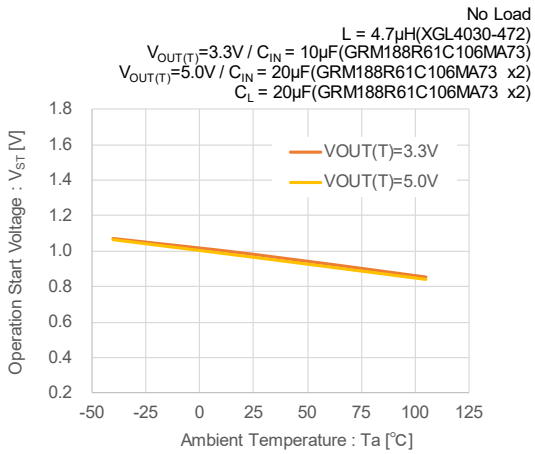


$V_{OUT(T)}$=5.0V

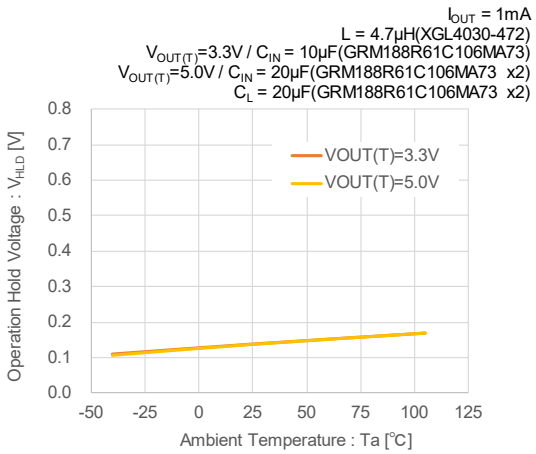


■TYPICAL PERFORMANCE CHARACTERISTICS

(17) Operation Start Voltage vs. Ambient temperture

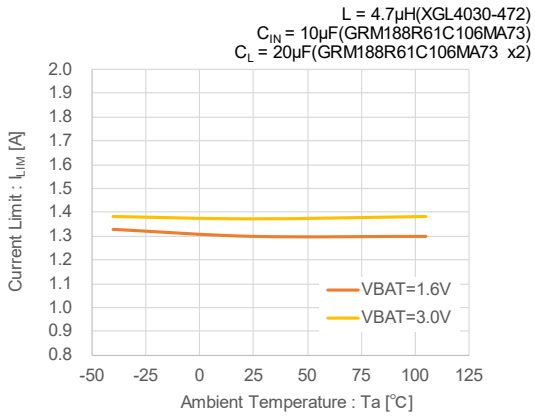


(18) Operation Hold Voltage vs. Ambient temperture

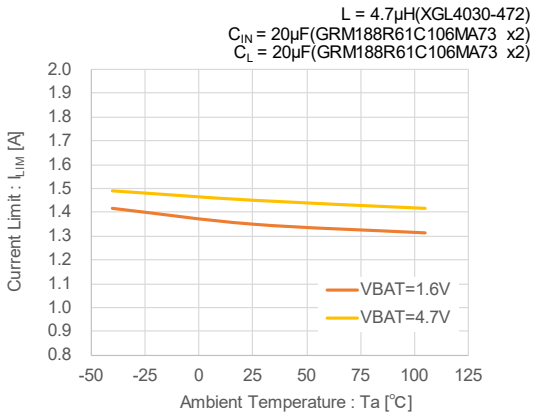


(19) Current Limit vs. Ambient temperture

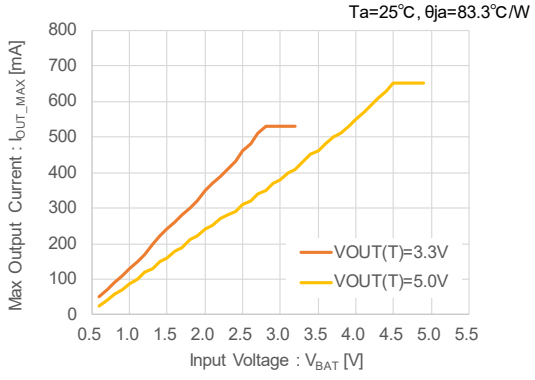
$V_{OUT(T)}$=3.3V



$V_{OUT(T)}$=5.0V



(20) Max Output Current vs. Input Voltage

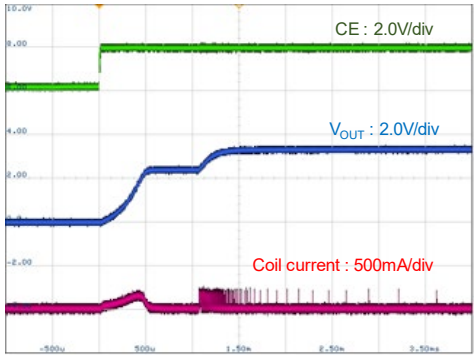


■TYPICAL PERFORMANCE CHARACTERISTICS

(21) Start-up Operation

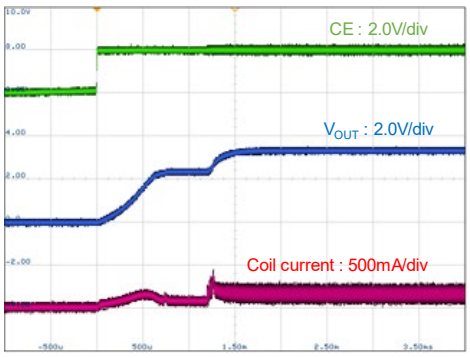
$V_{OUT(T)}$=3.3V

V_{BAT}=2.4V, No Load
L = 4.7μH(XGL4030-472)
C_{IN} = 10μF(GRM188R61C106MA73)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 500μs/div



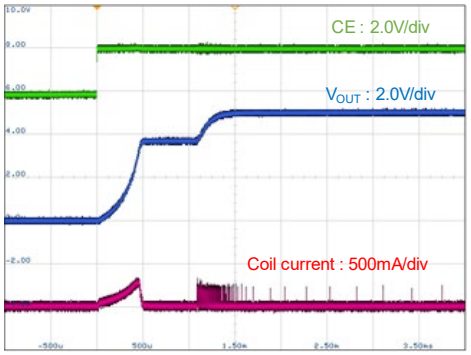
$V_{OUT(T)}$=3.3V

V_{BAT}=2.4V, I_{OUT}=100mA
L = 4.7μH(XGL4030-472)
C_{IN} = 10μF(GRM188R61C106MA73)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 500μs/div



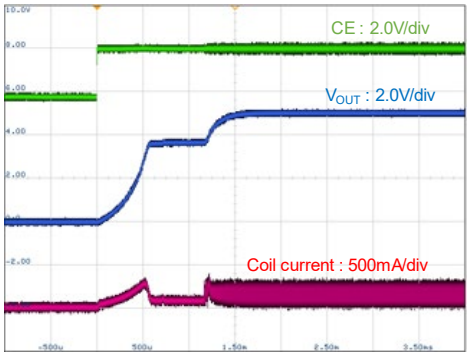
$V_{OUT(T)}$=5.0V

V_{BAT}=3.7V, No Load
L = 4.7μH(XGL4030-472)
C_{IN} = 20μF(GRM188R61C106MA73 x2)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 500μs/div



$V_{OUT(T)}$=5.0V

V_{BAT}=3.7V, I_{OUT}=100mA
L = 4.7μH(XGL4030-472)
C_{IN} = 20μF(GRM188R61C106MA73 x2)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 500μs/div

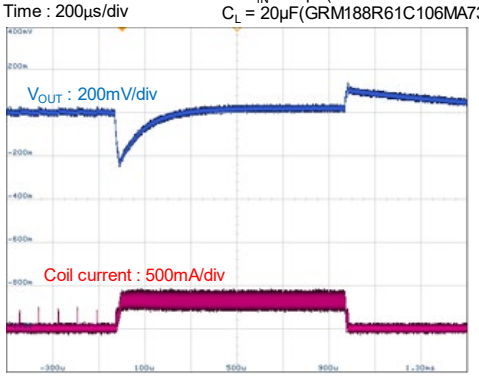


■TYPICAL PERFORMANCE CHARACTERISTICS

(22) Load Transient Response

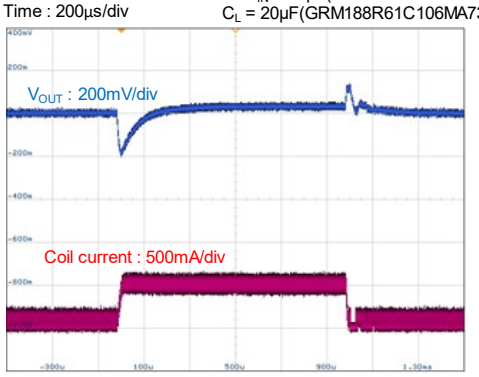
$V_{OUT(T)}$=3.3V

V_{BAT}=2.4V, I_{OUT}=1mA⇔200mA (tr/tf=250mA/μs)
L = 4.7μH(XGL4030-472)
C_{IN} = 10μF(GRM188R61C106MA73)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 200μs/div



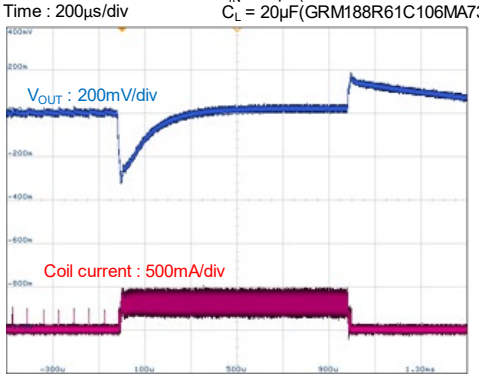
$V_{OUT(T)}$=3.3V

V_{BAT}=2.4V, I_{OUT}=50mA⇔300mA (tr/tf=250mA/μs)
L = 4.7μH(XGL4030-472)
C_{IN} = 10μF(GRM188R61C106MA73)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 200μs/div



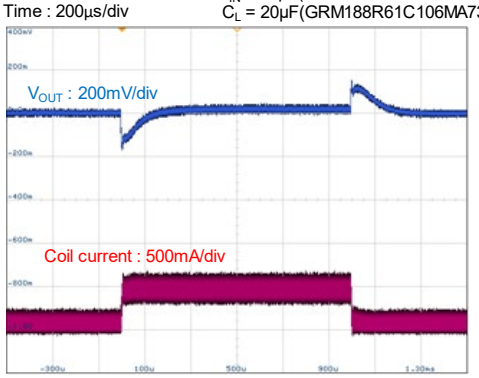
$V_{OUT(T)}$=5.0V

V_{BAT}=3.7V, I_{OUT}=1mA⇔200mA (tr/tf=250mA/μs)
L = 4.7μH(XGL4030-472)
C_{IN} = 20μF(GRM188R61C106MA73 x2)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 200μs/div



$V_{OUT(T)}$=5.0V

V_{BAT}=3.7V, I_{OUT}=50mA⇔300mA (tr/tf=250mA/μs)
L = 4.7μH(XGL4030-472)
C_{IN} = 20μF(GRM188R61C106MA73 x2)
C_L = 20μF(GRM188R61C106MA73 x2)
Time : 200μs/div



■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

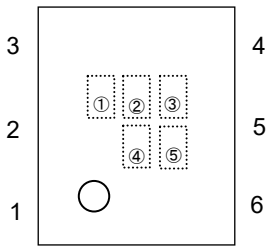
PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
USP-6C	USP-6C PKG	USP-6C Power Dissipation
WLP-6-05	WLP-6-05 PKG	WLP-6-05 Power Dissipation

■MARKING RULE

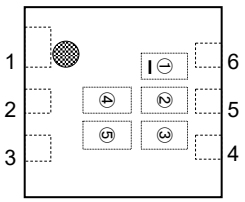
①represents product series

MARK	PRODUCT SERIES
B	XC9145******-G

WLP-6-05



USP-6C(with underline mark ①)



②represents output voltage and type

MARK	TYPE	Oscillation Frequency	PRODUCT SERIES
0	B	1.2MHz	XC9145B**C**-G

③represents output voltage

MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)
0	3.0	7	3.7	E	4.4	P	5.1
1	3.1	8	3.8	F	4.5	R	5.2
2	3.2	9	3.9	H	4.6	S	5.3
3	3.3	A	4.0	K	4.7	T	5.4
4	3.4	B	4.1	L	4.8	U	5.5
5	3.5	C	4.2	M	4.9		
6	3.6	D	4.3	N	5.0		

④, ⑤represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.
(G, I, J, O, Q, W excluded. No character inversion used.)

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

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4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. We assume no responsibility for damage or loss due to abnormal use.

8.

TOREX SEMICONDUCTOR LTD.

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>>Torex Semiconductor(特瑞仕)