MPQ7920

5V PMIC with Four 2A/2.5A/4.5A/4.5A Buck Converters, 5 LDOs, and Flexible System Settings via I²C and MTP, AEC-Q100

DESCRIPTION

The MPQ7920 is a complete power management solution that integrates four high-efficiency step-down DC/DC converters, five low-dropout regulators, and a flexible logic interface.

Constant-on-time (COT) control in the DC/DC converter provides fast transient response. The adjustable switching frequency (up to 2.75MHz) during CCM greatly reduces external inductor and capacitor value. Full protection features include UVLO, OCP, OVP, and thermal shutdown.

The output voltage is adjustable through the I²C bus or preset by the MTP (multiple-time programmable). The power-on/off sequence is also programmable via the MTP and can be controlled through I²C bus online.

The MPQ7920 requires a minimal number of external components, and is available in a space-saving QFN-26 (3.5mmx4.5mm) package with wettable flanks. This part is AEC-Q100 qualified.

FEATURES

- **High-Efficiency Step-Down Converters**
  - Buck 1: 4.5A DC/DC Converter
  - Buck 2: 2.5A DC/DC Converter
  - Buck 3: 4.5A DC/DC Converter
  - Buck 4: 2A DC/DC Converter
  - Buck 1 and Buck 3 Can Work in Parallel
  - Buck 2 and Buck 4 Can Work in Parallel
  - 2.7V to 5.5V Operating Input Range
  - 0.4V to 3.58V/12.5mV Step or 0.4V to 2.2V/7.4mV Step Option V_{OUT} Range for Buck 1, Buck 2, and Buck 3
  - 0.4V to 3.58V/12.5mV step V_{OUT} Range for Buck 4
  - Adjustable Switching Frequency
  - Adjustable Soft-Start Time
  - Adjustable Phase Delay
  - Programmable Forced PWM, Auto-PFM, PWM Mode
  - Output OCP, OVP
- **Low-Dropout Regulators**
  - One RTC Dedicated LDO
  - Four Low-Noise LDOs
  - Two Separate Input Power Supplies
  - 50mV Dropout at 300mA Load
- **System**
  - I²C Bus and User Programmable MTP
  - Two-Time Programmable MTP (1)
  - Power-On/Off Control
  - Multi-Function LDO2/EN1 Pin (EN1 Input Logic Level ≤ 3.3V)
  - Power-On Reset Output
  - Flexible Power-On/Off Sequence via MTP (0.5ms/2ms/8ms/16ms Selectable Time Slot)
  - Flexible DC/DC, LDO On/Off via the MTP
  - ±4kV HBM and ±2kV CDM ESD Rating for All Pins
  - Available in a QFN-26 (3.5mmx4.5mm) Package
  - Available in AEC-Q100 Grade 1

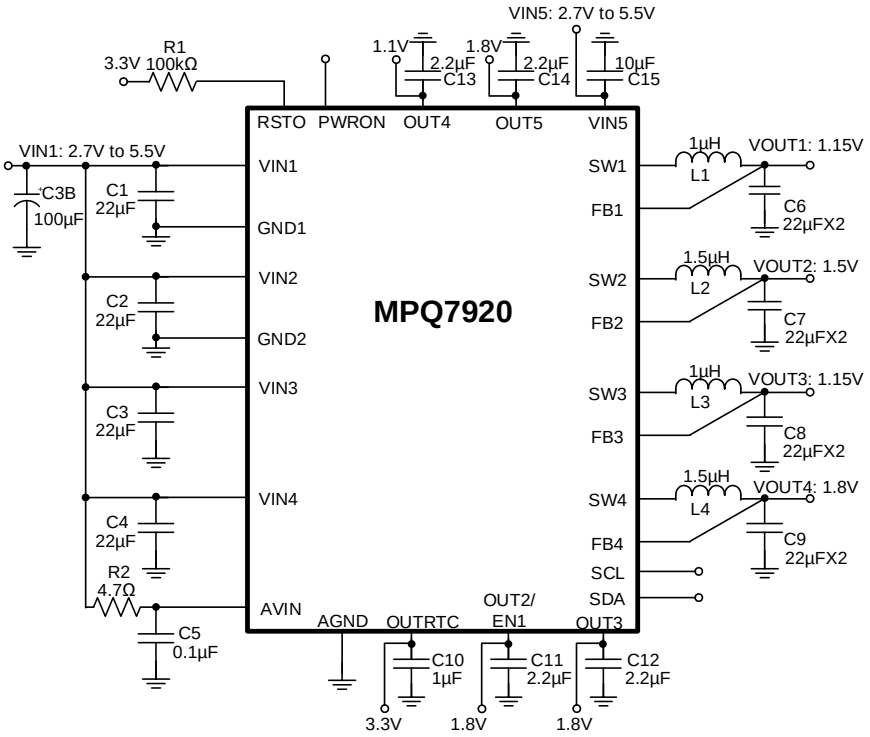
Note:

1) The two-time programmable MTP is only for the standard version of the MPQ7920GRM-0000-AEC1 (see page 41).

APPLICATIONS

- Automotive Infotainment
- Automotive Video Recorder
- Automotive Display Electronics

TYPICAL APPLICATION



MTP E-FUSE SELECTED TABLE BY DEFAULT (MPQ7920GRM-0003):

OTP Items	Buck 1	Buck 2	Buck 3	Buck 4	LDORTC	LDO2	LDO3	LDO4	LDO5
Output voltage	1.15V	1.5V	1.15V	1.8V	3.3V	1.8V	1.8V	1.1V	1.8V
Initial on/off	On	On	On	On	On	On	On	On	On
Mode	FPWM	FPWM	FPWM	FPWM	N/A				
Power-on delay	0ms	4.5ms	0ms	4.5ms	Always on	5.5ms	5.5ms	5.5ms	9.5ms
Soft-start time	300µs	300µs	300µs	300µs	N/A				
Switching frequency	2.2MHz								
PWRON MODE	0 (level trigger)								
RSTODELAY	50ms								
Buck 1 peak current limit	9.3A								
Buck 2 peak current limit	6.1A								
Buck 3 peak current limit	9.3A								
Buck 4 peak current limit	6.1A								
I²C slave address	0x69								
MTP configure code	0003								

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ7920GRM-xxxx-AEC1**	QFN-26 (3.5mmx4.5mm)	*See Below*	*1*
MPQ7920GRM-0003-AEC1	QFN-26 (3.5mmx4.5mm)	*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MPQ7920GRM-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the OTP.

The default number is “0003”. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0003” code.

MPQ7920GRM-0003-AEC1 is the default version, which can be MTP 1 time.
MPQ7920GRM-0000-AEC1 is the standard version for sampling, which can be MTP 2 times.

TOP MARKING

MPSYW
M7920
LLLLL

MPS: MPS prefix
Y: Year code
W: Week code
M7920: Part number
LLLLL: Lot number

EVALUATION KIT EVKT-MPQ7920

EVKT-MPQ7920 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVQ7920-R-00A	MPQ7920GRM evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I²C communication interface device, one USB cable, and one ribbon cable	1
3	MPQ7920-0000	MPQ7920 IC, which can be used for MTP programming	2

Order direct from MonolithicPower.com or our distributors.

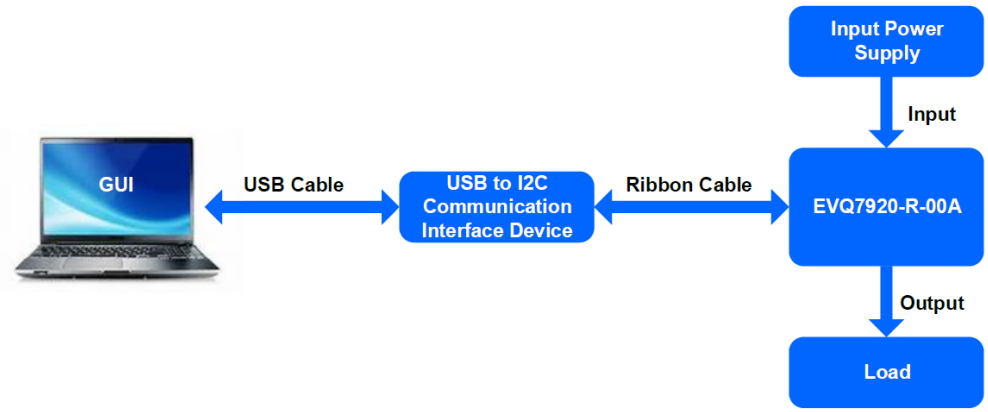
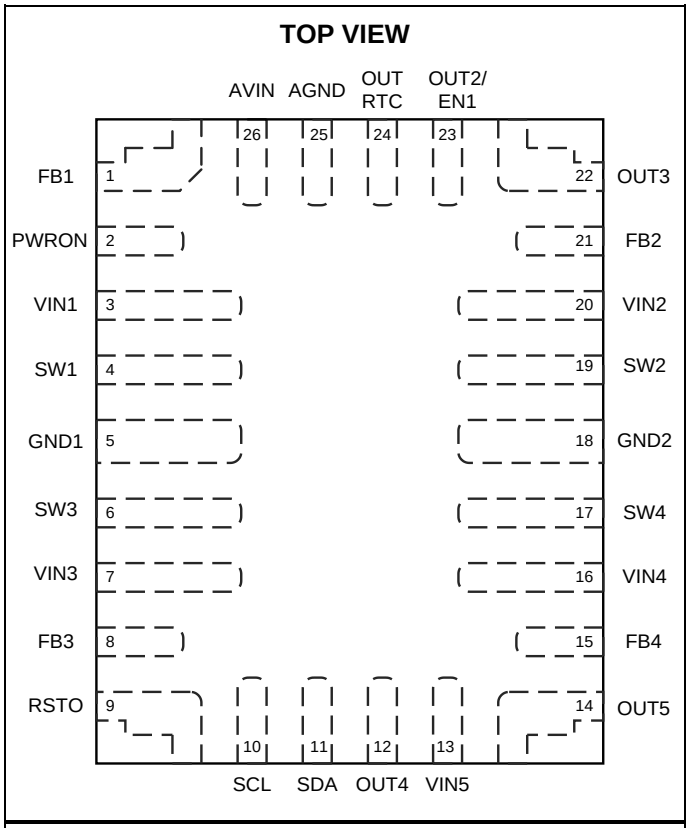


Figure 1: EVKT-MPQ7920 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-26 (3.5mmx4.5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	FB1	**Feedback of buck 1.** Connect buck 1's output directly to this pin.
2	PWRON	**Power-on/off input.** Logic input pin to start up or shut down the device. This pin should be pulled high by an external voltage.
3	VIN1	**Buck 1 supply voltage input.** The MPQ7920 operates from a 2.7V to 5.5V input rail. It requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage.
4	SW1	**Buck 1 switch output.** Connect using a wide PCB trace.
5	GND1	**Buck 1 and buck 3 power ground.** Requires special consideration during PCB layout. Connect to GND with copper traces and vias.
6	SW3	**Buck 3 switch output.** Connect using a wide PCB trace.
7	VIN3	**Buck 3 supply voltage input.** The MPQ7920 operates from a 2.7V to 5.5V input rail. It requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage.
8	FB3	**Buck 3 feedback.** Directly connect buck 3's output to this pin.
9	RSTO	**Reset output from the PMIC to CPU.** Open-drain output. This pin requires an external pull-up resistor.
10	SCL	**I²C clock signal input.**
11	SDA	**I²C data pin.**

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
12	OUT4	**LDO4 output.** LDO4 is powered by VIN5.
13	VIN5	**LDO4 and LDO5 power input pin.** VIN5 operates from a 2.7V to 5.5V input voltage. Connect VIN5 to VIN1 if LDO4 and LDO5 are not used.
14	OUT5	**LDO5 output.** LDO5 is powered by VIN5.
15	FB4	**Buck 4 feedback.** Directly connect buck 4's output to this pin.
16	VIN4	**Buck 4 supply voltage input.** The MPQ7920 operates from a 2.7V to 5.5V input rail. It requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage.
17	SW4	**Buck 4 switch output.** Connect using a wide PCB trace.
18	GND2	**Buck 2 and buck 4 power ground.** This pin requires special consideration during PCB layout. Connect to GND with copper traces and vias.
19	SW2	**Buck 2 switch output.** Connect using a wide PCB trace.
20	VIN2	**Buck 2, LDORTC, LDO2, and LDO3 supply voltage input.** The MPQ7920 operates from a 2.7V to 5.5V input rail. It requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage.
21	FB2	**Buck 2 feedback.** Directly connect buck 2's output to this pin.
22	OUT3	**LDO3 output.** LDO3 is powered by VIN2.
23	OUT2/EN1	**LDO2 output or EN1.** LDO2 is powered by VIN2. When configuring this pin as EN1, it acts as an input pin. Pull EN1 up or down to enable or disable the MPQ7920, respectively.
24	OUTRTC	**RTC LDO output.** This LDO is powered by VIN2.
25	AGND	**Analog ground.** Connect this pin to GND1 and GND2.
26	AVIN	**Power supply input for logic circuitry.** Bypass this pin with a 0.1µF ceramic capacitor to AGND. Connect AVIN to the system input through a 4.7Ω resistor. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage.

ABSOLUTE MAXIMUM RATINGS (1)

$V_{VIN1, VIN2, VIN3, VIN4, VIN5, AVIN}$ .... -0.3V to +6.5V (6.8V for 300ms)
V_{SWx}..... -0.6V (-5V for <10ns) to V_{IN} + 0.3V (7V for <10ns)
V_{EN1} ..... -0.3V to +3.5V
All other pins..... -0.3V to +6.25V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-26 (3.5mmx4.5mm).....6.25W
Junction temperature.....150°C
Lead temperature..... 260°C
Storage temperature.....-65°C to +150°C

ESD Ratings (3)

All other pins (HBM) .....±4kV
All pins (CDM) .....±2kV

Recommended Operating Conditions (4)

Step-down regulator (V_{IN}).....2.7V to 5.5V
Step-down regulator (V_{OUT}).....0.4V to 3.5875V or V_{IN}
LDO regulator (V_{OUTL}).....0.65V to 3.5875V or V_{IN}
Operating junction temp (T_J) .... -40°C to +125°C (5)

Thermal Resistance θ_{JA} θ_{JC}

QFN-26 (3.5mmx4.5mm)		
EVQ7920-R-00A (6)	20	5 °C/W
JESD51-7 (7)	44	9 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may cause excessive die temperature, and the regulator can go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions.
5) Operating devices at junction temperatures greater than 125°C is possible; contact MPS for details.
6) Measured on EVQ7920-R-00A, 4-layer PCB.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = AVIN = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted. (8)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (no switching)	I_{IN}	No switching, feedback is high, T_J = 25°C		300	600	μA
Shutdown current	I_{IN_STD}	All regulators disabled except LDORTC, T_J = 25°C		30	60	μA
		All regulators disabled except LDORTC, T_J = -40°C to +125°C		30	120	μA
Default oscillation frequency	f_{SW}		1.8	2.2	2.4	MHz
Thermal shutdown entry threshold (9)	T_{OTP_R}			153		°C
Thermal shutdown recovery threshold (9)	T_{HYS}			130		°C
Step-Down Regulator						
AVIN UVLO rising	V_{AIN1_R}		2.4	2.55	2.7	V
AVIN UVLO hysteresis	V_{AIN1_HYS}			300		mV
VIN1 UVLO rising	V_{IN1_R}		2.3	2.45	2.6	V
VIN1 UVLO hysteresis	V_{IN1_HYS}			300		mV
VIN2 UVLO rising	V_{IN2_R}		2.35	2.5	2.65	V
VIN2 UVLO hysteresis	V_{IN2_HYS}			300		mV
VIN3 UVLO rising	V_{IN3_R}		2.3	2.45	2.6	V
VIN3 UVLO hysteresis	V_{IN3_HYS}			300		mV
VIN4 UVLO rising	V_{IN4_R}		2.3	2.45	2.6	V
VIN4 UVLO hysteresis	V_{IN4_HYS}			300		mV
VIN5 UVLO rising	V_{IN5_R}		2.3	2.45	2.6	V
VIN5 UVLO hysteresis	V_{IN5_HYS}			300		mV
Feedback voltage accuracy	V_{FB1}	Default output of buck 1	1.127	1.15	1.173	V
	V_{FB2}	Default output of buck 2	1.47	1.5	1.53	V
	V_{FB3}	Default output of buck 3	1.127	1.15	1.173	V
	V_{FB4}	Default output of buck 4	1.764	1.8	1.836	V
Maximum duty cycle (9)	D_{MAX}	Buck 1 to buck 4		100		%
Buck 1, Buck 3 (4.5A/4.5A)						
HS-FET on resistance	$HS_{RDS-ON1}$	500mA, T_J = 25°C		25	35	mΩ
	$HS_{RDS-ON3}$					
	$HS_{RDS-ON1}$	500mA, T_J = -40°C to +125°C		25	45	mΩ
	$HS_{RDS-ON3}$					

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = AVIN = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted. (8)

Parameter	Symbol	Condition	Min	Typ	Max	Units
LS-FET on resistance	$LS_{RDS-ON1}$	500mA, T_J = 25°C		12	16	mΩ
	$LS_{RDS-ON3}$					
	$LS_{RDS-ON1}$	500mA, T_J = -40°C to +125°C		12	20	mΩ
	$LS_{RDS-ON3}$					
Switch leakage 1	HSW_{ILK1}	EN = 0V, V_{IN} = 5.5V, SW = 0V or 5.5V, T_J = 25°C		0	1	μA
	HSW_{ILK3}					
Switch leakage 2	LSW_{ILK1}	EN = 0V, V_{IN} = 5.5V, SW = 0V or 5.5V, T_J = 25°C		0	1	μA
	LSW_{ILK3}					
High-side current limit	I_{LIMIT1}	T_J = -40°C to +125°C	7.4	9.3	11.4	A
	I_{LIMIT3}	T_J = -40°C to +125°C	7.4	9.3	11.4	A
Minimum on time (9)	t_{ON_MIN1}			50		ns
	t_{ON_MIN3}			50		ns
Minimum off time (9)	t_{OFF_MIN1}			120		ns
	t_{OFF_MIN3}			120		ns
Output discharge resistance	R_{O_DIS1}		3	7	20	Ω
Soft-start time	t_{SS_B1}	V_{OUT} = 10% to 90%	140	300	430	μs
	t_{SS_B3}	V_{OUT} = 10% to 90%	140	300	430	μs
Output OVP rising threshold	V_{OVP1_H}		115	120	125	% V_{REF}
Output OVP recovery threshold	V_{OVP1_L}		105	110	115	% V_{REF}
Buck 2, Buck 4 (2.5A/2A)						
HS-FET on resistance	$HS_{RDS-ON2}$	500mA, T_J = 25°C		40	55	mΩ
	$HS_{RDS-ON4}$					
	$HS_{RDS-ON2}$	500mA, T_J = -40°C to +125°C		40	70	mΩ
	$HS_{RDS-ON4}$					
LS-FET on resistance	$LS_{RDS-ON2}$	500mA, T_J = 25°C		40	55	mΩ
	$LS_{RDS-ON4}$					
	$LS_{RDS-ON2}$	500mA, T_J = -40°C to +125°C		40	85	mΩ
	$LS_{RDS-ON4}$					
Switch leakage 3	HSW_{ILK2}	Shutdown, V_{IN} = 5.5V, SW = 0V or 5.5V, T_A = 25°C		0	1	μA
	HSW_{ILK4}					
Switch leakage 4	LSW_{ILK2}	Shutdown, V_{IN} = 5.5V, SW = 0V or 5.5V, T_A = 25°C		0	1	μA
	LSW_{ILK4}					
High-side current limit	I_{LIMIT2}		4.6	6.1	7.5	A
	I_{LIMIT4}		4.6	6.1	7.5	
Minimum on time (9)	t_{ON_MIN2}			50		ns
	t_{ON_MIN4}			50		ns
Minimum off time (9)	t_{OFF_MIN2}			100		ns
	t_{OFF_MIN4}			100		ns
Output discharge resistance	R_{O_DIS2}		3	7.5	20	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = AVIN = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted. (8)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start time	t_{SS_B2}	V_{OUT} = 10 to 90%	140	300	430	µs
	t_{SS_B4}	V_{OUT} = 10 to 90%	140	300	430	µs
Output OVP rising threshold	V_{OVP2_H}		115	120	125	% V_{REF}
Output OVP recovery threshold	V_{OVP2_L}		105	110	115	% V_{REF}
10mA RTC LDO						
Default output voltage	V_{RTC_LDO}	I_{OUT} = 10mA, power-on state	3.24	3.37	3.5	V
Ground current	I_{Q_RTC}	No load		6.5		µA
Dropout voltage	V_{DROP1}	V_{OUT} = 3V, I_{OUT} = 5mA		50		mV
Current limit	I_{LIM_RTC}	V_{IN} = 3.3V, V_{OUT} drops 33%, T_J = 25°C	25	55	85	mA
Soft-start slew rate	t_{SS_RTC}	V_{OUT} = 10% to 90%, C_{OUT} = 1µF		25		mV/µs
Low-Dropout LDO Regulator: LDO2 to LDO5						
Output voltage	V_{LDO2}	I_{OUT} = 10mA	1.764	1.8	1.836	V
	V_{LDO3}	I_{OUT} = 10mA	1.764	1.8	1.836	V
	V_{LDO4}	I_{OUT} = 10mA	1.078	1.1	1.122	V
	V_{LDO5}	I_{OUT} = 10mA	1.764	1.8	1.836	V
PSRR (8)	$PSRR_{1K}$	For LDO4 and LDO5, V_{OUT} = 1.8V		52		dB
Dropout voltage	V_{DROP1}	V_{OUT} = 3V, I_{OUT} = 300mA		50		mV
Current limit	I_{LIMIT_LDO}	For LDO2 and LDO3, V_{IN} = 3.3V, V_{OUT} drops 33%	300	430	600	mA
	$I_{LIMIT\_LDO\_L}$	LDO4 and LDO5 set ILIM bit = 0, V_{IN} = 3.3V, V_{OUT} drops 33%	380	520	660	mA
	$I_{LIMIT\_LDO\_H}$	LDO4 and LDO5 set ILIM bit = 1, V_{IN} = 3.3V, V_{OUT} drops 33%	580	790	1000	mA
Output discharge resistance	R_{O_DIS2}		3	7	20	Ω
Soft-start time	t_{SS_B2}	V_{OUT} = 10% to 90%, C_{OUT} = 2.2µF		50		µs
Line regulation		VIN2 = VIN5 = 2.7V to 5.5V		0.3		%/V
Load regulation		VIN2 = VIN5 = 3.3V, Iout from 10mA to 100mA		0.5		%
Logic Pins						
PWRON pull-up current	I_{PWRON}	Internal pull-up to AVIN	5	9	13	µA
PWRON rising threshold	V_{PWR_R}		0.8	1	1.2	V
PWRON voltage hysteresis	V_{PWR_HYS}			100		mV
EN1 rising threshold	V_{EN1_R}		0.8	1	1.2	V
EN1 rising hysteresis	V_{EN1_HYS}			100		mV
PG rising threshold	V_{PG_R}	RSTO_MODE = 01	86%	90%	94%	V_{FB}
PG falling threshold	V_{PG_F}	RSTO_MODE = 01	76%	80%	84%	V_{FB}
PFI rising threshold	V_{PFI_R}	RSTO_PFI_THLD = 01, adjustable via the I²C/MTP	2.78	2.9	3.02	V

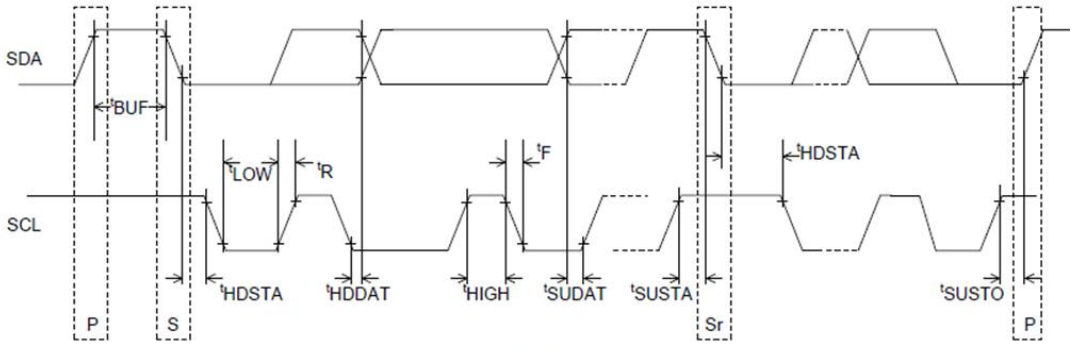
ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = AVIN = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted. (8)

Parameter	Symbol	Condition	Min	Typ	Max	Units
PFI hysteresis	V_{PFI_HYS}			7%		V_{PFI_R}
RSTO rising delay	t_{RSTO}	Adjustable via the I²C/MTP	20	50	70	ms
I²C Interface Specifications (10)						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	V_{OUT_L}	RSTO pin sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				3.4	MHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			70		ns
Set-up time for repeated start	t_{SU_STA}		160			ns
Hold time for repeated start	t_{HD_STA}		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	t_{SU_STO}		160			ns
SCL and SDA rise time	t_R		10		300	ns
SCL and SDA fall time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Notes:

8) Tested with default version MPQ7920GRM-0003-AEC1.
9) Guaranteed by engineering sample characterization.
10) It is recommended to begin operating the I²C function after the power-on sequence is complete (all enabled power rails have finished starting up). See the I²C timing chart below when reading I²C interface specifications.



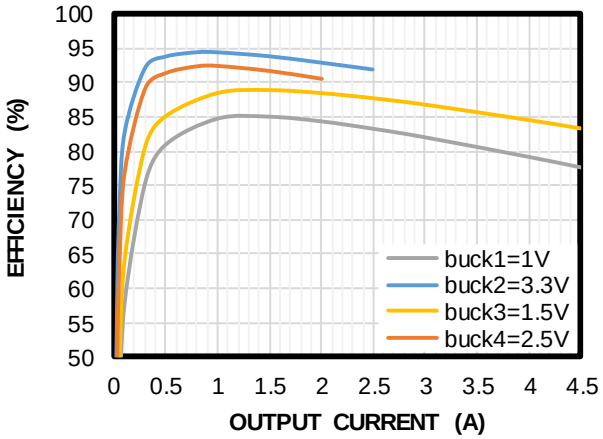
I²C Timing Diagram

TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using MPQ7920-0003 parts, unless otherwise noted.

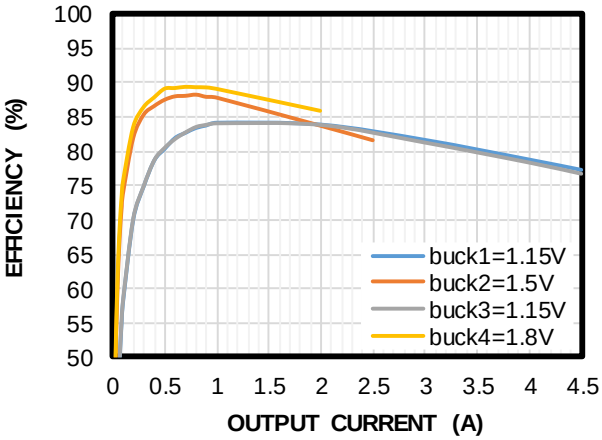
Efficiency

V_{IN} = 5V, f_{SW} = 1.65MHz, buck 1 through buck 4 work in PWM mode

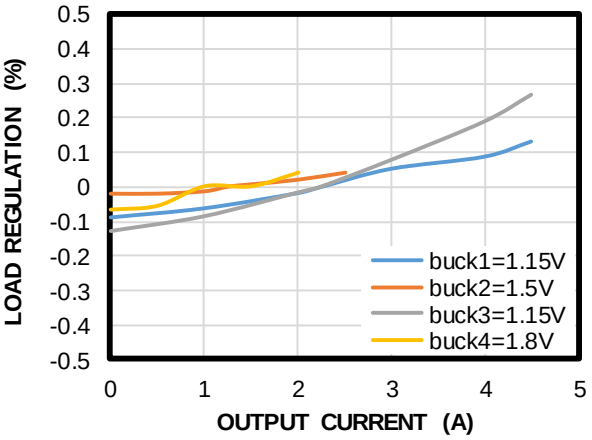


Efficiency

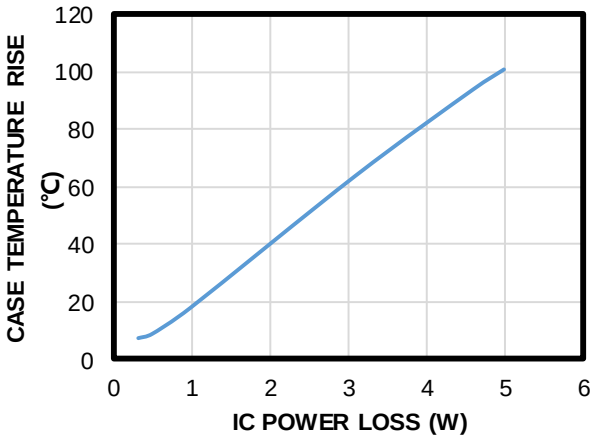
V_{IN} = 5V, f_{SW} = 2.2MHz, buck 1 through buck 4 work in PWM mode



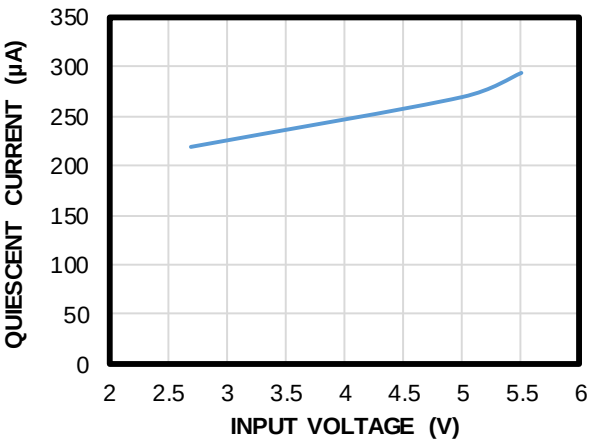
Load Regulation



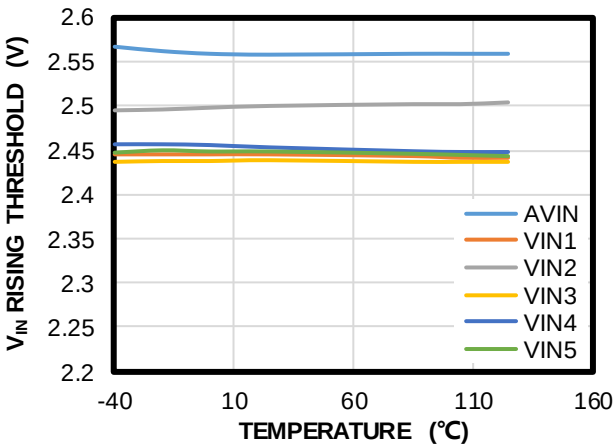
IC Power Dissipation vs. Case Temperature Rise



Quiescent Current vs. Input Voltage



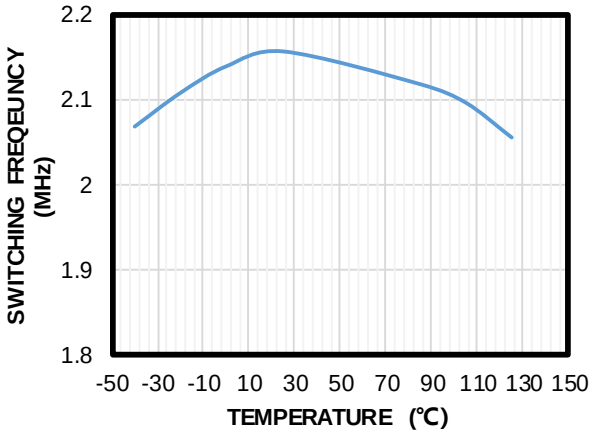
V_{IN} Rising Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using MPQ7920-0003 parts, unless otherwise noted.

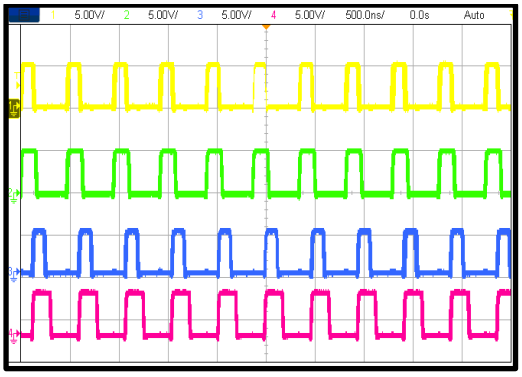
Switching Frequency vs. Temperature



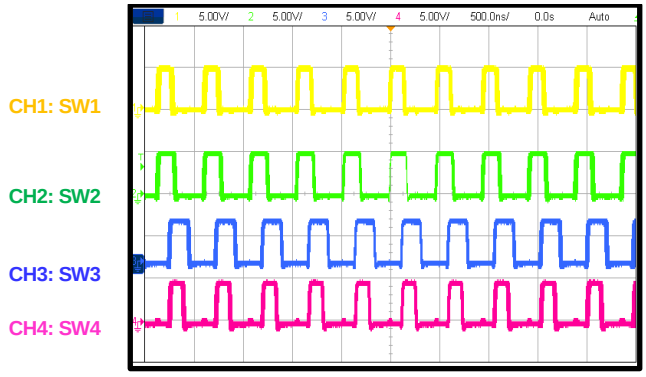
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using MPQ7920-0003 parts, unless otherwise noted.

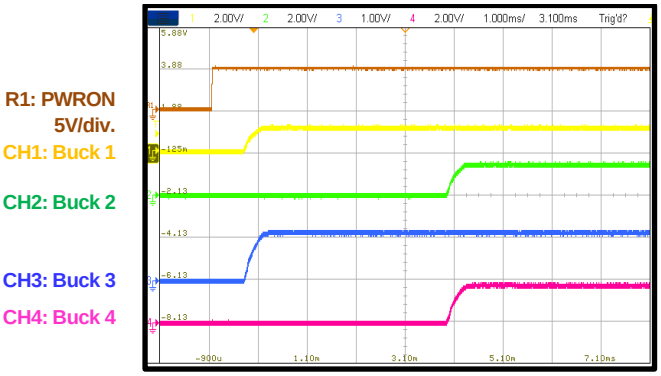
Steady State
All buck rails with no load



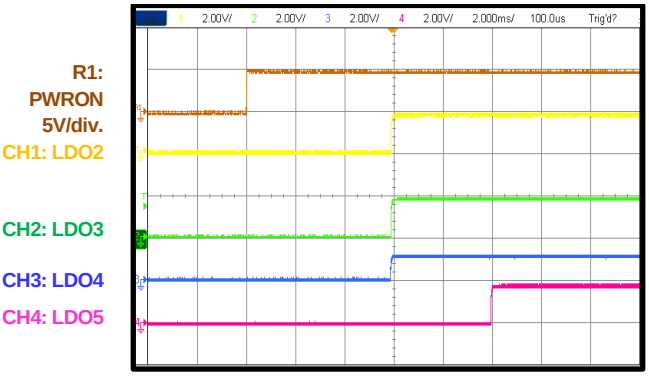
Steady State
All buck rails with full load



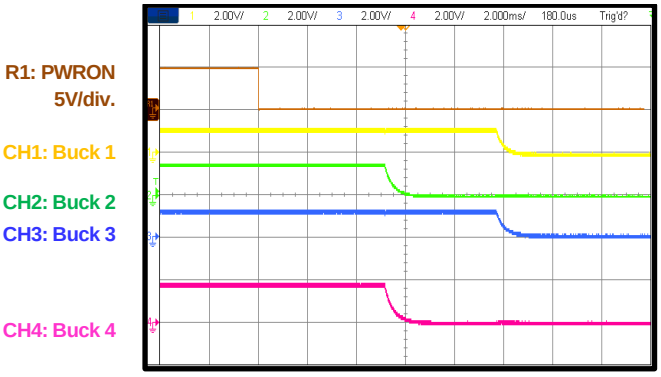
PWRON On
All buck rails without load



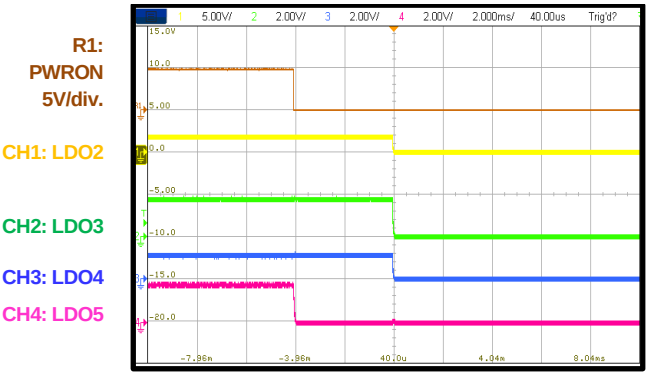
PWRON On
All LDO rails without load



PWRON Off
All buck rails without load



PWRON Off
All LDO rails without load, disable all buck rails

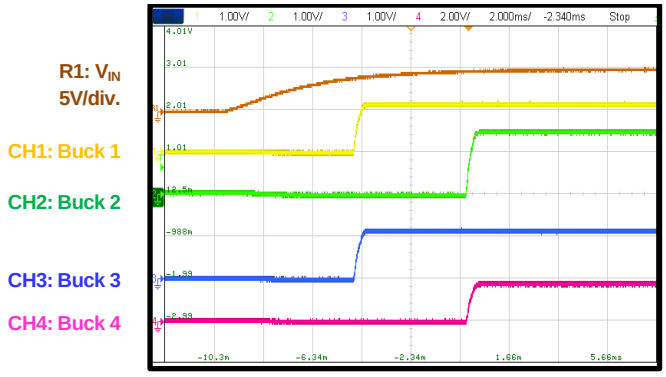


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using MPQ7920-0003 parts, unless otherwise noted.

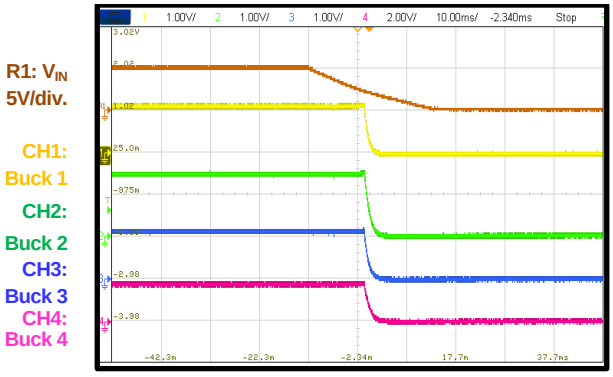
VIN Start-Up

All buck rails without load



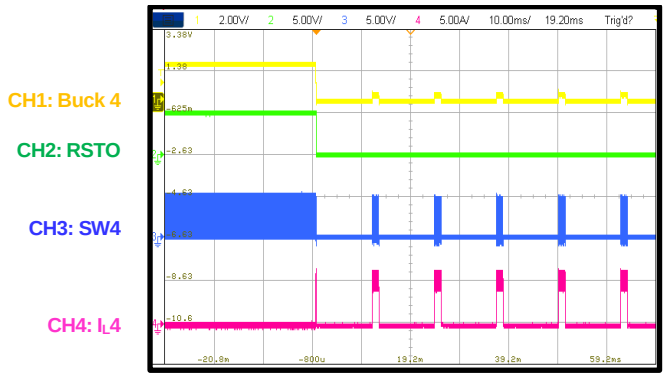
VIN Shutdown

All buck rails without load



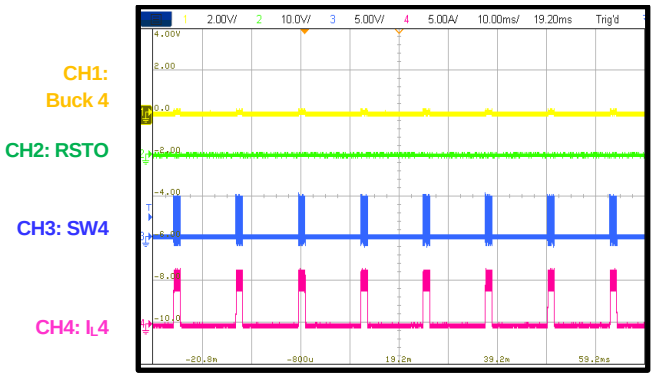
SCP Entry

Buck 4 output = 1.8V



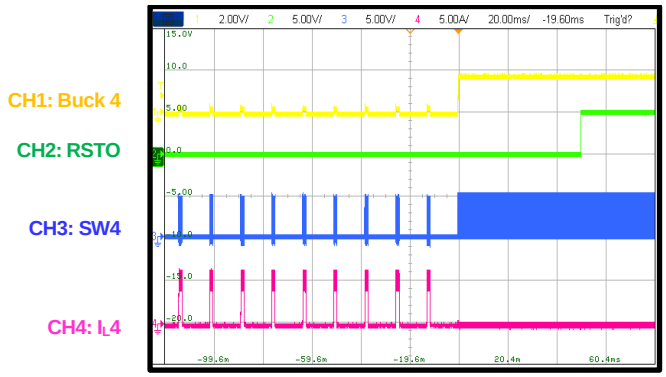
SCP Steady State

Buck 4 output = 1.8V



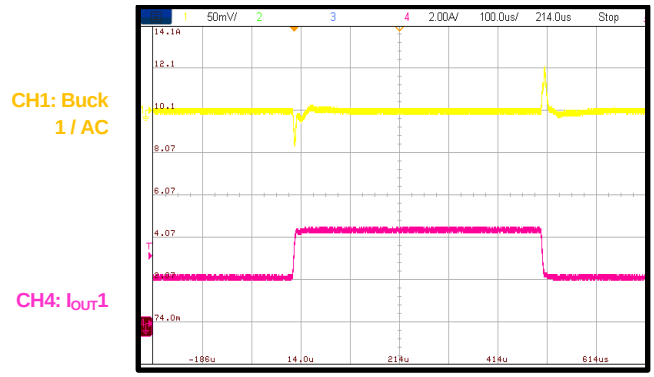
SCP Recovery

Buck 4 output = 1.8V



Load Transient Response

I_{OUT} transient from 2.25A to 4.5A, slew rate is 2.5A/µs



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

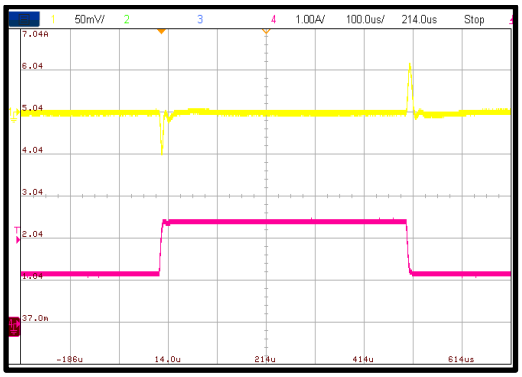
Performance waveforms are tested on the evaluation board, V_{IN} = 5V, T_A = 25°C, tested using MPQ7920-0003 parts, unless otherwise noted.

Load Transient Response

I_{OUT} transient from 1.25A to 2.5A, slew rate is 2.5A/μs

CH1: Buck 2 / AC

CH4: I_{OUT}2

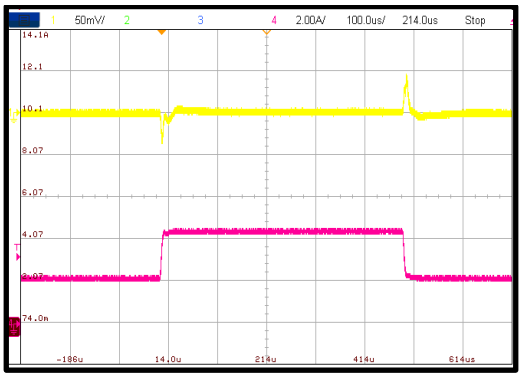


Load Transient Response

I_{OUT} transient from 2.25A to 4.5A, slew rate is 2.5A/μs

CH1: Buck 3 / AC

CH4: I_{OUT}3

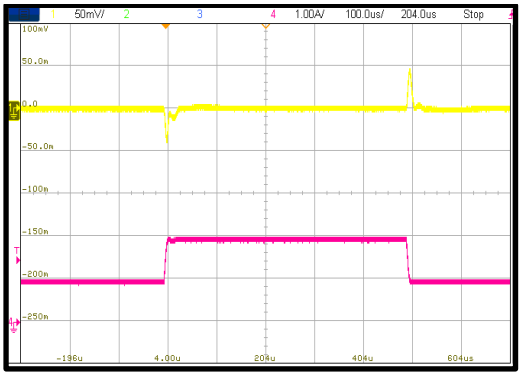


Load Transient Response

I_{OUT} transient from 1A to 2A, slew rate is 2.5A/μs

CH1: Buck 4 / AC

CH4: I_{OUT}4



FUNCTIONAL BLOCK DIAGRAM

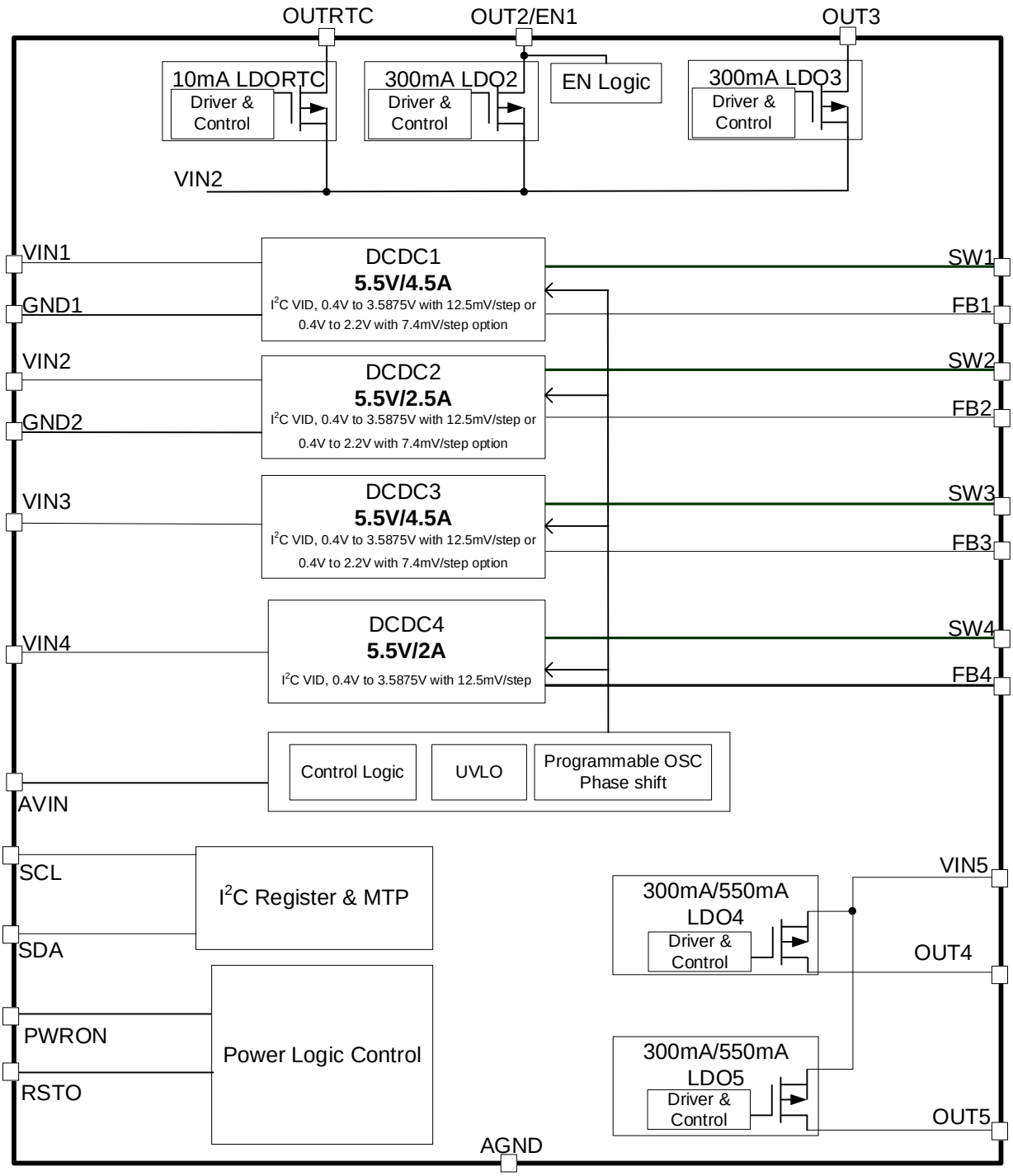


Figure 2: Functional Block Diagram

OPERATION

The MPQ7920 provides a complete power management solution for automotive 5V systems, including infotainment, video recorders, and more. It integrates four 4-channel high-frequency, synchronous, rectified, step-down, switch-mode converters and five low-dropout regulators. With all components inside a compact QFN-26 (3.5mmx4.5mm) package, it greatly reduces component count and PCB space.

I²C and MTP interfaces provide an adjustable default output voltage, power-on sequence, and dynamic voltage scaling. In addition, the I²C provides powerful logic functions. See the Register Map section on page 26 for more details.

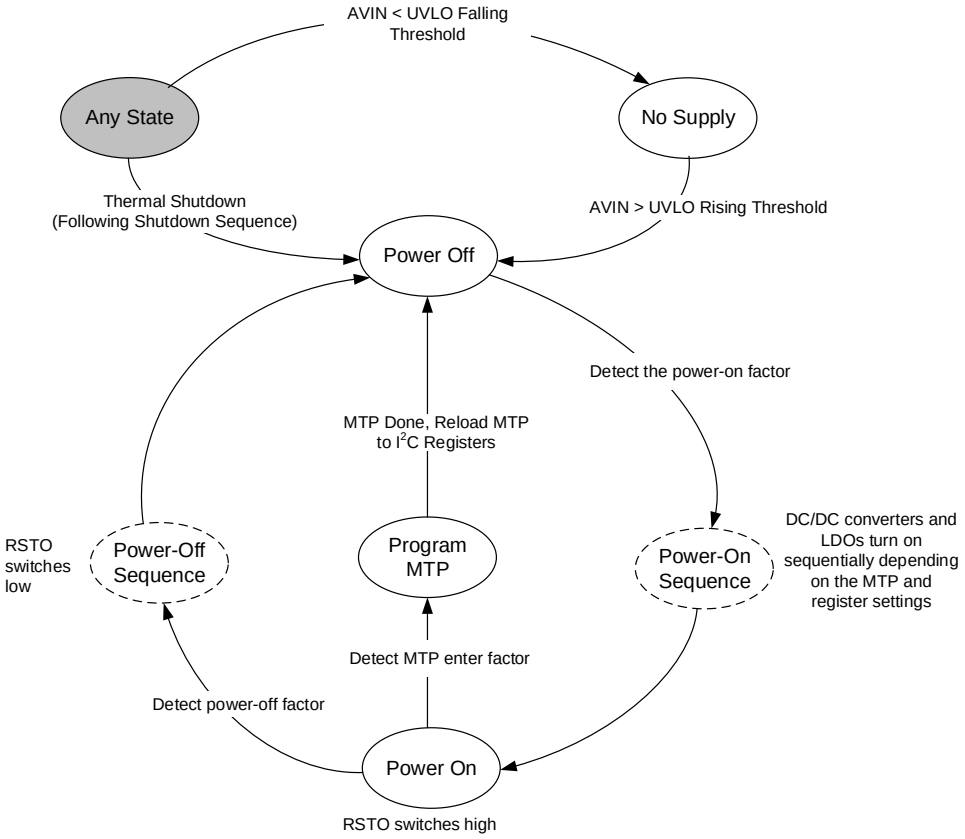


Figure 3: Power Control State Machine Diagram

Power Control

State Machine Description

The state machine (see Figure 3) has a number of status options, including no supply, power off, power-on sequence, power on, power-off sequence, program MTP, and shutdown. These statuses are described below.

No Supply

The PMIC's input pin has a UVLO detection circuit. If the input voltage (AVIN) is below the UVLO rising threshold, all of the PMIC's functions are disabled.

Power Off

All power rails are powered off. When AVIN exceeds its rising UVLO, the PMIC enters the power-off state. In this state, the PMIC is always monitoring the power-on factors; once a power-on factor is detected, the device changes to the power-on sequence state.

Power-On Sequence

The DC/DC converters and LDOs turn on sequentially according to the order programmed by the MTP e-fuse.

Power On

The DC/DC converters and LDOs are turned on. The RSTO pin's output switches high. In this state, the PMIC is always monitoring the power off and program MTP factors.

Power-Off Sequence

The PMIC enters this sequence when it detects the power off factors during a power on state. First, the RSTO is switched low, then the DC/DC converters and LDOs turn off sequentially according to the order programmed by the MTP e-fuse.

Program MTP

The PMIC shuts down all buck regulators and LDOs with the power-off sequence when entering program MTP mode. After MTP programming is complete, the PMIC reloads the MTP to the I²C registers and then monitors for power-on factors.

Shutdown Event

If the PMIC detects any of the conditions shown below, it immediately changes to a no supply or power off state, regardless of the current state.

- If the input voltage is below the UVLO falling threshold, the device enters a no supply state.
- If over-temperature protection (OTP) is triggered, the device enters a power-off state.

Note:

11) If the PMIC enters a power-off state due to OTP being triggered, then LDORTC is off.

Power-On Factor

The PMIC has several power-on factors, including PWR_ON, thermal recovery, and EN1. These factors are described below.

PWRON_ON

If the PWRON pin is pulled to logic high (PWRON_MODE = 0) or there is a falling edge on the PWRON pin (PWRON_MODE = 1), the PMIC enters the power-on sequence. See the PWRON Functions section on page 21 for more details.

Thermal Recovery

The part enters a power off state if the die temperature exceeds the thermal protection threshold. Once the die temperature falls below the threshold, the PMIC enters the power-on sequence again.

EN1

If pin 23 is selected as EN1, and EN1 is pulled to logic high (EN1_INV defines EN1 as active high) or EN1 is pulled to logic low (EN1_INV defines EN1 as active low), then the power rails controlled by EN1 enter the power-on sequence. See the EN1 Functions section on page 23 for more details.

Power-On Sequence

There are 16 time slots for the power-on sequence. All of the DC/DC converters and LDOs except OUTRTC LDO can be programmed between 0 and 15 time slots by the MTP e-fuse. The delay time between each time slot is adjustable with the MTP TIME_SLOT bits. The time does not change the switching frequency.

RSTO switches high with RSTO_DELAY time when the power-on sequence is complete. The DC/DC converter and LDO power-on sequence is set by POWER_ON_SLOT_NO and PWR_ON_TIME_SLOT_MODE. See the MTP table on page 26 for more details.

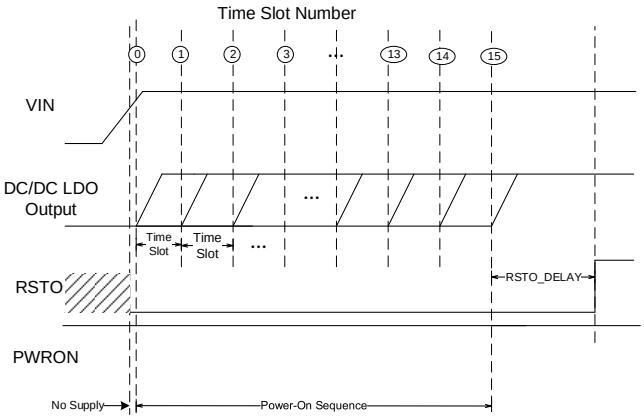


Figure 4: Power-On Sequence

OUTRTC ON

The OUTRTC LDO is always on if both VIN2 and AVIN are above their respective UVLO rising thresholds, regardless of any other pin statuses. OUTRTC turns off if either VIN2 or AVIN fall below their respective UVLO falling thresholds or if thermal shutdown is triggered.

Other Buck Regulators and LDOs On

The MPQ7920 provides a programmable power-on sequence. The MTP configuration table on page 26 shows bits to set the time slot number for each channel.

Power-Off Factor

The PMIC power-off factors are PWRON_OFF and EN1. They are described below.

PWRON_OFF

If the PWRON pin is pulled to logic low (PWRON_MODE = 0) or a falling edge on the PWRON pin (PWRON_MODE = 1), the PMIC enters a power-off sequence. See the PWRON Functions section on page 21 for more details.

EN1

If pin 23 is selected as EN1, and EN1 is pulled to logic low (EN1_INV defines EN1 as active high) or EN1 is pulled to logic high (EN1_INV defines EN1 as active low), then the power rails controlled by EN1 enter the power-off sequence. See the EN1 Functions section on page 23 for more details.

Power-Off Sequence

There are 16 time slots for the power-off sequence. All of the DC/DC converters and LDOs, except OUTRTC LDO, can be programmed between 0 and 15 time slots by the MTP e-fuse. The delay time between each time slot is adjustable with the MTP TIME_SLOT bits. The time does not change the switching frequency.

The power-off sequence begins at the maximum used time slot number. Therefore, the power-off sequence does not always start from time slot 15.

RSTO is pulled low prior to the DC/DC converters and LDOs starting to turn off. The DC/DC converter and LDO power-off sequence is set by POWER_OFF_SLOT_NO and POWER_OFF_SLOT_MODE. See the MTP table on page 26 for more details.

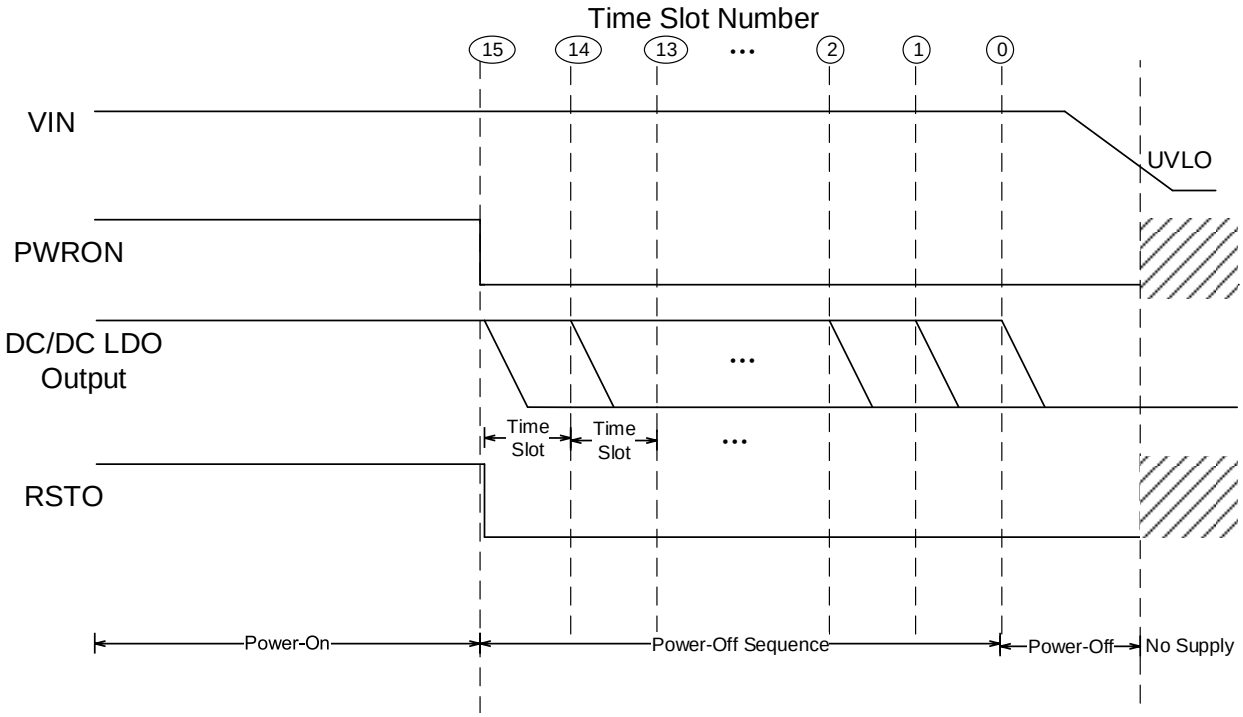


Figure 5: Power-Off Sequence (PWRON_MODE = 0)

Program MTP

Programming the MTP e-fuse through the I²C interface must strictly follow the steps below:

1. Ensure that all bucks and LDOs have no load before programming the MTP e-fuse.
2. Write the correct MTP program password to register 0x26.
3. Set ENTER_MTP_MODE = 1 to enter MTP program mode. All buck regulators and LDOs shut down in this mode.
4. Write the desired content to the I²C registers.
5. Increase the VIN1 and AVIN power supply to between 6.4V and 6.5V with a minimum 150mA current capability.
6. Set PROGRAM_MTP = 1 to start the MTP e-fuse program.
7. The PMIC calculates the sum of all related I²C registers to be burned to the MTP register. The checksum result will also be written to the MTP register.
8. After the MTP write operation finishes (typically takes 100ms), the PMIC sets the PROGRAM_MTP bit to 0, and the I²C register write protection is unlocked. ENTER_MTP_MODE is also set to 0.
9. After MTP programming, the MPQ7920 reloads the MTP to the related I²C registers and the PWRON pin function is re-enabled. The buck and LDO regulators then power up based on their power-on factors. After the power-up sequence completes, I²C communication is enabled.
10. Decrease the VIN1 and AVIN voltage to <5.5V, then restart the power supply for normal operation.

During VIN power-up, before loading the MTP data into the I²C register, the PMIC does a checksum calculation for all related MTP registers, then compares it with the checksum byte. If they match, the MTP data is loaded into the I²C register. If not, the I²C register uses the hard-coded default value. There is an I²C register flag bit to indicate a checksum error.

Shutdown Sequence

If the input voltage is below the UVLO falling threshold or if the IC is over-temperature, the PMIC enters the shutdown sequence immediately. All of the DC/DC and LDO regulators turn off at the same time.

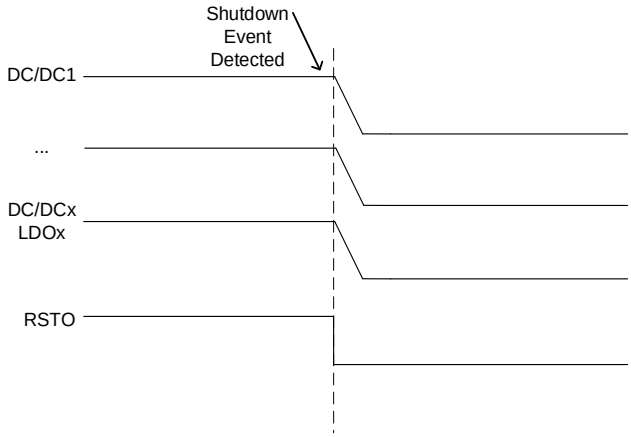


Figure 6: Shutdown Sequence

High-Efficiency Buck Regulator

Buck 1 through buck 4 are synchronous, step-down DC/DC converters that have built-in UVLO, soft start, compensation, and hiccup current limit protection. Fixed-frequency, constant-on-time (COT) control provides fast transient response. The switching clock is phase shifted from buck 1 through buck 4 during CCM operation. Buck 1 through buck 4 support 100% duty cycle mode.

Power Supply and UVLO

VIN1 is the power supply for buck 1. VIN2 is the power supply for buck 2, LDORTC, LDO2, and LDO3. VIN3 is the power supply for buck 3. VIN4 is the supply for buck 4. VIN5 is the power supply for LDO4 and LDO5. AVIN is the power input to bias the internal logic blocks.

VIN1, VIN2, VIN3, VIN4, VIN5, and AVIN have their own UVLO thresholds with proper hysteresis. Once AVIN ramps up and exceeds the UVLO rising threshold, the PWRON logic is enabled and ready to accept start-up and shutdown commands. LDORTC is active once VIN2 exceeds its rising threshold.

Internal Soft Start

Soft start is implemented to prevent the PMIC output voltage from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage. At this point, the reference voltage takes over.

For the four 4-channel buck outputs, the soft-start times are MTP-adjustable. For the LDO2 through LDO5 outputs, the soft-start times are internally fixed at 50µs. For LDORTC, the soft-start slew rate is consistent at 25mV/µs.

Output Discharge

In order to discharge the output capacitor during the power-off sequence, there is a passive discharge path from the DC/DC converters' and LDOs' output to ground. The discharge path is turned on when its corresponding channel is disabled. The typical discharge resistance is 7Ω. The discharge function can be enabled or disabled through the I²C interface.

Over-Voltage Protection (OVP)

The MPQ7920 monitors the feedback voltage to detect an over-voltage condition. When the feedback voltage exceeds 120% of the target voltage, the controller turns off both the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET), and the discharge path is turned on. The part exits this regulation period once the feedback voltage falls below 110% of the reference voltage.

Over-Current Protection (OCP)

If the peak inductor current reaches its limit (set via the I²C registers) when the HS-FET is on, OCP is triggered. The LS-FET is forced on until the inductor current drops to the valley current limit; then the HS-FET turns on again. The part does not exit OCP unless the inductor peak current falls below the limit. If the OCP time lasts for longer than 150µs (typical), the buck enters hiccup mode.

System Control Signals

PWRON Functions

PWRON is an input pin to the IC that generates a power-on or power-off event. This pin can be configured to detect a level or a falling edge via the MTP.

When the PWRON_MODE bit = 1, the PWRON_DEBOUNCE_TIMER bit can set the PWRON pin's debounce timer to filter out mechanical switch short press noise.

When the PWRON_MODE bit = 0, PWRON works as an enable pin. Apply a logic high voltage to turn the PMIC on; apply a logic low voltage to turn the PMIC off.

PWRON_MODE = 1 (Edge Trigger)

Power On

If AVIN is above the UVLO threshold and PWRON is asserted low for longer than PWRON_DEBOUNCE_TIMER when the PMIC is powered off, the power-on sequence begins. The power-on sequence must complete, and then the PWRON detection function is re-enabled.

Power Off

If PWRON asserts low for longer than PWRON_DEBOUNCE_TIMER when the device is powered on, the power-off sequence begins. The MPQ7920 turns off all regulators and LDOs (except OUTRTC). The power-off sequence is pre-programmed by the MTP e-fuse.

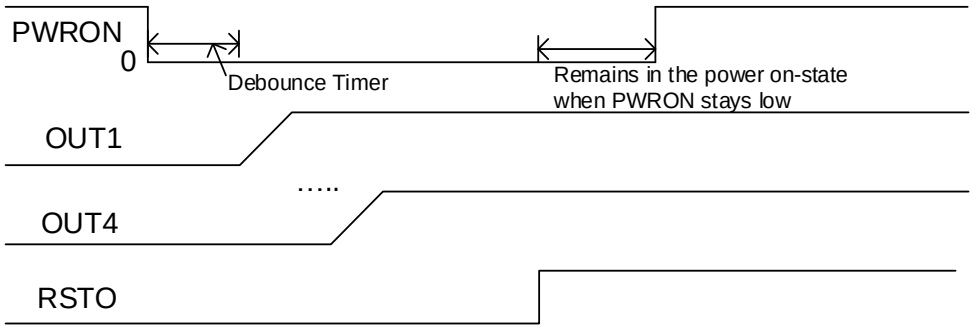


Figure 7: PWRON_MODE = 1, Press PWRON to Power On

If the PWRON pin is still pulled low after the power-off sequence completes, the MPQ7920 remains in its power off state. If the PWRON pin is pulled high after the power-off sequence completes, the MPQ7920 continues the power-off sequence.

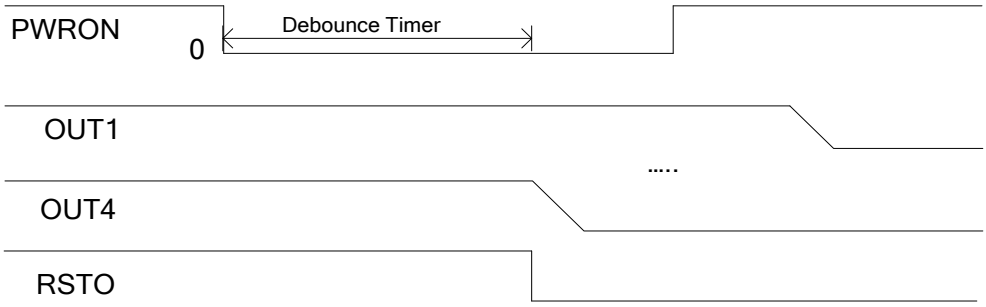


Figure 8: PWRON_MODE = 1, Press PWRON to Power Off

PWRON_MODE = 0 (Level Trigger)

The PMIC enters the power-on sequence once the input voltage (AVIN) exceeds its UVLO threshold and PWRON is pulled high.

If PWRON is pulled low when the MPQ7920 is powered on, the device executes the power-off sequence. If PWRON is pulled high when the MPQ7920 is powered off, the MPQ7920 executes a power-on sequence. During a power-on sequence or power-off sequence, the PWRON pin function is blanked until the sequence is complete. For example, during a power-off sequence, even if PWRON is pulled high, the PMIC finishes the power-off sequence first, then executes the power-on sequence (see Figure 9).

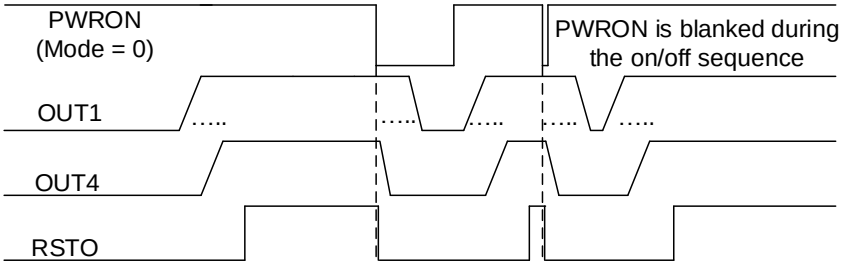


Figure 9: PWRON Enable and Disable Function

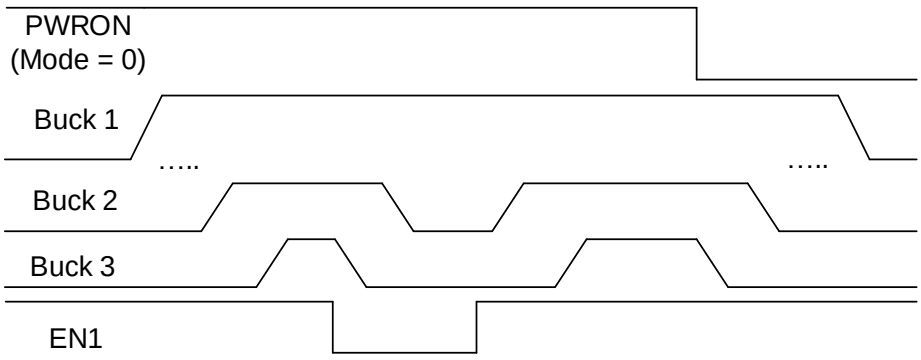


Figure 10: EN1 Function

EN1 Functions

EN1 is a multi-function pin with an LDO2 output. If the EN1 function is selected on pin 23, then the MPQ7920 supports the operations described below.

The EN1 pin can be used to control the on/off sequence of the power rails. This is especially useful for non-I²C interface applications.

Figure 10 on page 22 shows the EN1 function. EN1_INV defines EN1 as active high or active low. If EN1 controls buck 2 and buck 3 and EN1_INV is set to active high, then EN1 functions as follows:

- If EN1 is pulled low, then buck 2 and buck 3 power off sequentially.
- If EN1 is pulled high, then buck 2 and buck 3 power on sequentially.

PWRON has a higher priority than EN1. If PWRON is pulled low, then all the power rails enter the power-off sequence.

The buck converter and LDO regulator can be enabled and disabled via the PWRON and EN1 pins.

Thermal Warning and Shutdown

Thermal warning and shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MPQ7920 sets the OTWARNING bit to 1. When the temperature falls to 97°C, this bit can be cleared by writing 1 to it.

If the die temperature exceeds 153°C, the MPQ7920 sets the OTEMPP bit to 1, and the system enters the shutdown sequence. When the temperature falls to 130°C, the regulator enters the power-on sequence again.

I²C Timing

The PMIC's I²C interface is powered by an internal, fixed, 2V power supply. When VIN exceeds its under-voltage lockout (UVLO) threshold during VIN power-up, this indicates that the 2V LDO power supply is ready. The I²C function is disabled during the power-on sequence. When the power-on sequence is complete (for all enabled power rails), the I²C is available (see Figure 11).

When the I²C is not used, SCL and SDA should be pulled high by a resistor.

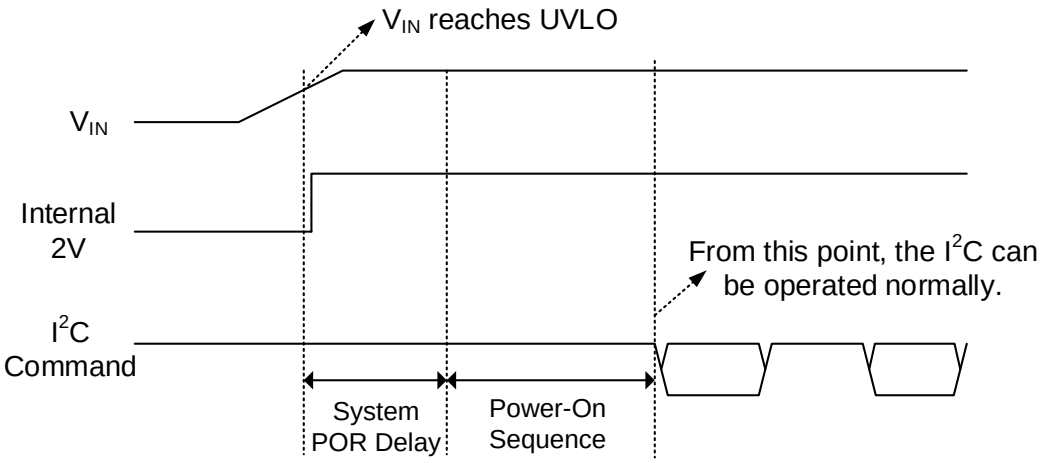


Figure 11: I²C Timing Graph

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. A master device is connected to the line; it generates the SCL signal and device address, and arranges the communication sequence.

The MPQ7920 interface is an I²C slave that can support fast mode (400kHz) and high-speed mode (3.4Mhz). The I²C interface adds flexibility to the power supply solution. Among other parameters, the output voltage and transition slew rate can be instantaneously controlled by the I²C interface. If the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a read or write (R/W) operation, respectively.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, and signify the beginning and the end of the I²C transfer. The start (S) condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop (P) condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 12).

The master then generates the SCL clocks, and transmits the device address and the R/W direction bit on the SDA line.

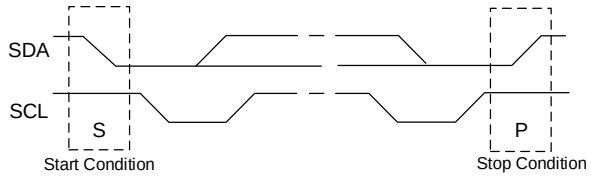


Figure 12: Start and Stop Conditions

Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data should be followed by an acknowledge bit.

I²C Update Sequence

The MPQ7920 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ7920 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ7920. The MPQ7920 performs an update on the falling edge of the LSB byte. Figure 13, Figure 14, and Figure 15 show examples of I²C write and read sequences.

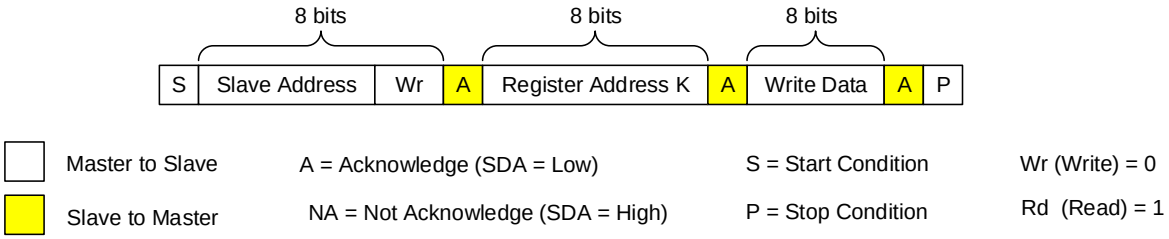


Figure 13: I²C Write Example – Write Single Register

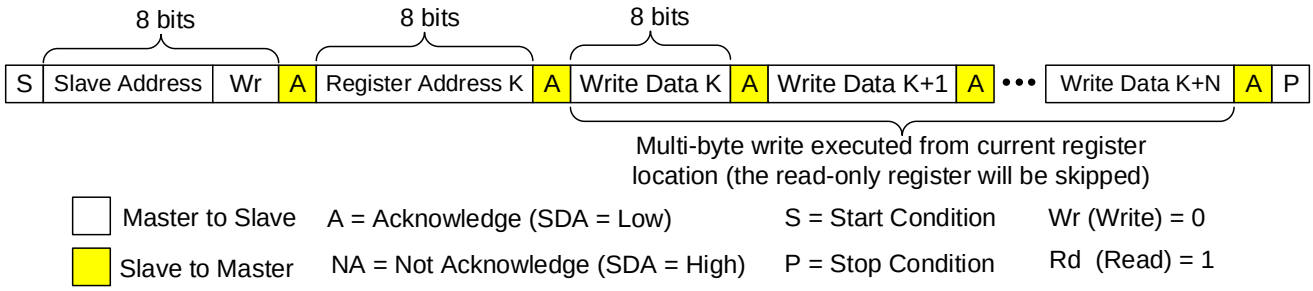


Figure 14: I²C Write Example – Write Multi-Register

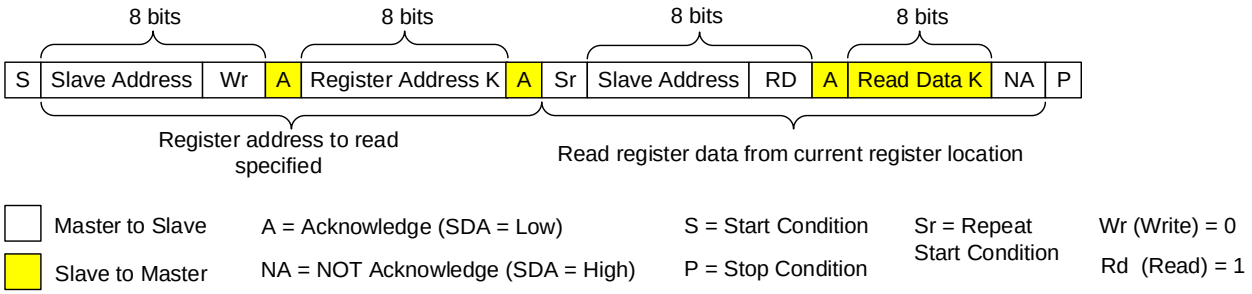


Figure 15: I²C Read Example – Read Single Register

REGISTER DESCRIPTION

MTP E-Fuse Configuration Table

Add	Name	D7	D6	D5	D4	D3	D2	D1	D0
00	CTL0	DVS SLEW RATE		FREQUENCY		N/A	PWRON_DEBOUNCE_TIMER		N/A
01	CTL1	RSTO_MODE		RSTO_DELAY		RSTO_PFI_THLD		N/A	
02	CTL2	N/A		N/A		TIME_SLOT		PWR_ON_TIME_SLOT_MODE	PWR_OFF_TIME_SLOT_MODE
03	Buck 1	BUCK1_VREF: 0.4V to 3.5875V/12.5mV or 0.4V to 2.2V/7.4mV							
04		N/A	OVPEN1	DISCHGEN1	MODE BUCK1	N/A			
05		ILIM1		PHASE_DELAY1		SOFTSTART1		N/A	
06		POWER_OFF_SLOT_NO_B1				POWER_ON_SLOT_NO_B1			
07	Buck 2	BUCK2_VREF: 0.4V to 3.5875V/12.5mV or 0.4V to 2.2V/7.4mV							
08		N/A	OVPEN2	DISCHGEN	MODEBUCK2	N/A			
09		ILIM2		PHASE_DELAY2		SOFTSTART2		N/A	
0A		POWER_OFF_SLOT_NO_B2				POWER_ON_SLOT_NO_B2			
0B	Buck 3	BUCK3_VREF: 0.4V to 3.5875V/12.5mV or 0.4V to 2.2V/7.4mV							
0C		N/A	OVPEN3	DISCHGEN	MODE BUCK3	N/A			
0D		ILIM3		PHASE_DELAY3		SOFTSTART3			
0E		POWER_OFF_SLOT_NO_B3				POWER_ON_SLOT_NO_B3			
0F	Buck 4	BUCK4_VREF: 0.4V to 3.5875V/12.5mV							
10		N/A	OVPEN4	DISCHGEN	MODE BUCK4	N/A			
11		ILIM4		PHASE_DELAY4		SOFTSTART4		N/A	
12		POWER_OFF_SLOT_NO_B4				POWER_ON_SLOT_NO_B4			
13	RTCLDO	RTCLDO_VREF: 0.65V to 3.5875V/12.5mV							
14	LDO2	LDO2_VREF: 0.65V to 3.5875V/12.5mV							
15		N/A	N/A	DISCHGEN_LDO2	I2C_SLAVE_ADDRESS				
16		POWER_OFF_SLOT_NO_LDO2				POWER_ON_SLOT_NO_LDO2			
17	LDO3	LDO3_VREF: 0.65V to 3.5875V/12.5mV							
18		N/A	N/A	DISCHGEN_LDO3	N/A	N/A			
19		POWER_OFF_SLOT_NO_LDO3				POWER_ON_SLOT_NO_LDO3			
1A	LDO4	LDO4_VREF: 0.65V to 3.5875V/12.5mV							
1B		N/A	ILIM_LDO4	DISCHGEN_LDO4	N/A	N/A			
1C		POWER_OFF_SLOT_NO_LDO4				POWER_ON_SLOT_NO_LDO4			
1D	LDO5	LDO5_VREF: 0.65V to 3.5875V/12.5mV							
1E		N/A	ILIM_LDO5	DISCHGEN_LDO5	N/A	N/A			
1F		POWER_OFF_SLOT_NO_LDO5				POWER_ON_SLOT_NO_LDO5			
20	Mode	PARALLEL1	PARALLEL2	PWRON_MODE	EN_EN1 PIN	N/A	N/A		
21	EN1	EN1_INV	EN1_POWER_RAILS_CONTROL						
22	EN	EN_BUCK1	EN_BUCK2	EN_BUCK3	EN_BUCK4	EN_LDO2	EN_LDO3	EN_LDO4	EN_LDO5
23	ID1	MTP configuration code. “0x00” refers to a standard MPQ7920. “0x03” refers to the MPQ7920-0003 part.							
24	ID2	MTP revision number: This is where the revision number is stored if the user must update the MTP value.							
25	CRC	Checksum of MTP registers 0x00 to 0x24: While writing the I²C register’s data to the MTP, the IC initiates a checksum of all related I²C registers, and writes the result in this byte. During power-up, the IC calculates and compares the MTP data with the 0x25 register’s content. If they match, the MTP data is loaded to the I²C register; otherwise, the I²C register ignores the MTP data and uses the default setting.							

Notes:

12) The default register value is based on the MPQ7920-0003 specifications.

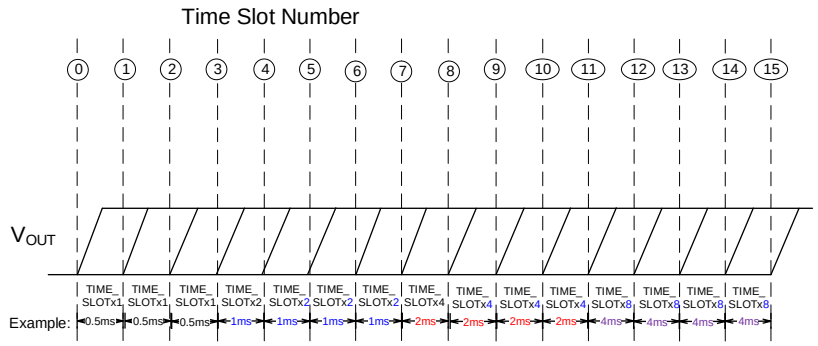
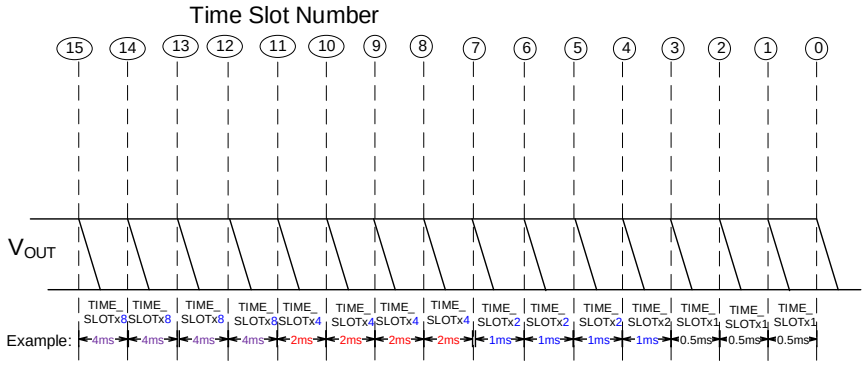
REGISTER DESCRIPTION

MTP E-Fuse Table Description

Bits	Bit Name	Default	Description
D[7:6]	DVS_SLEW_ RATE	10	Voltage scaling slew rate for the buck 1 to buck 4 converters. The soft-start slew rate is determined by the SOFTSTART bits. 00: Reserved 01: Reserved 10: 8mV/µs 11: 4mV/µs
D[5:4]	FREQUENCY	10	Switching frequency set bit. 00: 1.1MHz 01: 1.65MHz 10: 2.2MHz 11: 2.75MHz
D[2:1]	PWRON_ DEBOUNCE_ TIMER	01	Sets the PWRON pin's debounce timer. It is valid only if PWRON_MODE is set to 1. (see the PWRON_MODE section on page 21 for more information). The debounce time is not related to the PMIC switching frequency. 00: 0.5ms 01: 10ms 10: 40ms 11: 160ms
D[7:6]	RSTO_MODE	01	Sets RSTO behavior. 00: Do not monitor any power rails. Switch low when the power-off sequence starts or VIN1 drops below the under-voltage lockout (UVLO) threshold. Switch high when the RSTO delay is complete 01: Monitor buck 4's PG. RSTO goes high once buck 4's PG is OK after the RSTO delay. If buck 4 is disabled by the I²C, PG4 is always high. When PG4 goes low, RSTO has no delay 10: Monitor the VIN1 voltage (see the RSTO_PFI_THLD section below for details). RSTO goes high when VIN1 > UVLO threshold. RSTO goes low when VIN1 < UVLO threshold. RSTO switches high after a delay; RSTO switches low with no delay. RSTO monitors VIN1 while the device is on (if VIN1 > UVLO and PWRON are active) 11: Monitor all enabled buck and LDO power rails (including RTCLDO). RSTO goes high after the enabled bucks and LDOs have an OK PG, and the RSTO delay is complete. When any PG goes low, RSTO has no delay. When power rail is disabled via I2C, even PG goes low, RSTO has no action.
D[5:4]	RSTO_DELAY	01	Sets the RSTO delay time before switching high. The RSTO delay time is not related to the PMIC switching frequency. 00: 100ms 01: 50ms 10: 10ms 11: 1ms
D[3:2]	RSTO_PFI_ THLD	10	Sets the VIN1 rising threshold when RSTO_MODE is set to 10. 00: 2.7V 01: 2.9V 10: 4.0V 11: 4.4V
D[3:2]	TIME_SLOT	00	Sets the power-on and power-off sequences' time slot interval. These sequences share the same time slot value. The time slot value is not related to the PMIC switching frequency. 00: 0.5ms 01: 2ms 10: 8ms 11: 16ms

REGISTER DESCRIPTION *(continued)*

MTP E-Fuse Table Description

Bits	Name	Default	Description
D[1]	PWR_ON_ TIME_SLOT _MODE	1	Selects the power-on sequence's time slot mode. 0: The time slot is a fixed number set by TIME_SLOT 1: The time slot increases linearly in the following ways: • Time slot 0 to slot 3 has a (TIME_SLOT x 1) interval • Time slot 3 to slot 7 has a (TIME_SLOT x 2) interval • Time slot 7 to slot 11 has a (TIME_SLOT x 4) interval • Time slot 11 to slot 15 has a (TIME_SLOT x 8) interval  In a standard application, the power-on sequence ends at the maximum time slot of enabled channels. For example, if time slot 7 is the maximum slot number of enabled channels (no slot number above 7 is enabled) during the power-on sequence, the counter only works until time slot 7. Then the power-on sequence is complete, and the higher time slots are not executed.
D[0]	PWR_OFF_ TIME_SLOT _MODE	1	Selects the power-off sequence's time slot mode. 0: The time slot is a fixed number set by TIME_SLOT 1: The time slot increases linearly in the following ways: • Time slot 0 to slot 3 has a (TIME_SLOT x 1) interval • Time slot 3 to slot 7 has a (TIME_SLOT x 2) interval • Time slot 7 to slot 11 has a (TIME_SLOT x 4) interval • Time slot 11 to slot 15 has a (TIME_SLOT x 8) interval  In a standard application, the power-off sequence starts at the maximum time slot of enabled channels. For example, if time slot 7 is the maximum slot number of enabled channels (no slot number above 7 is enabled), during the power-off sequence, the counter only works from time slot 7 to time slot 0. Then the power-off sequence is complete. The higher time slots are not executed.

REGISTER DESCRIPTION *(continued)*

MTP E-Fuse Table Description

Bits	Name	Default	Description
D[7:0]	BUCK1_VREF BUCK2_VREF BUCK3_VREF BUCK4_VREF RTCLDO_VREF LDO2_VREF LDO3_VREF LDO4_VREF LDO5_VREF	1150mV 1500mV 1150mV 1800mV 3300mV 1800mV 1800mV 1100mV 1800mV	Sets the internal reference voltage. Buck outputs are from 400mV to 3587.5mV with 12.5mV per step. LDO outputs are from 650mV to 3587.5mV with 12.5mV per step. D[7:0] = 0000 0000: 400mV D[7:0] = 0000 0001: 412.5mV ... D[7:0] = 1111 1111: 3587.5mV See Table 2 on page 38 for details.
D[6]	OVPEN1 OVPEN2 OVPEN3 OVPEN4	1	Enable bit for buck 1 through buck 4's output over-voltage protection (OVP) function. 0: Disable the over-voltage protection (OVP) function 1: Enable the OVP function
D[5]	DISCHGEN1 DISCHGEN2 DISCHGEN3 DISCHGEN4	1	Enable bit for buck 1 through buck 4's output discharge function. 0: Disable the discharge function 1: Enable the discharge function
D[4]	MODEBUCK1 MODEBUCK2 MODEBUCK3 MODEBUCK4	1	Selects the mode (auto-PFM/PWM mode or forced PWM mode) 0: Auto-PFM/PWM mode 1: Forced PWM mode (FPWM)
D[7:6]	ILIM1 ILIM3	11	Configures the current limit threshold for the buck regulator. 00: 4.6A typical high-side peak current limit 01: 6.6A typical high-side peak current limit 10: 7.6A typical high-side peak current limit 11: 9.3A typical high-side peak current limit
D[7:6]	ILIM2 ILIM4	11	Configures the current limit threshold for the buck regulator. 00: 2.7A typical high-side peak current limit 01: 3.9A typical high-side peak current limit 10: 5.1A typical high-side peak current limit 11: 6.1A typical high-side peak current limit
D[5:4]	PHASE_DELAY1 PHASE_DELAY2 PHASE_DELAY3 PHASE_DELAY4	00 00 01 01	Sets the phase delay for buck 1 through buck 4. 00: 0° delay 01: 90° delay 10: 180° delay 11: 270° delay
D[3:2]	SOFTSTART1 SOFTSTART2 SOFTSTART3 SOFTSTART4	01	Soft-start time setting bit for each buck regulator. The soft-start time is between 10% and 90% of the target output voltage. 00 :150μs 01: 300μs 10: 610μs 11: 920μs

REGISTER DESCRIPTION *(continued)*

MTP E-Fuse Table Description

Bits	Name	Default	Description
D[7:4]	POWER_OFF_SLOT_NO_B1 POWER_OFF_SLOT_NO_B2 POWER_OFF_SLOT_NO_B3 POWER_OFF_SLOT_NO_B4 POWER_OFF_SLOT_NO_LDO2 POWER_OFF_SLOT_NO_LDO3 POWER_OFF_SLOT_NO_LDO4 POWER_OFF_SLOT_NO_LDO5	0000 0110 0000 0110 0111 0111 0111 1001	This bit sets each power rail's time slot number during the power-off sequence (see the TIME_SLOT section on page 27 and the PWR_OFF_TIME_SLOT_MODE section on page 28 for more details). The delay time between neighboring slots are not related to the PMIC default switching frequency. 0000: Time slot 0 0001: Time slot 1 0010: Time slot 2 0011: Time slot 3 0100: Time slot 4 0101: Time slot 5 0110: Time slot 6 0111: Time slot 7 1000: Time slot 8 1001: Time slot 9 1010: Time slot 10 1011: Time slot 11 1100: Time slot 12 1101: Time slot 13 1110: Time slot 14 1111: Time slot 15
D[3:0]	POWER_ON_SLOT_NO_B1 POWER_ON_SLOT_NO_B2 POWER_ON_SLOT_NO_B3 POWER_ON_SLOT_NO_B4 POWER_ON_SLOT_NO_LDO2 POWER_ON_SLOT_NO_LDO3 POWER_ON_SLOT_NO_LDO4 POWER_ON_SLOT_NO_LDO5	0000 0110 0000 0110 0111 0111 0111 1001	This bit sets each power rail's time slot number during the power-on sequence (see the TIME_SLOT section on page 27 and the PWR_ON_TIME_SLOT_MODE section on page 28 for more details). The delay time between neighboring slots are not related to the PMIC default switching frequency. 0000: Time slot 0 0001: Time slot 1 0010: Time slot 2 0011: Time slot 3 0100: Time slot 4 0101: Time slot 5 0110: Time slot 6 0111: Time slot 7 1000: Time slot 8 1001: Time slot 9 1010: Time slot 10 1011: Time slot 11 1100: Time slot 12 1101: Time slot 13 1110: Time slot 14 1111: Time slot 15
D[5]	DISCHGEN_LDO2 DISCHGEN_LDO3 DISCHGEN_LDO4 DISCHGEN_LDO5	1	Enable bit for LDO2 through LDO5's output discharge function. 0: Disable the discharge function 1: Enable the discharge function
D[4:0]	I2C_SLAVE_ADDRESS	01001	Sets the A5 to A1 bit of the slave I²C address (see the I²C Bus Slave Address section on page 34 for more details).
D[6]	ILIM_LDO4 ILIM_LDO5	0	Selects the LDO4 and LDO5 current limit. 0: Lower current limit supports 300mA I_{OUT} 1: Higher current limit supports 550mA I_{OUT}

REGISTER DESCRIPTION *(continued)*

MTP E-Fuse Table Description

<table>
<tr><th>Bits</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7]</td><td>PARALLEL_1</td><td>0</td><td>Sets buck 1 and buck 3 to work in parallel mode. Use FB1 as the feedback pin. After entering parallel mode, buck 3's I²C/MTP register is invalid. Parallel mode only takes effect during V_{IN} power-up. After powering up, the PMIC does not respond to changes of this bit in the I²C register. The current limit is doubled based on buck 1's register setting.

0: Buck 1 and buck 3 do not work in parallel mode
1: Buck 1 and buck 3 work in parallel mode</td></tr>
<tr><td>D[6]</td><td>PARALLEL_2</td><td>0</td><td>Sets buck 2 and buck 4 to work in parallel mode. Use FB2 as the feedback pin. After entering parallel mode, buck 4's I²C/MTP register is invalid. Parallel mode only takes effect during V_{IN} power-up. After powering up, the PMIC does not respond to changes on this bit. The current limit is doubled based on buck 2's register setting.

0: Buck 2 and buck 4 do not work in parallel mode
1: Buck 2 and buck 4 work in parallel mode</td></tr>
<tr><td>D[5]</td><td>PWRON_
MODE</td><td>0</td><td>This bit defines the PWRON pin's behavior (level trigger or falling edge trigger).

0: Level trigger. This functions like an EN pin. When the PWRON pin's input voltage exceeds the rising threshold, the PMIC begins the power-on sequence
1: Falling edge trigger. When the PWRON pin detects a high-to-low transition, if the PMIC is off, the PMIC starts the power-on sequence after a delay. If the PMIC is on, the PMIC begins the power-off sequence after a delay. The delay time is edited by PWRON_DEBOUNCE_TIMER</td></tr>
<tr><td>D[4]</td><td>EN_EN1_PIN</td><td>0</td><td>Sets pin 23 as the LDO2 output or EN1 pin. EN1 is an input pin to turn several power rails on and off. EN1_POWER_RAILS_CONTROL defines which power rails are controlled by EN1; EN1_INV defines the EN1 pin's active low or active high.

0: Pin 23 is an LDO2 output
1: Pin 23 is EN1</td></tr>
<tr><td>D[7]</td><td>EN1_INV</td><td>1</td><td>Sets EN1 to active low or active high.

0: A low-level input to EN1 turns on the related power rails
1: A high-level input voltage to EN1 turns on the related power rails</td></tr>
<tr><td>D[6:0]</td><td>EN1_
POWER_
RAILS_
CONTROL</td><td>0000111</td><td>This bit sets which power rails are controlled by EN1.

<table><tr><th>D[6]</th><th>D[5]</th><th>D[4]</th><th>D[3]</th><th>D[2]</th><th>D[1]</th><th>D[0]</th></tr><tr><td>Buck 1</td><td>Buck 2</td><td>Buck 3</td><td>Buck 4</td><td>LDO3</td><td>LDO4</td><td>LDO5</td></tr></table>
From D[6] to D[0], each bit controls 1 power rail.

0: EN1 does not control this power rail's on/off sequence
1: EN1 controls this power rail's on/off sequence</td></tr>
<tr><td>D[7:0]</td><td>EN_BUCK1
EN_BUCK2
EN_BUCK3
EN_BUCK4
EN_LDO2
EN_LDO3
EN_LDO4
EN_LDO5</td><td>0xFF</td><td>Enable control bit for each power rail.

0: Disable
1: Enable</td></tr>
</table>

Table 1: Output Reference Voltage Chart (Used for 12.5mV DVS Resolution)

D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)
00000000	400	01010110	1475	10101100	2550
00000001	412.5	01010111	1487.5	10101101	2562.5
00000010	425	01011000	1500	10101110	2575
00000011	437.5	01011001	1512.5	10101111	2587.5
00000100	450	01011010	1525	10110000	2600
00000101	462.5	01011011	1537.5	10110001	2612.5
00000110	475	01011100	1550	10110010	2625
00000111	487.5	01011101	1562.5	10110011	2637.5
00001000	500	01011110	1575	10110100	2650
00001001	512.5	01011111	1587.5	10110101	2662.5
00001010	525	01100000	1600	10110110	2675
00001011	537.5	01100001	1612.5	10110111	2687.5
00001100	550	01100010	1625	10111000	2700
00001101	562.5	01100011	1637.5	10111001	2712.5
00001110	575	01100100	1650	10111010	2725
00001111	587.5	01100101	1662.5	10111011	2737.5
00010000	600	01100110	1675	10111100	2750
00010001	612.5	01100111	1687.5	10111101	2762.5
00010010	625	01101000	1700	10111110	2775
00010011	637.5	01101001	1712.5	10111111	2787.5
00010100	650	01101010	1725	11000000	2800
00010101	662.5	01101011	1737.5	11000001	2812.5
00010110	675	01101100	1750	11000010	2825
00010111	687.5	01101101	1762.5	11000011	2837.5
00011000	700	01101110	1775	11000100	2850
00011001	712.5	01101111	1787.5	11000101	2862.5
00011010	725	01110000	1800	11000110	2875
00011011	737.5	01110001	1812.5	11000111	2887.5
00011100	750	01110010	1825	11001000	2900
00011101	762.5	01110011	1837.5	11001001	2912.5
00011110	775	01110100	1850	11001010	2925
00011111	787.5	01110101	1862.5	11001011	2937.5
00100000	800	01110110	1875	11001100	2950
00100001	812.5	01110111	1887.5	11001101	2962.5
00100010	825	01111000	1900	11001110	2975
00100011	837.5	01111001	1912.5	11001111	2987.5
00100100	850	01111010	1925	11010000	3000
00100101	862.5	01111011	1937.5	11010001	3012.5
00100110	875	01111100	1950	11010010	3025
00100111	887.5	01111101	1962.5	11010011	3037.5

Table 1: Output Reference Voltage Chart (Used for 12.5mV DVS Resolution) *(continued)*

D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)
00101000	900	01111110	1975	11010100	3050
00101001	912.5	01111111	1987.5	11010101	3062.5
00101010	925	10000000	2000	11010110	3075
00101011	937.5	10000001	2012.5	11010111	3087.5
00101100	950	10000010	2025	11011000	3100
00101101	962.5	10000011	2037.5	11011001	3112.5
00101110	975	10000100	2050	11011010	3125
00101111	987.5	10000101	2062.5	11011011	3137.5
00110000	1000	10000110	2075	11011100	3150
00110001	1012.5	10000111	2087.5	11011101	3162.5
00110010	1025	10001000	2100	11011110	3175
00110011	1037.5	10001001	2112.5	11011111	3187.5
00110100	1050	10001010	2125	11100000	3200
00110101	1062.5	10001011	2137.5	11100001	3212.5
00110110	1075	10001100	2150	11100010	3225
00110111	1087.5	10001101	2162.5	11100011	3237.5
00111000	1100	10001110	2175	11100100	3250
00111001	1112.5	10001111	2187.5	11100101	3262.5
00111010	1125	10010000	2200	11100110	3275
00111011	1137.5	10010001	2212.5	11100111	3287.5
00111100	1150	10010010	2225	11101000	3300
00111101	1162.5	10010011	2237.5	11101001	3312.5
00111110	1175	10010100	2250	11101010	3325
00111111	1187.5	10010101	2262.5	11101011	3337.5
01000000	1200	10010110	2275	11101100	3350
01000001	1212.5	10010111	2287.5	11101101	3362.5
01000010	1225	10011000	2300	11101110	3375
01000011	1237.5	10011001	2312.5	11101111	3387.5
01000100	1250	10011010	2325	11110000	3400
01000101	1262.5	10011011	2337.5	11110001	3412.5
01000110	1275	10011100	2350	11110010	3425
01000111	1287.5	10011101	2362.5	11110011	3437.5
01001000	1300	10011110	2375	11110100	3450
01001001	1312.5	10011111	2387.5	11110101	3462.5
01001010	1325	10100000	2400	11110110	3475
01001011	1337.5	10100001	2412.5	11110111	3487.5
01001100	1350	10100010	2425	11111000	3500
01001101	1362.5	10100011	2437.5	11111001	3512.5
01001110	1375	10100100	2450	11111010	3525
01001111	1387.5	10100101	2462.5	11111011	3537.5

Table 1: Output Reference Voltage Chart (Used for 12.5mV DVS Resolution) *(continued)*

D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)	D[7:0]	V_{REF} (mV)
01010000	1400	10100110	2475	11111100	3550
01010001	1412.5	10100111	2487.5	11111101	3562.5
01010010	1425	10101000	2500	11111110	3575
01010011	1437.5	10101001	2512.5	11111111	3587.5
01010100	1450	10101010	2525	N/A	N/A
01010101	1462.5	10101011	2537.5	N/A	N/A

I²C Bus Slave Address

The slave address is a 7-bit address followed by an 8th read or write (R/W) data direction bit. The A5 to A1 bits can be configured by the MTP e-Fuse.

	A7	A6	A5	A4	A3	A2	A1
Setting Value	1	1	0*	1*	0*	0*	1*

Notes:

13) This bit is configurable by the MTP e-fuse.
14) By default, the slave address is 0x69, A[7:1] = 110 1001.

I²C REGISTER MAP

Add	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	CTL0	R/W	DVS SLEW RATE		FREQUENCY		RESERVED (16)	PWRON_DEBOUNCE_TIMER		RESERVED
01	CTL1	R/W	RSTO_MODE		RSTO_DELAY		RSTO_PFI_THLD	RESERVED		
02	CTL2	R/W	RESERVED		RESERVED		TIME_SLOT	PWR_ON_TIME_SLOT_MODE		PWR_OFF_TIME_SLOT_MODE
03	BUCK1	R/W	BUCK1_VREF: 0.4V to 3.5875V/12.5mV or 0.4V to 2.2V/7.4mV							
04		R/W	RESERVED	OVPEN1	DISCHGEN1	MODEBUCK1	RESERVED			
05		R/W	ILIM1		PHASE_DELAY1		SOFTSTART1	RESERVED		
06		R/W	POWER_OFF_SLOT_NO_B1				POWER_ON_SLOT_NO_B1			
07	BUCK2	R/W	BUCK2_VREF: 0.4V to 3.5875V/12.5mV or 0.4V to 2.2V/7.4mV							
08		R/W	RESERVED	OVPEN2	DISCHGEN2	MODEBUCK2	RESERVED			
09		R/W	ILIM2		PHASE_DELAY2		SOFTSTART2	RESERVED		
0A		R/W	POWER_OFF_SLOT_NO_B2				POWER_ON_SLOT_NO_B2			
0B	BUCK3	R/W	BUCK3_VREF: 0.4V to 3.5875V/12.5mV or 0.4V to 2.2V/7.4mV							
0C		R/W	RESERVED	OVPEN3	DISCHGEN3	MODEBUCK3	RESERVED			
0D		R/W	ILIM3		PHASE_DELAY3		SOFTSTART3	RESERVED		
0E		R/W	POWER_OFF_SLOT_NO_B3				POWER_ON_SLOT_NO_B3			
0F	BUCK4	R/W	BUCK4_VREF: 0.4V to 3.5875V/12.5mV							
10		R/W	RESERVED	OVPEN4	DISCHG EN4	MODE BUCK4	RESERVED			
11		R/W	ILIM4		PHASE_DELAY4		SOFTSTART4	RESERVED		
12		R/W	POWER_OFF_SLOT_NO_B4				POWER_ON_SLOT_NO_B4			
13	RTCLDO	R/W	RTCLDO_VREF: 0.65V to 3.5875V/12.5mV							
14	LDO2	R/W	LDO2_VREF: 0.65V to 3.5875V/12.5mV							
15		R/W	RESERVED	RESERVED	DISCHG EN_LDO2	I2C_SLAVE_ADDRESS				
16		R/W	POWER_OFF_SLOT_NO_LDO2				POWER_ON_SLOT_NO_LDO2			
17	LDO3	R/W	LDO3_VREF: 0.65V to 3.5875V/12.5mV							
18		R/W	RESERVED	RESERVED	DISCHG EN_LDO3	RESERVED	RESERVED			
19		R/W	POWER_OFF_SLOT_NO_LDO3				POWER_ON_SLOT_NO_LDO3			
1A	LDO4	R/W	LDO4_VREF: 0.65V to 3.5875V/12.5mV							
1B		R/W	RESERVED	ILIM_LDO4	DISCHG EN_LDO4	RESERVED	RESERVED			
1C		R/W	POWER_OFF_SLOT_NO_LDO4				POWER_ON_SLOT_NO_LDO4			
1D	LDO5	R/W	LDO5_VREF: 0.65V to 3.5875V/12.5mV							
1E		R/W	RESERVED	ILIM_LDO5	DISCHG EN_LDO5	RESERVED	RESERVED			
1F		R/W	POWER_OFF_SLOT_NO_LDO5				POWER_ON_SLOT_NO_LDO5			
20	Parallel Mode	R/W	PARALLEL_1 (15)	PARALLEL_2 (15)	PWRON_MODE (15)	EN_EN1_PIN (15)	RESERVED			
21	Standby1	R/W	EN1_INV*	EN1_POWER_RAILS_CONTROL*						
22	EN	R/W	EN_BUCK1	EN_BUCK2	EN_BUCK3	EN_BUCK4	EN_LDO2	EN_LDO3	EN_LDO4	EN_LDO5
23	MTP_CTL	R/W	MTP configuration code: "0x00" means the standard MPQ7920. "0x03" means the MPQ7920-0003.							
24		R/W	MTP revision number: the revision number is stored here, in case the user must update the MTP.							
25		R/W	ENTER_MTP_MODE	PROGRAM_MTP	RESERVED					
26		W	MTP program password							
27	Status1	R	PGLDO4	PGLDO3	PGLDO2	PGRTC	PGBUCK4	PGBUCK3	PGBUCK2	PGBUCK1
28	Status2	R	OTWARNING	OTEMPP	CRC_ERROR	Checksum Flag	RESERVED			
29	ID2	R	VENDOR ID				RESERVED	PGLDO5	Current MTP Page Index	

Notes:

15) The I²C bits do not control the circuitry. The MTP bits control these functions. The MTP value reloads the circuitry while PWRON turns off, the MTP is configured, or AVIN exceeds the UVLO threshold.

16) Reserved bits must be written to 0.

Register Description

Most of the register bits share the same description as the MTP table. Table 2 lists the descriptions of different register bits.

The I²C register's default value is determined by the MTP table.

The I²C register can be reset to the hard coded default values under two conditions:

1. There is a CRC error while loading the MTP.
2. The MTP page is 0.

Over-temperature protection (OTP) does not reset the I²C register.

Table 2: I²C Register Description

Bits	Name	Default	Description
D[7]	ENTER_MTP_MODE	0	Set this bit to 1 to enter the pre-MTP configuration mode. After MTP configuration is complete, this bit auto-resets to 0.
D[6]	PROGRAM_MTP	0	Set this bit to 1 to force the PMIC to execute the MTP configuration action. After MTP configuration is complete, this bit auto-resets to 0.
D[X]	PGx	0	Power good indicator for bucks and LDOs. PG = 1 when the output voltage exceeds 90% of the reference voltage; PG = 0 when the output voltage is below 80% of the reference voltage. During I²C-controlled dynamic voltage scaling, the PG deglitch timer blanks the possible PG glitch. These PG bits change dynamically to indicate the power good of each buck's and LDO's status.
D[7]	OTWARNING	0	Die temperature early warning bit. If this bit is high, the die temperature exceeds 120°C. This bit latches once it is triggered. Write 1 to this bit to clear it.
D[6]	OTEMPP	0	Over-temperature indicator. If this bit is high, the IC is in thermal shutdown. This bit latches once it is triggered. Write 1 to this bit to clear it.
D[7:4]	VENDOR_ID	1000	Vendor identification.
D[4]	CHECKSUM_FLAG	0	D[4] = 1: The current MTP page has a CRC or checksum error D[4] = 0: The current MTP's data passes the CRC test
D[1:0]	CURRENT_MTP_PAGE_INDEX	01	This bit stores the current MTP page index information. The IC cannot access the MTP again when D[1:0] = 10b. The MPQ7920 only can be configured two times. 00: The default page. Two other pages can be used 01: First page 10: Second page 11: Reserved

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use a 0.47µH to 2.2µH inductor with a DC current rating at least 25% percent greater than the maximum load current. For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Use an inductor with higher inductance to improve efficiency under light-load conditions (<100mA).

Selecting the Step-Down Converter Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics because of their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Step-Down Converter Output Capacitor

The output capacitor for the step-down regulator maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. For most applications, 22µF x 2 ceramic capacitors are recommended.

The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation.

Table 3 lists the recommended components for DC/DC and LDO converters.

Table 3: Recommended External Components for DC/DC and LDO Converters (17)

Component	Value	Notes
VIN1 C_{IN}	22µF	0805 size/10V ceramic capacitor
VIN2 C_{IN}	22µF	0805 size/10V ceramic capacitor
VIN3 C_{IN}	22µF	0805 size/10V ceramic capacitor
VIN4 C_{IN}	22µF	0805 size/10V ceramic capacitor
VIN5 C_{IN}	10µF	0805 size/10V ceramic capacitor
AVIN C_{IN}	0.1µF	0603 size/10V ceramic capacitor
Buck 1 C_{OUT}	22µF x 2	0805 size/10V ceramic capacitor
Buck 1 L	1µH	I_{SAT} > current limit
Buck 2 C_{OUT}	22µF x 2	0805 size/10V ceramic capacitor
Buck 2 L	1.5µH	I_{SAT} > current limit
Buck 3 C_{OUT}	22µF x 2	0805 size/10V ceramic capacitor
Buck 3 L	1µH	I_{SAT} > current limit
Buck 4 C_{OUT}	22µF x 2	0805 size/10V ceramic capacitor
Buck 4 L	1.5µH	I_{SAT} > current limit
RTCLDO C_{OUT}	1µF	0603 size/6.3V ceramic capacitor
LDO2 C_{OUT}	2.2µF	0603 size/6.3V ceramic capacitor
LDO3 C_{OUT}	2.2µF	0603 size/6.3V ceramic capacitor
LDO4 C_{OUT}	2.2µF	0603 size/6.3V ceramic capacitor
LDO5 C_{OUT}	2.2µF	0603 size/6.3V ceramic capacitor
RSTO pull-up resistor	100kΩ	0603 or 0402 size film resistor
AVIN series resistor to VIN1	4.7Ω	0603 or 0402 size film resistor

Note:

17) The recommended external components are based on Figure 16 on page 39.

PCB Layout Guidelines (18)

PCB layout is critical for stable operation. It is recommended to use a 4-layer board for optimal performance. For the best results, refer to Figure 16 and follow the guidelines below:

1. Connect the input ground to the GND pin using the shortest and widest trace possible.
2. Connect the input capacitor to the VIN pin using the shortest and widest trace possible.
3. Ensure FB1 through FB4 are Kelvin-connected to the buck 1 to buck 4 output capacitors. Do not directly connect FB to the inductor's output node.
4. Route SW away from sensitive analog areas, such as FB1 through FB4.

Note:

18) The recommended layout is based on Figure 17 on page 40.

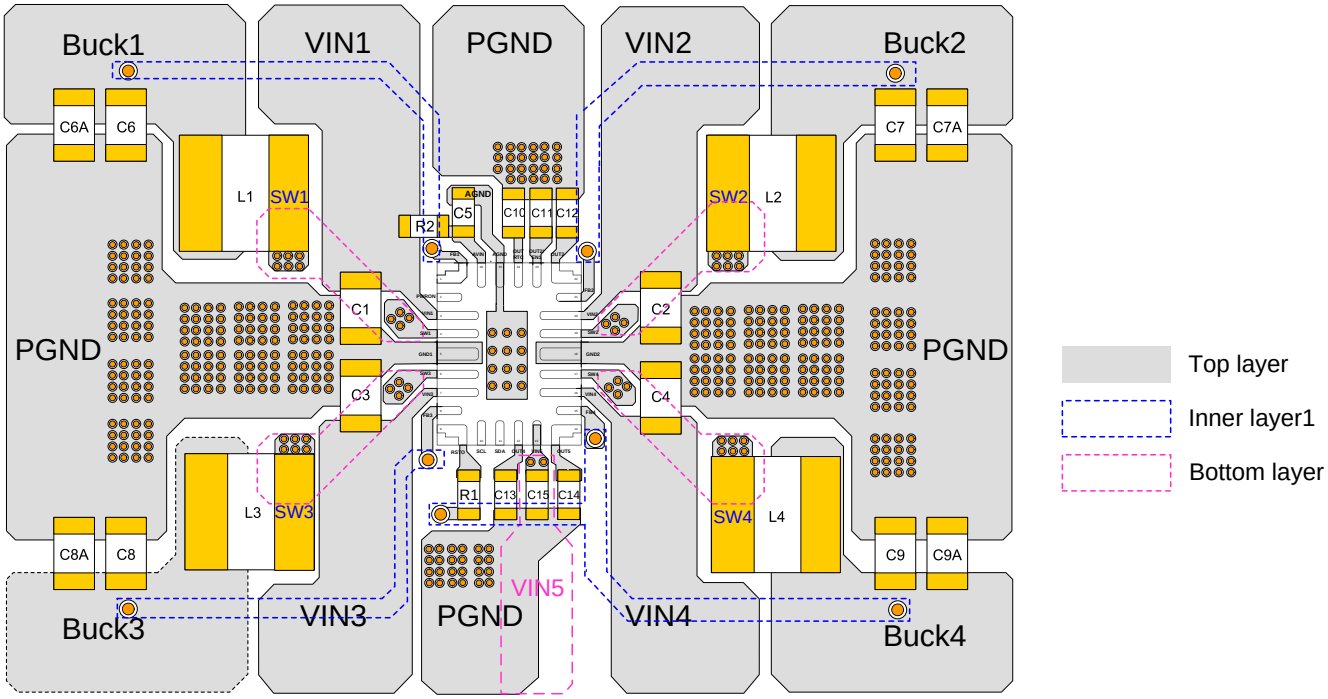


Figure 16: Recommended PCB Layout (19)

Note:

19) It is recommended to separate the buck 1 and buck 3's PGND from buck 2 and buck 4's PGND on the top layer.

TYPICAL APPLICATION CIRCUITS

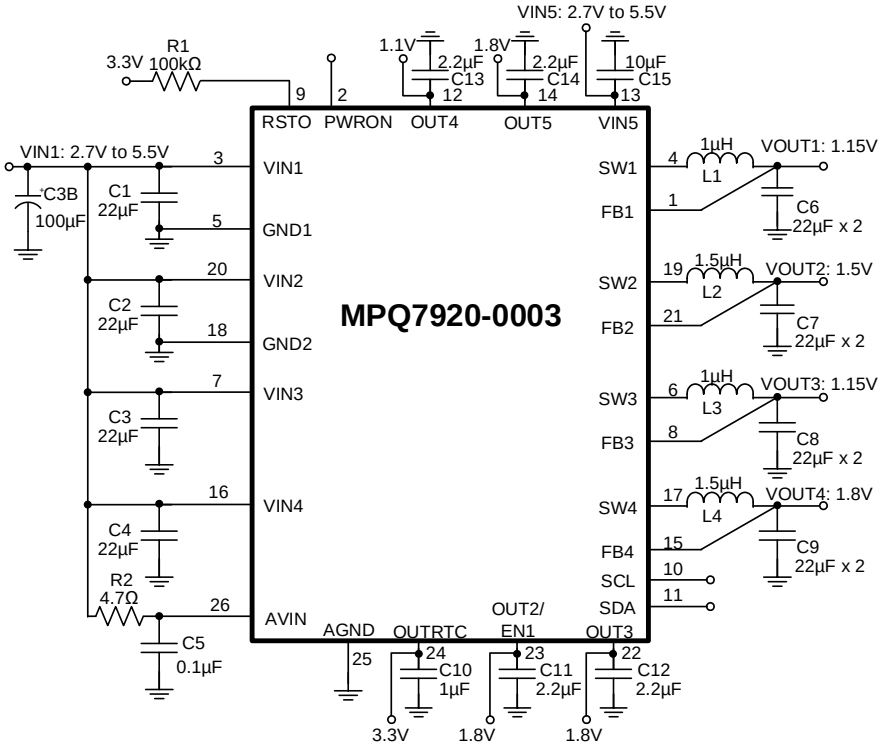


Figure 17: Typical Application Circuit 1 (20) (21)

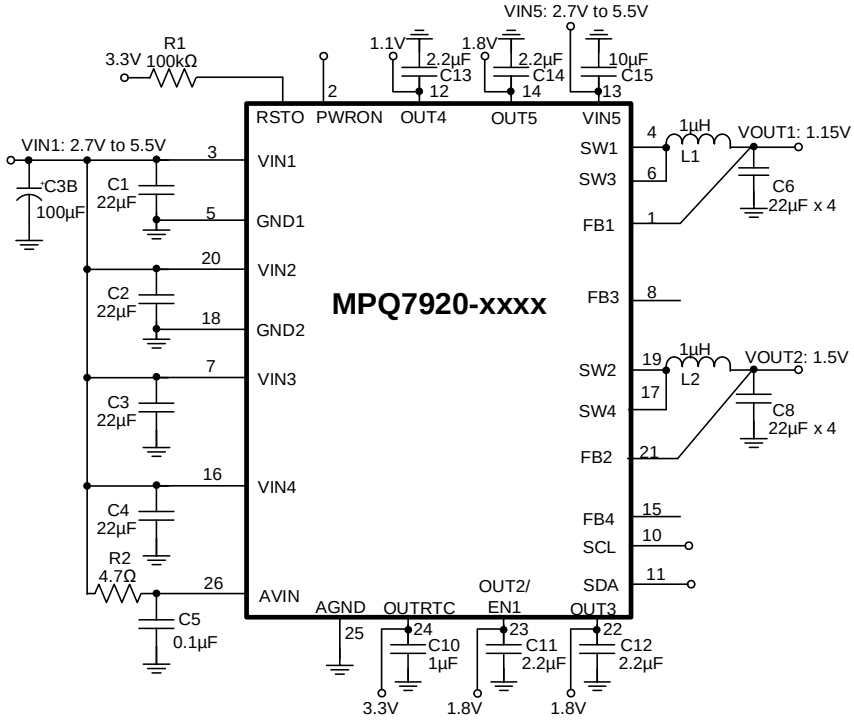


Figure 18: Typical Application Circuit 2 – Parallel Mode (20) (21)

Notes:

20) VIN5's minimum input voltage is equal to the maximum nominal output voltage of LDO4 and LDO5. Connect VIN5 to VIN1 if LDO4 and LDO5 are not used.

21) In the 2.2MHz frequency and small duty cycle condition, ensure that the buck on time is >100ns for better stability.

APPENDIX

MTP E-FUSE SELECTED TABLE BY MPQ7920GRM-0000 (21)

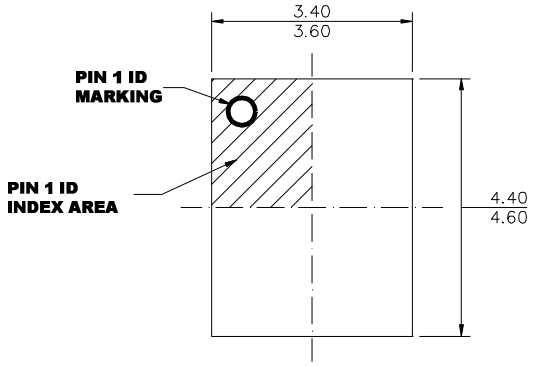
OTP Items	Buck 1	Buck 2	Buck 3	Buck 4	LDOR TC	LDO2	LDO3	LDO4	LDO5
Output voltage	1.35V	1.5V	1.35V	1.8V	1.8V	1.8V	1.8V	3.3V	3.3V
Initial on/off	On	On	On	On	On	On	On	On	On
MODE	FPWM	FPWM	FPWM	FPWM	N/A				
Power-on delay	1.5ms	1ms	1.5ms	0.5ms	Always on	0ms	2ms	5ms	5.5ms
Power-off delay	4ms	4.5ms	4ms	5ms		5.5ms	3.5ms	0.5ms	0ms
Soft-start time	300µs	300µs	300µs	300µs	N/A				
Time slot	0.5ms								
PWR_ON_TIME_SLOT_MODE	Time slot is a fixed number set by TIME_SLOT								
PWR_OFF_TIME_SLOT_MODE	Time slot is a fixed number set by TIME_SLOT								
Switching frequency	2.2MHz								
PWRON mode	0 (level trigger)								
PWRON_DEBOUNCE_TIMER	10ms								
RSTO mode	Not monitor any power rails								
RSTO delay	50ms								
Buck 1 peak current limit	7.6A								
Buck 2 peak current limit	3.9A								
Buck 3 peak current limit	7.6A								
Buck 4 peak current limit	3.9A								
I²C slave address	0x69								
MTP configuration code	0000								

Note:

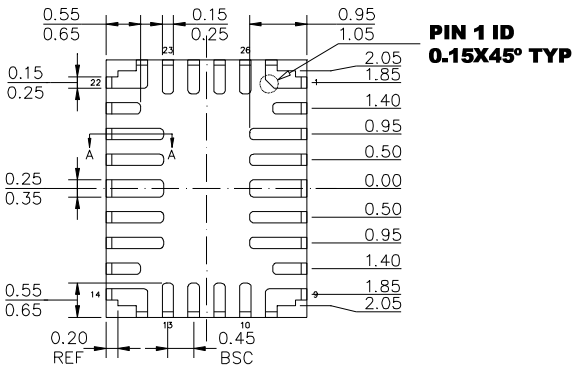
22) MPQ7920GRM-0000-AEC1 is the standard sample version, which can access the MTP 2 times.

PACKAGE INFORMATION

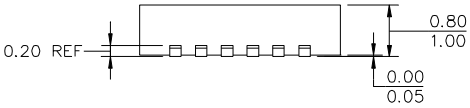
QFN-26 (3.5mmx4.5mm)



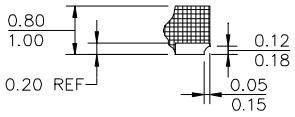
TOP VIEW



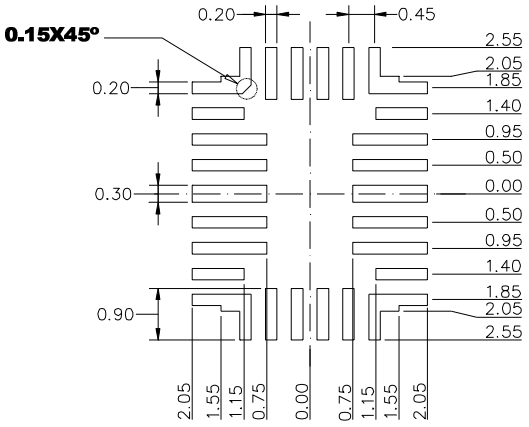
BOTTOM VIEW



SIDE VIEW



SECTION A-A

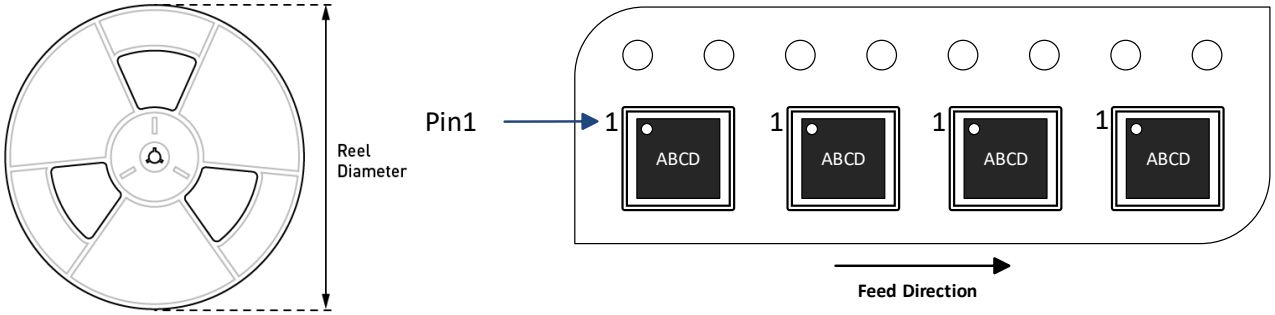


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,9,14,22 HAVE THE SAME LENGTH AND WIDTH.
2)ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7920GRM-0003-AEC1-Z	QFN-26 (3.5mmx4.5mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/13/2020	Initial Release	-
1.1	1/12/2022	Updated the EN1 sections	18–19, 31
		Updated the EN1 Functions section	23
		Updated VIN5 pin description in the Pin Functions section	5
		Updated the package information	1, 43
		Updated RSTO_MODE, RSTO_DELAY, PWR_ON_TIME_SLOT_MODE, PWR_OFF_TIME_SLOT_MODE, and VREF register descriptions	27–29
		Updated LDO4/5 high ILIM to 550mA	16, 30
		Updated Note 20	40
		Grammar and formatting updates	All

单击下面可查看定价，库存，交付和生命周期等信息

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