CQAOS 重庆万国

Green Product

CQA34P01

30V P-CHANNEL MOSFET

Product Summary

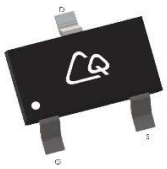
V(BR)DSS	RDS(ON) max	ID max
-30V	<48mΩ @ VGS = -10V	-4A
	<60mΩ @ VGS = -4.5V	

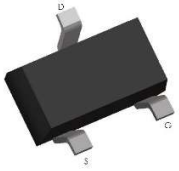
Description and Applications

The CQA34P01 uses advanced trench technology to provide excellent RDS(ON). This device is suitable for use as a load switch or other general applications.

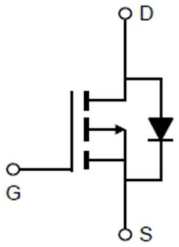
RoHS and Halogen-Free Compliant.

View and Internal Schematic Diagram





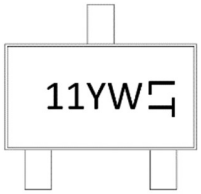
SOT23-3L



Internal Schematic

Marking Information

SOT23-3L



PN=11
YW= Date Code Marking
Y= Year W = Week
LT= Lot code

Ordering Information

Part Number	Case	Packaging
CQA34P01	SOT23	3,000/Tape & Reel; 21,000/Inner Box

Maximum Ratings (@TA = +25°C unless otherwise specified.)

Parameters		Symbol	Max	Units
Drain-Source Voltage		VDSS	-30	V
Gate-Source Voltage		VGSS	±12	V
Continuous Drain Current	TA = +25°C TA = +70°C	ID	-4 -3.2	A
Pulsed Drain Current C		IDM	-27	A
Power Dissipation B	TA = +25°C TA = +70°C	PD	1.4 0.9	W
Operating and Storage Temperature Range		TJ, TG	-55 to+150	°C

Thermal Characteristics

Characteristic		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	70	90	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		100	125	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	33	40	°C/W

Electrical Characteristics (@T_A = +25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
		TJ=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-0.5	-0.9	-1.3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-4.0A		39	48	mΩ
		TJ=125°C		55	75	
		V_{GS}=-4.5V, I_D=-3.5A		43	60	mΩ
		V_{GS}=-2.5V, I_D=-2.5A		50	85	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-4.0A		19		S
V_{SD}	Diode Forward Voltage	I_S=-4.1A,V_{GS}=0V		-0.7	-1.2	V
I_S	Maximum Body-Diode Continuous Current				-1.6	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		753		pF
C_{oss}	Output Capacitance			69		pF
C_{rss}	Reverse Transfer Capacitance			59		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V,		11.5		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-24V, I_D=-4.0A		21		nC
Q_{gs}	Gate Source Charge			2.0		nC
Q_{gd}	Gate Drain Charge			2.4		nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=-10V, V_{DS}=-15V, R_L=15Ω, R_{GEN}=2.5Ω		4.5		ns
t_r	Turn-On Rise Time			32		ns
$t_{D(off)}$	Turn-Off Delay Time			79.5		ns
t_f	Turn-Off Fall Time			62		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-4.0A, dI/dt=100A/μs		8.8		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-4.0A, dI/dt=100A/μs		2.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERIS

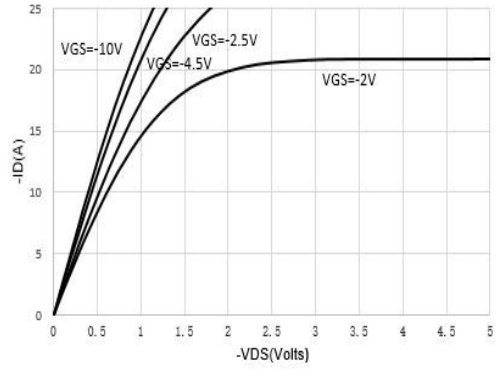


Figure 1：On-Region Characteristics (Note E)

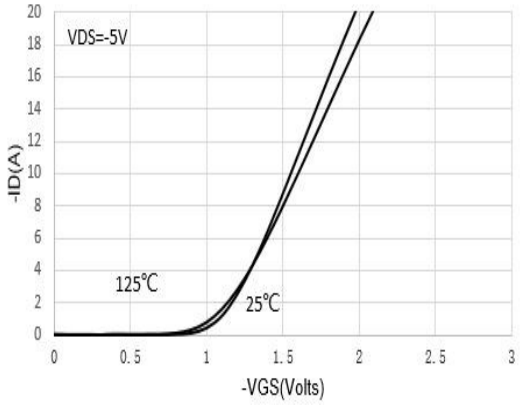


Figure 2 Transfer Characteristics (Note E)

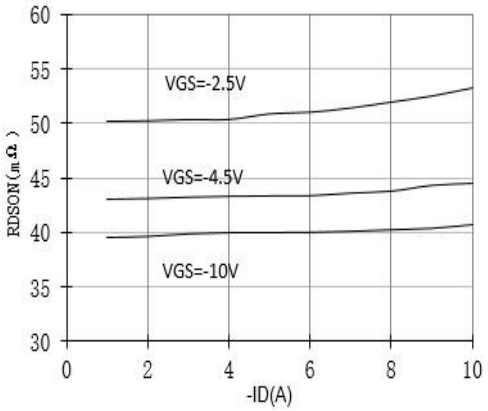


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

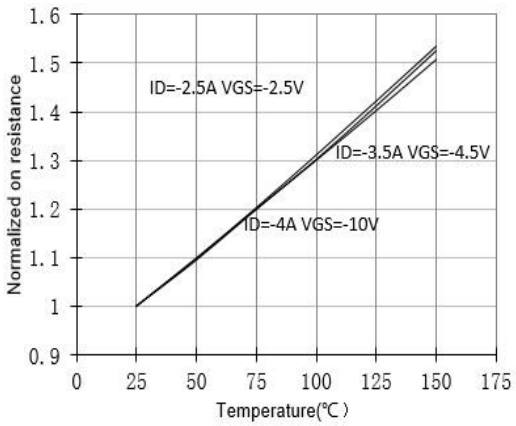


Figure 4: On-Resistance vs. Junction Temperature (Note E)

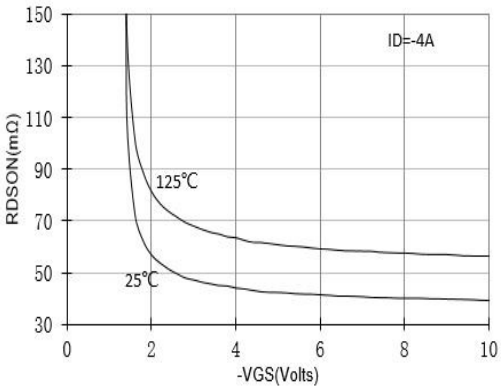


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

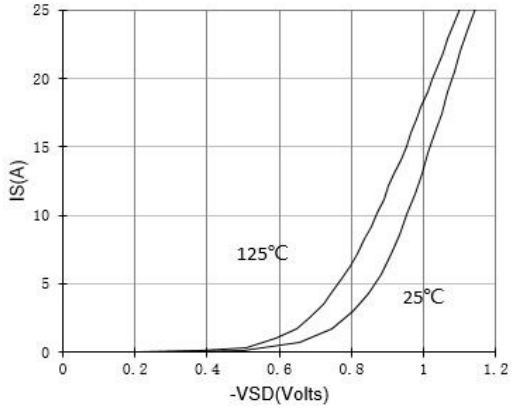


Figure 6: Body-Diode Characteristics (Note E)

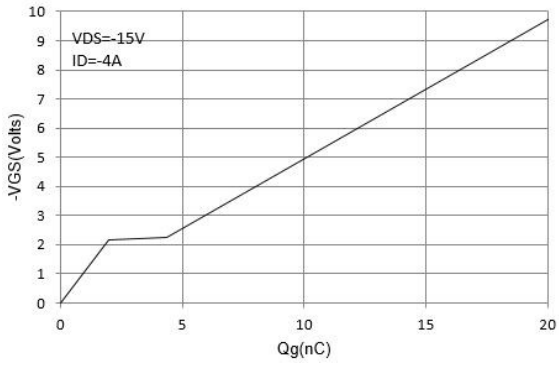


Figure 7: Gate-Charge Characteristics

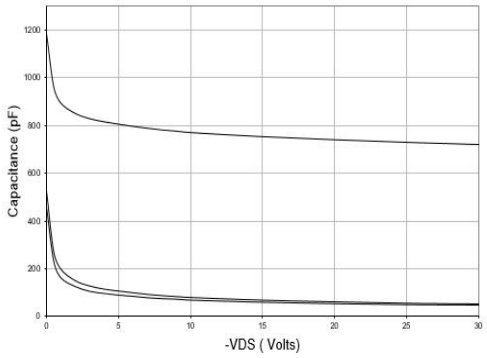


Figure 8: Capacitance Characteristics

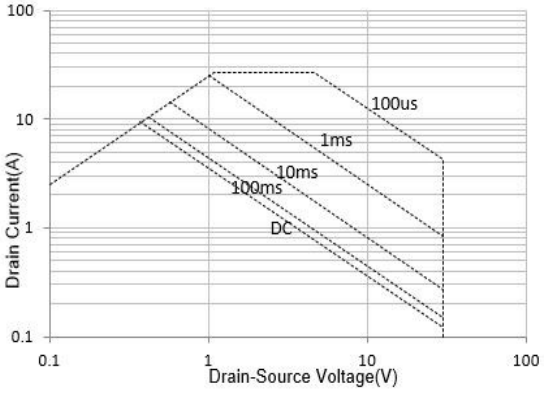


Figure 9: Maximum Forward Biased Safe Operating Area

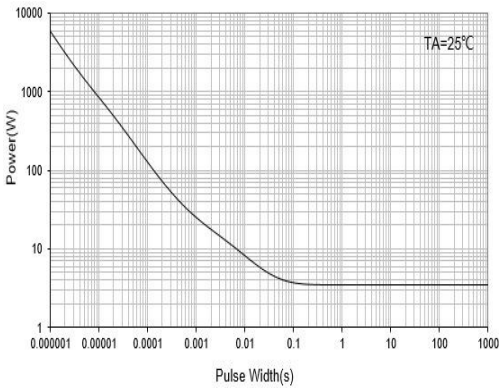


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

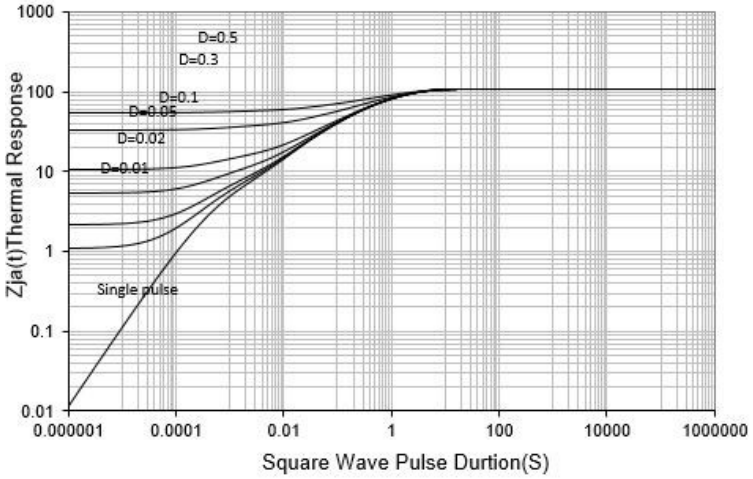


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

单击下面可查看定价，库存，交付和生命周期等信息

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