



GT25Q80A

8M Bits
SPI Nor Flash

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GT25Q80A

1.Features

- Single Power Supply Voltage
 - Full voltage range: 1.65~3.6V
- Operating Temperature range:
 - -40 to +85 °C
- 8M/bit Serial Flash
 - 1M-byte
 - 256 bytes per programmable page
- Standard, Dual, Quad SPI
 - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
 - Dual SPI: CLK, CS#, IO0, IO1, WP#, HOLD#
 - Quad SPI: CLK, CS#, IO0, IO1, IO2, IO3
- High Speed Clock Frequency
 - 80MHz (1.65~2.3V), 120MHz(2.3~3.6V)
 - 120MHz for fast read with 30PF load
 - Dual I/O Data transfer up to 240Mbits/s
 - Quad I/O Data transfer up to 480Mbits/s
- Software/Hardware Write Protection
 - Write protect all/portion of memory via software
 - Enable/Disable protection with WP# Pin
 - Top/Bottom Block protection
- Allows XIP (execute in place) Operation
 - Continuous Read With 8/16/32/64-byte Wrap
- Data Retention
 - 20-year data retention typical
- Minimum 200,000 Program/Erase Cycles
- ESD protection (Human Body Model)
 - -6500V to +6500V
- Fast Program/Erase Speed
 - Page Program time: 1.25ms typical
 - Sector Erase time: 2.5ms typical
 - Block Erase time: 2.5ms typical
 - Chip Erase time: 5ms typical
- Flexible Architecture
 - Uniform Sector of 1K-byte
 - Uniform Sector of 4K-byte
 - Uniform Block of 32/64K-byte
 - Erase/Program Suspend/Resume
- Low Power Consumption
 - 7uA typical Standby current
 - 0.1uA typical power down current
- Advanced security Features
 - 4*256-Byte Security Registers With OTP Lock
 - 64-Bit Unique Serial Number for each device
- Space Efficient Packaging:
 - 8-pin SOIC 208/150 mil
 - 8-pad WSON 6X5 mm
 - USON8 2X3 mm
 - 8-pin TSSOP
 - 8-ball WLCSP
 - Contact Giantec for KGD and other



GT25Q80A

2. General Description

GT25Q80A is 8Mb bits Serial NOR Flash, the array is organized into 4096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 4 (1Kb sector erase), groups of 16 (4KB Sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase), The device operates on a single 1.65V to 3.6V power supply with current consumption as low as 1mA active and 0.1 μ A for power-down. All devices are offered in space-saving packages.

The GT25Q80A supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 120MHz are supported allowing equivalent clock rates of 240MHz (120MHz x 2) for Dual I/O and 480MHz (120MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

A Hold pin, Write Protect pin and programmable write protection, with top, bottom or complement array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique ID. GT25Q80A features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (CLK), a serial data input (DI), and a serial data output (DO). Serial access to the device is enabled by CS# input.

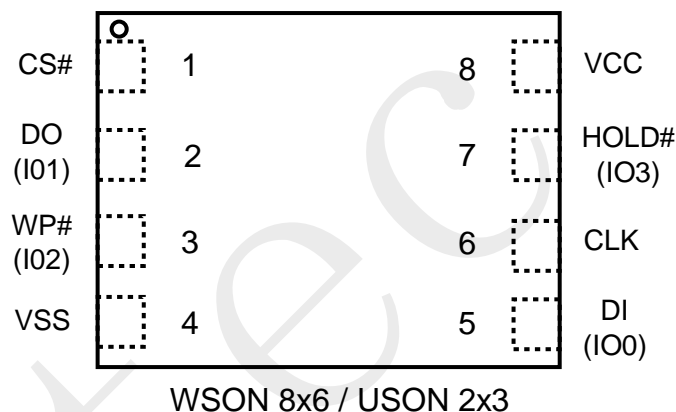
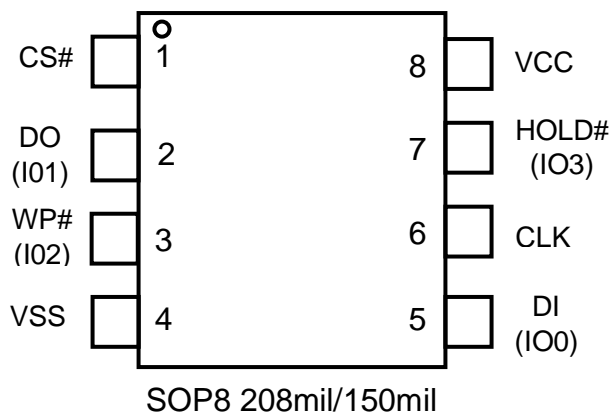


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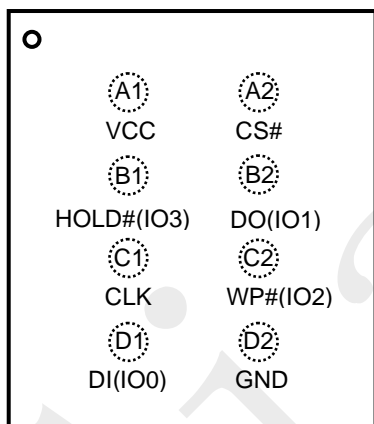
3. Package Types:

GT25Q80A is offered in an 8-pin plastic 208mil/150-mil width SOIC (package code SN), an 8-pad WSON 6X5-mm (package code ZP), an 8-pad USON 2x3-mm (package code UX), and 8-pad WLCSP as below. Package diagrams and dimensions are illustrated at the end of this datasheet.

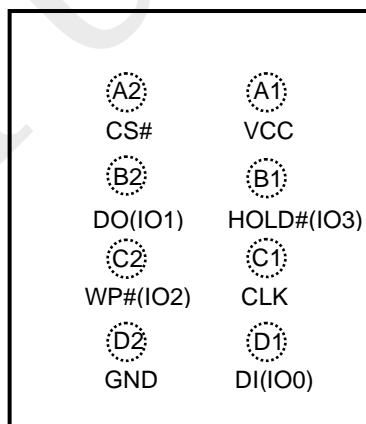
3.1 Pin Configuration



Top View



Bottom View



8Ball WLCSP



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3.2 Pin Description

| Pin Name | I/O | Function |
|-------------|-----|--|
| /CS | I | Chip Select Input |
| DO(IO1) | I/O | Data Output (Data Input Output 1)*1 |
| /WP(I/O2) | I/O | Write Protect Input (Data Input Output 2)*2 |
| GND | | Ground |
| DI(I/O0) | I/O | Data Input (Data Input Output 0)*1 |
| CLK | I | Serial Clock Input |
| /HOLD(I/O3) | I/O | Hold Input (Data Input Output 3)*2 |
| VCC | | Power Supply |

3.3 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and figure instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see "Write Protection"). If needed a pull-up resistor on /CS can be used to accomplish this.

3.4 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The GT25Q80A supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

3.5 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2.

3.6 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See the pin configuration of Quad I/O operation.

3.7 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

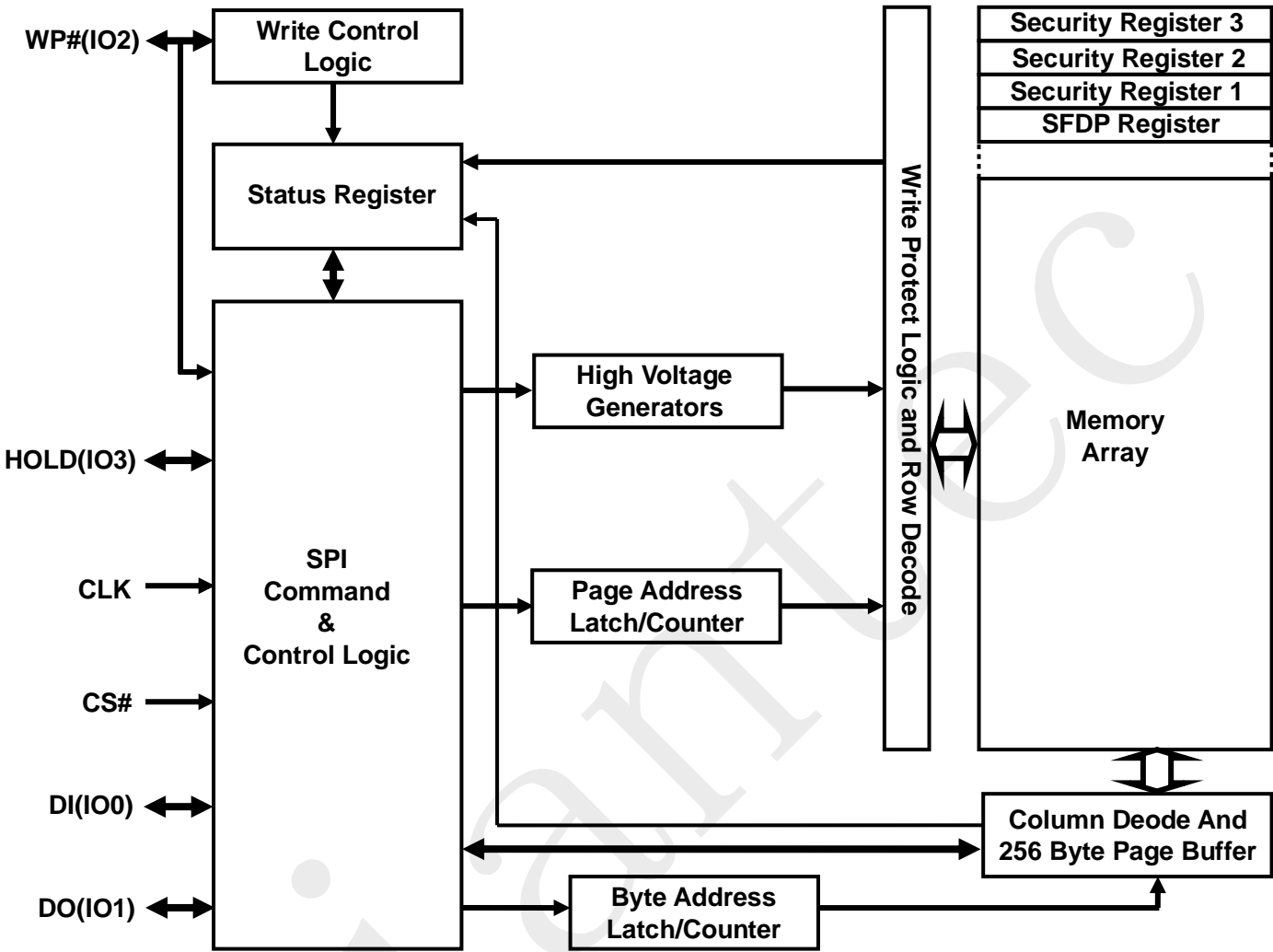
Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.



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4. BLOCK DIAGRAM





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5. Memory Architecture Diagram (8Mb)

| 64KB Block | 32KB Block | 4KB Block | Block Address Range | 256Byte Page | Page Address Range |
|------------|------------|-----------|---------------------|--------------|--------------------|
| 64KB | 32KB | 4KB | 0FFFFh – 0FF000h | 256 Bytes | 0FFFFh – 0FF00h |
| | | 4KB | 0FEFFh – 0FE000h | 256 Bytes | 0FEFFh – 0FE00h |
| | | 4KB | 0FDFFh – 0FD000h | 256 Bytes | 0FDFFh – 0FD00h |
| | | 4KB | 0FCFFh – 0FC000h | 256 Bytes | 0FCFFh – 0FC00h |
| | | 4KB | 0FBFFh – 0FB000h | 256 Bytes | 0FBFFh – 0FB00h |
| | | 4KB | 0FAFFh – 0FA000h | 256 Bytes | 0FAFFh – 0FA00h |
| | | 4KB | 0F9FFh – 0F9000h | 256 Bytes | 0F9FFh – 0F900h |
| | | 4KB | 0F8FFh – 0F8000h | 256 Bytes | 0F8FFh – 0F800h |
| | 32KB | 4KB | 0F7FFh – 0F7000h | 256 Bytes | 0F7FFh – 0F700h |
| | | 4KB | 0F6FFh – 0F6000h | 256 Bytes | 0F6FFh – 0F600h |
| | | 4KB | 0F5FFh – 0F5000h | 256 Bytes | 0F5FFh – 0F500h |
| | | 4KB | 0F4FFh – 0F4000h | 256 Bytes | 0F4FFh – 0F400h |
| | | 4KB | 0F3FFh – 0F3000h | 256 Bytes | 0F3FFh – 0F300h |
| | | 4KB | 0F2FFh – 0F2000h | 256 Bytes | 0F2FFh – 0F200h |
| | | 4KB | 0F1FFh – 0F1000h | 256 Bytes | 0F1FFh – 0F100h |
| | | 4KB | 0F0FFh – 0F0000h | 256 Bytes | 0F0FFh – 0F000h |
| . | . | . | . | . | . |
| . | . | . | . | . | . |
| . | . | . | . | . | . |
| 64KB | 32KB | 4KB | 00FFFh – 00F000h | 256 Bytes | 00FFFh – 00F00h |
| | | 4KB | 00EFFh – 00E000h | 256 Bytes | 00EFFh – 00E00h |
| | | 4KB | 00DFFh – 00D000h | 256 Bytes | 00DFFh – 00D00h |
| | | 4KB | 00CFFh – 00C000h | 256 Bytes | 00CFFh – 00C00h |
| | | 4KB | 00BFFh – 00B000h | 256 Bytes | 00BFFh – 00B00h |
| | | 4KB | 00AFFh – 00A000h | 256 Bytes | 00AFFh – 00A00h |
| | | 4KB | 009FFh – 009000h | 256 Bytes | 009FFh – 00900h |
| | | 4KB | 008FFh – 008000h | 256 Bytes | 008FFh – 00800h |
| | 32KB | 4KB | 007FFh – 007000h | 256 Bytes | 007FFh – 00700h |
| | | 4KB | 006FFh – 006000h | 256 Bytes | 006FFh – 00600h |
| | | 4KB | 005FFh – 005000h | 256 Bytes | 005FFh – 00500h |
| | | 4KB | 004FFh – 004000h | 256 Bytes | 004FFh – 00400h |
| | | 4KB | 003FFh – 003000h | 256 Bytes | 003FFh – 00300h |
| | | 4KB | 002FFh – 002000h | 256 Bytes | 002FFh – 00200h |
| | | 4KB | 001FFh – 001000h | 256 Bytes | 001FFh – 00100h |
| | | 4KB | 000FFh – 000000h | 256 Bytes | 000FFh – 00000h |



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6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings(1)

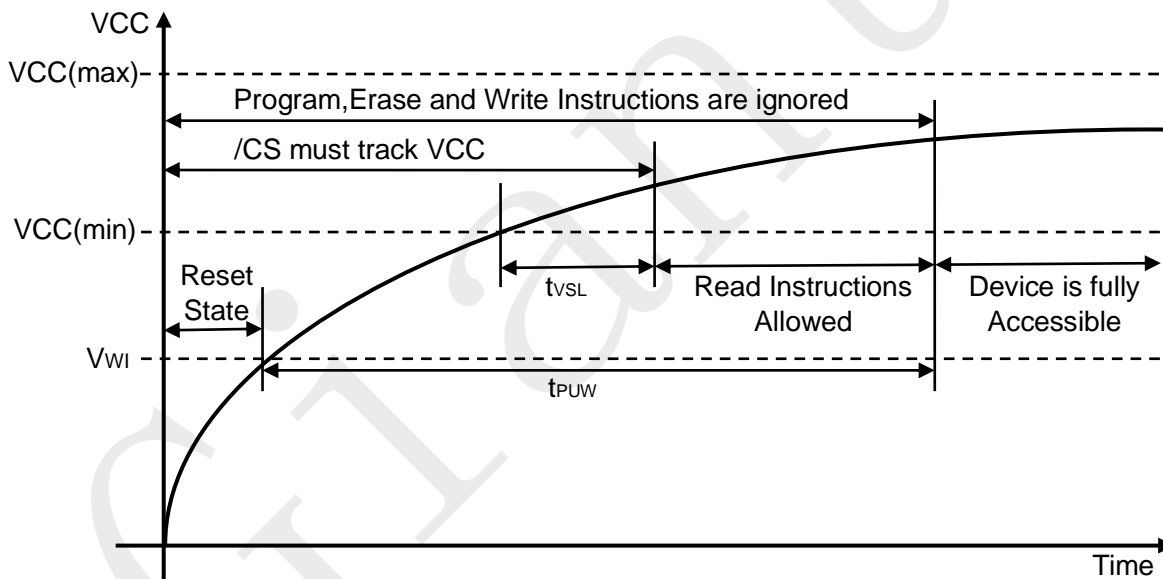
| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---------------------------------|-------------------|------------------------------------|-------------------|------|
| Supply Voltage | VCC | | -0.6 to VCC+0.6V | V |
| Voltage Applied to Any Pin | V _{IO} | Relative to Ground | -0.6 to VCC+0.4V | V |
| Transient Voltage on any Pin | V _{IO} T | <20nS Transient Relative to Ground | -2.0V to VCC+2.0V | V |
| Storage Temperature | T _{STG} | | -65 to +150 °C | °C |
| Ambient Operating Temperature | T _a | | -45 to +85 °C | °C |
| Electrostatic Discharge Voltage | V _{ESD} | Human Body Model(2) | -6500 to +6500 V | V |

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

6.2 Power-up Timing and Write Inhibit Threshold



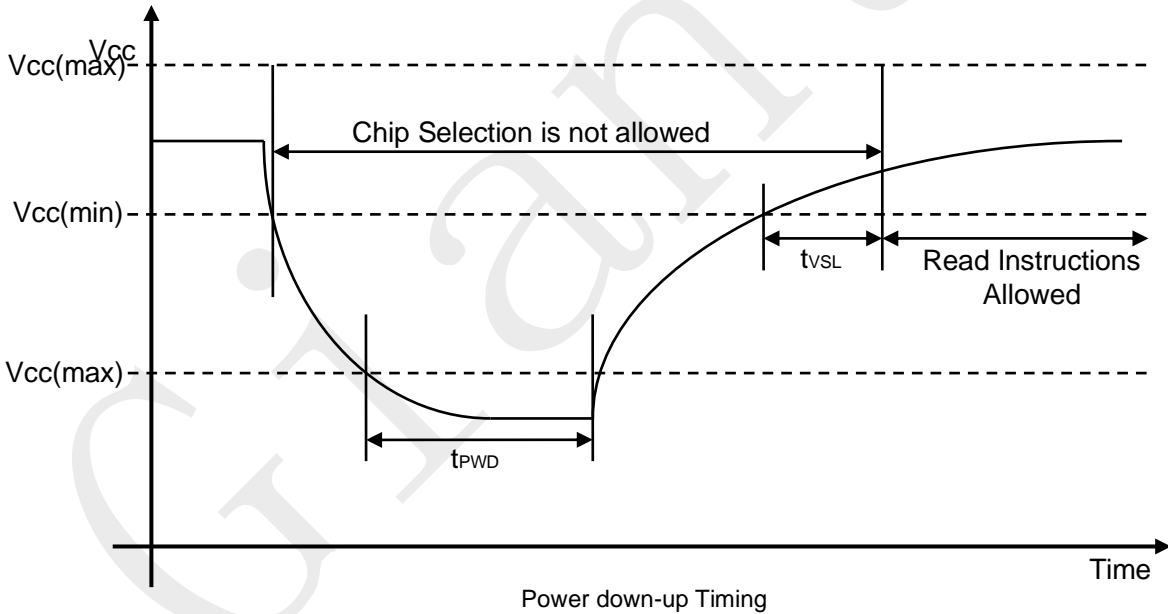
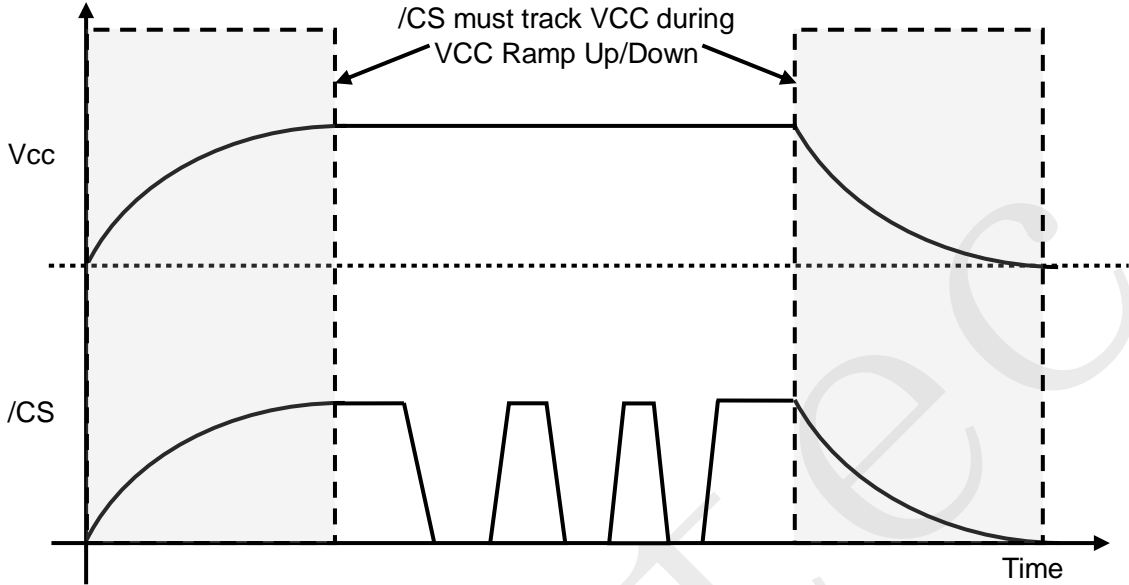
Power-up Timing and Voltage Levels

| PARAMETERS | SYMBOL | spec | | UNIT |
|-------------------------------------|----------------------|------|-----|------|
| | | Min | Max | |
| VCC (min) to /CS Low | t _{VSL} (1) | 10 | | μs |
| Time Delay Before Write Instruction | t _{PUW} (1) | 5 | | ms |
| Write Inhibit Threshold Voltage | V _{WI} (1) | 1.0 | 1.4 | V |



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6.3 Power Up/Down and Voltage Drop



Power down-up Timing

| Symbol | Parameter | min | max | unit |
|--------|---|-----|--------|------|
| VPWD | VCC voltage needed to below VPWD for ensuring initialization will occur | | 1 | V |
| tPWD | The minimum duration for ensuring initialization will occur | 300 | | us |
| tvR | VCC Rise Time | 1 | 500000 | us/V |



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6.4 DC Electrical Characteristics:

| Symbol | Parameter | Conditions | 1.65 to 2.3V | | | 2.3 to 3.6V | | | Unit |
|--------|-----------------------------|--|--------------|------|---------|-------------|------|---------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| ISB | Standby Current | CS#=Vcc, all other inputs at 0V or Vcc | | 7.0 | | | 7.0 | | μA |
| IDBD | Deep power down current | CS#=Vcc, all other inputs at 0V or Vcc | | 0.1 | | | 0.2 | | μA |
| ICC1 | Current Read Data(03h) | Fr=1MHz | | 0.5 | 1 | | 1.0 | 2 | mA |
| | | Fr=33MHz | | 1 | 1.5 | | 2.0 | 3 | mA |
| ICC2 | Current Read Data Excep 03h | Fr=50MHz | | 1.2 | 1.8 | | 2.5 | 4 | mA |
| | | Fr=80MHz | | 1.5 | 2.5 | | 3.6 | 5 | mA |
| | | Fr=120MHz | | | | | 5.0 | 8 | mA |
| ICC3 | Program current | CS#=Vcc | | 1.0 | 1.5 | | 1.5 | 2.5 | mA |
| ICC4 | Erase Current 4K | CS#=Vcc | | 0.5 | 1.0 | | 0.9 | 1.5 | mA |
| ICC5 | Erase Current 32K | CS#=Vcc | | 0.5 | 1.0 | | 0.9 | 1.5 | mA |
| ICC6 | Erase Current 64K | CS#=Vcc | | 0.5 | 1.0 | | 0.9 | 1.5 | mA |
| ICC7 | Erase Current Chip | CS#=Vcc | | 0.5 | 1.0 | | 1.0 | 2 | mA |
| ILI | Input Leakage Current | | | 0.2 | 0.5 | | 0.2 | 0.5 | μA |
| ILO | Output Leakage Current | | | 0.2 | 0.5 | | 0.2 | 0.5 | μA |
| VIL | Input Low Voltage | | -0.5 | | 0.2VCC | -0.5 | | 0.3VCC | V |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.4 | 0.7VCC | | VCC+0.4 | V |
| VOL | Output Low Voltage | IOL=100μA | | | 0.2 | | | 0.2 | V |
| VOH | Output High Voltage | IOH=-100μA | VCC-0.2 | | | VCC-0.2 | | | V |

Note:

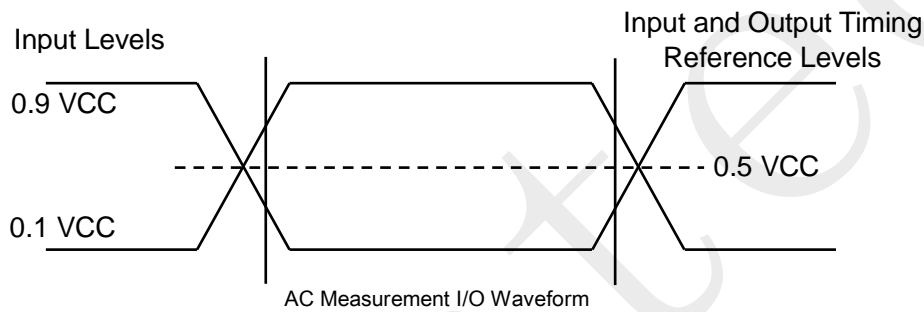
13. Typical values measured at 1.8V @ 25°C for the 1.65V to 2.3V range, 3.0V @ 25°C for the 2.3V to 3.6V range .



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6.5 AC Measurement Conditions

| PARAMETER | SYMBOL | SPEC | | UNIT |
|----------------------------------|--------|--------------------|-----|------|
| | | MIN | MAX | |
| Load Capacitance | CL | | 30 | pF |
| Input Rise and Fall Times | TR,TF | | 5 | ns |
| Input Pulse Voltages | VIN | 0.1 VCC to 0.9 VCC | | V |
| Input Timing Reference Voltages | IN | 0.3 VCC to 0.7 VCC | | V |
| Output Timing Reference Voltages | OUT | 0.5 VCC to 0.5 VCC | | V |



6.6 AC Characteristics

| Symbol | Description | 1.65V~3.6V | | | Unit |
|----------|---|------------|------|------|----------|
| | | Min. | Typ. | Max. | |
| Fr | Clock frequency for all instructions vdd from 1.65-2.3V | D.C. | | 80 | MHz |
| | Clock frequency for all instructions vdd from 2.3-2.7V | D.C. | | 120 | MHz |
| | Clock frequency for all instructions vdd from 2.7-3.6V | D.C. | | 120 | MHz |
| Tch(1) | Clock High Time | 5.5 | | | ns |
| Tcl(1) | Clock Low Time | 5.5 | | | ns |
| Tclch(4) | Clock Rise Time peak to peak | 0.1 | | | V/ ns |
| Tchcl(4) | Clock Fall Time peak to peak | 0.1 | | | V/ ns |
| Tsich | CS# Active Setup Time (relative to CLK) | 7 | | | ns |
| Tchsl | CS# Not Active Hold Time (relative to CLK) | 5 | | | ns |
| Tdvch | Data In Setup Time | 2 | | | ns |
| Tchdx | Data In Hold Time | 3 | | | ns |
| Tchsh | CS# Active Hold Time (relative to CLK) | 5 | | | ns |
| Tshch | CS# Not Active Setup Time (relative to CLK) | 5 | | | ns |



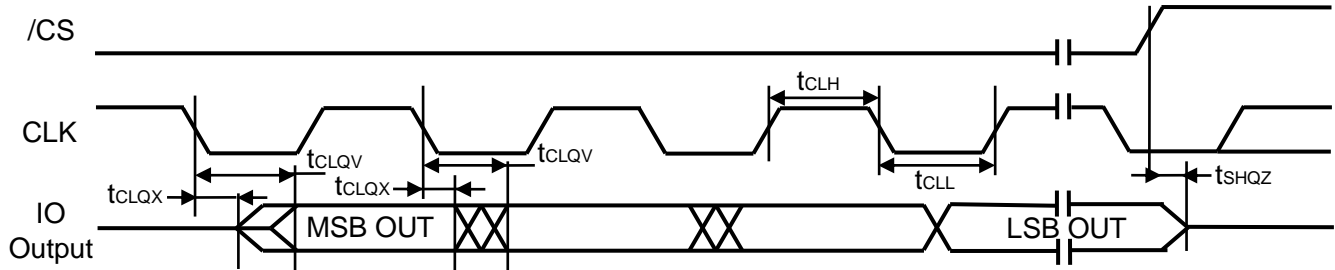
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| Symbol | Description | 1.65V to 3.6V | | | Unit |
|----------|---|---------------|------|--|------|
| | | Min. | Typ. | Max. | |
| Tshsl | CS# Deselect Time From Read to next Read | 15 | | | ns |
| | CS# Deselect Time From Erase ,Program to Read Status Register | 30 | | | ns |
| Tshqz(4) | Output Disable Time | | | 6 | ns |
| Tclqv | Clock Low to Output Valid | | | 7@2.7~3.6V 9@2.3~2.7V 13@1.65~2.3V | ns |
| Tclqx | Output Hold Time | 0 | | | ns |
| Thlch | HOLD# Active Setup Time (relative to CLK) | 5 | | | ns |
| Tchhh | HOLD# Active Hold Time (relative to CLK) | 5 | | | ns |
| Thhch | HOLD# Not Active Setup Time (relative to CLK) | 5 | | | ns |
| Tchhl | HOLD# Not Active Hold Time (relative to CLK) | 5 | | | ns |
| Thhqx | HOLD# to Output Low-Z | | | 6 | ns |
| Thlqz | HOLD# to Output High-Z | | | 6 | ns |
| Twhsl(3) | Write Protect Setup Time | 20 | | | ns |
| Tshwl(3) | Write Protect Hold Time | 100 | | | ns |
| Tdp | CS# High to Deep Power-down Mode | | | 3 | us |
| Tres1 | CS# High To Standby Mode Without ID Read | | | 3 | us |
| Tres2 | CS# High To Standby Mode With ID Read | | | 1.8 | us |
| Tsus | CS# High to next Instruction after Suspend | | | 20 | μs |
| Trst | CS# High to next Instruction after reset (except chip erase 60/C7h) | | | 30 | μs |
| | CS# High to Chip erase after reset | | | 150 | us |
| Tw | Write Status Register Cycle Time | | 2 | 3 | ms |
| Tbp | Byte Program Time (First Byte) | | 100 | 150 | μs |
| Tpp | Page Program Time | | 1.25 | 1.5 | ms |
| Tse | Sector erase time | | 2.5 | 3 | ms |
| Tbe1 | Block erase time for 32K bytes | | 2.5 | 3 | ms |
| Tbe2 | Block erase time for 64K bytes | | 2.5 | 3 | ms |
| Tce | Chip erase time | | 5 | 6 | ms |

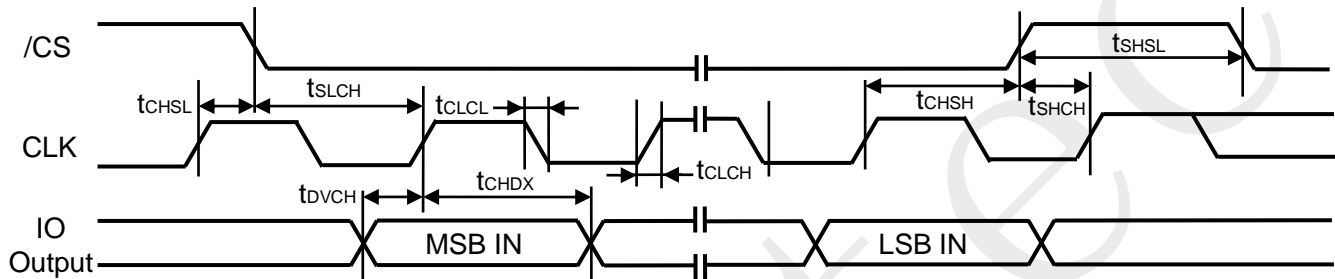


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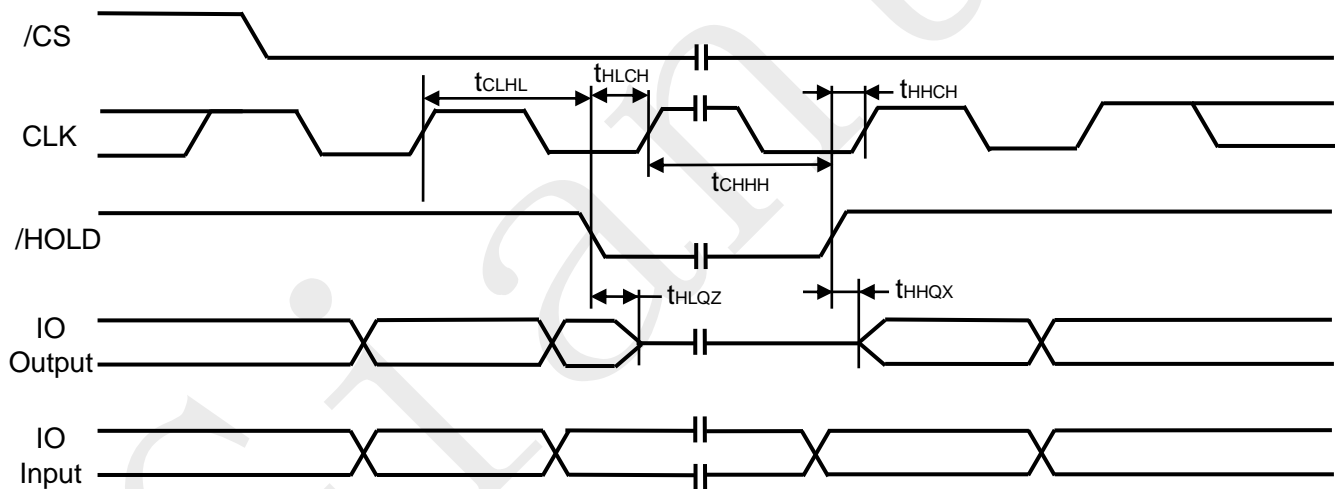
6.7 Serial Output Timing



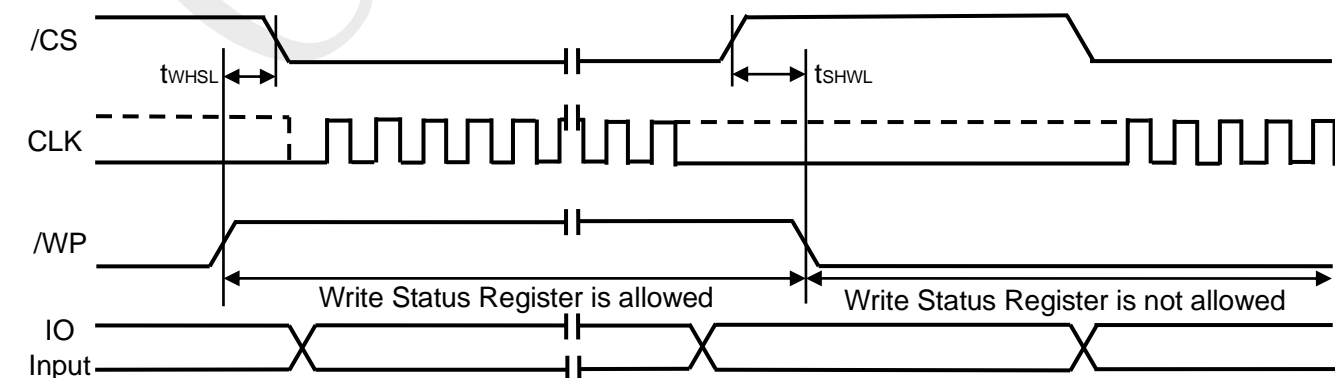
6.8 Serial Input Timing



6.9 /HOLD Timing



6.9 /WP Timing





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7 FUNCTIONAL DESCRIPTION

7.1 Standard SPI Instructions

The GT25Q80A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

7.2 Dual SPI Instructions

The GT25Q80A supports Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

7.3 Quad SPI Instructions

The GT25Q80A supports Quad SPI operation when using the “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)” instructions. These instructions allow data to be transferred to or from the device six to eight times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

7.4 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the GT25Q80A operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD, when QE=1, the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active low for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.



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7.5 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the [GT25Q80A](#) provides several means to protect the data from inadvertent writes.

7.6 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up
- One Time Program (OTP) write protection*

* Note: This feature is available upon special order. Please contact Giantec for details.

Upon power-up or at power-down, the GT25Q80A will maintain a reset condition while VCC is below the threshold value of VWI, (See Power-up Timing and Voltage Levels). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached. If needed a pull-up resistor on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits. These settings allow a portion as small as 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

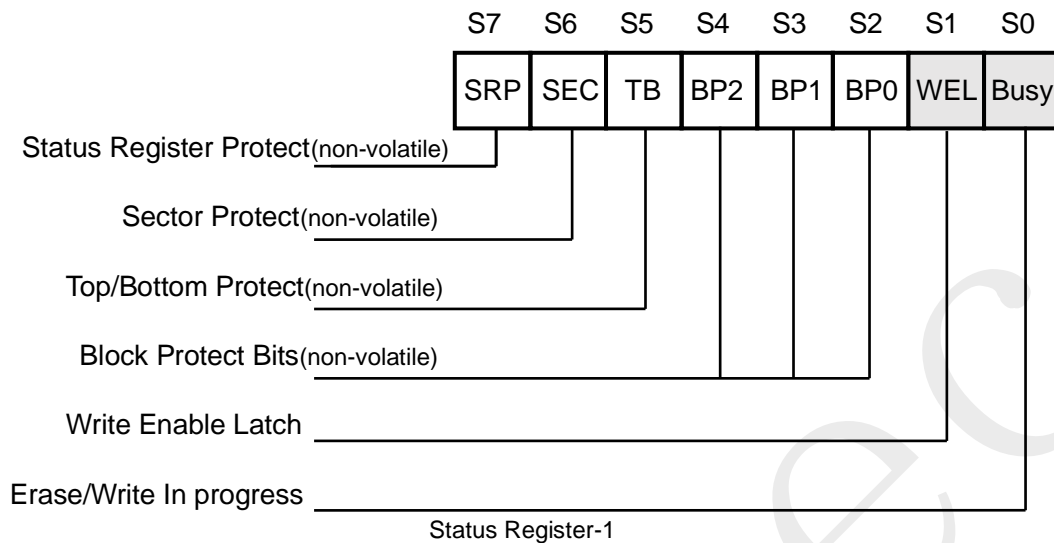
8 STATUS REGISTERS AND INSTRUCTIONS

The Read Status Register-1 and Status Register-2 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status and Erase/Program Suspend status. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting and Security Register OTP lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.



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8.1 STATUS REGISTER 1



8.1.1 BUSY Status (BUSY)

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.1.2 Write Enable Latch Status (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

8.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

8.1.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP and WEL bits.

8.1.5 Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.



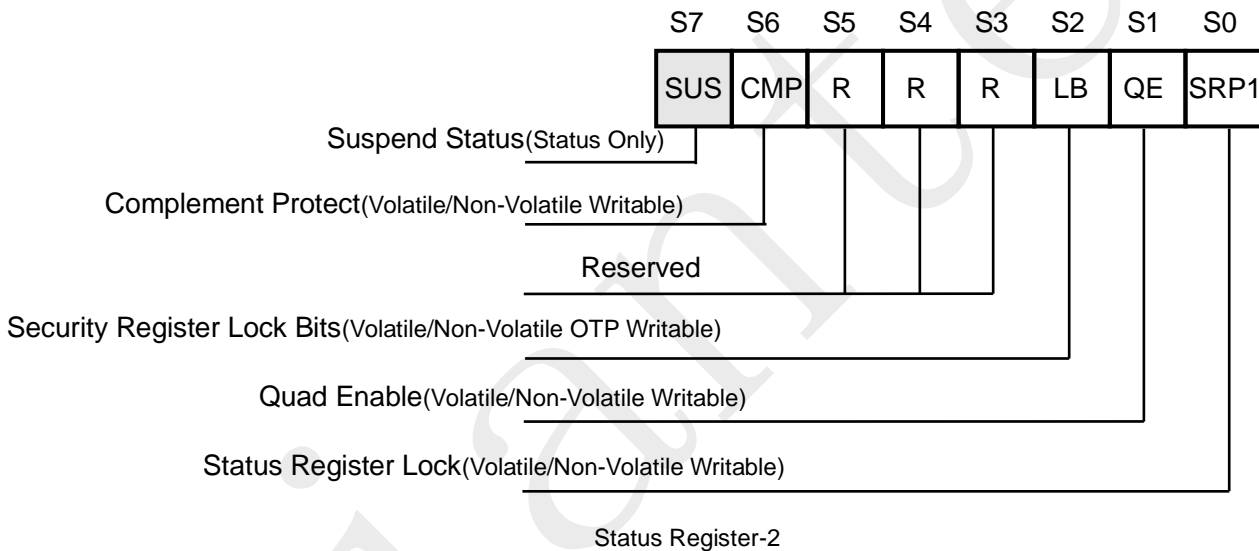
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8.1.7 Status Register Protect (SRP)

The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bits control the method of write protection: software protection.

| SRP | /WP | Status Protection | Description |
|-----|-----|----------------------|--|
| 0 | X | Software Protection | /WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default] |
| 1 | 0 | Hardware Protected | When /WP pin is low the Status Register can not be written to. |
| | 1 | Hardware Unprotected | When /WP pin is high the Status register can be written to after a Write Enable instruction, WEL=1. |

8.2 STATUS REGISTER 2



8.2.1 Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75H or B0H) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7AH or 30H) instruction as well as a power-down, power-up cycle.

8.2.2 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

8.2.3 Security Register Lock Bits (LB) – Volatile/Non-Volatile OTP Writable

The Security Register Lock Bits (LB) are non-volatile One Time Program (OTP) bits in Status Register-2(S2) that provide the write protect control and status to the Security Registers. The default state of LB is 0, Security Registers are unlocked. LB can be set to 1 individually using the Write Status Register instruction. LB are One Time Programmable (OTP), once it's set to 1, the



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corresponding 4x256-Byte Security Register will become read-only permanently.

8.2.4 Quad Enable (QE) – Non-Volatile Writable

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

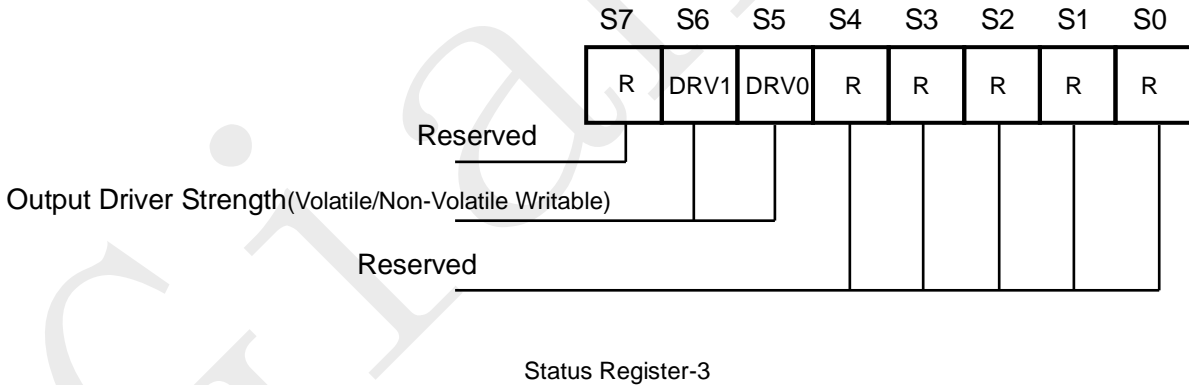
8.2.5 Lock Down and OTP (SRL)

| SRL | Status Protection | Description |
|-----|---|--|
| 0 | Non-Lock | Status Register is unlocked |
| 1 | Lock-Down(1) (temporary/Volatile) | Status Register is locked by standard status register write command and can not be written to again until the next power-down, power-up cycle. |
| | One Time Program(2) (Permanently/Non-Volatile) | Status Register is permanently locked by special command flow* and can not be written to |

Note:

- When SRP = 1, a power-down, power-up cycle will change SRP = 0 state.
- Special One Time Protection feature is available upon special order; please contact Giantec for details

8.3 STATUS REGISTER 3



8.3.1 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

| DRV1 | DRV0 | Driver Strength |
|------|------|-----------------|
| 0 | 0 | 100% |
| 0 | 1 | 50% |
| 1 | 0 | 25% |
| 1 | 1 | 10%(default) |



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8.3.2 Reserved Bits - Non Functional

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

8.4 Status Register Memory Protection (CMP = 0)

Table1

| STATUS REGISTER(1) | | | | | GT25Q80L (8M-BIT) MEMORY PROTECTION(2) | | | |
|--------------------|----|-----|-----|-----|--|--------------------|---------|-------------|
| SEC | TB | BP2 | BP1 | BP0 | BLOCK(S) | ADDRESSES | DENSITY | PORTION |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 15 | 0F0000h – 0FFFFFFh | 64KB | Upper 1/16 |
| 0 | 0 | 0 | 1 | 0 | 14 and 15 | 0E0000h – 0FFFFFFh | 128KB | Upper 1/8 |
| 0 | 0 | 0 | 1 | 1 | 12 and 15 | 0C0000h – 0FFFFFFh | 256KB | Upper 1/4 |
| 0 | 0 | 1 | 0 | 0 | 8 and 15 | 080000h – 0FFFFFFh | 512KB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 | 000000h – 00FFFFh | 64KB | Lower 1/16 |
| 0 | 1 | 0 | 1 | 0 | 0 and 1 | 000000h – 01FFFFh | 128KB | Lower 1/8 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 3 | 000000h – 03FFFFh | 256KB | Lower 1/4 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 7 | 000000h – 07FFFFh | 512KB | Lower 1/2 |
| 0 | 1 | 1 | 0 | 1 | 0 thru 15 | 000000h – 0FFFFFFh | 1MB | ALL |
| X | X | 1 | 1 | X | 0 thru 31 | 000000h – 0FFFFFFh | 1MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 15 | 0FF000h – 0FFFFFFh | 4KB | Upper 1/256 |
| 1 | 0 | 0 | 1 | 0 | 15 | 0FE000h – 0FFFFFFh | 8KB | Upper 1/128 |
| 1 | 0 | 0 | 1 | 1 | 15 | 0FC000h – 0FFFFFFh | 16KB | Upper 1/64 |
| 1 | 0 | 1 | 0 | X | 15 | 0F8000h – 0FFFFFFh | 32KB | Upper 1/32 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h – 00FFFFh | 4KB | Lower 1/256 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h – 001FFFh | 8KB | Lower 1/128 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h – 003FFFh | 16KB | Lower 1/64 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h – 007FFFh | 32KB | Lower 1/32 |
| 1 | X | 1 | 1 | 1 | 0 thru 15 | 000000h – 0FFFFFFh | 1MB | ALL |

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.



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8.5 Status Register Memory Protection (CMP = 1)

Table2

| STATUS REGISTER(1) | | | | | GT25Q80L (8M-BIT) MEMORY PROTECTION(2) | | | |
|--------------------|----|-----|-----|-----|--|--------------------|---------|---------------|
| SEC | TB | BP2 | BP1 | BP0 | BLOCK(S) | ADDRESSES | DENSITY | PORTION |
| X | X | 0 | 0 | 0 | 0 thru 15 | 000000h – 0FFFFFFh | 1MB | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 14 | 000000h – 0EFFFFh | 960KB | Lower 15/16 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 13 | 000000h – 0DFFFFh | 896KB | Lower 7/8 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 11 | 000000h – 0BFFFFh | 768KB | Lower 3/4 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 7 | 000000h – 07FFFFh | 512KB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 1 thru 15 | 010000h – 0FFFFFFh | 960KB | Upper 15/16 |
| 0 | 1 | 0 | 1 | 0 | 2 thru 15 | 020000h – 0FFFFFFh | 896KB | Upper 7/8 |
| 0 | 1 | 0 | 1 | 1 | 4 thru 15 | 040000h – 0FFFFFFh | 768KB | Upper 3/4 |
| 0 | 1 | 1 | 0 | 0 | 8 thru 15 | 080000h – 0FFFFFFh | 512KB | Upper 1/2 |
| 0 | X | 1 | 0 | 1 | NONE | NONE | NONE | NONE |
| 0 | X | 1 | 1 | X | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 thru 15 | 000000h – 0EFFFFh | 1020KB | Lower 255/256 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 15 | 000000h – 0FDFFFh | 1016KB | Lower 127/128 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 15 | 000000h – 0FBFFFh | 1008KB | Lower 63/64 |
| 1 | 0 | 1 | 0 | X | 0 thru 15 | 000000h – 0F7FFFh | 992KB | Lower 31/32 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 15 | 001000h – 0FFFFFFh | 1020KB | Upper 255/256 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 15 | 002000h – 0FFFFFFh | 1016KB | Upper 127/128 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 15 | 004000h – 0FFFFFFh | 1008KB | Upper 63/64 |
| 1 | 1 | 1 | 0 | X | 0 thru 15 | 008000h – 0FFFFFFh | 992KB | Upper 31/32 |
| 1 | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.



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9 Commands DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of CLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on DI, and each bit is latched on the rising edges of CLK.

See below Table, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power- Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

9.1 Commands Table

| Command Name | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte6 | Byte N |
|--------------------------|--------|--------------------|-------------------|------------|---------|------------|------------|
| Number of Clock | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Write Enable | 06h | | | | | | |
| Write Disable | 04h | | | | | | |
| Volatile SR Write Enable | 50h | | | | | | |
| Read Status Register1 | 05h | S7-S0 | | | | | continuous |
| Read Status Register2 | 35h | S15-S8 | | | | | continuous |
| Read Status Register3 | 15h | S23-S16 | | | | | continuous |
| Write Status Register1 | 01H | S7-S0 | S15-S8 | | | | |
| Write Status Register2 | 31H | S15-S8 | | | | | |
| Write Status Register3 | 11H | S23-S16 | | | | | |
| Read Data | 03h | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | Next byte | continuous |
| Fast Read | 0Bh | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | continuous |
| Dual Output Fast Read | 3Bh | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | continuous |
| Dual I/O Fast Read | BBH | A23-A8(2) | A7-A0 M7-M0(2) | (D7-D0)(1) | | | continuous |
| Quad Output Fast Read | 6BH | A23-A16 | A15-A8 | A7-A0 | Dummy | (D7-D0)(3) | continuous |
| Quad I/O Fast Read | EBH | A23-A0 M7-M0(4) | dummy(5) | (D7-D0)(3) | | | continuous |
| Page Program | 02H | A23-A16 | A15-A8 | A7-A0 | D7-D0 | Next byte | |
| Quad Page Program | 32H | A23-A16 | A15-A8 | A7-A0 | D7-D0 | Next byte | |
| Sector Erase(1KB) | 82H | A23-A16 | A15-A8 | A7-A0 | | | |
| Sector Erase(4KB) | 20H | A23-A16 | A15-A8 | A7-A0 | | | |



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| Command Name | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte6 | Byte N |
|--|--------|----------------|---------------|-------------------|-----------|-----------|------------|
| Block Erase(32KB) | 52H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(64K) | D8H | A23-A16 | A15-A8 | A7-A0 | | | |
| Chip Erase | C7/60H | | | | | | |
| Enable Reset | 66H | | | | | | |
| Reset | 99H | | | | | | |
| Set Burst with Wrap | 77H | W6-W4 | | | | | |
| Program/Erase Suspend | 75H | | | | | | |
| Program/Erase Resume | 7AH | | | | | | |
| Deep Power-Down | B9H | | | | | | |
| Release From Deep Power-Down, And Read Device ID | ABH | dummy | dummy | dummy | (ID7-ID0) | | continuous |
| Manufacturer / Device ID | 90H | dummy | dummy | 00h | (M7-M0) | (ID7-ID0) | continuous |
| Manufacturer/ Device ID by Dual I/O | 92H | A23-A8 | A7-A0, M[7:0] | (M7-M0) (ID7-ID0) | | | continuous |
| Manufacturer/ Device ID by Quad I/O | 94H | A23-A0, M[7:0] | dummy | (M7-M0) (ID7-ID0) | | | continuous |
| Read Identification | 9FH | (M7-M0) | (ID15-ID8) | (ID7-ID0) | | | continuous |
| Read Unique ID | 4Bh | dummy | dummy | dummy | dummy | UID63-0) | |
| Read SFDP Register | 5AH | A23-A16 | A15-A8 | A7-A0 | Dummy | | continuous |
| Erase Security Registers(8) | 44h | A23-A16 | A15-A8 | A7-A0 | | | |
| Program Security Registers(8) | 42H | A23-A16 | A15-A8 | A7-A0 | D7-D0 | D7-D0 | |
| Read Security Registers(8) | 48H | A23-A16 | A15-A8 | A7-A0 | dummy | D7-D0 | |

NOTE:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

IO0 = (D4, D0,)

IO1 = (D5, D1,)

IO2 = (D6, D2,)

IO3 = (D7, D3,.....)

4. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2



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IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Data

IO0 = (x, x, x, x, D4, D0,...)

IO1 = (x, x, x, x, D5, D1,...)

IO2 = (x, x, x, x, D6, D2,...)

IO3 = (x, x, x, x, D7, D3,...)

6. Fast Word Read Quad I/O Data

IO0 = (x, x, D4, D0,...)

IO1 = (x, x, D5, D1,...)

IO2 = (x, x, D6, D2,...)

IO3 = (x, x, D7, D3,...)

7. Fast Word Read Quad I/O Data: the lowest address bit must be 0.

8. Security Registers Address:

Security Register1: A23-A16=00H, A15-A9=0001000b, A8-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A9=0010000b, A8-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A9=0011000b, A8-A0= Byte Address.

9.2 Manufacturer and Device Identification

| Command | M7-M0 | ID15-ID8 | ID7-ID0 |
|---------|-------|----------|---------|
| 9FH | C4h | 60 | 14 |
| 90H | C4h | | 13 |
| ABH | | | 13 |

9.3 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

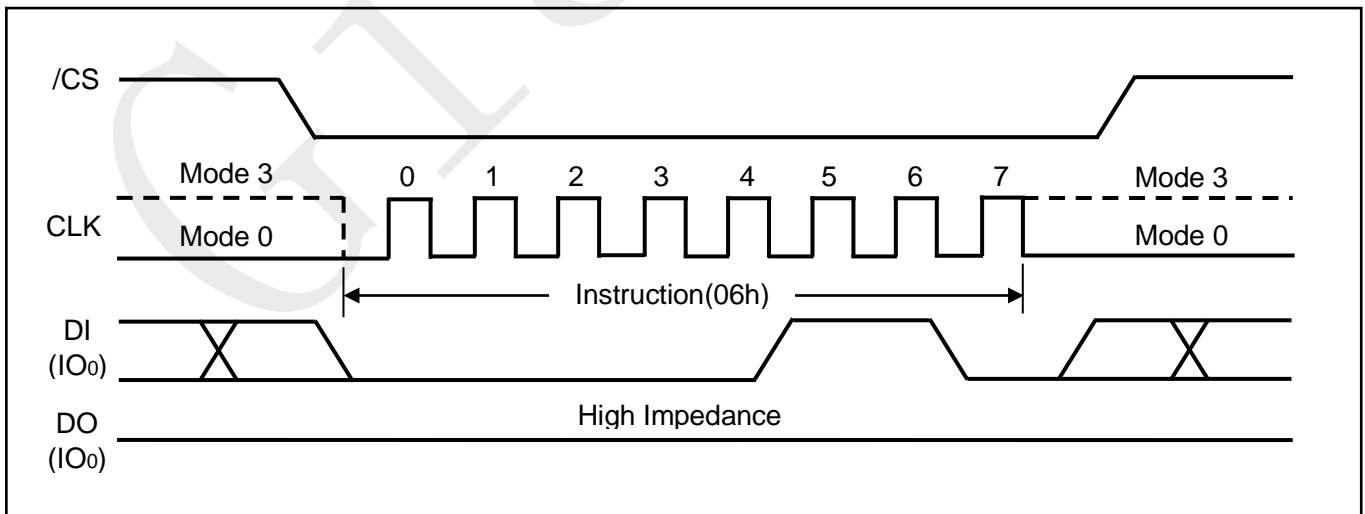


Figure1 Write Enable Sequence Diagram



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9.4 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low → Sending the Write Disable command → CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, Chip Erase, Erase/Program Security Registers and Reset commands.

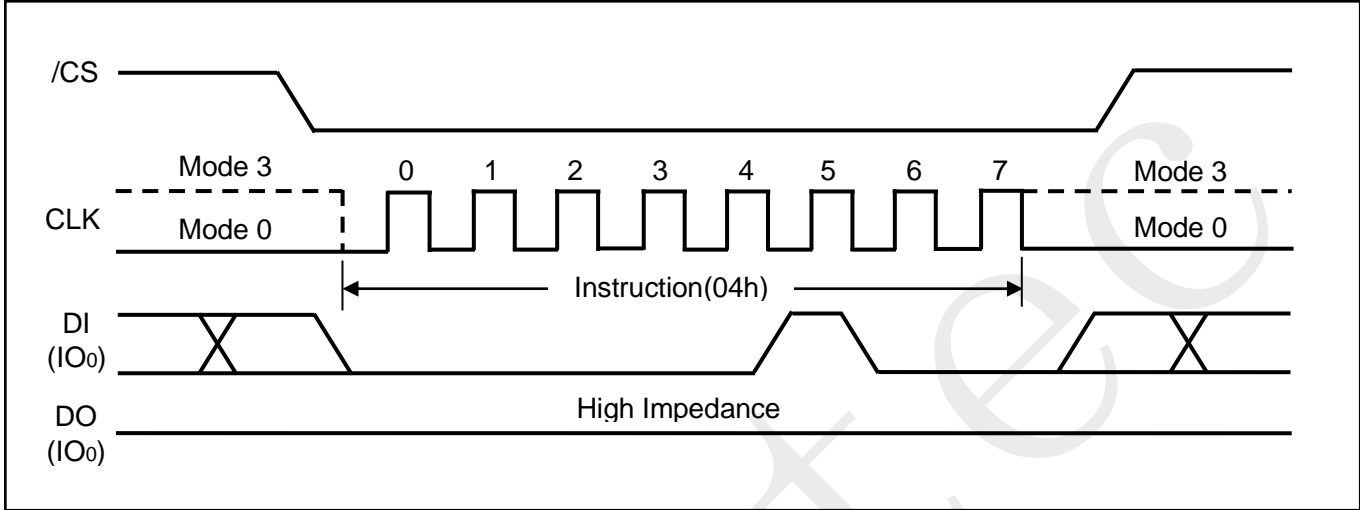


Figure2. Write Disable Sequence Diagram

9.5 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

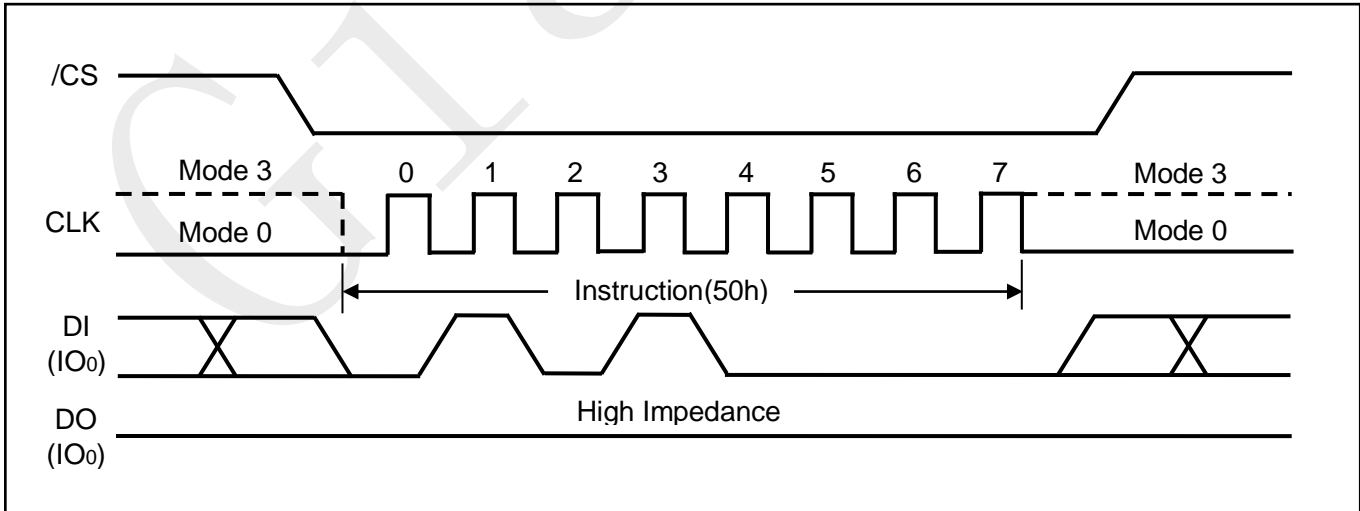


Figure3. Write Enable for Volatile Status Register Sequence Diagram



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9.6 Read Status Register (05h/35h/15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1 or “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 4. The Status Register bits in Status register1 and 2 include the BUSY, WEL, BP2-BP0, TB, SEC, SRP, SRL, QE, LB, CMP and SUS bits (see Status Register section earlier in this datasheet).

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 4. The instruction is completed by driving /CS high.

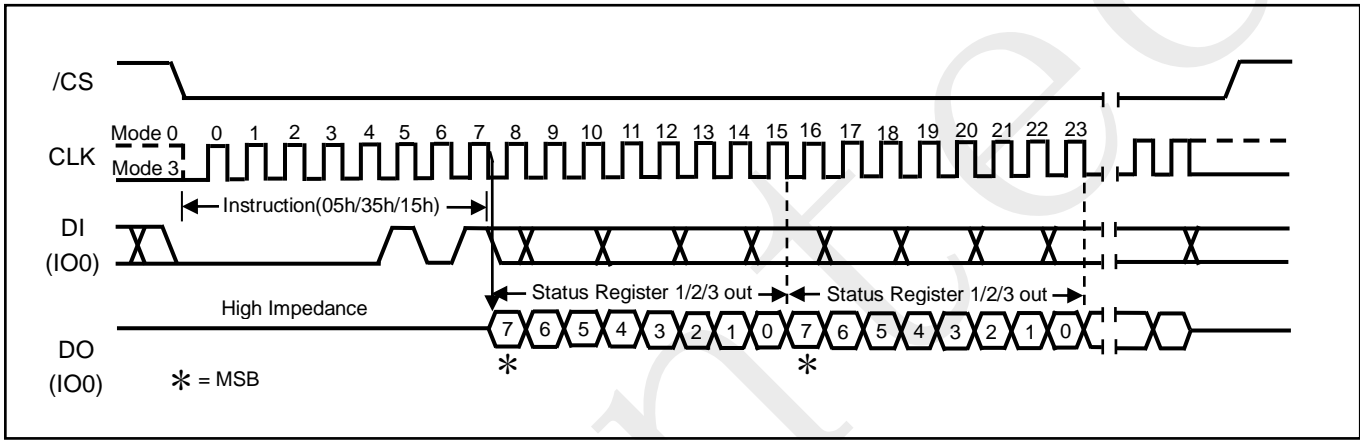


Figure4. Read Status Register Sequence Diagram



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9.7 Write Status Register (WRSR) (01h/31h/11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP, SEC, TB, BP[2:0] in Status Register-1; CMP, LB, QE, SRL in Status Register-2. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 5a.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h, after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

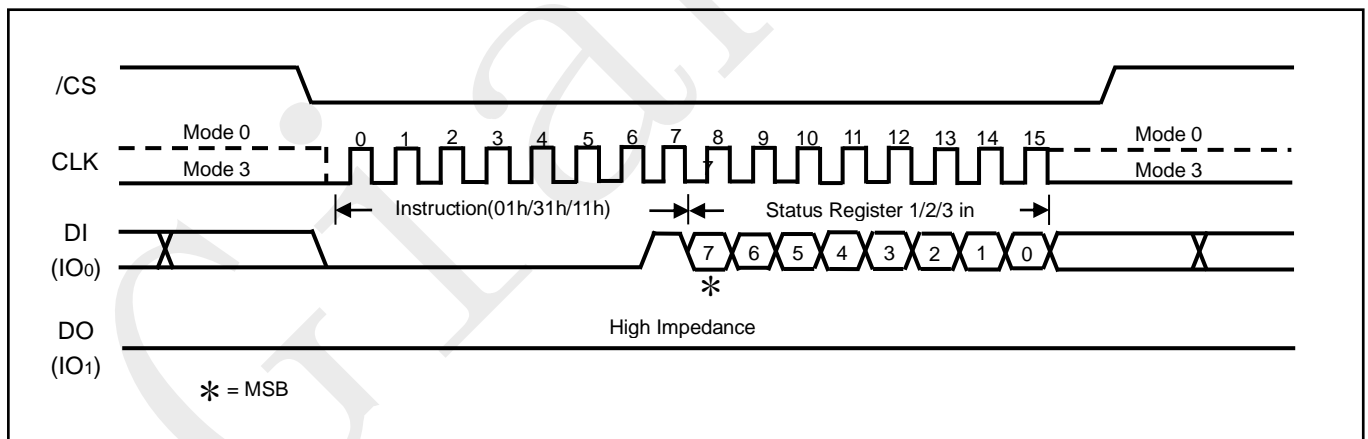


Figure5a. Write Status Register Sequence Diagram

The GT25Q40/20/10/05C is also backward compatible to Giantec’s previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single “Write Status Register-1 (01h)” command. To complete the Write Status Register-1&2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 9c & 9d. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected (Previous generations will clear CMP and QE bits).



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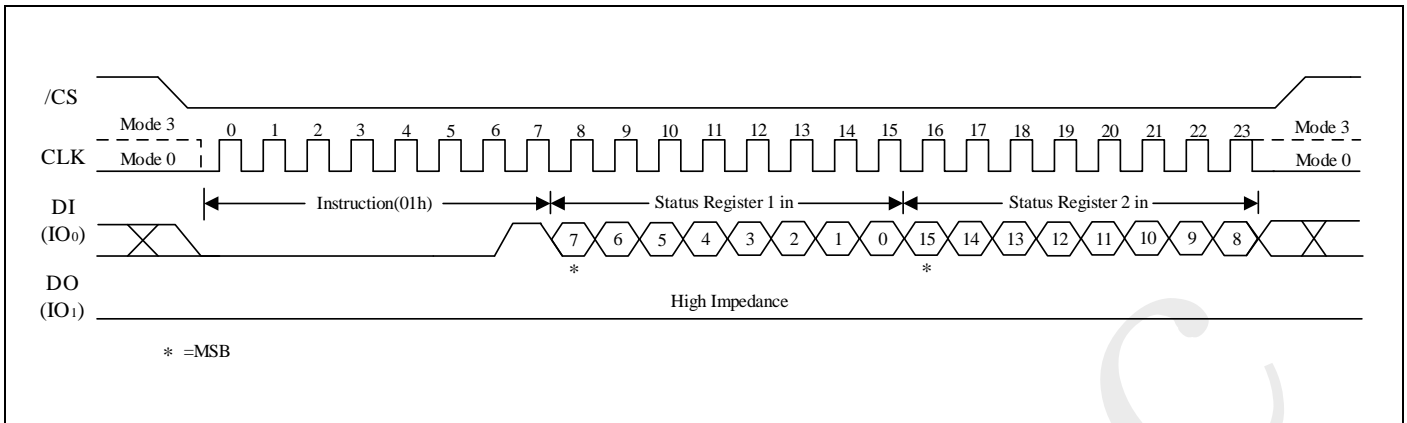


Figure 5b. Write Status Register Sequence Diagram

9.8 Read Data Bytes (READ) (03h)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), and each bit is latched-in on the rising edge of CLK. Then the memory content, at that address, is shifted out on DO, and each bit is shifted out, at a Max frequency f_R , on the falling edge of CLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

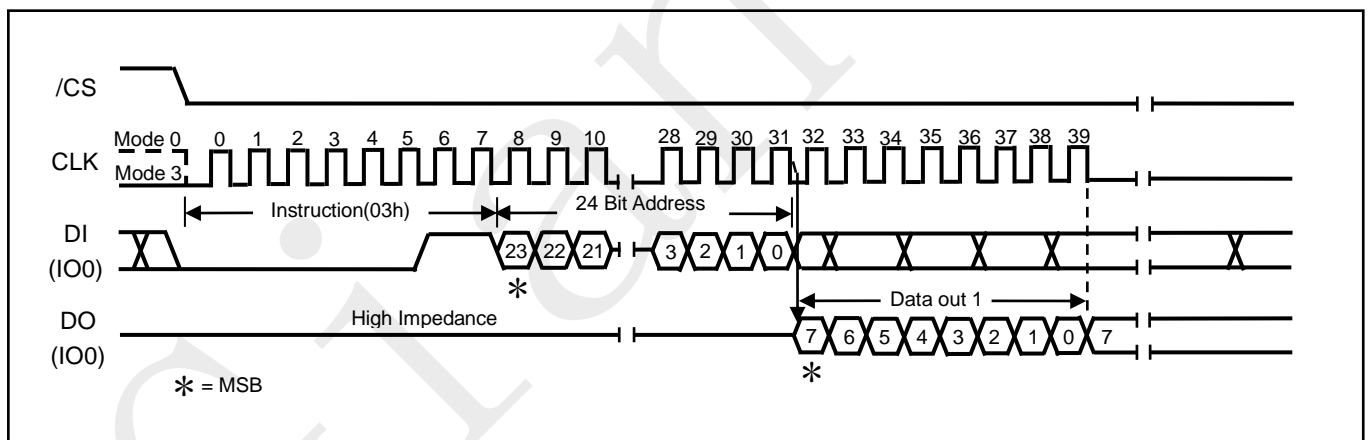


Figure 6. Read Data Bytes Sequence Diagram



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9.9 Fast Read (0Bh)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of CLK. Then the memory content, at that address, is shifted out on DO, and each bit is shifted out, at a Max frequency fC, on the falling edge of CLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

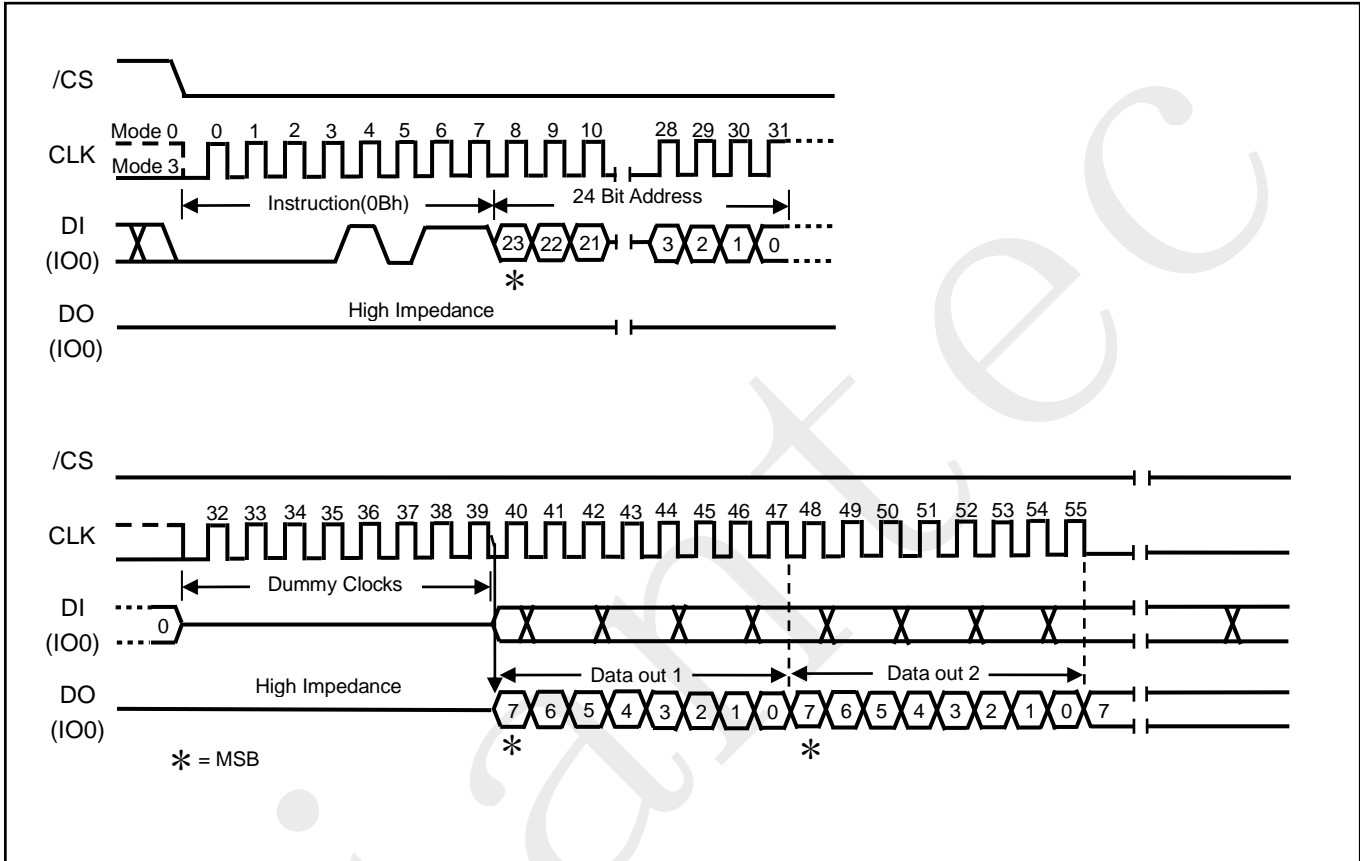


Figure7. Read Data Bytes at Higher Speed Sequence Diagram



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9.10 Dual Output Fast Read (3Bh)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 2-bit per clock cycle from DI and DO. The command sequence is shown in followed Figure8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

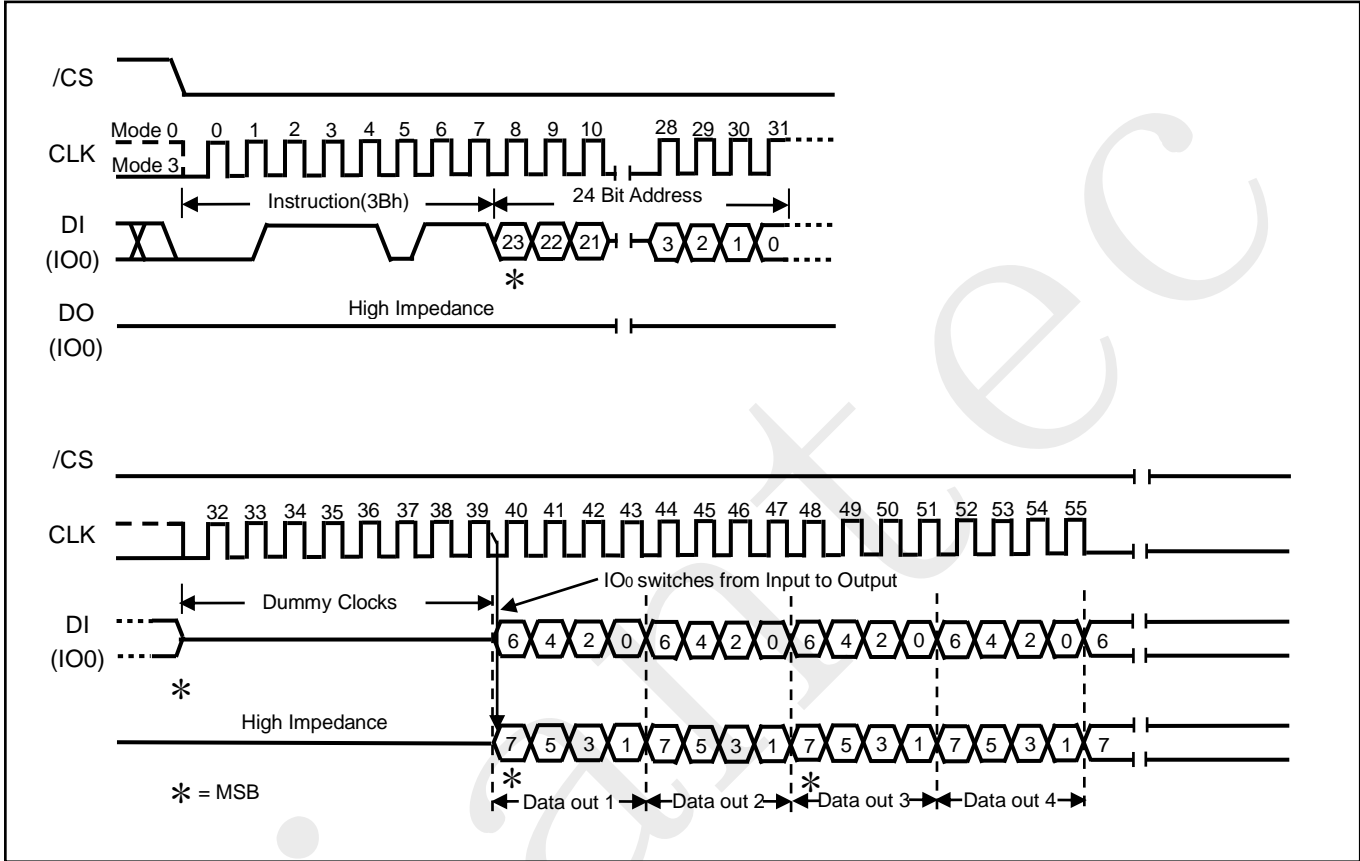


Figure8. Dual Output Fast Read Sequence Diagram



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9.11 Quad Output Fast Read (6Bh)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad Output Fast Read command.

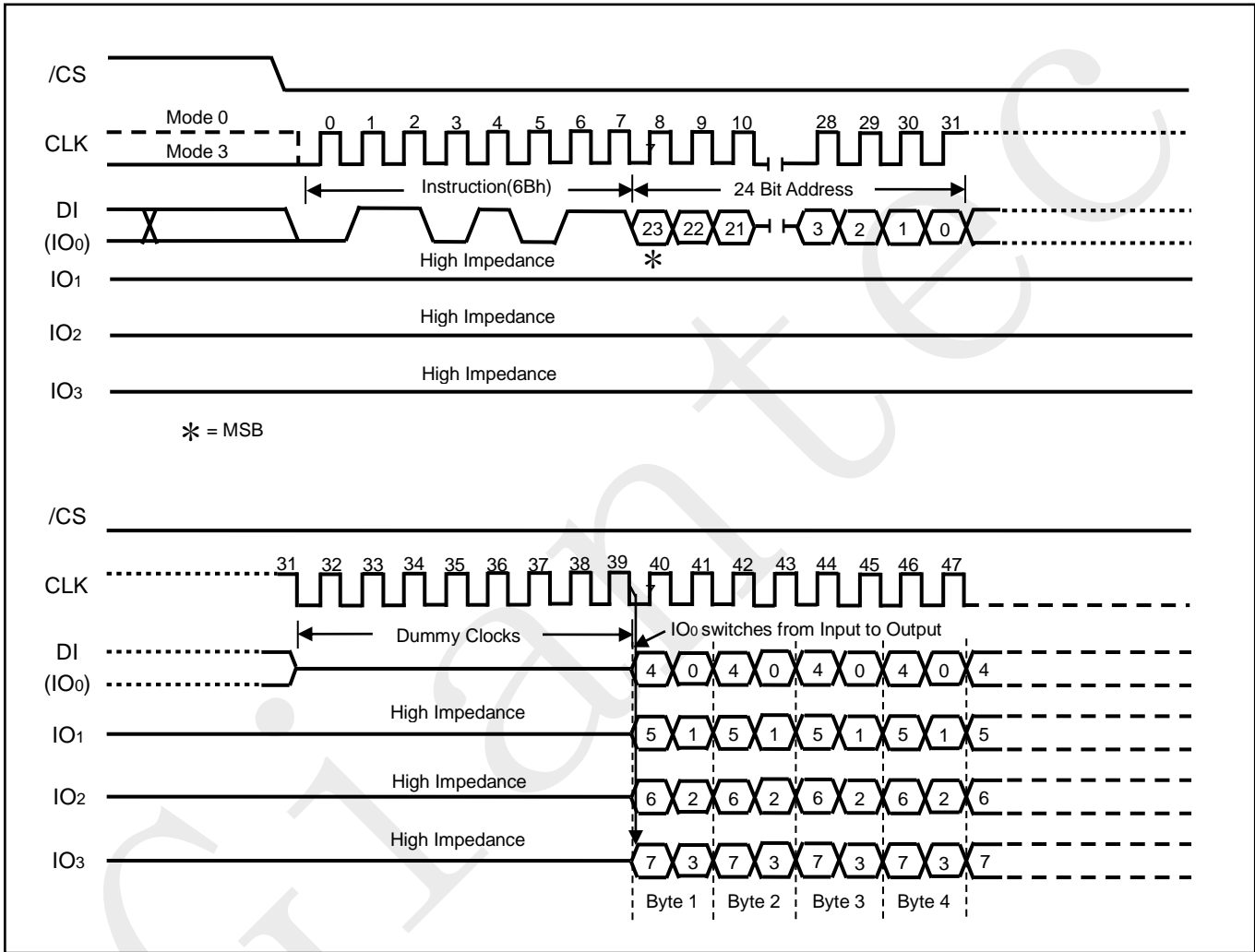


Figure9. Quad Output Fast Read Sequence Diagram



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9.12 Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3- byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by DI and DO, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 2-bit per clock cycle from DI and DO. The command sequence is shown in followed Figure10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure10. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

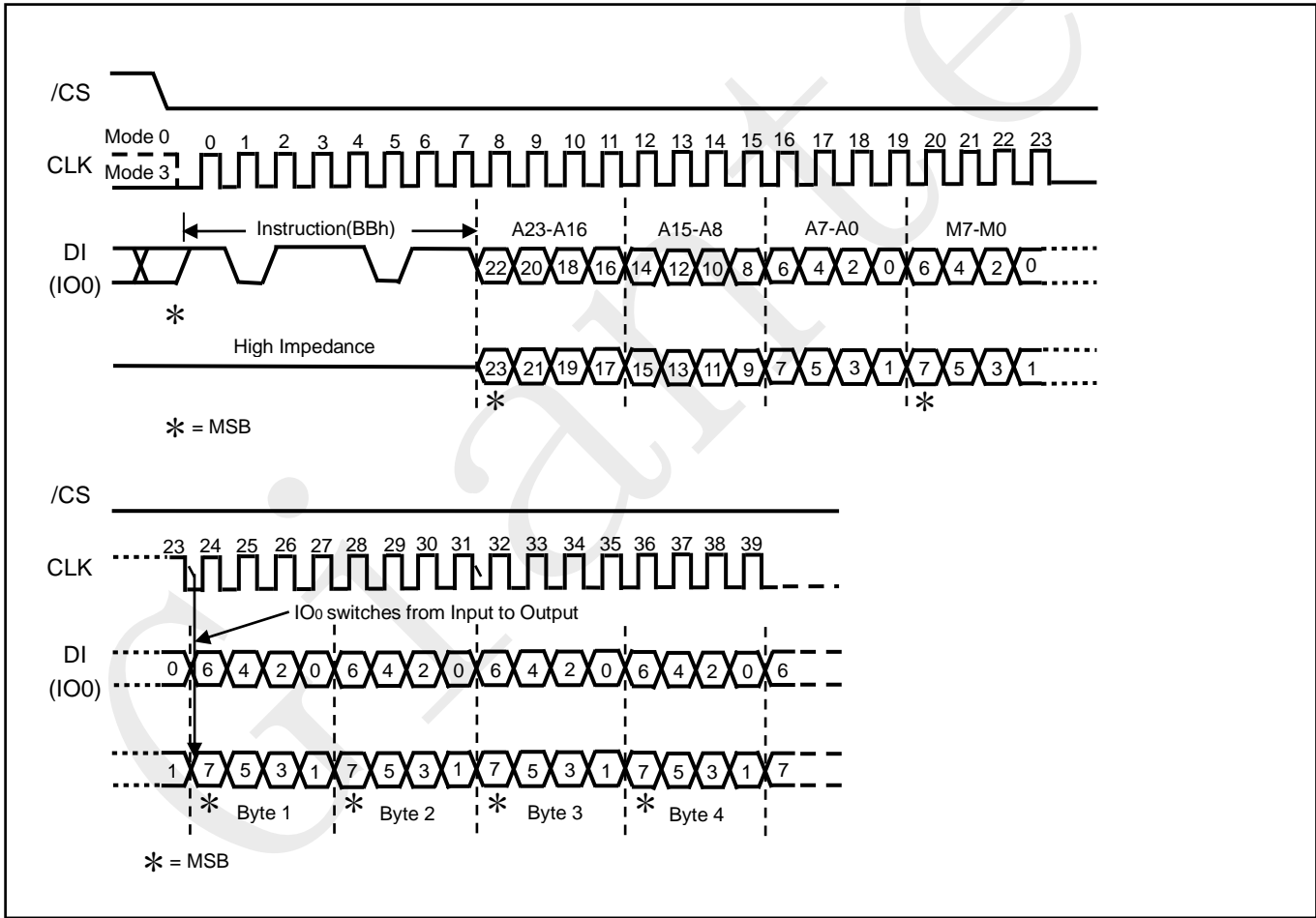


Figure10. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))



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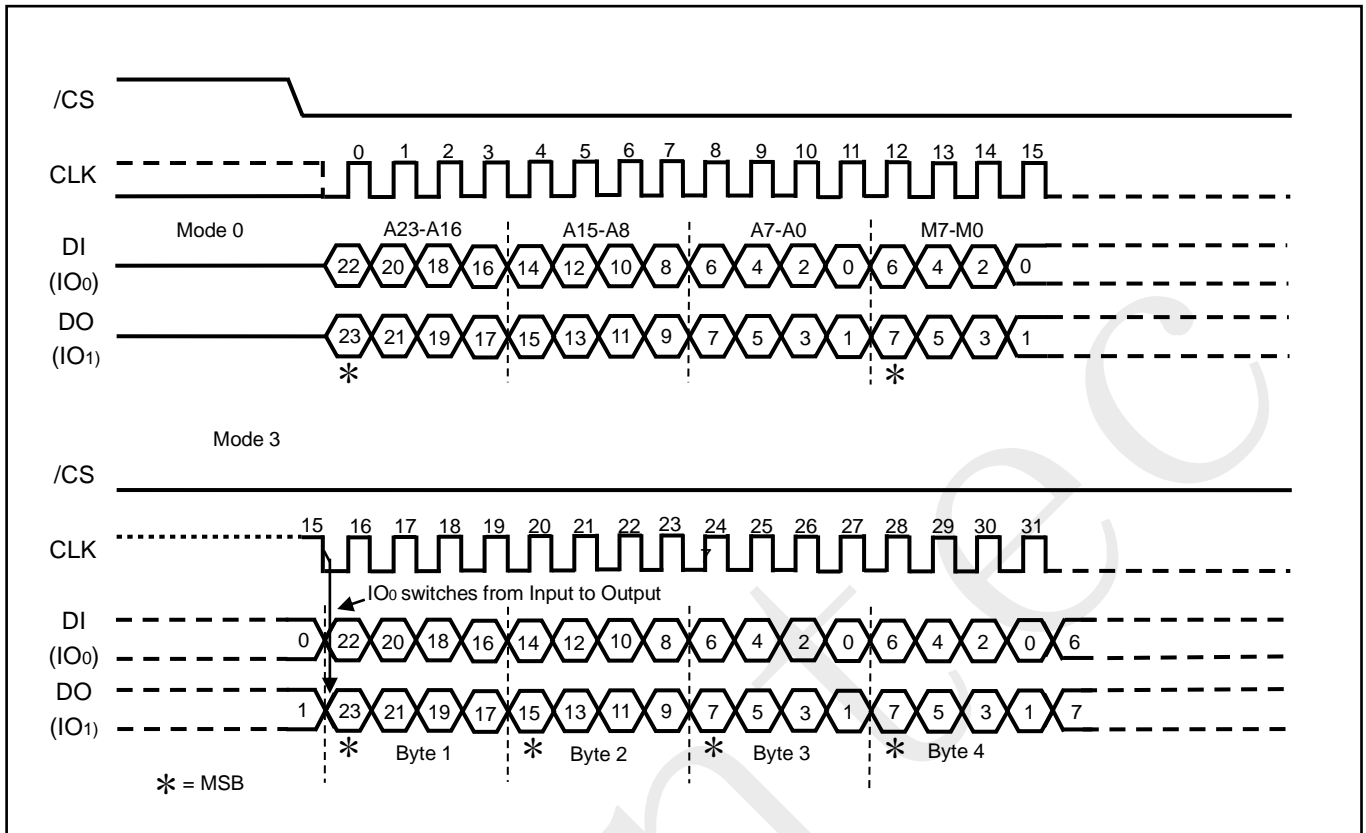


Figure10a. Dual/O Fast Read Sequence Diagram (M5-4= (1, 0))



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9.13 Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure11. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure11a. If the “Continuous Read Mode” bits (M5-4) do not equal to (1, 0), the next command requires the command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

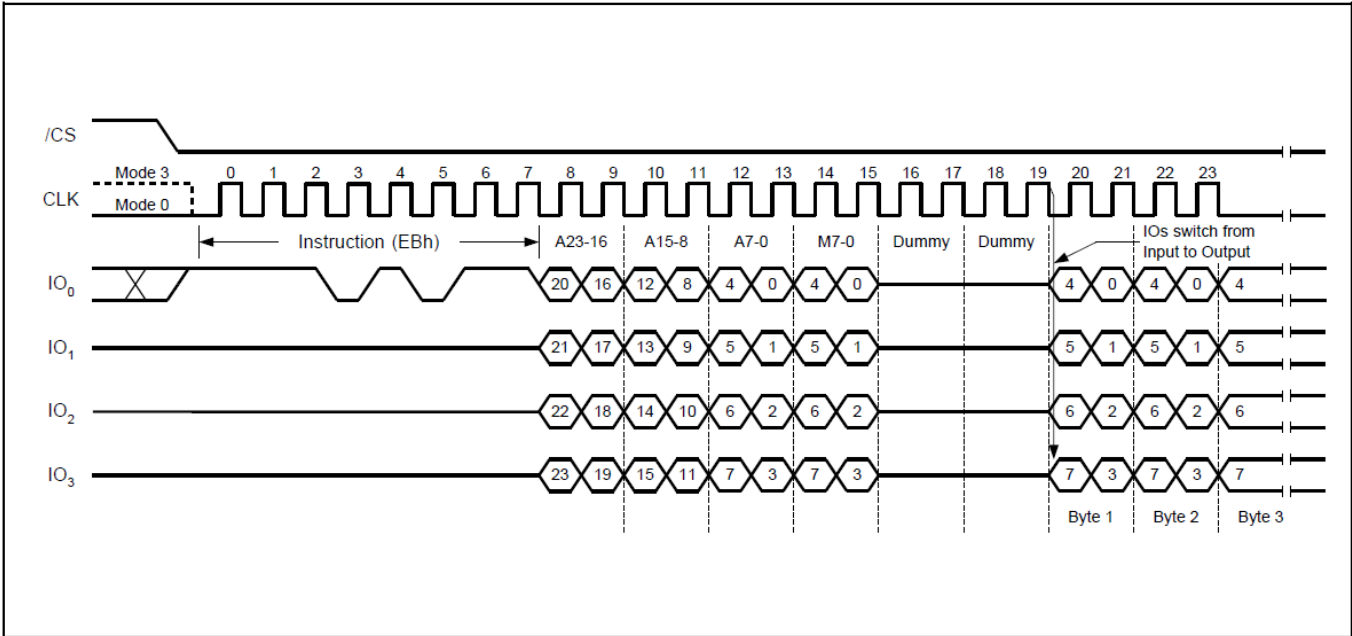


Figure11. Quad I/O Fast Read Sequence Diagram (M5-4≠(1, 0))



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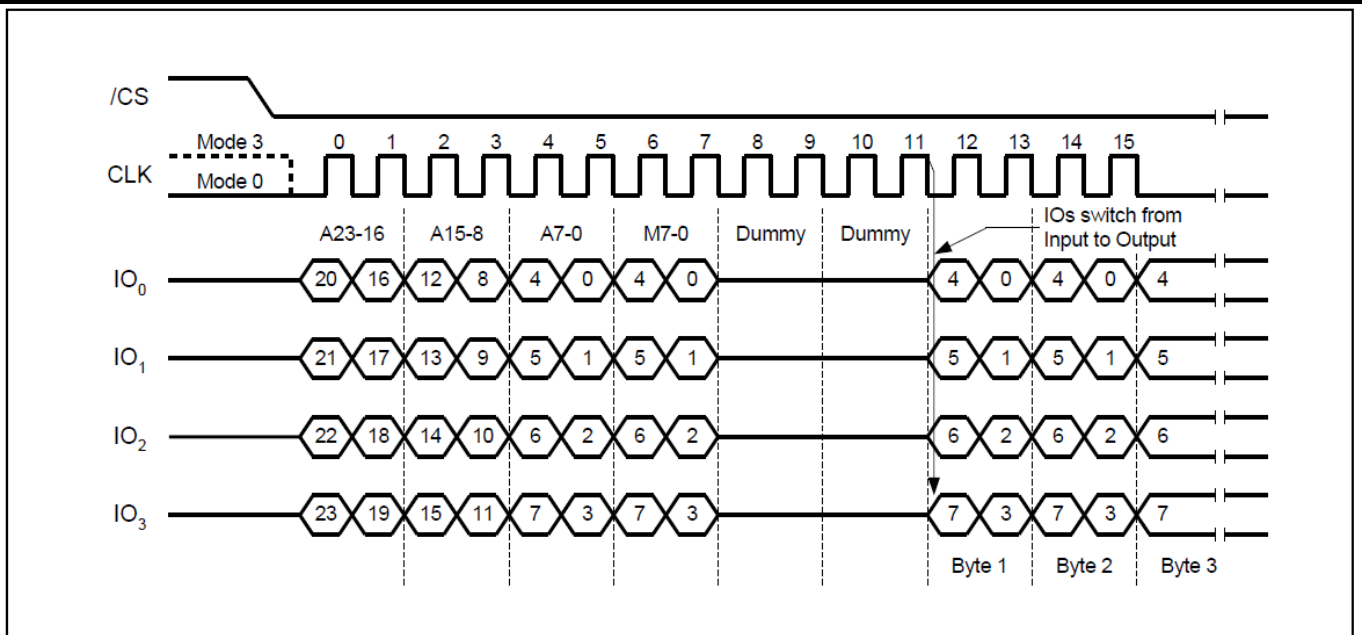


Figure 11a. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0))

Quad I/O Fast Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap” (77H) commands prior to EBH. The “Set Burst with Wrap” (77H) command can either enable or disable the “Wrap Around” feature for the following EBH commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The “Set Burst with Wrap” command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.



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9.14 Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with “Quad I/O Fast Read” command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits “Wrap bits” → CS# goes high.

| W6,W5 | W4=0 | | W4=1 (Default) | |
|-------|-------------|-------------|----------------|-------------|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0, 0 | Yes | 8-byte | No | N/A |
| 0, 1 | Yes | 16-byte | No | N/A |
| 1, 0 | Yes | 32-byte | No | N/A |
| 1, 1 | Yes | 64-byte | No | N/A |

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following “Quad I/O Fast Read” command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

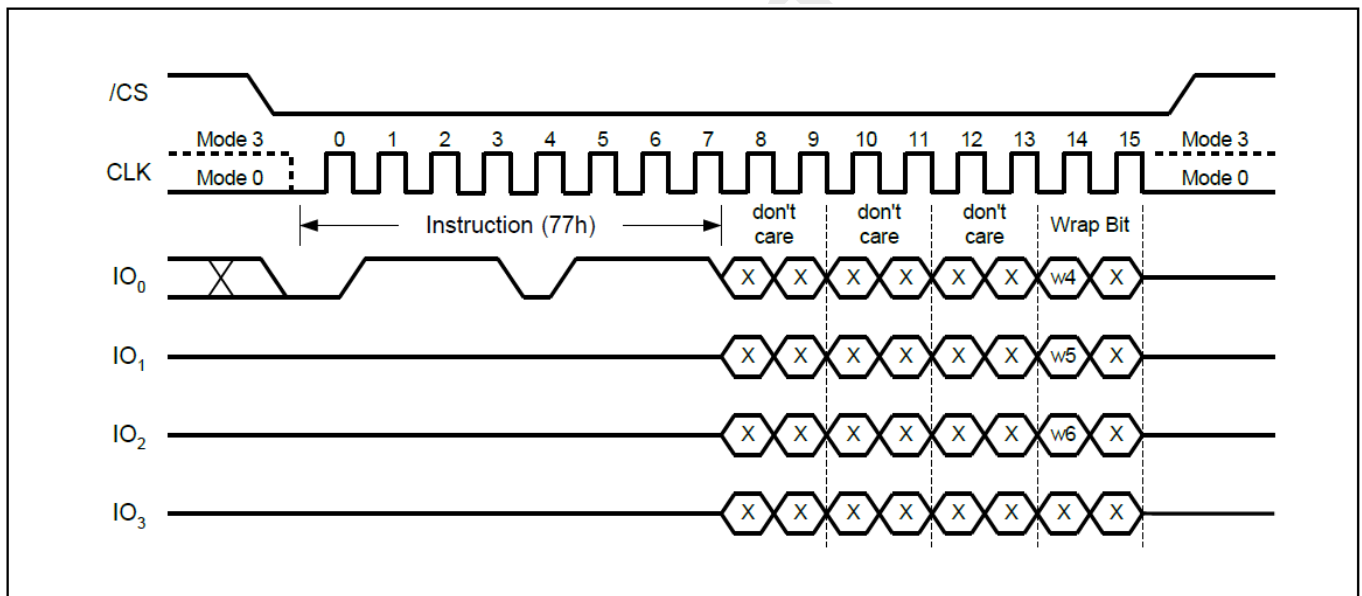


Figure12 Set Burst with Wrap Sequence Diagram



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9.15 Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on DI → at least 1 byte data on DI → CS# goes high. The command sequence is shown in Figure13. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) is not executed.

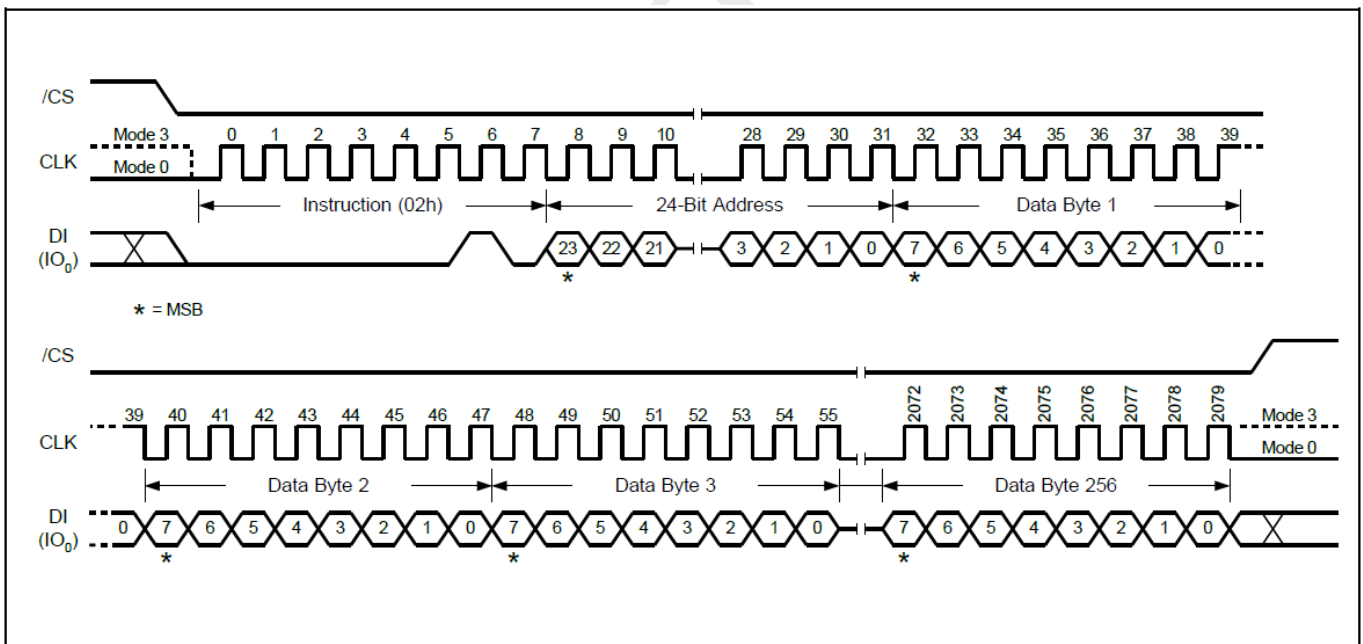


Figure13 Page Program Sequence Diagram



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9.16 Quad Page Program (32H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure14 If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) is not executed.

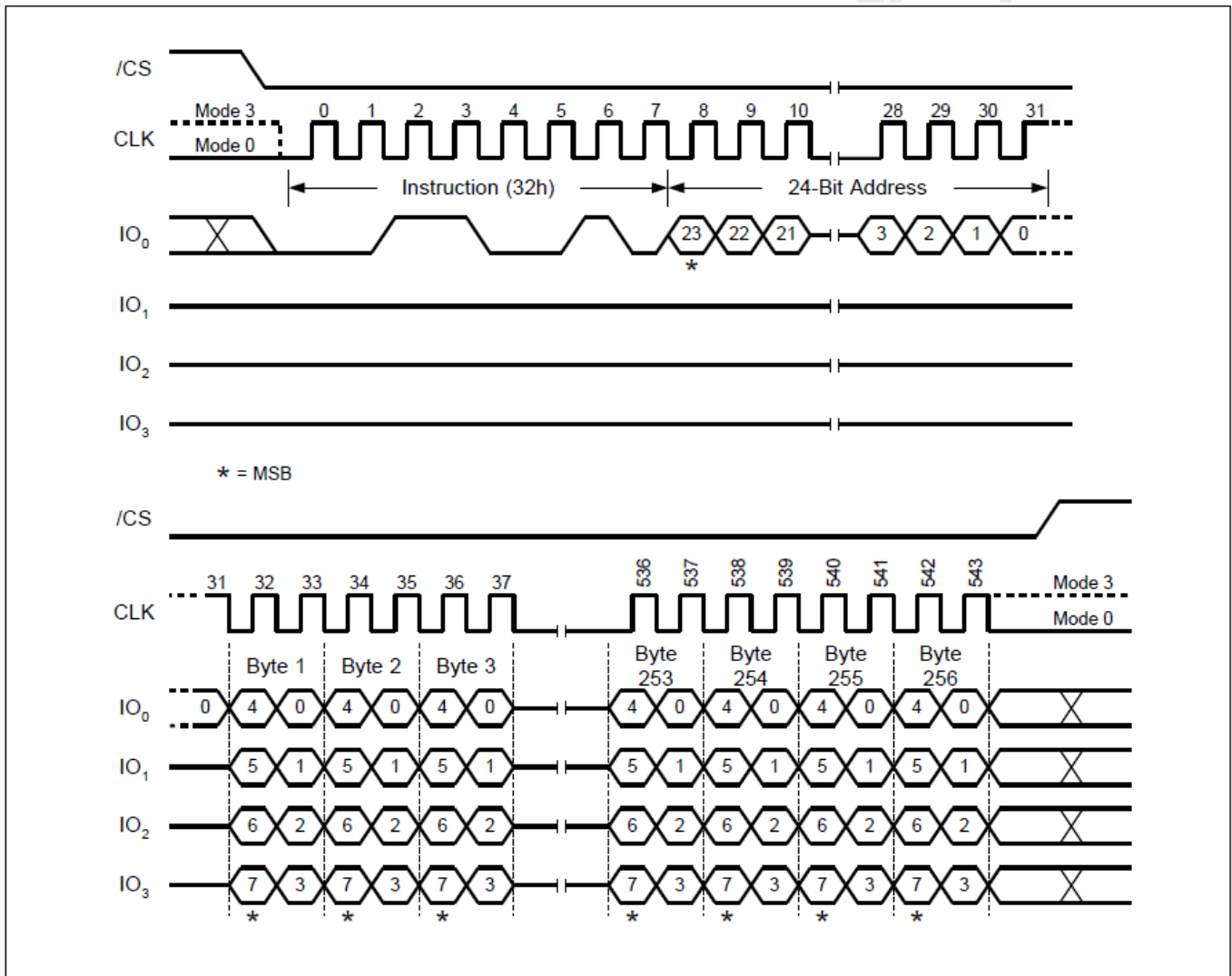


Figure14 Quad Page Program Sequence Diagram



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9.17 Mini Sector Erase (MSE) (82H)

The Mini Sector Erase (MSE) (82H) command is for erasing the all data of the chosen 1KB sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Mini Sector Erase (MSE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Mini Sector Erase (MSE) command. CS# must be driven low for the entire duration of the sequence.

The Mini Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on DI → CS# goes high. The command sequence is shown in Figure15. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Mini Sector Erase (MSE) command is not executed. As soon as CS# is driven high, the self-timed Mini Sector Erase cycle (whose duration is t_{MSE}) is initiated. While the Mini Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Mini Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Mini Sector Erase (MSE) command applied to a sector which is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bit (see Table 1-6) is not executed.

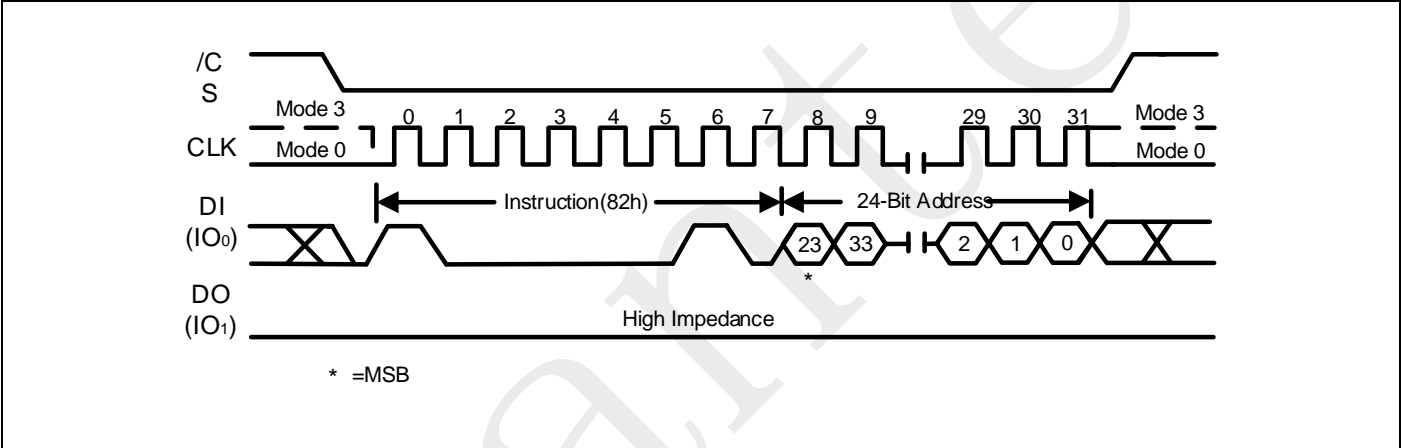


Figure15. Mini Sector Erase Sequence Diagram



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9.18 Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen 4KB sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on DI → CS# goes high. The command sequence is shown in Figure15. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bit (see Table 1-6) is not executed.

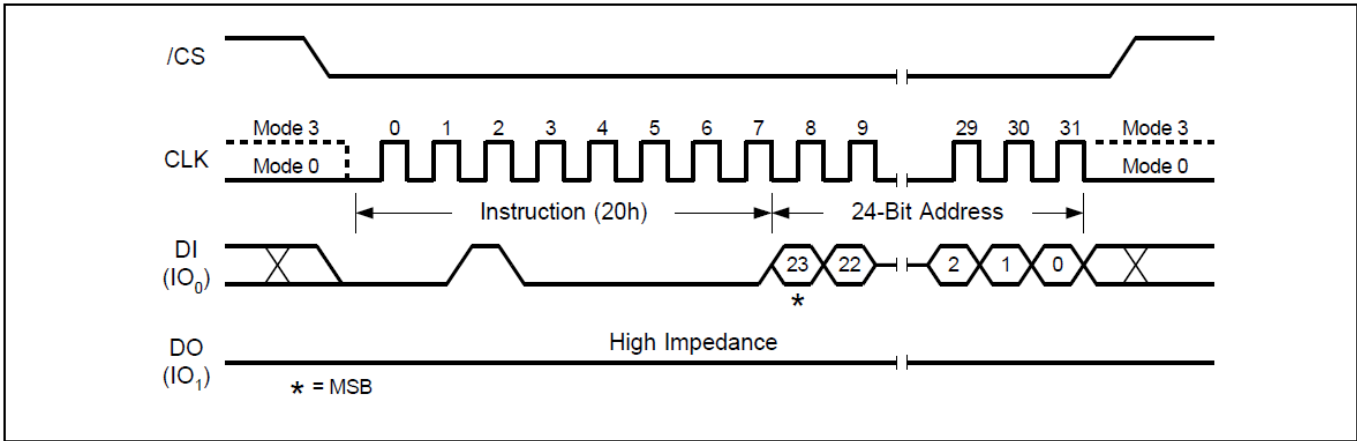


Figure16. Sector Erase Sequence Diagram



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9.19 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on DI → CS# goes high. The command sequence is shown in Figure16. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tSE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Table 1-6) is not executed.

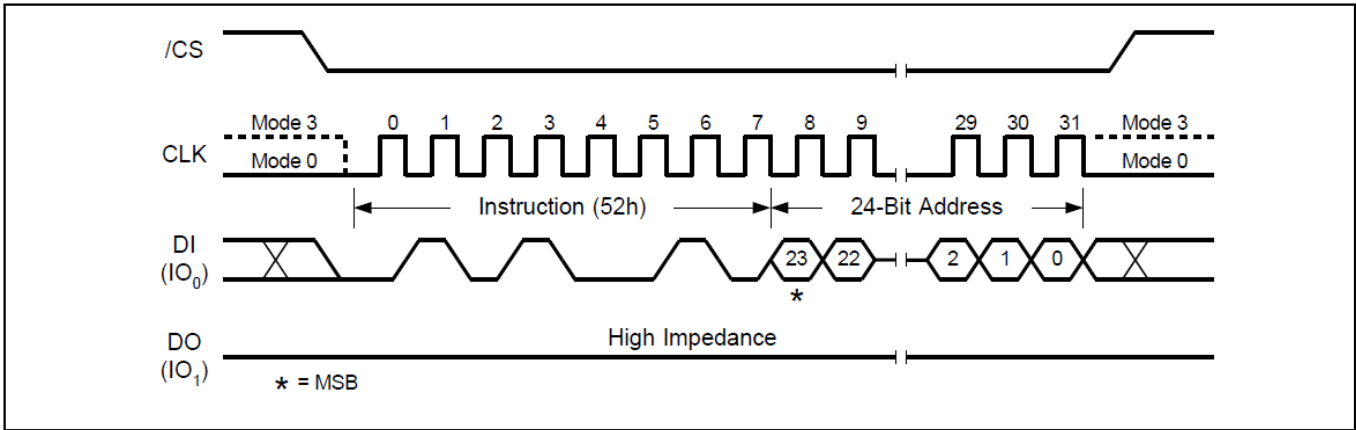


Figure17. 32KB Block Erase Sequence Diagram



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9.20 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on DI → CS# goes high. The command sequence is shown in Figure 17. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tSE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Table 1-2) is not executed.

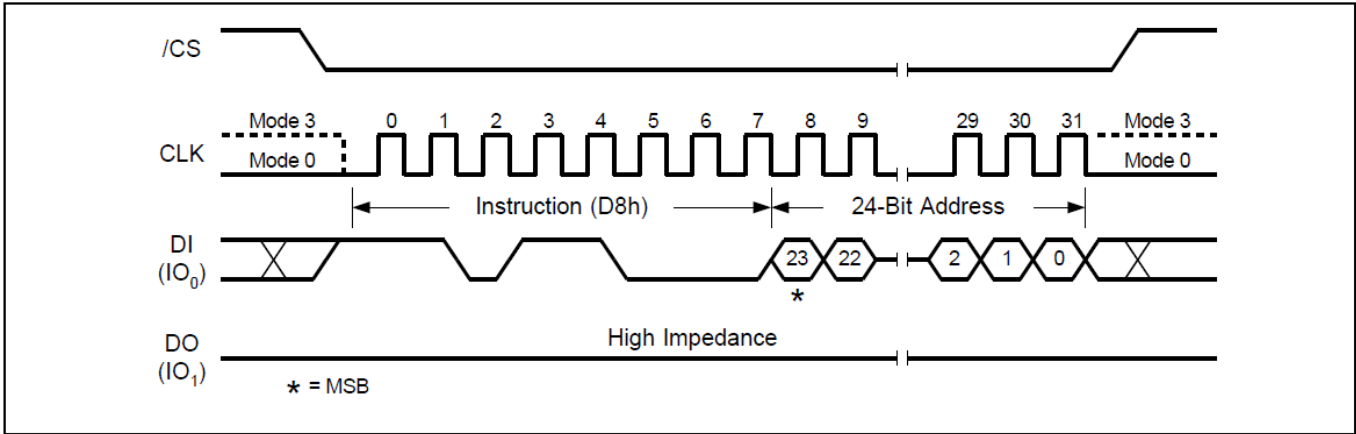


Figure18. 64KB Block Erase Sequence Diagram



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9.21 Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure18. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (BUSY) bit. The Write in Progress (BUSY) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1.

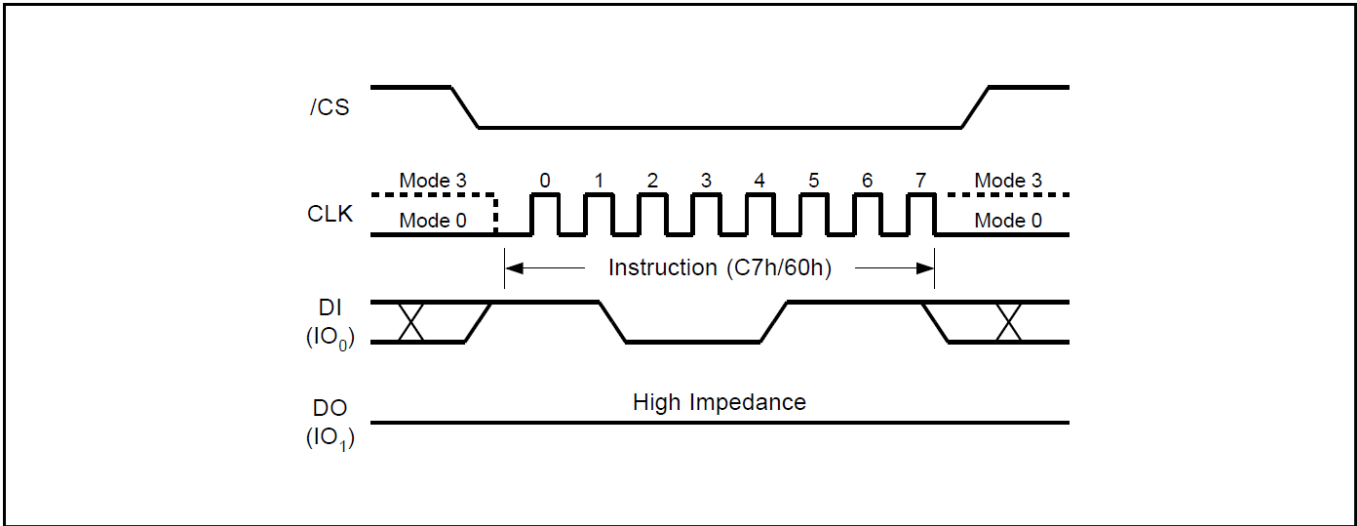


Figure19. Chip Erase Sequence Diagram



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9.22 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on DO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power-Up. The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure19. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

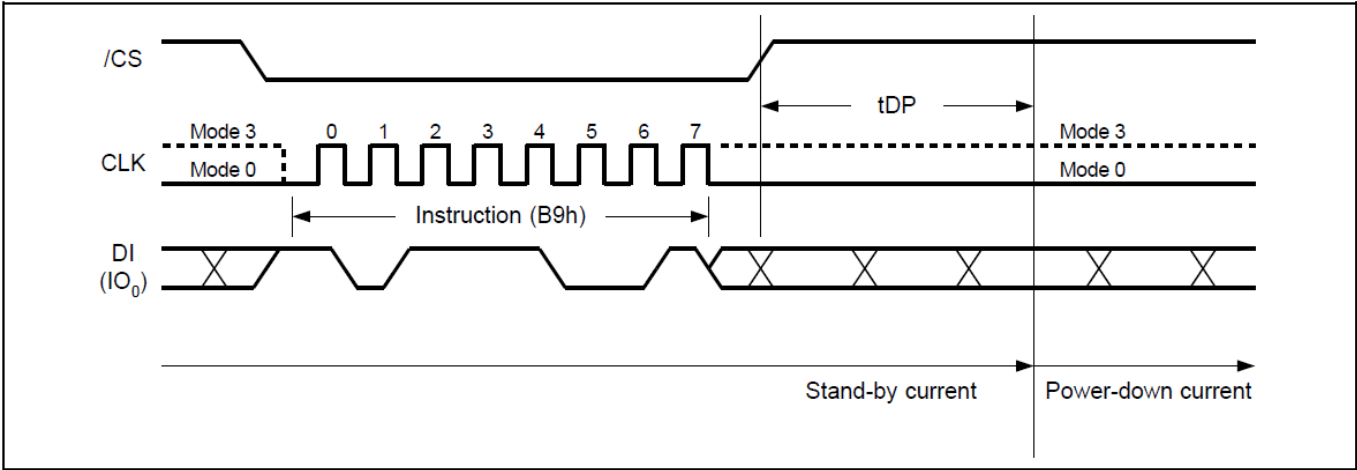


Figure20. Deep Power-Down Sequence Diagram



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9.23 Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure20. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure21. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure21, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when BUSY equal 1) the command is ignored and will not have any effects on the current cycle.

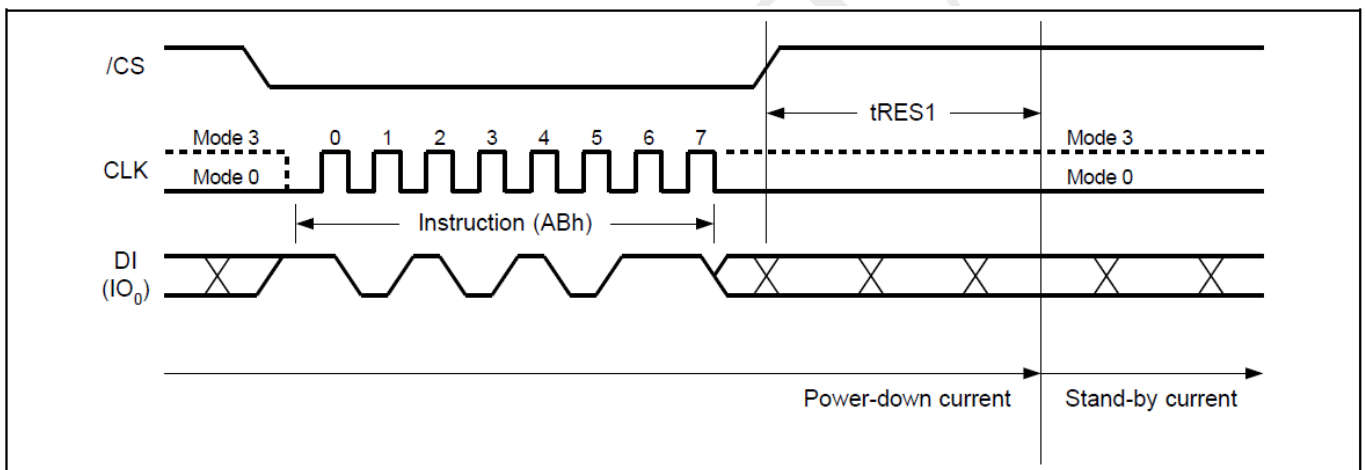


Figure21. Release Power-Down Sequence Diagram

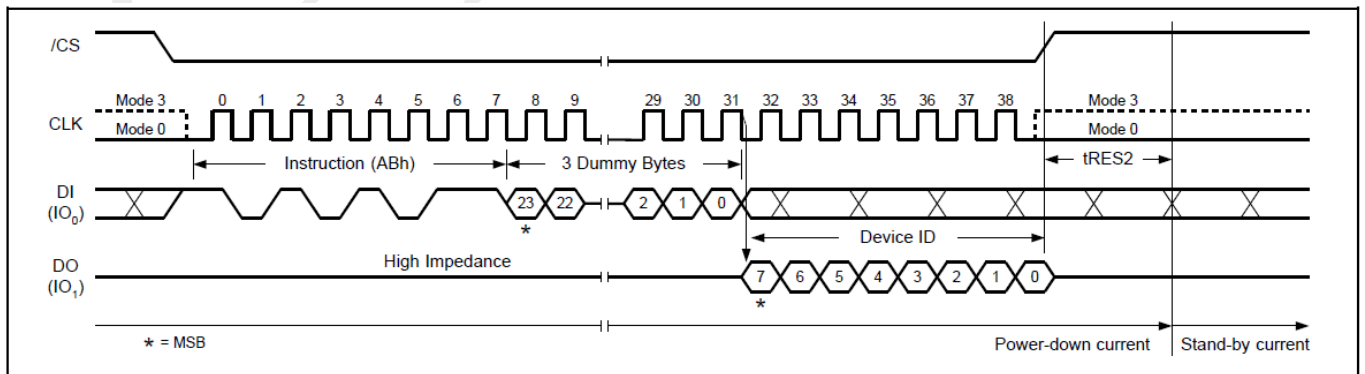


Figure22. Release Power-Down/Read Device ID Sequence Diagram



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9.24 Read Manufacture Id/ Device Id (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure22. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

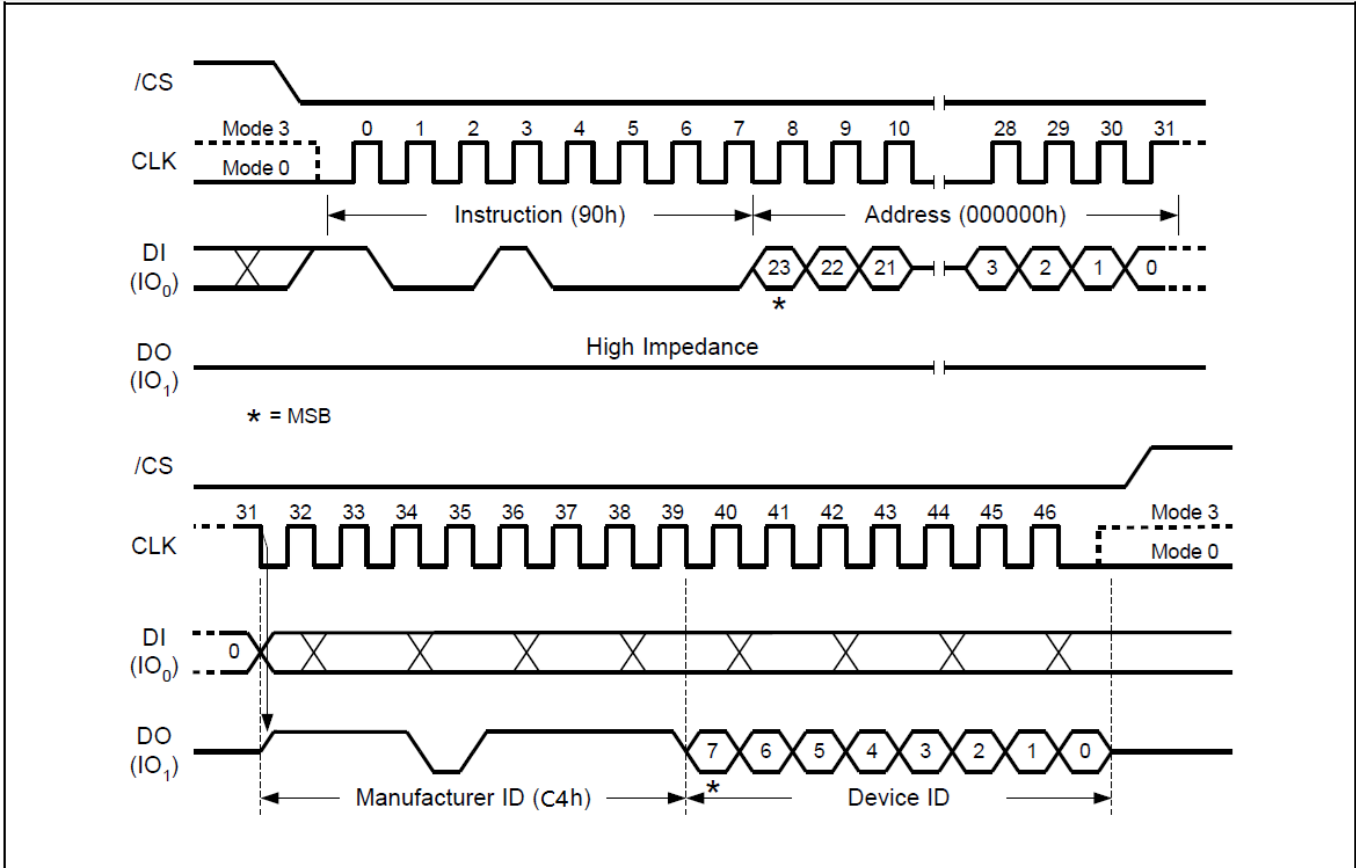


Figure23 Read Manufacture ID/ Device ID Sequence Diagram



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9.25 Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code “92H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure23. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

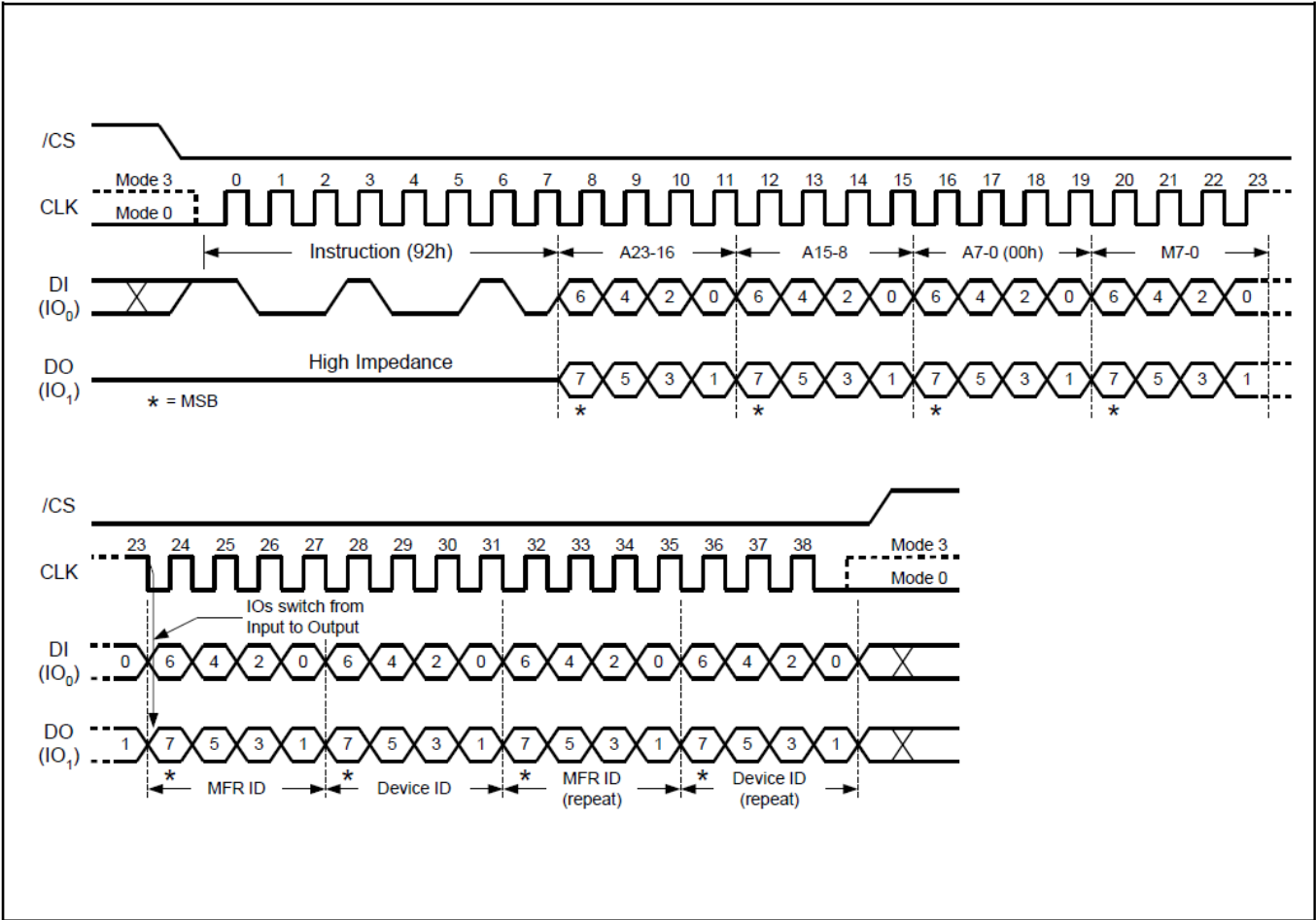


Figure24. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram



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9.26 Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the CS# pin low and shifting the command code “94H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure24. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

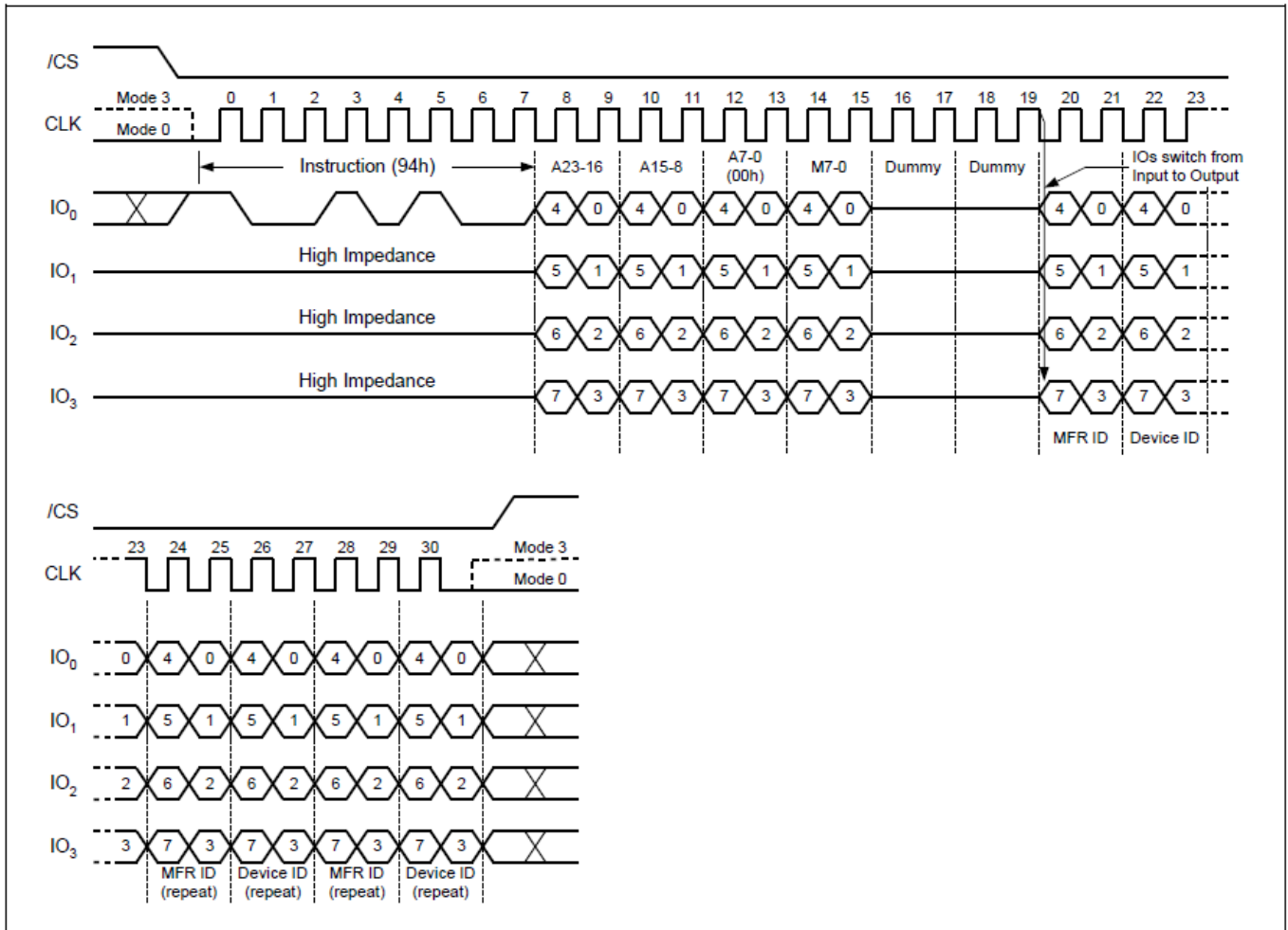


Figure25. Read Manufacture ID/ Device ID Quad I/O Sequence Diagram



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9.27 Read Identification (RDID) (9Fh)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The command sequence is shown in Figure 25. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

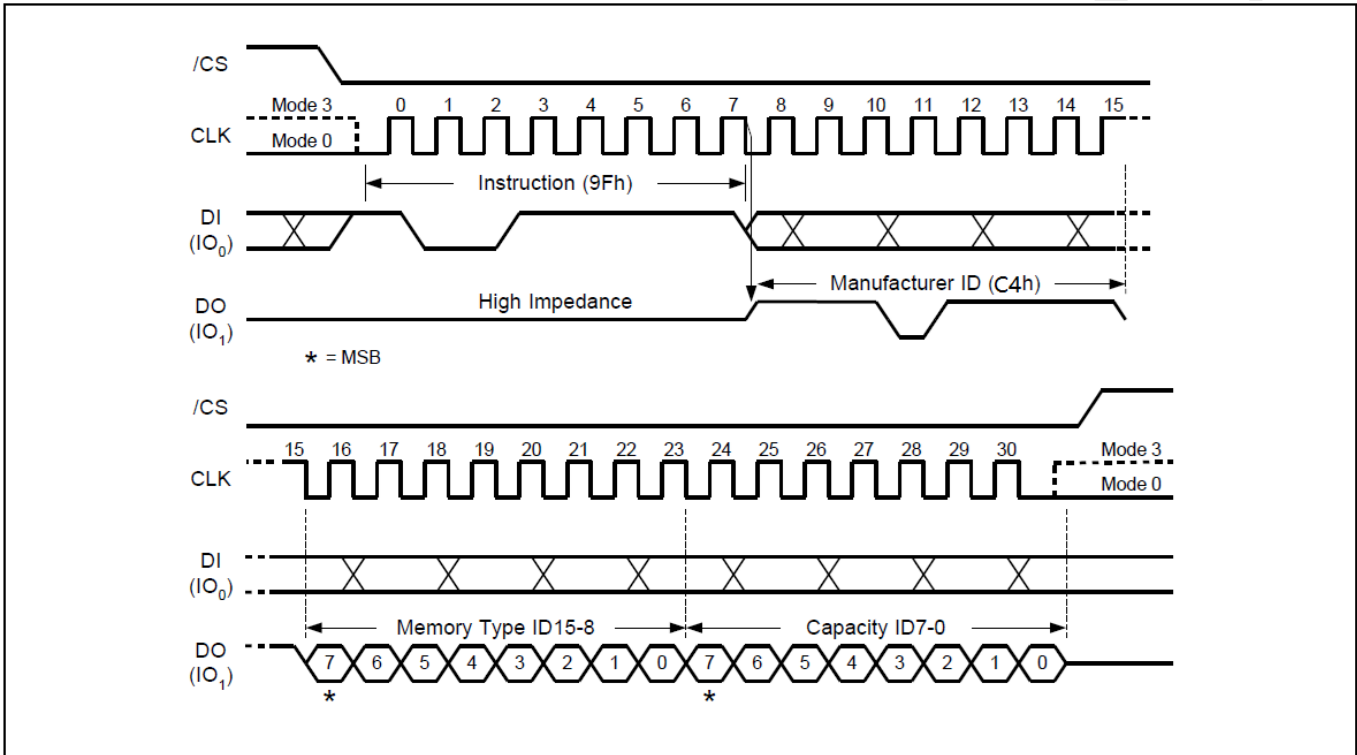


Figure26.Read Identification ID Sequence Diagram



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9.28 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each GT25Q40/20/10/05C device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in figure 26.

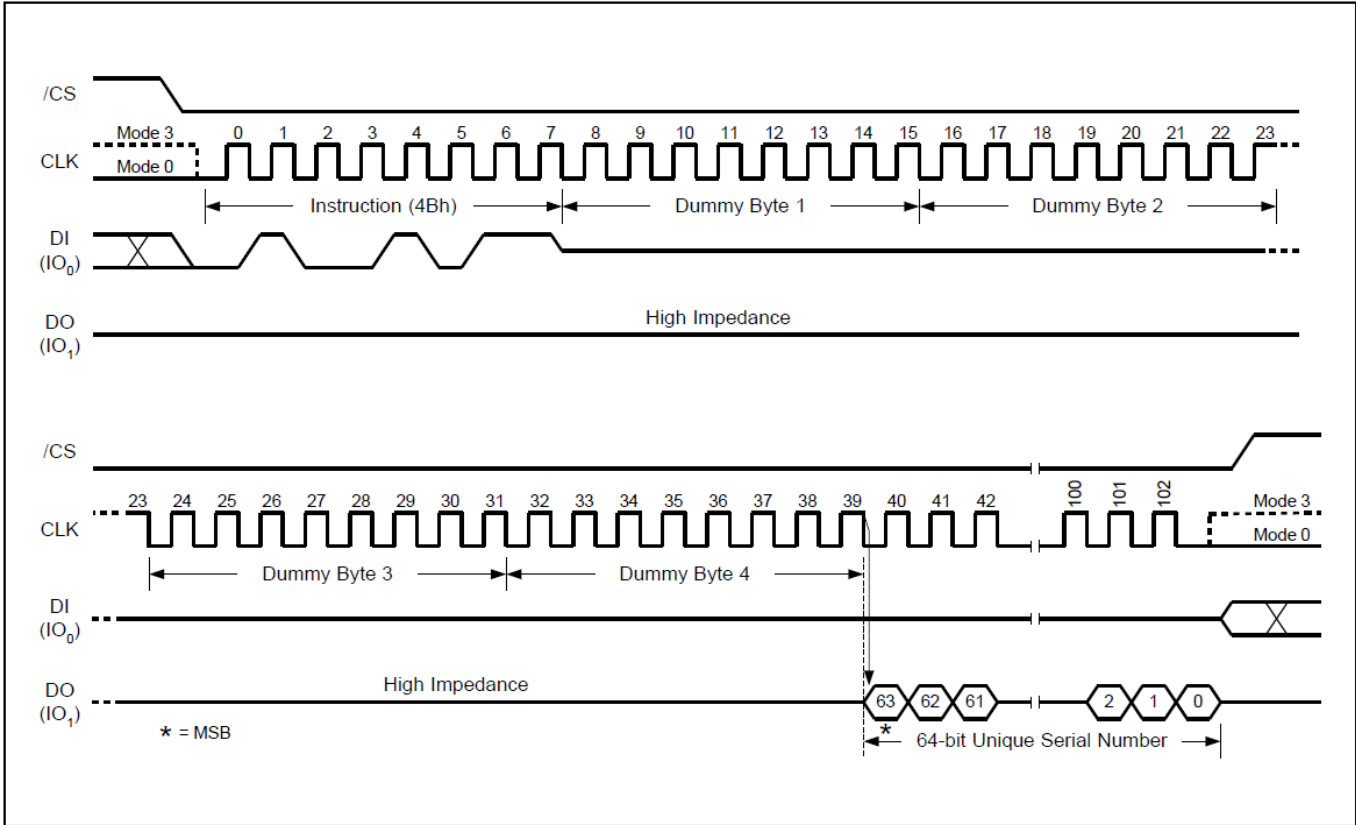


Figure27. Read Unique ID Number Instruction Sequence



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9.29 Program/Erase Suspend (PES) (75H or B0H)

The Erase/Program Suspend instruction “75H or B0H”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure27.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75H or B0H” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75H or B0H” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7AH or 30H”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

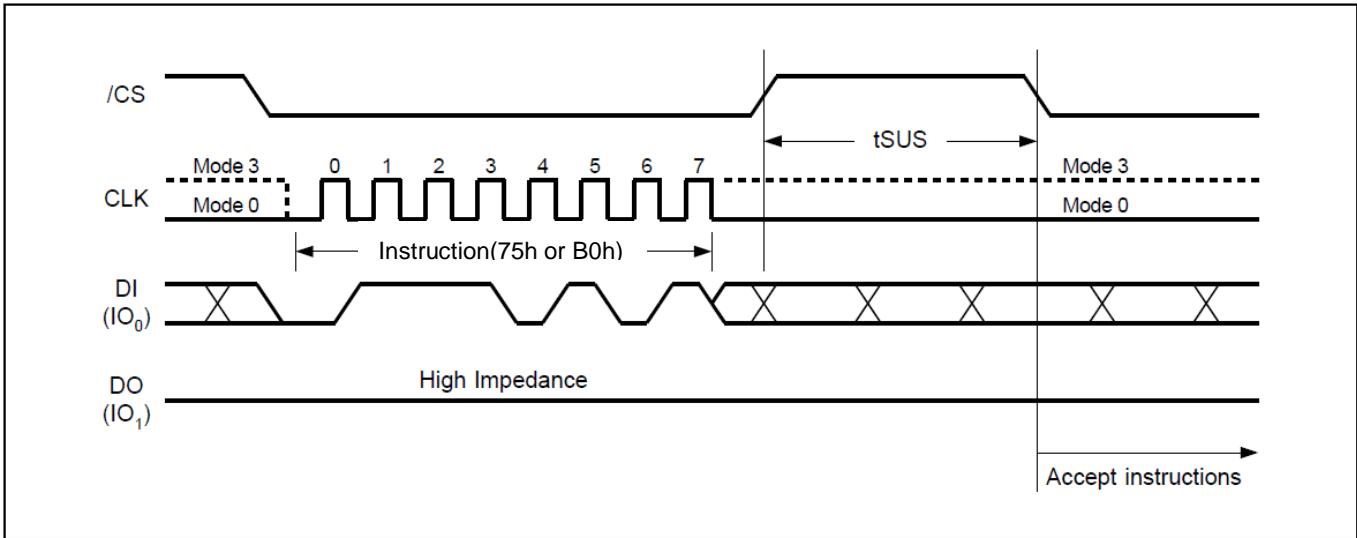


Figure28. Program/Erase Suspend Sequence Diagram



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9.30 Program/Erase Resume (PER) (7AH or 30H)

The Erase/Program Resume instruction “7AH or 30H” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7AH or 30H” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7AH or 30H” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure28.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of “tSUS” following a previous Resume instruction.

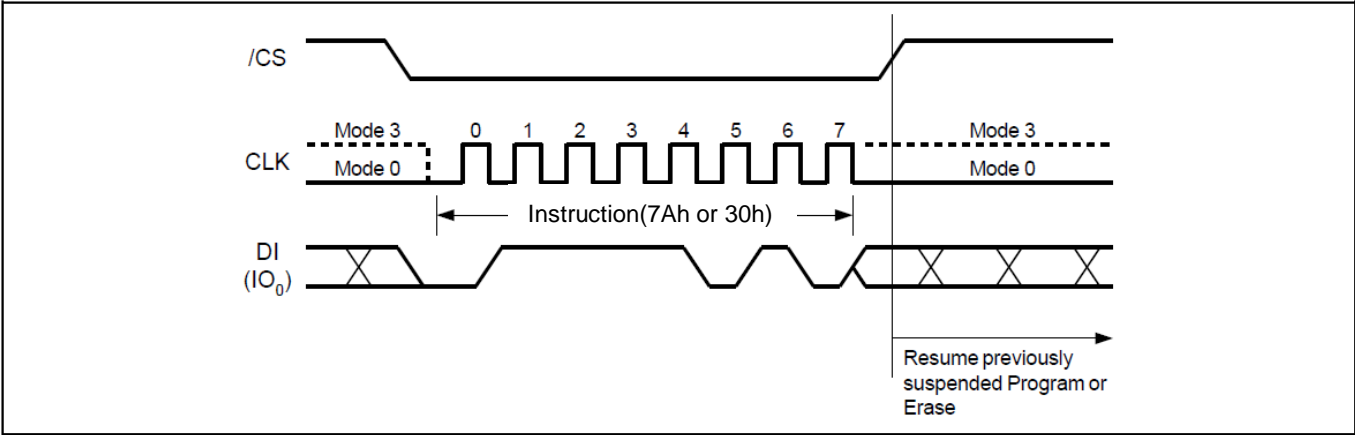


Figure29. Program/Erase Resume Sequence Diagram



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9.31 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in either SPI mode. The “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST/tRST_E to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

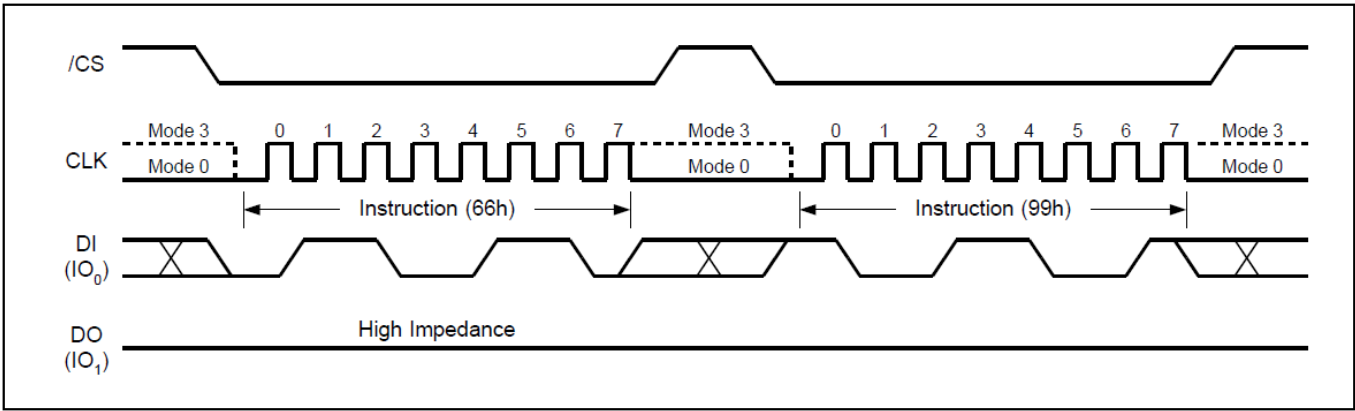


Figure30. Enable Reset and Reset Instruction Sequence



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9.32 Read SFDP Register (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

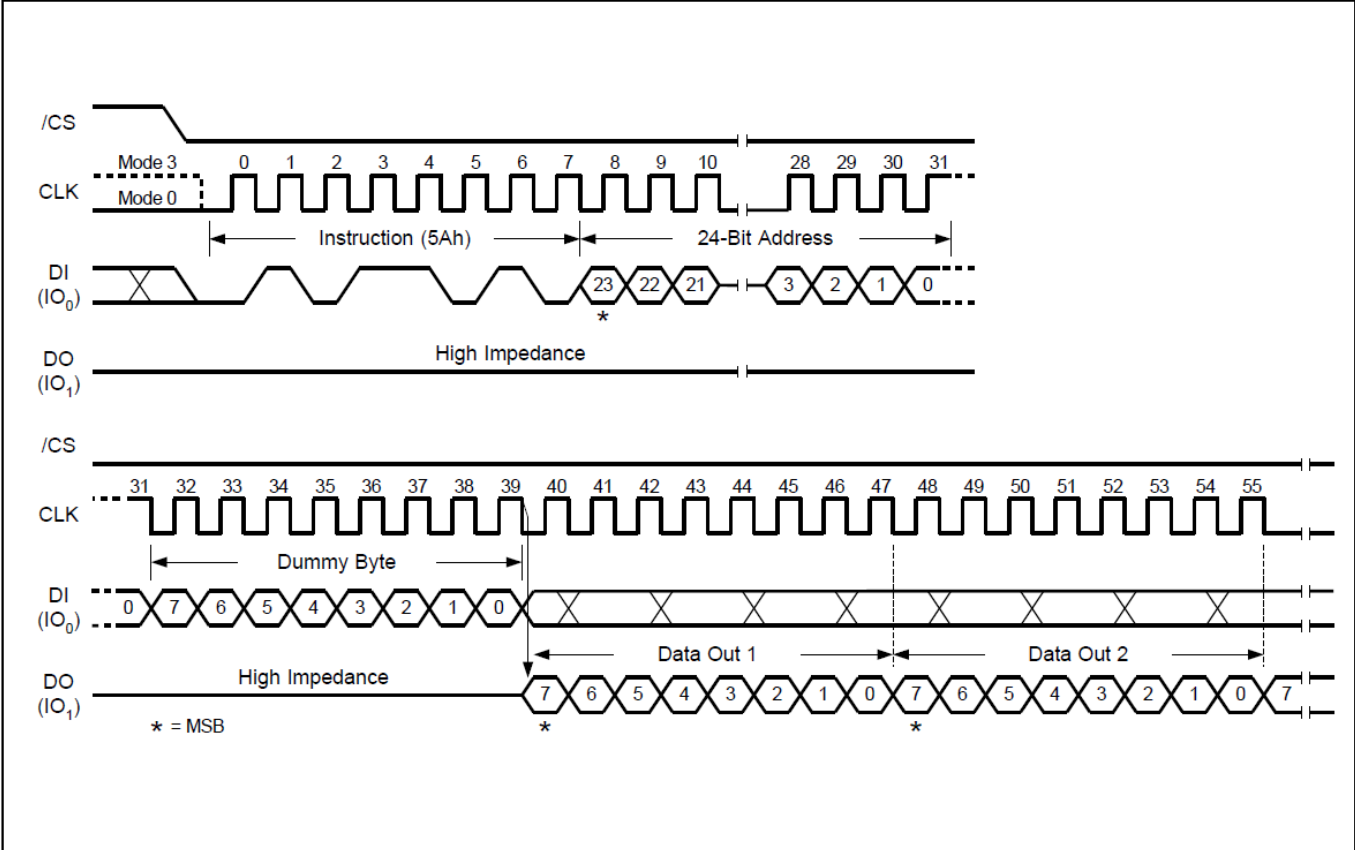


Figure 30. Read SFDP Register Instruction Sequence Diagram(SPI mode only)



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Signature and Parameter Identification Data Values

| Description | Comment | Byte Add(H) | Bit Add | Data | Data |
|---|--|-------------|---------|------|------|
| SFDP Signature | Fixed:50444653H | 00H | 07:00 | 53H | 53H |
| | | 01H | 15:08 | 46H | 46H |
| | | 02H | 23:16 | 44H | 44H |
| | | 02H | 31:24 | 50H | 50H |
| SFDP Minor Revision Number | Start from 00H | 04H | 07:00 | 00H | 00H |
| SFDP Major Revision Number | Start from 01H | 05H | 15:08 | 01H | 01H |
| Number of Parameters Headers | Start from 00H | 06H | 23:16 | 01H | 01H |
| Unused | Contains 0xFFH and can never be changed | 07H | 31:24 | FFH | FFH |
| ID number (JEDEC) | 00H: It indicates a JEDEC specified header | 08H | 07:00 | 00H | 00H |
| Parameter Table Minor Revision Number | Start from 0x00H | 09H | 15:08 | 00H | 00H |
| Parameter Table Major Revision Number | Start from 0x01H | 0AH | 23:16 | 01H | 01H |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 0BH | 31:24 | 09H | 09H |
| Parameter Table Pointer (PTP) | First address of JEDEC Flash Parameter table | 0CH | 07:00 | 30H | 30H |
| | | 0DH | 15:08 | 00H | 00H |
| | | 0EH | 23:16 | 00H | 00H |
| Unused | Contains 0xFFH and can never be changed | 0FH | 31:24 | FFH | FFH |
| ID Number LSB (Giantec Manufacturer ID) | It is indicates Giantec manufacturer ID | 10H | 07:00 | C4H | C4H |
| Parameter Table Minor Revision Number | Start from 0x00H | 11H | 15:08 | 00H | 00H |
| Parameter Table Major Revision Number | Start from 0x01H | 12H | 23:16 | 01H | 01H |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 13H | 31:24 | 03H | 03H |
| Parameter Table Pointer (PTP) | First address of Giantec Flash Parameter table | 14H | 07:00 | 60H | 60H |
| | | 15H | 15:08 | 00H | 00H |
| | | 16H | 23:16 | 00H | 00H |
| Unused | Contains 0xFFH and can never be changed | 17H | 31:24 | FFH | FFH |



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| Description | Comment | Byte Add(H) | Bit Add | Data | Data |
|---|---|-------------|---------|-----------------|------|
| Unuse | . | . | . | FFH | FFH |
| Block/Sector Erase Size | 00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase | 30H | 01:00 | 01b | E5H |
| Write Granularity | 0: 1Byte, 1: 64Byte or larger | | 02 | 1b | |
| Write Enable Instruction Requested for Writing to Volatile Status Registers | 0: Nonvolatile status bit 1: Volatile status bit (BP status register bit) | | 03 | 0b | |
| Write Enable Opcode Select for Writing to Volatile Status Registers | 0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b. | | 04 | 0b | |
| Unused | Contains 111b and can never be changed | | 07:05 | 111b | |
| 4KB Erase Opcode | | 31H | 15:08 | 20H | 20H |
| (1-1-2) Fast Read | 0=Not support, 1=Support | 32H | 16 | 1b | F1H |
| Address Bytes Number used in addressing flash array | 00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved | | 18:17 | 00b | |
| Double Transfer Rate (DTR) clocking | 0=Not support, 1=Support | | 19 | 0b | |
| (1-2-2) Fast Read | 0=Not support, 1=Support | | 20 | 1b | |
| (1-4-4) Fast Read | 0=Not support, 1=Support | | 21 | 1b | |
| (1-1-4) Fast Read | 0=Not support, 1=Support | | 22 | 1b | |
| Unused | | | 23 | 1b | |
| Unused | | 33H | 31:24 | FFH | FFH |
| Flash Memory Density | | 37H:34H | 31:00 | 007FFFFFFH(8Mb) | |
| (1-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 38H | 04:00 | 00100b | 44H |
| (1-4-4) Fast Read Number of Mode Bits | 000b:Mode Bits not support | | 07:05 | 010b | |
| (1-4-4) Fast Read Opcode | | 39H | 15:08 | EBH | EBH |



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| Description | Comment | Byte Add(H) | Bit Add | Data | Data |
|---|---|-------------|---------|--------|-------|
| (1-1-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3AH | 20:16 | 01000b | 08H |
| (1-1-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (1-1-4) Fast Read Opcode | | 3BH | 31:24 | 6BH | 6BH |
| (1-1-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3CH | 04:00 | 01000b | 08H |
| (1-1-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 07:05 | 000b | |
| (1-1-2) Fast Read Opcode | | 3DH | 15:08 | 3BH | 3BH |
| (1-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3EH | 20:16 | 00010b | 42H |
| (1-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 010b | |
| (1-2-2) Fast Read Opcode | | 3FH | 31:24 | BBH | BBH |
| (2-2-2) Fast Read | 0=not support 1=support | 40H | 00 | 0b | EEH |
| Unused | | | 03:01 | 111b | |
| (4-4-4) Fast Read | 0=not support 1=support | | 04 | 0b | |
| Unused | | | 07:05 | 111b | |
| Unused | | 43H:41H | 31:08 | 0xFFH | 0xFFH |
| Unused | | 45H:44H | 15:00 | 0xFFH | 0xFFH |
| (2-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 46H | 20:16 | 00000b | 00H |
| (2-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (2-2-2) Fast Read Opcode | | 47H | 31:24 | FFH | FFH |
| Unused | | 49H:48H | 15:00 | 0xFFH | 0xFFH |
| (4-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 4AH | 20:16 | 00000b | 00H |
| (4-4-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (4-4-4) Fast Read Opcode | | 4BH | 31:24 | FFH | FFH |
| Sector Type 1 Size | Sector/block size=2^N bytes 0x00b: this sector type don't exist | 4CH | 07:00 | 0CH | 0CH |
| Sector Type 1 erase Opcode | | 4DH | 15:08 | 20H | 20H |
| Sector Type 2 Size | Sector/block size=2^N bytes 0x00b: this sector type don't exist | 4EH | 23:16 | 0FH | 0FH |



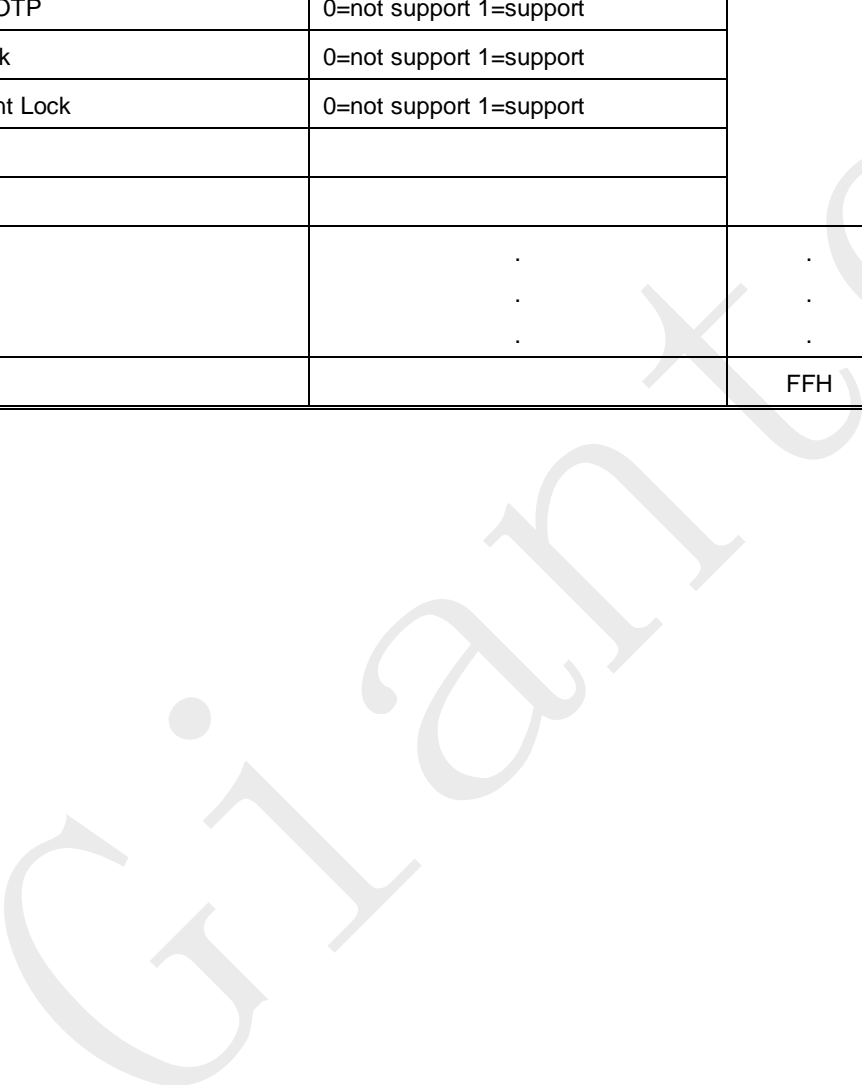
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| Description | Comment | Byte Add(H) | Bit Add | Data | Data |
|------------------------------|---|-------------|---------|-------|-------|
| Sector Type 2 erase Opcode | | 4FH | 31:24 | 52H | 52H |
| Sector Type 3 Size | Sector/block size=2^N bytes 0x00b: this sector type don't exist | 50H | 07:00 | 10H | 10H |
| Sector Type 3 erase Opcode | | 51H | 15:08 | D8H | D8H |
| Sector Type 4 Size | Sector/block size=2^N bytes 0x00b: this sector type don't exist | 52H | 23:16 | 00H | 00H |
| Sector Type 4 erase Opcode | | 53H | 31:24 | FFH | FFH |
| Unused | . | . | . | FFH | FFH |
| Vcc Supply Maximum Voltage | 1950H=1.950V | 61H:60H | 15:00 | 3600H | 3600H |
| | 2000H=2.000V | | | | |
| | 2100H=2.100V | | | | |
| | 2700H=2.700V | | | | |
| | 3600H=3.600V | | | | |
| Vcc Supply Minimum Voltage | 1650H=1.650V | 63H:62H | 31:16 | 1650H | 1650H |
| | 2250H=2.250V | | | | |
| | 2350H=2.350V | | | | |
| | 2700H=2.700V | | | | |
| HW Reset# pin | 0=not support 1=support | 65H:64H | 00 | 0b | F99EH |
| HW Hold# pin | 0=not support 1=support | | 01 | 1b | |
| Deep Power Down Mode | 0=not support 1=support | | 02 | 1b | |
| SW Reset | 0=not support 1=support | | 03 | 1b | |
| SW Reset Opcode | Should be issue Reset Enable(66H) before Reset cmd. | | 11:04 | 99H | |
| Program Suspend/Resume | 0=not support 1=support | | 12 | 1b | |
| Erase Suspend/Resume | 0=not support 1=support | | 13 | 1b | |
| Unused | | | 14 | 1b | |
| Wrap-Around Read mode | 0=not support 1=support | | 15 | 1b | |
| Wrap-Around Read mode Opcode | | | 66H | 23:16 | |
| Wrap-Around Read data length | 08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B | 67H | 31:24 | 64H | 64H |



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| Description | Comment | Byte Add(H) | Bit Add | Data | Data |
|---|--------------------------|-------------|---------|-------|-------|
| Individual block lock | 0=not support 1=support | 6BH:68 H | 00 | 0b | CBFCH |
| Individual block lock bit (Volatile/Nonvolatile) | 0=Volatile 1=Nonvolatile | | 01 | 0b | |
| Individual block lock Opcode | | | 09:02 | FFH | |
| Individual block lock Volatile protect bit default protect status | 0=protect 1=unprotect | | 10 | 0b | |
| Secured OTP | 0=not support 1=support | | 11 | 1b | |
| Read Lock | 0=not support 1=support | | 12 | 0b | |
| Permanent Lock | 0=not support 1=support | | 13 | 0b | |
| Unused | | | 15:14 | 11b | |
| Unused | | | 31:16 | FFFFH | |
| Unused | . | . | . | FFH | FFH |
| Unused | . | . | . | FFH | FFH |
| Unused | . | . | . | FFH | FFH |
| Unused | | FFH | FFH | FFH | FFH |





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9.33 Erase Security Registers (44h)

The GT25Q40/20/10/05C offers four 256-byte Security Registers which can be programmed individually. **Four 256-Byte security registers will be erased simultaneously.** These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. Once Nor flash received Erase Security Registers command, 4x256-Byte security registers will be Erase at the same time, A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

| ADDRESS | A23-A16 | A15-A8 | A7-A0 |
|-------------------------------|---------|--------|------------|
| Security Register #1,#2,#3,#4 | 00h | 00H | Don't Care |

The Erase Security Register instruction sequence is shown in Figure 31. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits LB in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored.

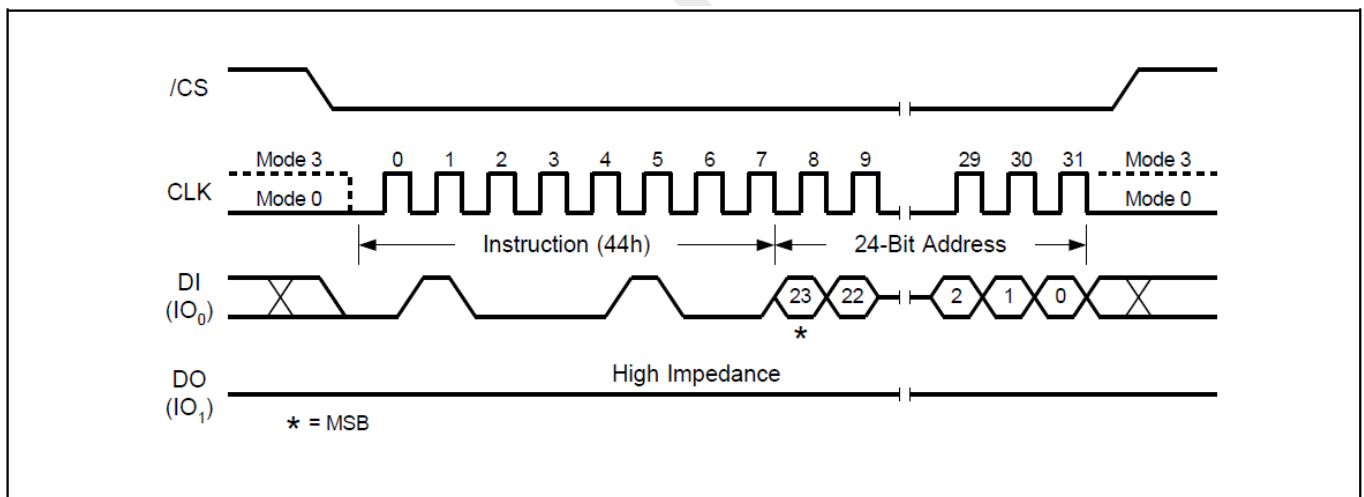


Figure 31. Erase Security Registers Instruction (SPI Mode only)



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9.34 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

| ADDRESS | A23-A16 | A15-A8 | A7-A0 |
|----------------------|---------|--------|--------------|
| Security Register #1 | 00h | 00H | Byte Address |
| Security Register #2 | 00h | 01H | Byte Address |
| Security Register #3 | 00h | 02H | Byte Address |
| Security Register #3 | 00h | 03H | Byte Address |

The Program Security Register instruction sequence is shown in Figure 32. The Security Register Lock Bits LB in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored

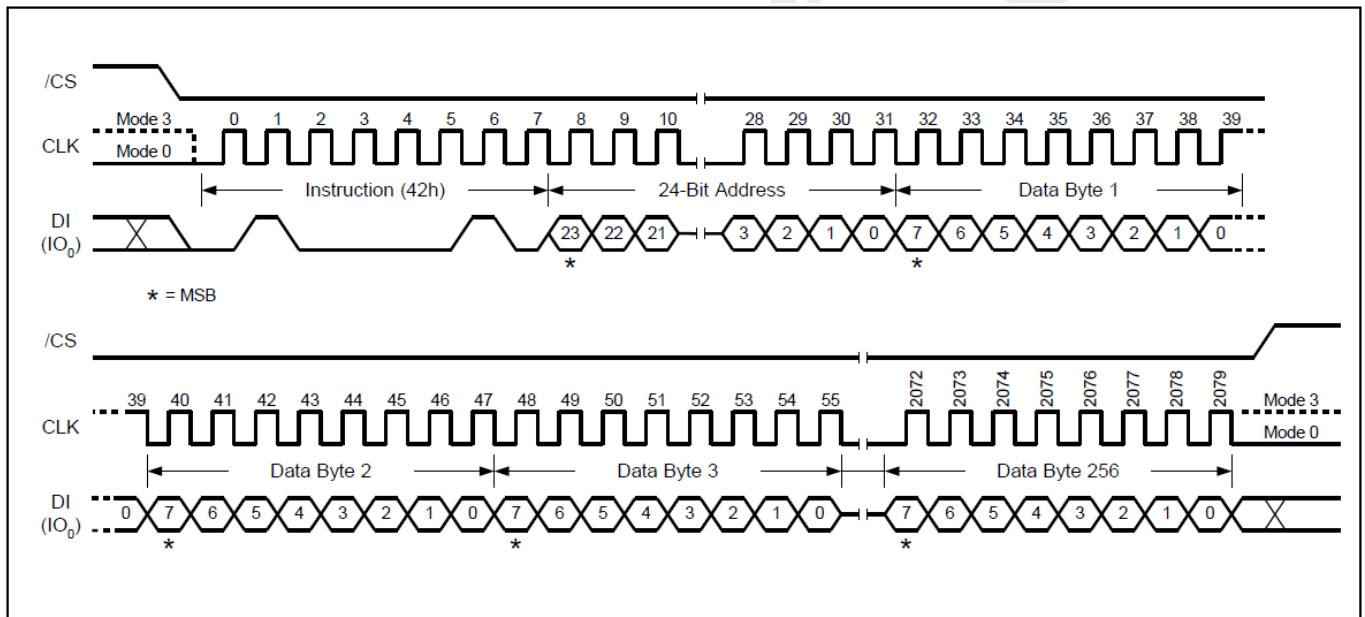


Figure 32. Program Security Registers Instruction (SPI Mode only)



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9.35 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 33. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

| ADDRESS | A23-A16 | A15-A8 | A7-A0 |
|----------------------|---------|--------------------------------|--------------|
| Security Register #1 | 00h | 00H | Byte Address |
| Security Register #2 | 00h | 01H | Byte Address |
| Security Register #3 | 00h | 02H </td <td>Byte Address</td> | Byte Address |
| Security Register #3 | 00h | 03H | Byte Address |

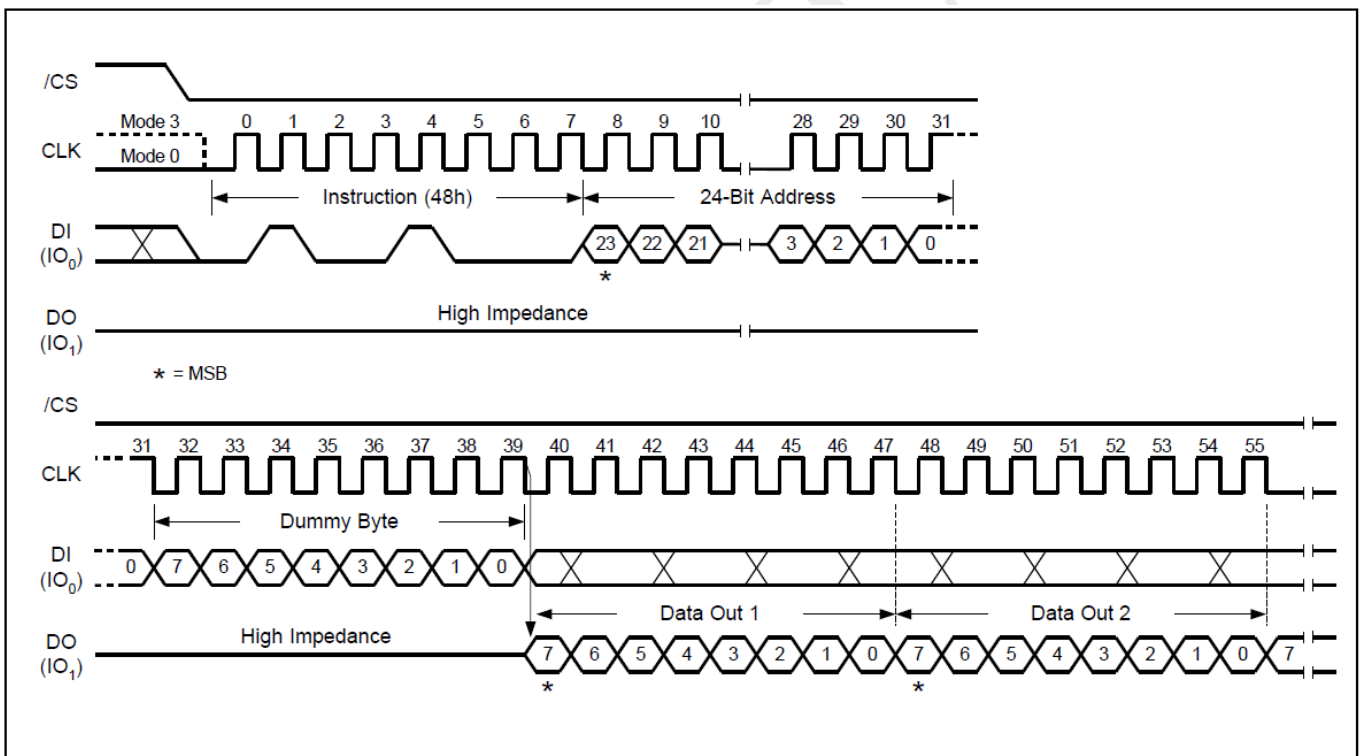


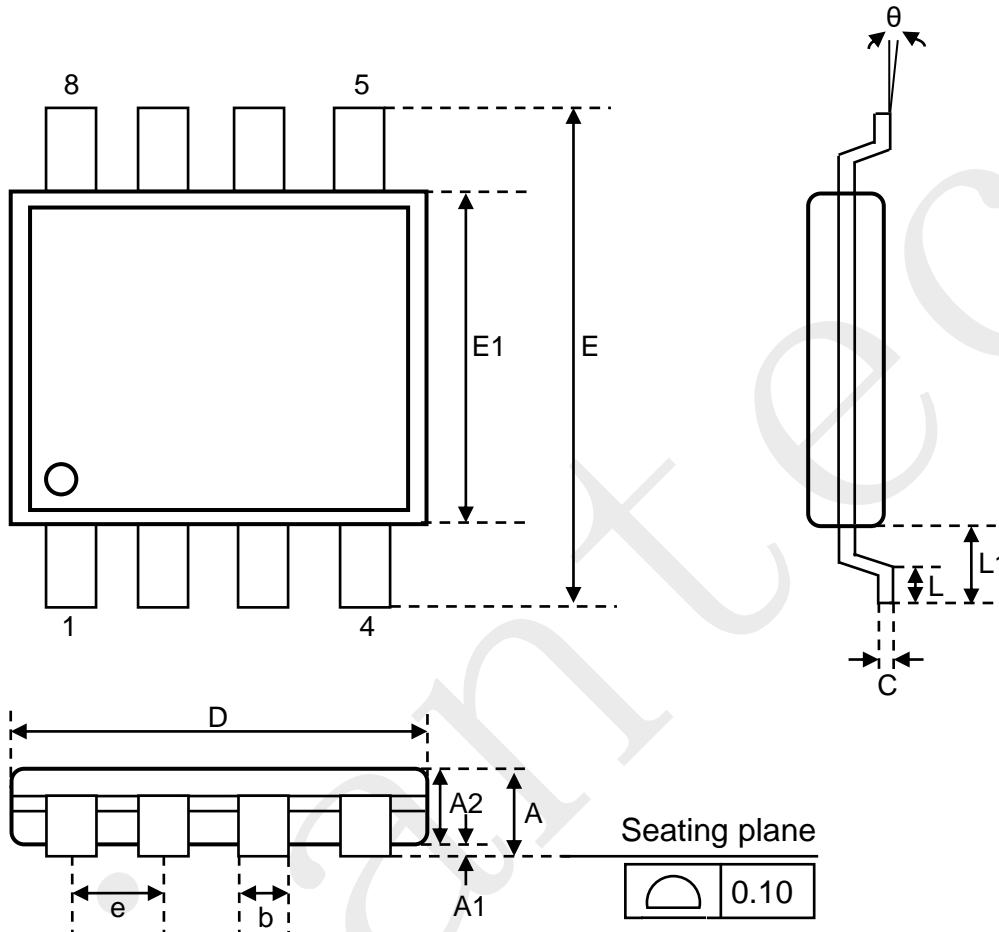
Figure 33. Read Security Registers Instruction (SPI Mode only)



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10 Package Information

10.1 Package SOP8 208MIL

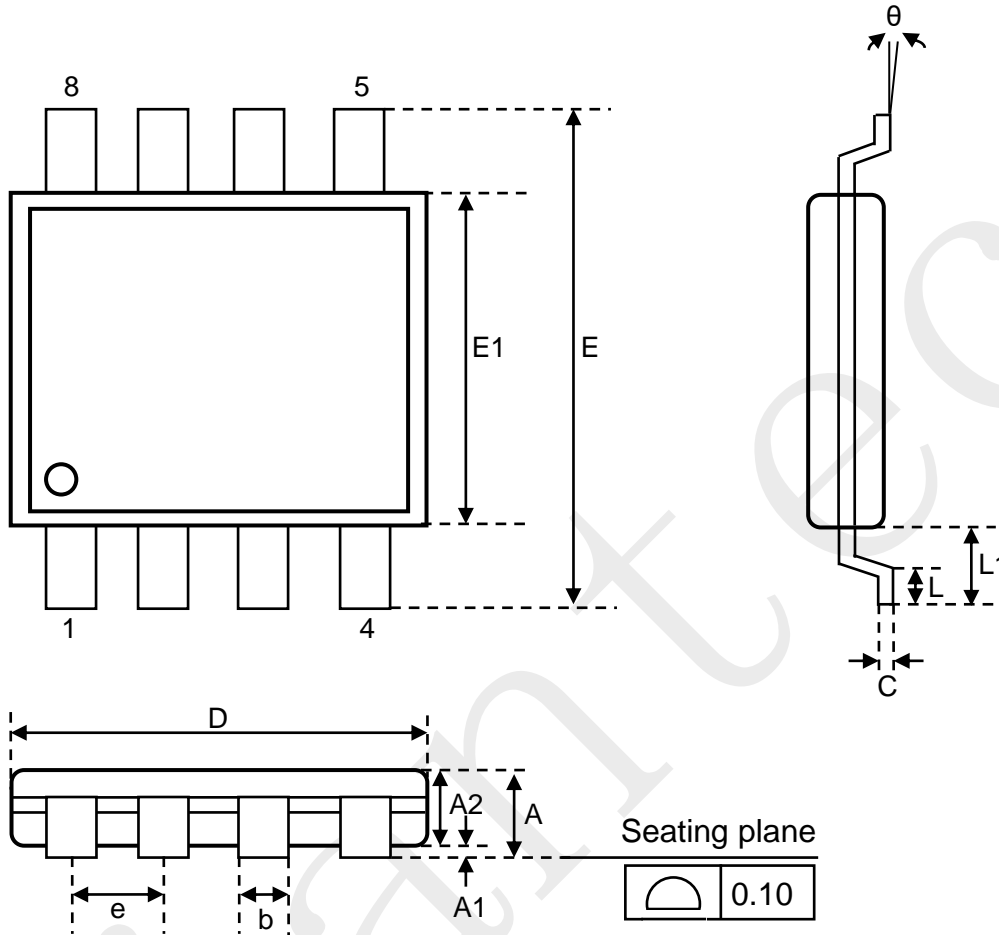


| Symbol | mm | | | Inch | | |
|----------|------|------|------|-------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.75 | 1.95 | 2.16 | 0.069 | 0.077 | 0.085 |
| A1 | 0.05 | 0.15 | 0.25 | 0.002 | 0.006 | 0.010 |
| A2 | 1.70 | 1.80 | 1.91 | 0.067 | 0.071 | 0.075 |
| b | 0.31 | 0.41 | 0.51 | 0.012 | 0.016 | 0.020 |
| C | 0.18 | 0.21 | 0.25 | 0.007 | 0.008 | 0.010 |
| D | 5.13 | 5.23 | 5.33 | 0.202 | 0.206 | 0.210 |
| E | 7.70 | 7.90 | 8.10 | 0.303 | 0.311 | 0.319 |
| E1 | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| e | | 1.27 | | | 0.050 | |
| L | 0.50 | 0.67 | 0.85 | 0.020 | 0.026 | 0.033 |
| L1 | 1.21 | 1.31 | 1.41 | 0.048 | 0.052 | 0.056 |
| θ | 0° | 5° | 8° | 0° | 5° | 8° |



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10.2 Package SOP8 150MIL

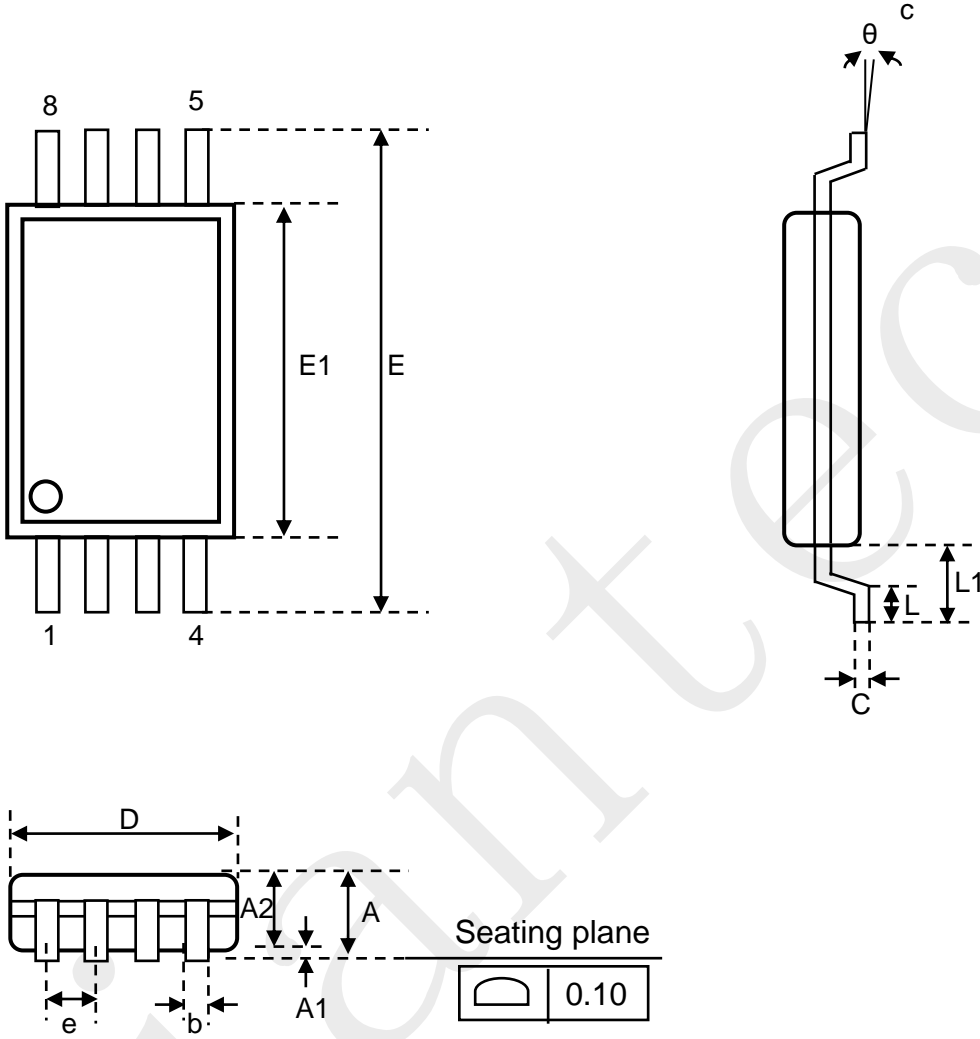


| Symbol | mm | | | Inch | | |
|--------|------|------|------|-------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.35 | - | 1.75 | 0.053 | - | 0.069 |
| A1 | 0.05 | - | 0.25 | 0.002 | - | 0.010 |
| A2 | 1.35 | - | 1.55 | 0.053 | - | 0.061 |
| b | 0.31 | - | 0.51 | 0.012 | 0.016 | 0.020 |
| C | 0.15 | - | 0.25 | 0.006 | - | 0.010 |
| D | 4.77 | 4.90 | 5.03 | 0.188 | 0.193 | 0.198 |
| E | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| E1 | 3.80 | 3.90 | 4.00 | 0.149 | 0.154 | 0.158 |
| e | - | 1.27 | - | - | 0.050 | - |
| L | 0.40 | - | 0.90 | 0.016 | - | 0.035 |
| L1 | 0.85 | 1.06 | 1.27 | 0.033 | 0.042 | 0.050 |
| θ | 0° | - | 8° | 0° | - | 8° |



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10.3 Package TSSOP8L (173mil)



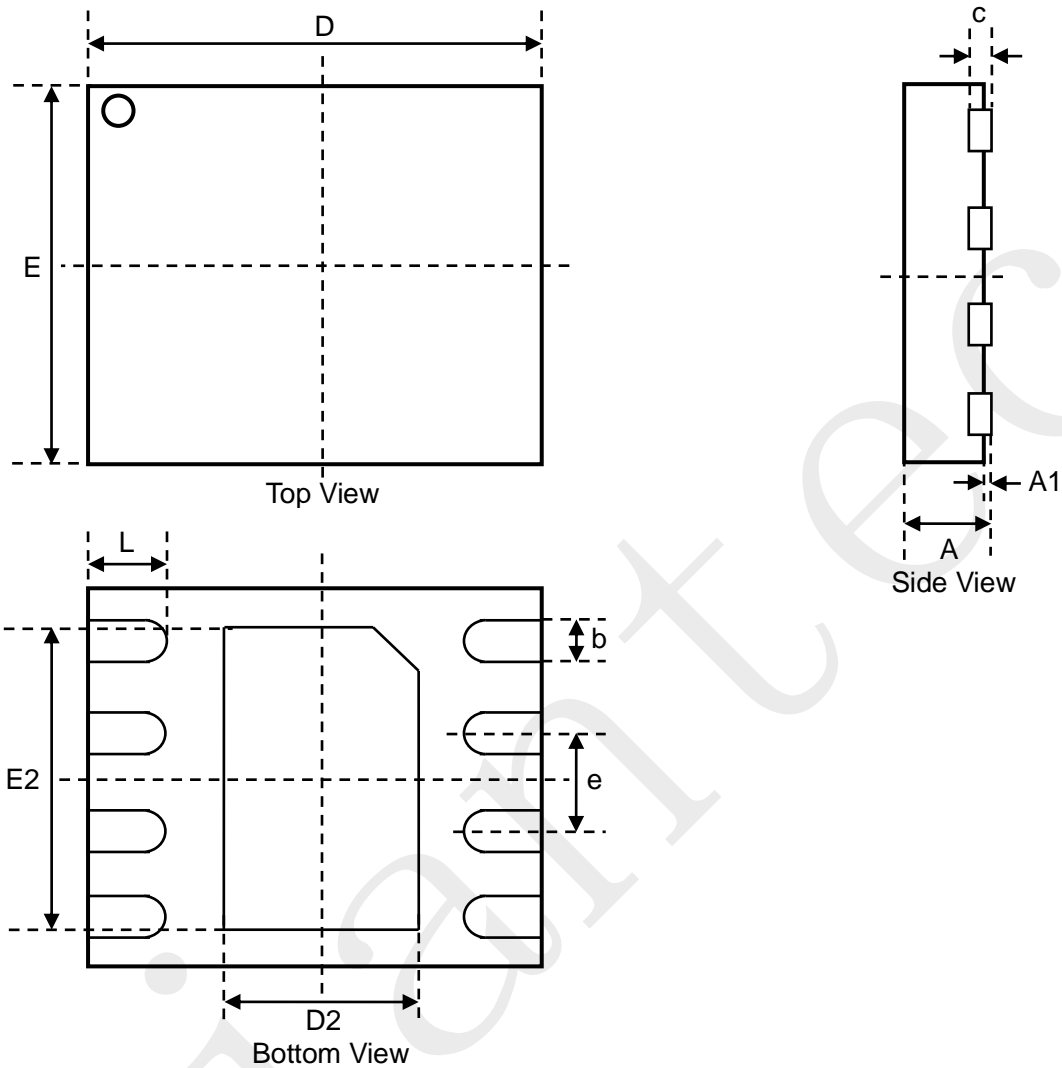
| Symbol | mm | | | Inch | | |
|--------|------|------|------|-------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 1.20 | - | - | 0.047 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.112 |
| E | 6.30 | 6.40 | 6.50 | 0.248 | 0.252 | 0.256 |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | - | 0.65 | - | - | 0.026 | - |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 0.85 | 1.00 | 1.15 | 0.033 | 0.039 | 0.045 |
| theta | 0 | 4 | 8 | 0 | 4 | 8 |

Note:
1. The exposed metal pad area on the bottom of the package is floating.



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10.4 Package WSON8 (6*5mm)



| Symbol | mm | | | Inch | | |
|--------|-------|-------|-------|-------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| c | 0.180 | 0.203 | 0.250 | 0.007 | 0.008 | 0.010 |
| b | 0.35 | 0.40 | 0.50 | 0.014 | 0.016 | 0.020 |
| D | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| D2 | 3.30 | 3.40 | 3.50 | 0.130 | 0.134 | 0.138 |
| E | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E2 | 3.90 | 4.00 | 4.10 | 0.154 | 0.157 | 0.161 |
| e | | 1.27 | | | 0.05 | |
| L | 0.50 | 0.60 | 0.75 | 0.020 | 0.024 | 0.030 |

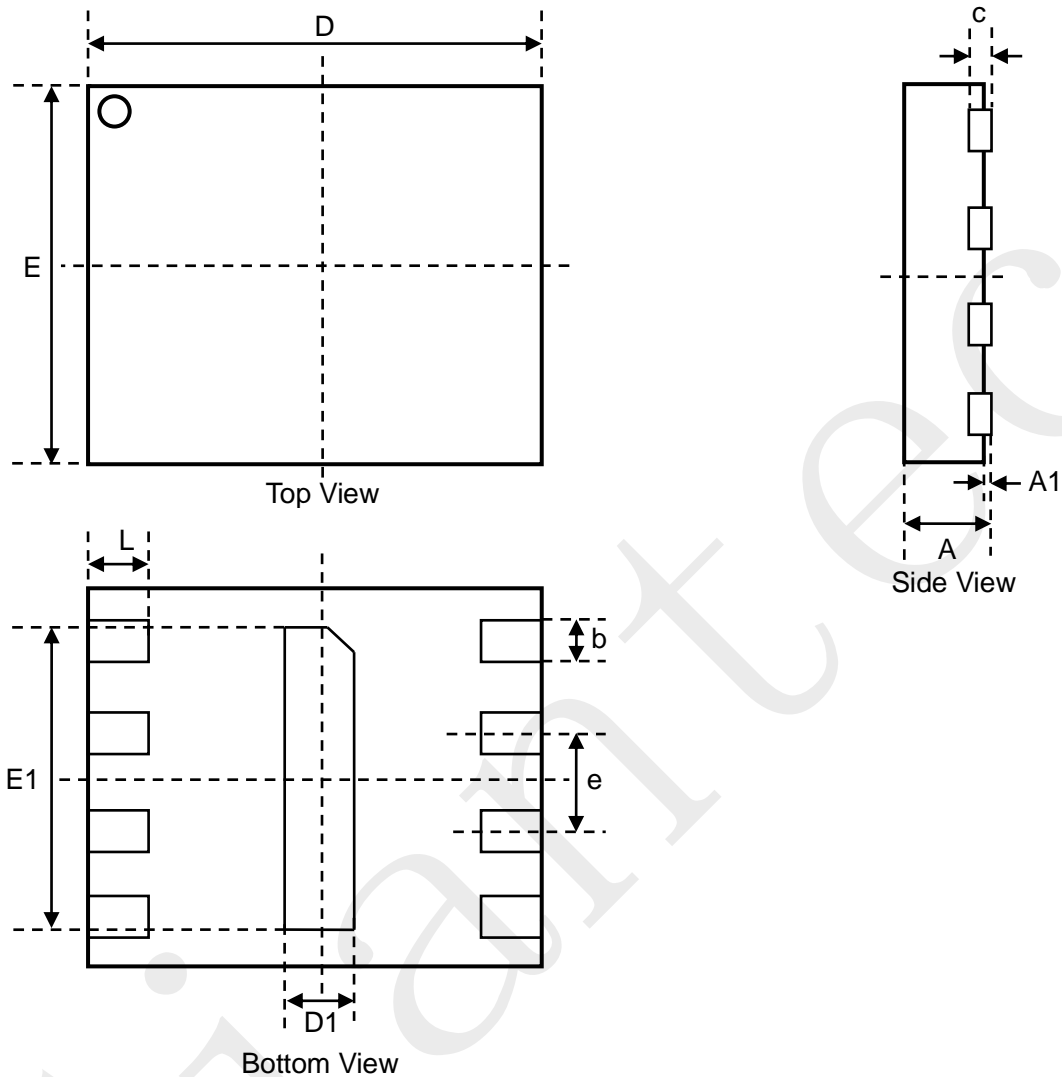
Note:

1. The exposed metal pad area on the bottom of the package is floating.



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10.5 Package USON8 (2*3mm)



| Symbol | mm | | | Inch | | |
|--------|------|------|------|-------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| A1 | 0.00 | 0.02 | 0.05 | | 0.001 | 0.002 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| D1 | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| E | 1.90 | 2.00 | 2.10 | 0.075 | 0.079 | 0.083 |
| E1 | 1.55 | 1.60 | 1.65 | 0.061 | 0.063 | 0.065 |
| e | | 0.50 | | | 0.020 | |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |

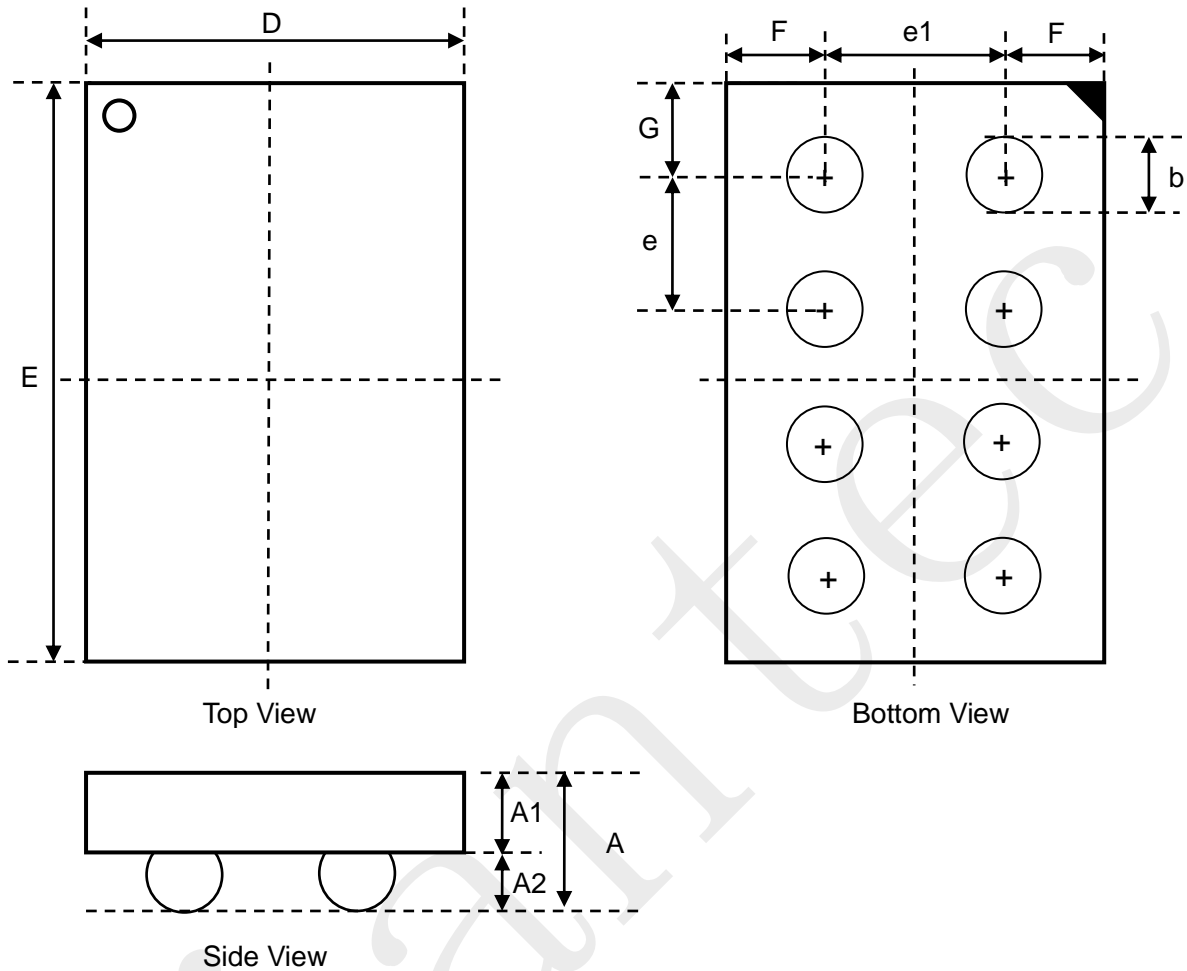
Note:

- The exposed metal pad area on the bottom of the package is floating.



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10.6 Package 8ball WLCSP



| Symbol | mm | | | Inch | | |
|--------|----------|-------|-------|-----------|--------|--------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.26 | 0.28 | 0.30 | 0.0102 | 0.0110 | 0.0118 |
| A1 | | | | | | |
| A1 | 0.047 | 0.055 | 0.063 | 0.0019 | 0.0022 | 0.0024 |
| b | 0.10 | 0.16 | 0.32 | 0.0039 | 0.0063 | 0.0126 |
| D | - | - | - | - | - | - |
| E | - | - | - | - | - | - |
| F | - | - | - | - | - | - |
| e | 0.32 BSC | | | 0.0126BSC | | |
| e1 | 0.35 BSC | | | 0.0138BSC | | |
| G | - | - | - | - | - | - |

Note:

1. Please contact local Giantec for complete package dimensions.



GT25Q80A

11 Ordering Information

GT XXX XX X - X XX X X - XX

Company

GT=Giantec

Product Family

25Q = Spi Nor Flash,SPI/ Dual/Quad I/O

Density

| | | |
|------------|---------|-----------|
| 05 = 512Kb | 80=8Mb | 128=128Mb |
| 10 = 1Mb | 16=16Mb | 256=256Mb |
| 20 = 2Mb | 32=32Mb | |
| 40 = 4Mb | 64=64Mb | |

Version

A = A Version

Operation Voltage

L = 1.65V ~ 1.95V U = 1.65V ~ 3.6V H=2.7V~3.6V

Package Type

| | |
|------------------|---------------------------------|
| W = SOP8 208 mil | VD = USON 1.5x1.5 mm |
| G = SOP8 150 mil | CS = WLCSP 8 ball |
| WS = WSON 6x5 mm | Z = TSSOP8 173mil |
| WU = WSON 4x3 mm | BG = BGA |
| ED = USON 2x3 mm | XKU30 = Sorted and Un-inked KGD |

Green Code

L=Pb Free

Temperature Range

| | |
|---------------------------------|----------------------------------|
| I = Industrial(-40°C to +85°C) | A2= Automotive(-40°C to +105°C) |
| IH= Industrial(-40°C to +125°C) | A1 = Automotive(-40°C to +125°C) |
| A0= Automotive(-40°C to +150°C) | |

Packing

TR= Tape & Reel



GT25Q80A

12 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the GT25Q80A SpiFlash Memory. Please contact Giantec for specific availability by density and package type.

| Density | Package Type | Product Number | Top Side Marking |
|---------|--------------|-------------------|------------------|
| 8Mb | SOP8 208mil | GT25Q80A-UWLI-TR | 580A-UWLI |
| | SOP8 150mil | GT25Q80A-UGLI-TR | 580A-UGLI |
| | TSSOP 173mil | GT25Q80A-UZLI-TR | 580A-UZLI |
| | WSON 5x6 | GT25Q80A-UWSLI-TR | 580A-UWSLI |
| | USON 2x3 | GT25Q80A-UEDLI-TR | 580A |
| | WLCSP 8ball | GT25Q80A-UCSLI-TR | |





GT25Q80A

13 REVISION HISTORY

| Revision | Date | Descriptions |
|----------|----------|--------------------------------------|
| V1.0 | Mar.2021 | Initial Version |
| V1.1 | May.2022 | Update Temperature of the partition |
| V1.2 | May.2022 | Update Driver Strength Default value |

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