USB 2.0 Video Class

PC Camera Controller

SN9C263

Datasheet

Document No.: SA3TD-111014-C

Version: v1.00

Revision	Date	Description
0.01	2011-04-20	Draft
1.00	2011-10-14	Formal Release
Apply to		SN9C263

Table of Contents

1 General Description

SN9C263 is a USB 2.0 compatible PC Camera controller. The built-in extreme low-power transceiver provides the superior compatibility with various USB host and the best quality for image applications. It is fully compliant with USB Video Class. With the integrated sensor interface and color processing engine, it can support most VGA, SXGA and UXGA CMOS SOC sensors.

SN9C263 integrates 2 voltage regulators for sensor power. One is for sensor's analog parts. The other one is for sensor's core power. These build-in regulators can help saving BOM cost and PCB area.

SN9C263 integrates Clock Synthesizer for performance and power saving. An external crystal is not needed, so it can help saving BOM cost and PCB area.

SN9C263 is controlled by the embedded micro-controller and the statistics for AF is built-in. The flexible architecture is consisted of mask ROM, internal RAM and external serial-flash or EEPROM which can store the customized codes and parameters. It's also possible to store all the program code in the external flash memory for customized design purpose. With the highly-integrated firmware architecture and the developing kit provided by SONiX, it's easy for 3rd party to integrate a new type of CMOS sensor and GPIO definition for variant board configuration.

2 Features

2.1 System

- 3.3V single power supply, 1.8V Core (generated by internal regulator)
- Extreme low power consumption, when standby & suspend (Power consumption of sensor is not included)
- Built-in Clock Synthesizer for performance and power saving
- Built-in PLL for internal clock generation
- Using external serial flash to store customized code and data, or using EEPROM to store data.
- No external RAM needed
- 1.8V output power source to supply CMOS sensor's core power
- 2.8V output power source to supply CMOS sensor's analog power
- 32-pin QFN package is available; please see later section for more detail.

2.2 USB Controller

- USB 2.0 compatible
- USB2.0 HS/FS auto sense and switch
- USB FS mode and USB disconnection are programmable
- USB Video Class 1.1 compliant

- 4 endpoints: CONTROL pipe, UVC Interrupt IN and Isochronous-IN (video, 24MB/s max), HID interrupt IN
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

- Support VGA, SXGA and UXGA CMOS ISP sensor
- Support YUY2 image data format from sensor
- Up to 48Mhz output clock for clock request of CMOS sensor silicon.
- Up to 96Mhz pixel clock is acceptable
- Support industrial standard 2-wire serial interface for sensor control

2.4 Image Pre-processing

- Configurable windowing function after sensor output

2.5 Color Processing

- AF edge statistics
- Programmable gamma table for Y channel
- Configurable windowing function after processed image

2.6 Scaling Engine

- 1/2, 1/4 smooth scaling on Y/Cb/Cr
- 3/5 second linear scaling for VGA input

2.7 Video / Still Image

- Output video / still image format:
  - ♦ USB Video Class Uncompressed YUY2 payload (16bits/pixel)
- Still Image capture support UVC still image capture method 1/2

2.8 Frame rate

- Frame rate considering USB bandwidth limitation

High-speed mode							
Output format	UXGA	SXGA	VGA	CIF	QVGA	QCIF	QQVGA
YUY2	5.5fps	8.5fps	30fps	30fps	30fps	30fps	30fps

- Frame rate depends on sensor characteristic

  The maximum frame rate is limited by how many frame per second that sensor can output under maximum pixel clock and is limited on High-Speed USB ISO bandwidth 24MB/s

2.9 GPIO

- 4 GPIOs are available, 3 of them are predefined as LED control and sensor reset pin and serial flash write-protection control

2.10 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 3K bytes data memory, and maximum CPU clock rate is 24MHz
- 4K bytes programmable SRAM
- Load extended 18KB F/W from external serial flash.
- Load VID/PID , manufacturer, product and serial number string from external serial flash / EEPROM.
- Load UVC parameter definition from external serial flash / EEPROM.
- F/W is upgradeable from PC
- Force USB disconnect
- CPU watch dog

2.11 Pre-defined Function for USB Video Class

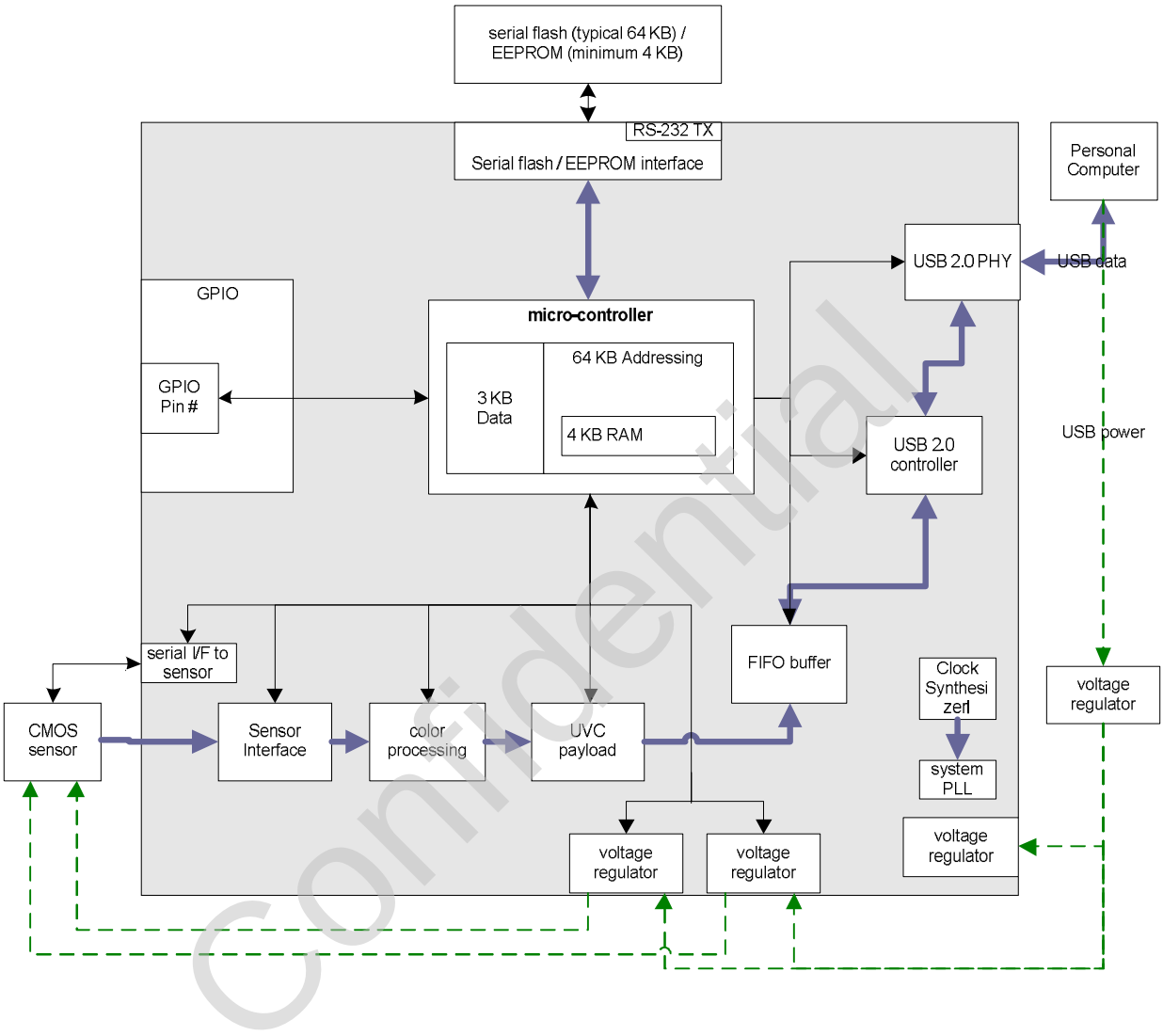
- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- Privacy control (UVC defined)
- LED indicator on video streaming
- Extension unit support

2.12 Platform Support

- Microsoft Windows XP 32bit SP2, Microsoft Windows XP 64bit, Microsoft Windows Vista 32bit, Microsoft Windows Vista 64bit, Microsoft Windows 7 32bit, Microsoft Windows 7 64bit
- Mac - OS X 10.4.8 or later
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

3 Function Block Diagram

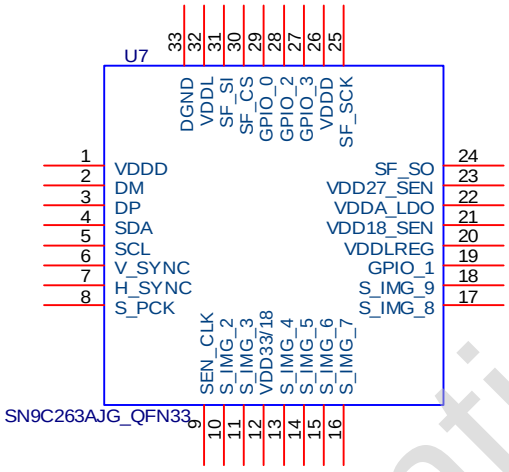
3.1 Block Diagram



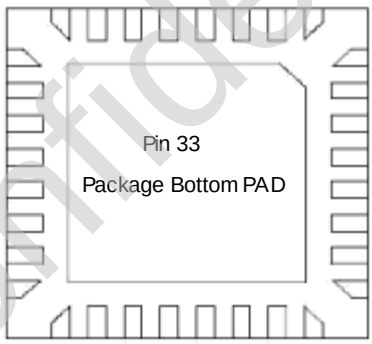
4 Pin Assignment

4.1 SN9C263 – 32 pins QFN

4.1.1 Pin-out Diagram



****Pin33 is the package bottom pad of IC, Must be connected to DGND**



Package Bottom View

4.1.2 Pin Description

Pin No	Mnemonic	DIR			Current	Description
		Power up	Normal	Suspend		
1	VDDD	P	P	P	--	3.3v analog PWR for USB driver
2	DM	A	A	A	--	D- for USB
3	DP	A	A	A	--	D+ for USB
4	SDA	I	B	F	4mA	SDA for I2C interface(data)

5	SCL	I	B	F	4mA	SCL for I2C interface(clock)
6	S_VSYNC	I	I	I	4mA	Sensor vsync
7	S_HSYNC	I	I	I	4mA	Sensor hsync
8	S_PCK	I	I	I	4mA	Sensor pixel clock
9	SEN_CLK	OU	O	F	12mA	Sensor clock
10	S_IMG_2	I	I	I	4mA	Sensor image data
11	S_IMG_3	I	I	I	4mA	Sensor image data
12	VDDPST_18V	P	P	P	--	Sensor interface I/O power. Connect to VDDD will be 3.3V sensor interface. Connect to VDDLREG will be 1.8V sensor interface.
13	S_IMG_4	I	I	I	4mA	Sensor image data
14	S_IMG_5	I	I	I	4mA	Sensor image data
15	S_IMG_6	I	I	I	4mA	Sensor image data
16	S_IMG_7	I	I	I	4mA	Sensor image data
17	S_IMG_8	I	I	I	4mA	Sensor image data
18	S_IMG_9	I	I	I	4mA	Sensor image data
19	GPIO_1	I	B	B	4mA	General purpose I/O
20	VDDLREG	P	P	P	--	Output for USB and digital core power 1.8v
21	VDD18_SEN	P	P	P	--	Output for sensor power 1.8v
22	VDDA_LDO	P	P	P	--	Power
23	VDD28_SEN	P	P	P	--	Output for sensor power 2.8v
24	SF_SO	OL	O	OL	4mA	SF_SO
25	SF_SCK	OL	O	OL	8mA	SF_SCK for SPI interface(clock) / SCL1 for I2C interface(clock)
26	VDDPST	P	P	P	--	3.3V system power
27	GPIO_3	I	B	B	4mA	General purpose I/O
28	GPIO_2	I	B	B	4mA	General purpose I/O
29	GPIO_0	I	B	B	8mA	General purpose I/O
30	SF_CS_	OH	O	F	4mA	SF_CS_
31	SF_SI	I	I	I	4mA	SF_SI for SPI interface(serial in) / SDA1 for I2C interface(data)
32	VDDL	P	P	P	--	1.8v analog PWR for PLL

Direction denotation:

O	Output	OU	Output unknown	OH	Output high	OL	Output low
I	Input	B	Bi-direction	F	Firmware control		
A	Analog	P	Power				

5 Electrical Characteristics

5.1 DC operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD18	Power Supply	-0.18 ~ 1.98	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD33	Power Supply	---	3.3	---	V
VDD18	Power Supply	---	1.8	---	V
Vin	Input voltage	0		VDD33	V
Topr	Operating Temperature	0		70	°C

5.1.3 DC Electrical Characteristics

(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, Tj=0 to +70 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input low voltage	TTL	-0.3		0.8	V
Vih	Input high voltage	TTL	2.0		VDD33+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	μA
Iih	Input high current	no pull-up or pull-down	-1		1	μA
Ioz	Tri-state leakage current		-1		1	μA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

5.1.4 Low Dropout Regulator Electrical Characteristics

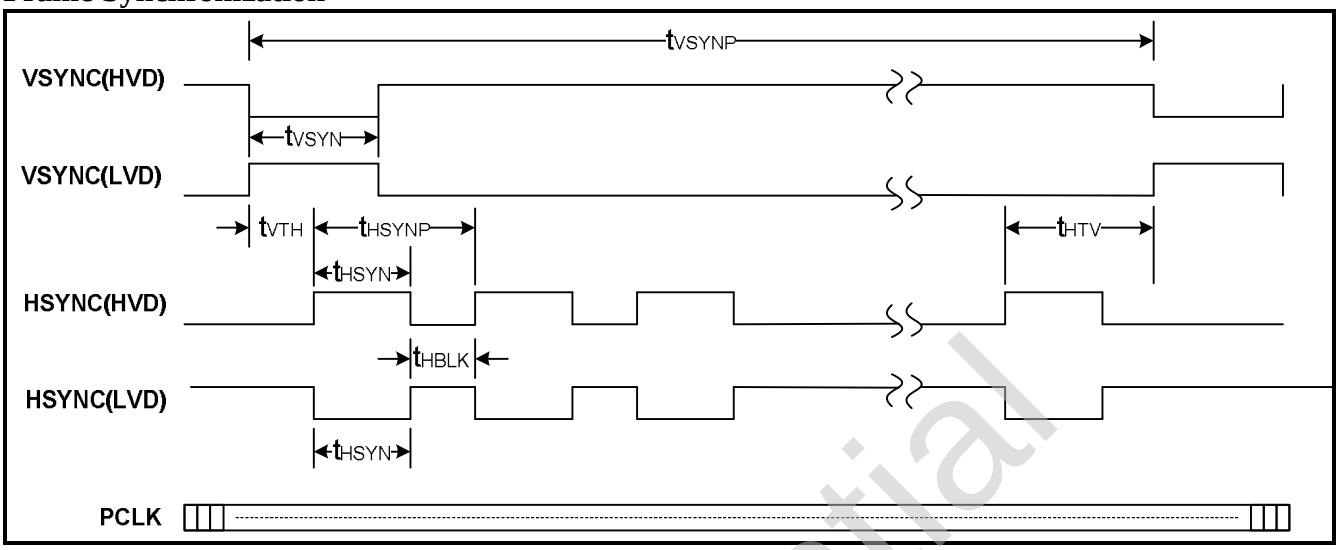
(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, Tj=0 to +70 °C)

Symbol	Parameter	Typ	Units
VDDA1	Power Supply for 2.75V LDO	3.3	V
VO275	Voltage output of 2.75V LDO	2.8	V
IO275	Output current capacity of 2.75V LDO	60	mA
VDD33	Power Supply for 1.80V LDO	3.3	V
VO180	Voltage output of 1.80V LDO	1.8	V
IO180	Output current capacity of 1.8V LDO	60	mA

5.2 AC operating Condition

5.2.1 Sensor Interface

Frame Synchronization



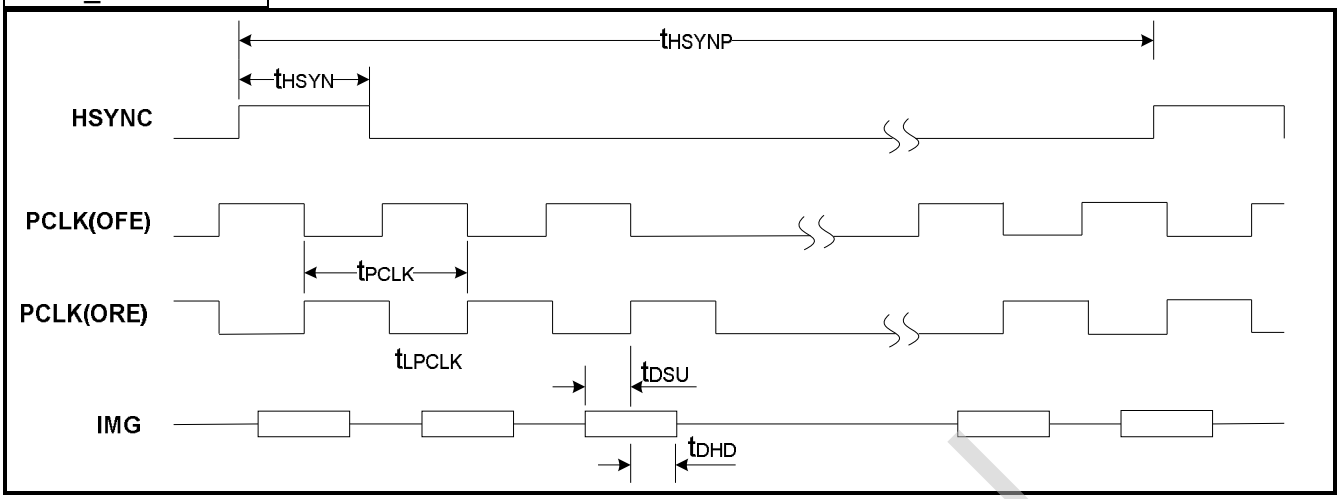
Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	t_{VSYNC}	t_{PCLK}	-	-	ns
VSYNC to HSYNC	t_{VTH}	t_{PCLK}	-	-	ns
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
Blank time between two HSYNC	t_{HBLK}	t_{PCLK}	-	-	ns
HSYNC to VSYNC	t_{HTV}	t_{HSYNP}			ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing.
2. t_{HSYNP} is period of Hsync, t_{VSYNP} is period of Vsync.
3. HVD (High Valid), LVD (Low Valid).

Data Synchronization

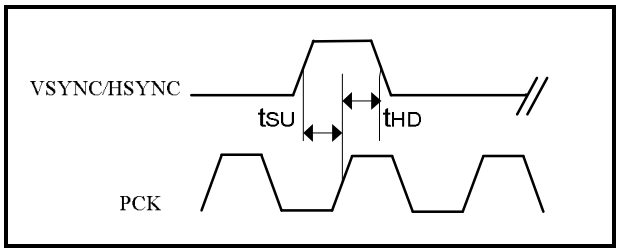
SYNC_MODE = 1 :



Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
PCLK Low Pulse Width	t_{LPCLK}	2	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2	-	-	ns
Frequency of pixel clock (YUV Mode)	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2	-	-	ns
Image data hold time	t_{DHD}	2	-	-	ns

Note:

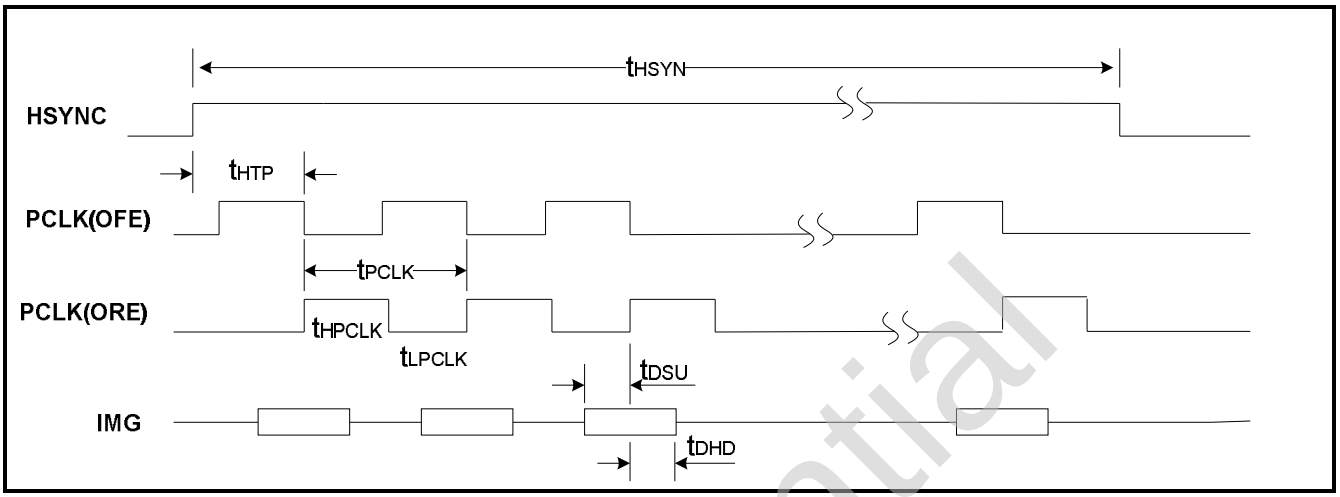
1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC / HSYNC setup time	t_{SU}	2	-	-	ns

VSYNC / HSYNC hold time	t_{HD}	2	-	-	ns

SYNC_MODE = 0 :

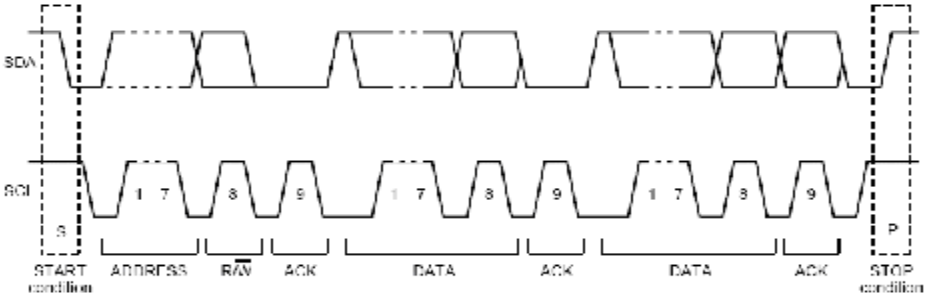


Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	HSIZE * t_{PCLK}	-	-	ns
HSYNC to PCLK	t_{HTP}	t_{SENCK}	-	-	
PCLK Low Pulse Width	t_{LPCLK}	2	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2	-	-	ns
Frequency of pixel clock (YUV Mode)	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2	-	-	ns
Image data hold time	t_{DHD}	2	-	-	ns

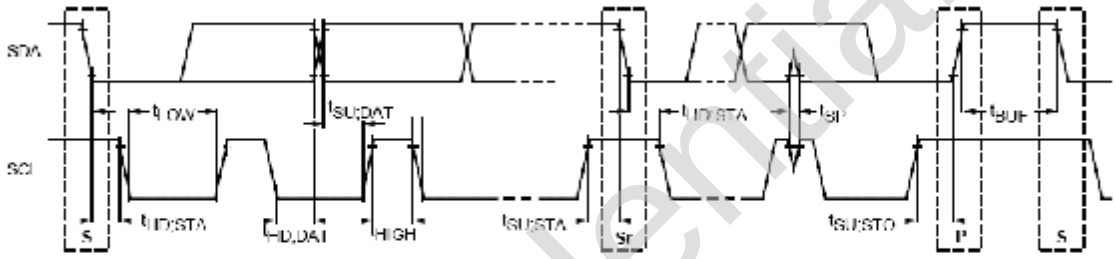
Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge
4. HSIZE represents total valid PCLK number per horizontal line

5.2.2 Sensor Control Interface



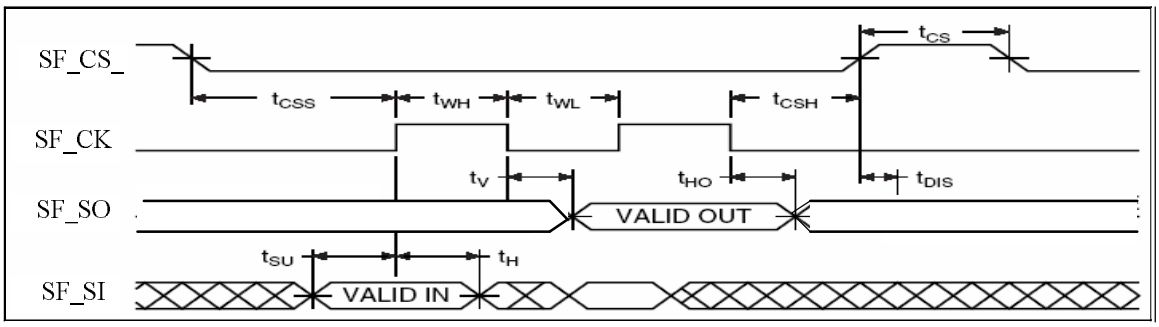
A complete data transfer.



Definition of timing for F/S-mode devices on the I²C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write Data hold time: Read	$t_{HD:DAT}$ $t_{HD:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Data setup time: Write Data setup time: Read	$t_{SU:DAT}$ $t_{SU:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.3 Serial Flash Interface



When f_{SCK} = 24 Mhz (SPEED=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

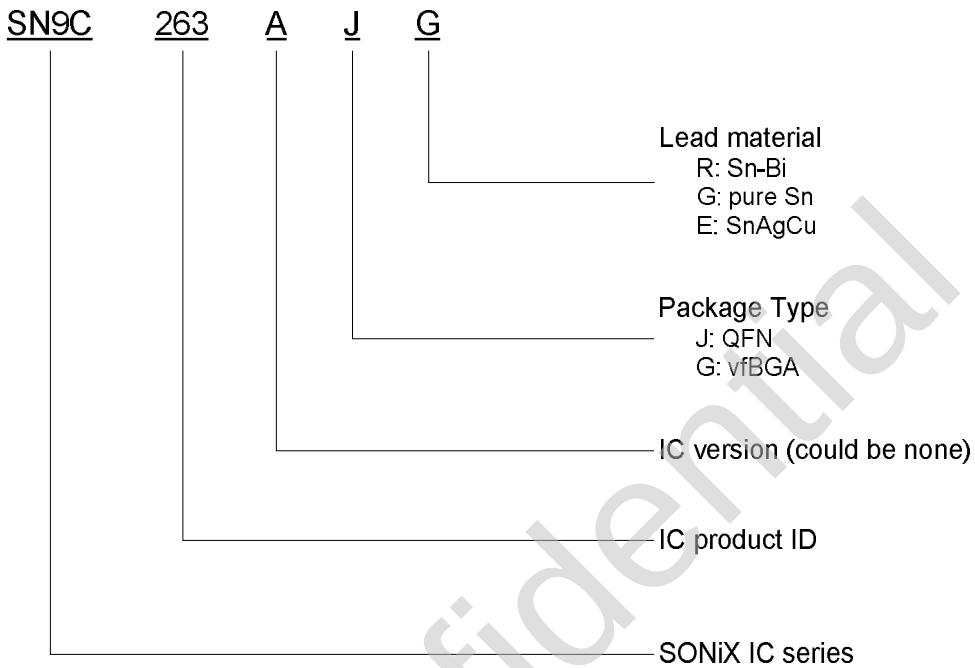
When f_{SCK} = 12 Mhz (SPEED=3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	41.67	-	-	ns
Clock low period	t_{WL}	41.67	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	78	-	-	ns

6 Package Information

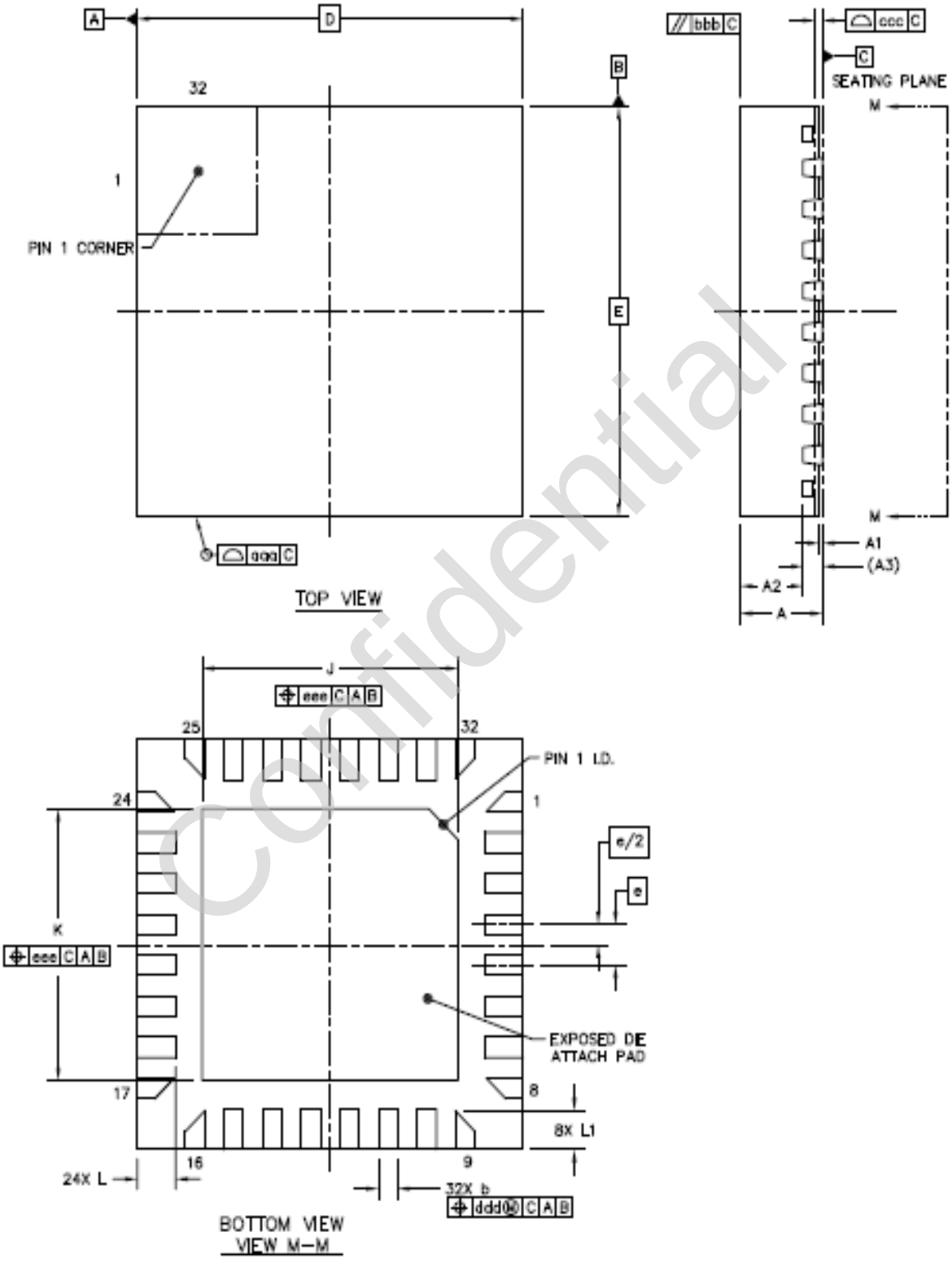
6.1 Nomenclature

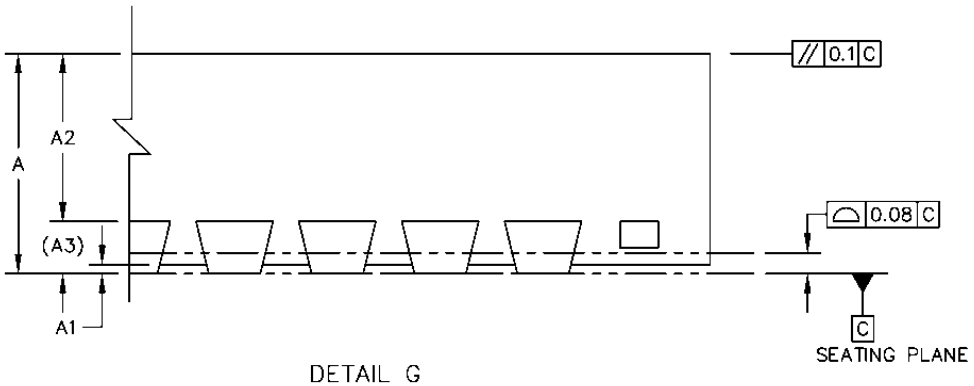
(Example)



6.2 SN9C263

6.2.1 32pins QFN





DETAIL G
VIEW ROTATED 90° CLOCKWISE

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.55	2.65	2.75
	Y	K	2.55	2.65	2.75
LEAD LENGTH		L	0.35	0.4	0.45
		L1	0.332	0.382	0.432
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

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