MPQ2022

Automotive Dual Phantom Antenna LDO with I²C and ADC for Digital Diagnosis 40V, Dual 300mA, AEC-Q100 Qualified

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPQ2022 is a dual-channel low-dropout (LDO) regulator with I²C interface and one-time programmable (OTP) memory. The device provides phantom power to low-noise amplifiers (LNAs) for active antennas in automotive systems from a cold-crank through load-dump (4.5V to 40V) input voltage conditions.

It delivers up to 300mA per channel with excellent load and line regulation. Low 32µA quiescent current makes the devices suitable for always-on power supplies.

The MPQ2022 dual LDO outputs are programmable through I²C interface. The output voltage level is adjustable from 1V to 13.6V. The various parameters can be adapted by writing the settings in the device.

During bench evaluations, different configurations can be easily obtained through the I²C interface instead of reworking external components. Once the desired optimum setting has been reached, a multipage OTP is available allowing the settings to be permanently stored.

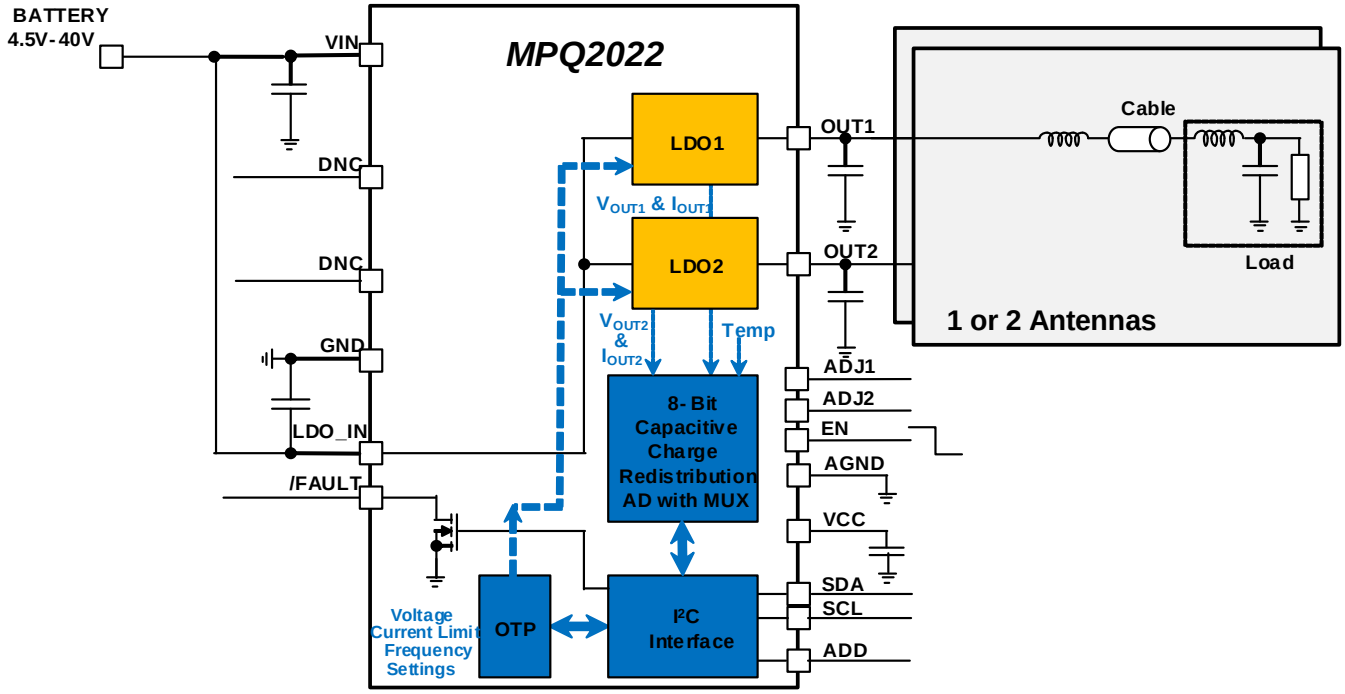
FEATURES

- Wide Input Voltage Range (4.5V to 40V)
- 32µA Low Quiescent Current
- Soft-Start Feature for All Regulator Outputs
- No External Resistor Network for Output Voltage Settings
- Programmable Dual LDOs
  - 300mA Continuous Output Current Per Channel
  - 1V to 13.6V Output Range
  - Over Temperature Protection
- I²C interface
- ADC for LDO Output Voltages and Load Currents
- Multi-Page One-Time Programmable (OTP) Memory
- Available in QFN-16 (4mmx4mm) Package
- Available with Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Antenna Phantom Power
- Automotive Camera
- ADAS Systems with Functional Safety and ASIL Requirements

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ2022GRE-xxxx-AEC1**, ****	QFN-16 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g.: MPQ2022GRE-xxxx-AEC1–Z)

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "x" can be a hexadecimal value between 0 and F. Please contact an MPS FAE to create this unique number.

*** Moisture Sensitivity Level Rating

**** In development, contact MPS for details

TOP MARKING

MPSYWW

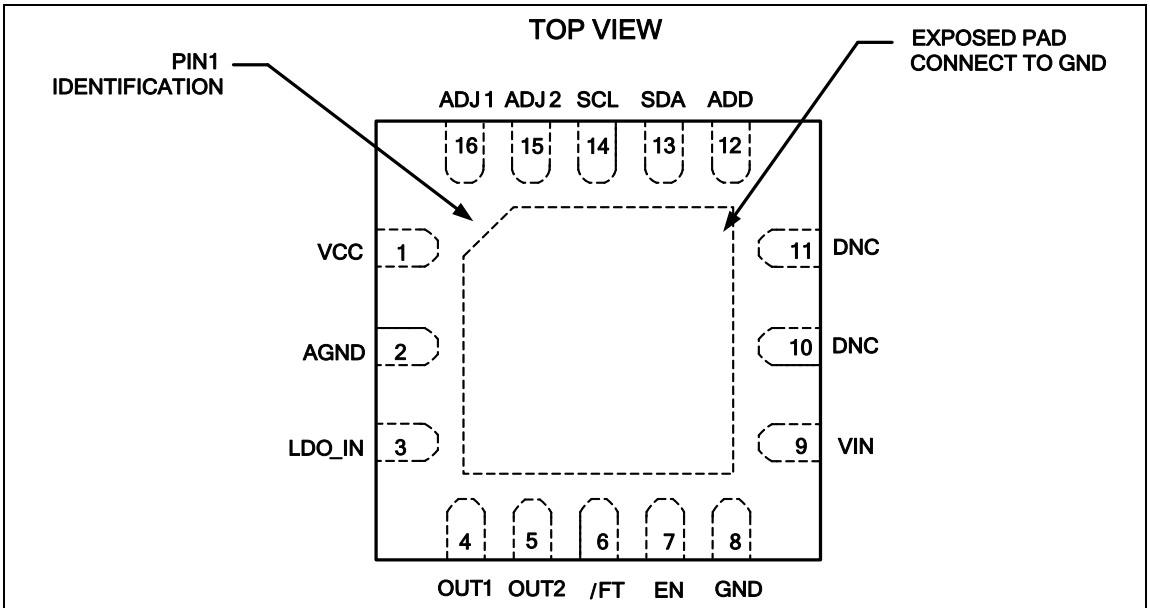
MP2022

LLLLLL

E

MPS: MPS prefix
Y: Year code
WW: Week code
MP2022: Part number
LLLLLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE



QFN-16 (4mmx4mm)

PIN FUNCTIONS

PIN #	Name	Description
1	VCC	**Bias Supply.** This is 5V internal regulator output, supplies power to the I²C interface, internal control circuit and gate drivers. External low-ESR decoupling capacitor to ground is required close to this pin. A 1μF to 10μF ceramic capacitor is recommended.
2	AGND	**Analog Ground.** Ground for internal logic and signal control blocks.
3	LDO_IN	**Supply Input of the Dual LDOs.** Tie to VIN pin and place a 1μF to 10μF ceramic between this pin and ground.
4	OUT1	**Output of LDO1.** Only a low-value ceramic capacitor is required as output capacitor for stability. A 10μF ceramic capacitor is recommended for most applications.
5	OUT2	**Output of LDO2.** Only a low-value ceramic capacitor is required as output capacitor for stability. A 10μF ceramic capacitor is recommended for most applications.
6	/FT	**Fault Pin Output.** This pin is an open-drain status pin. Connect with a resistor (e.g. 100kΩ) to a voltage source ≤5V. Leave this pin floating if not used.
7	EN	**Enable.** Pulling this pin below the falling threshold 2.3V shuts the chip down. Pulling it above the rising threshold 2.5V enables the chip. There is an internal 3.3M pull-down resistor, leaving EN pin floating disables the chip.
8	GND	**Power Ground.** Reference ground of the regulated output voltage. Connect these pins to larger copper areas for best thermal result.
9	VIN	**Input Supply.** VIN supplies power to all of the internal control circuitries. Tie to LDO_IN pin and a decoupling capacitor to ground must be placed as close to this pin as possible.
10	DNC	**Do Not Connect.** Reserved for factory functions, it is recommended to leave floating.
11	DNC	**Do Not Connect.** Reserved for factory functions, it is recommended to leave floating.
12	ADD	**Address setting for I²C.** Connect a resistor between this pin and ground to set I²C address. Leave this pin floating if not used.
13	SDA	**I²C Serial Data.** This pin is an open-drain port. An external pull-up resistor is needed to connect this pin to the supply rail of the I²C bus. If SDA is not used, it is recommend to connect SCL to the VCC pin through a resistor.
14	SCL	**I²C Serial Clock.** This pin is an open-drain port. An external pull-up resistor is needed to connect this pin to the supply rail of the I²C bus. If SCL is not used, it is recommend to connect SCL to the VCC pin through a resistor.
15	ADJ2	**The reference voltage input for LDO2.** In tracking mode of LDO output voltage, connect this pin to the voltage reference directly or with a voltage divider for lower output voltages. Leave this pin floating if not used.
16	ADJ1	**The reference voltage input for LDO1.** In tracking mode of LDO output voltage, connect this pin to the voltage reference directly or with a voltage divider for lower output voltages. Leave this pin floating if not used.
		Exposed Thermal Power Pad. Connect the exposed pad to the ground plane for optimal heat dissipation. Do not use EP as the primary electrical ground connection.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, DNC, DNC, LDO_IN, OUT1, OUT2 ..... -0.3V to +45V
ADJ1, ADJ2 ..... -0.3V to +15V
All Other Pins ..... -0.3V to +5.5 V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN-16 (4mmX4mm) ..... 4 W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

ESD Capability

HBM (Human Body Mode) ..... ±2000V
CDM (Charged Device Mode) ..... ±750V

Recommended Operating Conditions

V_{IN} Voltage ..... 4.5V to 40V
Output Voltage V_{OUT1}, V_{OUT2} ..... 1V to 13.6V
Load Current Range I_{OUT1}, I_{OUT2} 300mA
Operating Junction Temp. (T_J). -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (4mmx4mm)		
JESD51-7 (3)	46	10 °C/W
T-MPQ2022-R-00A (4)	31	5.5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
4) Measured on T-MPQ2022-R-00A, 4-layer PCB, 2oz, 9cmx9cm.

ELECTRICAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage-Current Parameters						
Input Voltage	V_{IN}		4.5		40	V
Supply Current (Quiescent)	I_Q	Enabled, V_{OUT1} =V_{OUT2} = 9V No load, T_J = +25°C		32		μA
Supply Current (Quiescent)	I_Q	Enabled, V_{OUT1} =V_{OUT2} = 9V No load, T_J =-40°C to +150°C			85	μA
Supply Current (Shutdown)	I_{SD}	V_{EN} = 0V			5	μA
V_{IN} Under Voltage Lockout Threshold Rising	$UVLO_{Vth-R}$			4.2		V
V_{IN} Under Voltage Lockout Threshold Falling	$UVLO_{Vth-F}$			3.8		V
Thermal Shutdown and Over Temperature Protection						
Thermal Shutdown (5)	T_{SD}	Junction Temperature Rising		170		°C
Thermal Shutdown Hysteresis (5)	T_{SD-HYS}			20		°C
/FT						
/FT Sink Current Capacity	$V_{PG-SINK}$	Sink 4mA			300	mV
/FT Delay Time	$t_{PG-DELAY}$	Rising Edge		90		μs
		Falling Edge		40		μs
/FT Leakage Current	I_{PG-LKG}			10	100	nA
Enable						
Enable Threshold	EN_{Vth}	Level Sensitive Input	2	2.5	3	V
Enable Threshold Hysteresis	V_{EN-HYS}			200		mV
Enable Input Current	I_{EN}	V_{EN} =2V		0.5	1	μA
Internal VCC						
VCC Regulator	V_{CC}	I_{CC}=0mA	4.8	5	5.2	V
Fault Detection						
Power On Short-to-battery Detection Window	t_{BLK-RC}			16		ms
Short to Battery Threshold	V_{StB}	V_{OUT}–V_{IN} , check during turn-on sequence	-500	-80	-10	mV

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Dual Linear Regulator (LDO1 & LDO2)						
Regulated Output Range	$V_{OUT1,2}$	Programmable Range	1		13.6	V
		Default Setting		9		V
Line Regulation	dV_{Aline}	V_{IN} = 3V to 40V, 5mA Load Current, V_{OUT}=8.5V,	-10	1	10	mV
Load Regulation	dV_{Aload}	I_{LOAD} = 5mA to 300mA, V_{OUT}=8.5V, T_J = +25°C		1	20	mV
Power Supply Rejection Ratio (5)	PSRR	I_{LOAD} = 100mA at 100Hz, V_{OUT}=8.5V		60		dB
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD} = 100mA, Measured between LDO_IN and OUTx		250	300	mV
Over current Limit	$I_{LDO-LIMIT}$	Programmable Range	100		500	mA
		Default Value		400		mA

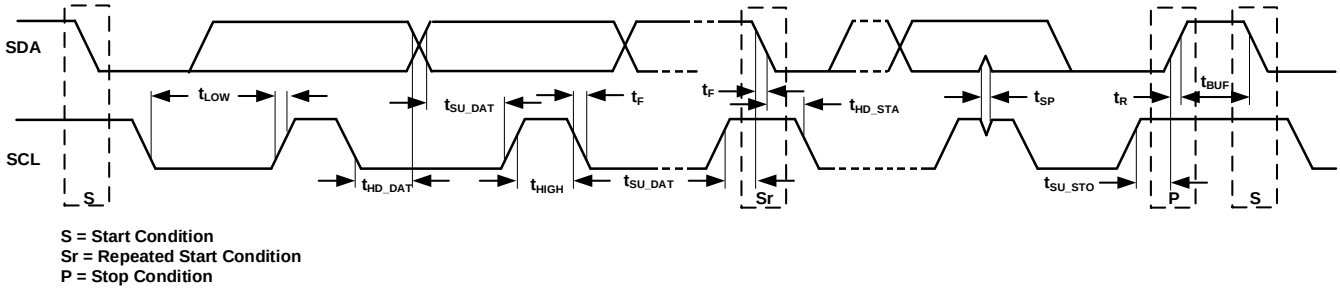
Note:

5) Not tested in production and guaranteed by design and characterization.

I²C PORT SIGNAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications						
Input Logic Low	V_{IL}		0		0.4	V
Input Logic High	V_{IH}		1.3			V
Output Logic Low	V_{OL}	I_{LOAD}=3mA			0.4	V
SCL Clock Frequency	f_{SCL}				400	kHz
SCL High Time	t_{HIGH}		0.6			µs
SCL Low Time	t_{LOW}		1.3			µs
Data Setup Time	$t_{SU,DAT}$		100			ns
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
Setup Time for Repeated Start	$t_{SU,STA}$		0.6			µs
Hold Time for Start	$t_{HD,STA}$		0.6			µs
Bus Free Time between a Start and a Stop Condition	t_{BUF}		1.3			µs
Setup Time for Stop Condition	$t_{SU,STO}$		0.6			µs
Rise Time of SCL and SDA	t_R		20+0.1×C_B		120	ns
Fall Time of SCL and SDA	t_F		20+0.1 ×C_B		120	ns
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Capacitance Bus for Each Bus Line	C_B				400	pF



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

Figure 1: I²C Compatible Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

BLOCK DIAGRAM

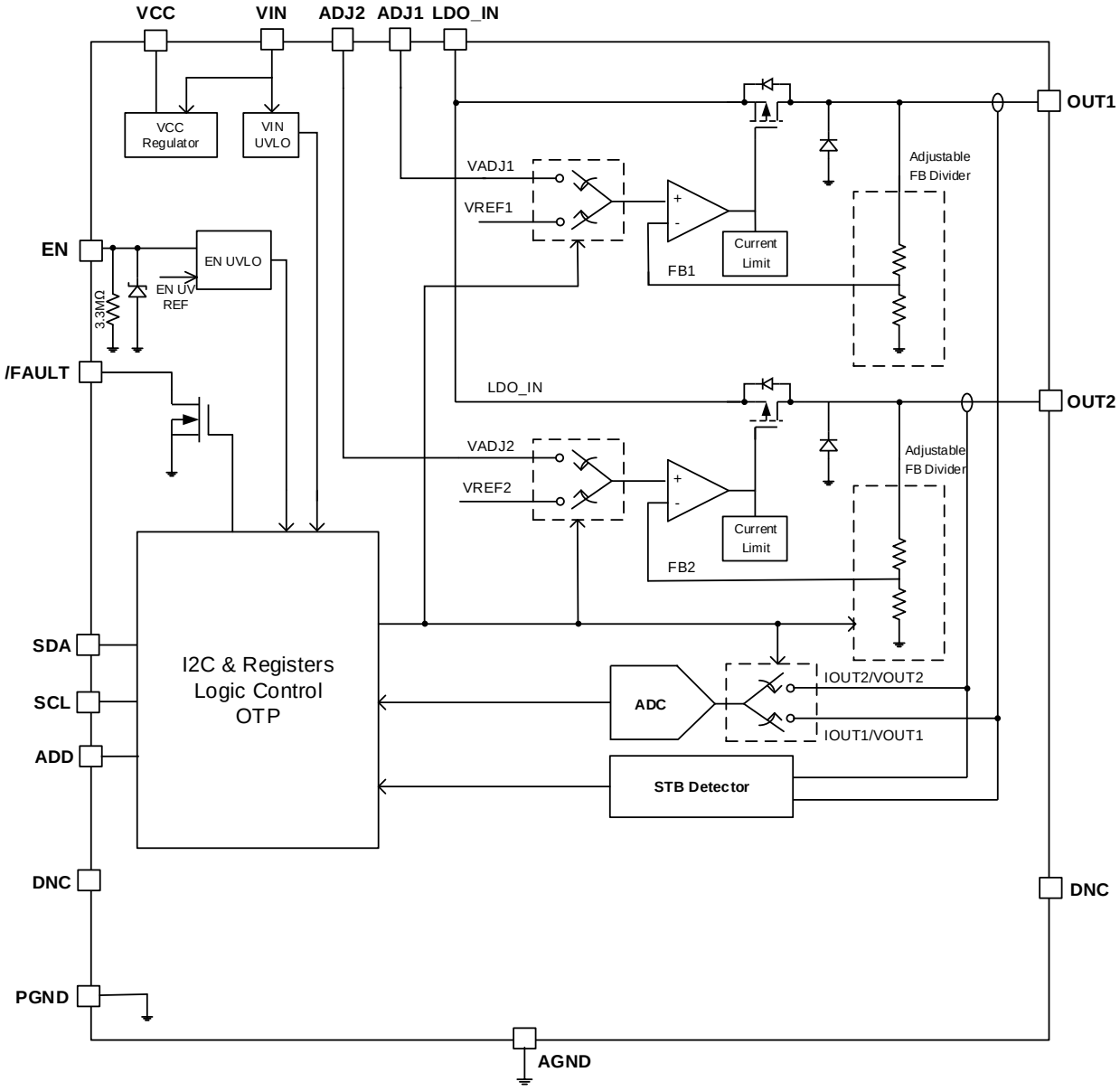


Figure 2: Functional Block Diagram

OPERATION

The MPQ2022 is a dual phantom antenna linear regulator with I²C interface. It supplies power to systems with high-voltage batteries. It features a wide 4.5V to 40V input range, low-dropout voltage, and a low-quiescent supply current.

Its two output-adjustable LDOs are supplied from LDO_IN and have outputs that are adjustable via I²C interface from 1V to 13.6V with 200mV step or from 1V to 7.3V with 100mV step.

The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions.

The dual LDO peak output current limitation range can be configured from 100mA to 500mA via I²C interface.

When the junction temperature is too high, the thermal sensor sends a signal to the control logic that shuts down the IC. The IC will re-start when the temperature has sufficiently cooled.

The maximum power-output current is a function of the package's maximum power dissipation for a given temperature. The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of airflow. GND and the exposed pad must be connected to the ground plane for proper dissipation.

Fault Indicator and Diagnostics

The device provides full diagnostics of different fault conditions. MPQ2022 monitors the load current through an internal sense resistor to protect against over current and short-circuit. In addition, the device also detects output over voltage and under voltage conditions, short-to-battery and features thermal shutdown.

/FT pin will be pulled high at normal operation, and any fault or warning will pull down this pin to indicate a fault status, referring to Table1.The /FT pin is an open drain of a MOSFET. It should be connected to a ≤5V voltage source through a resistor (e.g. 100kΩ).

Besides, MPQ2022 has dedicated register bits serve as fault flag and device status indication for system diagnostics. Refer the Register Map and Register Description sections for details.

Short-Circuit and Over current

The current limit of each LDO channel is programmed via I²C interface to protect the device during short-circuit or over current conditions. When the output current of either LDO reaches its internal threshold, the output current of the LDO is limited, and a dedicated bit in the register is set to indicate the fault. The /FT pin is asserted low as well, but the output is not disabled.

The /FT and the status of internal register diagnostic bits should be monitored by the external microcontroller (MCU), and the channel experiencing short-circuit or over current condition should be disabled by MCU through I²C interface by setting dedicated register bits. If severe condition occurs, MCU can shut down entire unit by pulling EN pin low.

If this condition persists, thermal shutdown could occur and both outputs will be disabled.

Short-to-Battery (STB) Detection

Shorting the LDO output pins to the battery because of a fault in the system is possible. MPQ2022 each LDO channel can detect this failure by comparing the corresponding voltage at the OUT1/2 and VIN pins before the device internal switches turn on.

A 16ms blank time is asserted each time the device is enabled when both VIN and EN exceed their rising threshold or recover from the thermal shutdown or hiccup. The short-to-battery detection occurs during this 16ms blank time. If the device detects the short-to-battery fault, both dual LDO switches are latched off or hiccup (based on Reg0x04 D[0] bit set), the /FT pin is asserted low, and the dedicated bits in the register are set to indicate fault-channel. After the short-to-battery fault is removed, the device can recover to normal operation automatically if hiccup mode selected or by recycling VIN power or EN to reset VCC if latched off mode is selected.

Thermal Shutdown

Thermal shutdown circuitry protects the device from overheating. The switch turns off immediately when the junction temperature exceeds +170°C (typ). The switch turns on again

after the device temperature drops by approximately 20°C (typ).

Integrated Inductive Clamp

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between OUT1/2 and GND pins with a DC-current capability of 300mA for inductive clamp protection.

VCC Regulator

In normal operation, an internal low-dropout (LDO) regulator outputs a nominal 5V VCC supply from VIN. This supplies power to all control blocks and I²C block. Add a 1µF to 10µF, low-ESR ceramic capacitor to act as the bypass capacitor from VCC to GND.

VCC has an internal under voltage lockout (UVLO) block. Chip is shutdown when VCC drops below its falling threshold 2.4V, and startup again when VCC exceeds its rising threshold 2.6V.

Input Under Voltage Lockout

The device VIN has an under voltage lockout (UVLO) threshold that is internally fixed. The under voltage lockout activates when the input voltage on the VIN pin drops below falling threshold 3.8V. UVLO ensures the regulator is not latched into an unknown state during low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the UVLO rising threshold 4.2V.

Enable

EN pin can be used to enable and disable entire device. Pull EN below the falling threshold 2.3V shuts the chip down. Drive it to exceed the rising threshold 2.5V enables the chip.

Besides, there are dedicated register bits adopted to realize software enable of LDO1 and LDO2 separately.

The physical EN pin has a higher priority than software enable.

Adjustable LDO Output Voltage

MPQ2022 dual LDOs output voltage are adjustable from 1V to 13.6V via I²C interface. Besides, the dual LDO output voltage are also can be adjustable by tracking external voltage on ADJ1/2 pin.

This external voltage tracking mode is enabled via I²C interface. After enabled, the dual LDO output voltage V_{OUT1}, V_{OUT2} equals to the voltage at ADJ1, ADJ2 pin separately. The applied voltage ranges on ADJ1, ADJ2 are 3V to 13V. To track higher voltage, a resistor divider can be used to scale down voltage level.

Note that if external voltage tracking mode enabled, /FT pin indication and LDO output OV/UV/PG indication in I²C registers are invalid. The /FT remains at high.

LDO Output Voltage and Current Monitor

MPQ2022 has dedicated ADC block to monitor the dual LDO output voltage and load current The ADC can be enabled via I²C, and read Reg05 to Reg08 to monitor LDO1/2 output voltage and load current.

Multipage One-Time Programmable Memory

The MPQ2022 features 2 pages of one-time programmable memory to store desired settings permanently.

Differential one-time programmable cell instead of single ended is used for long-term reliability. Data is stored on two floating gate avalanche injection metal oxide semiconductor (FAMOS), and an output comparators are used for differential reading.

The first page of the multipage one-time programmable memory has been programmed with manufacture default values.

Once the device is enabled, the default values on the first page are used to set the control parameters in the registers. If there is data on other pages of the one-time programmable memory, the newest setting is identified by an internal indicator to write registers. Refer the Register Map and Register Description sections for details.

Table 1: Fault Indicator

Fault	Registers Fault Flag	/FT Indication	Fault Actions
Thermal	**Y**	**Y**	**Hiccup or latch off**
Short to battery	**Y**	**Y**	**Hiccup or latch off**
LDO_OC	**Y**	**Y**	**No action**
LDO_OV	**Y**	**Y**	**No action**
LDO_UV	**Y**	**Y**	**No action**

I²C INTERFACE

I²C Serial Interface Description

I²C is a 2-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are “idle”. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. MPQ2022 interface is an I²C slave which will support the Fast Mode (400kHz), adding flexibility to the power supply solution. The output voltage, transition slew rate or other interesting parameters can be instantaneously controlled by I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 3).

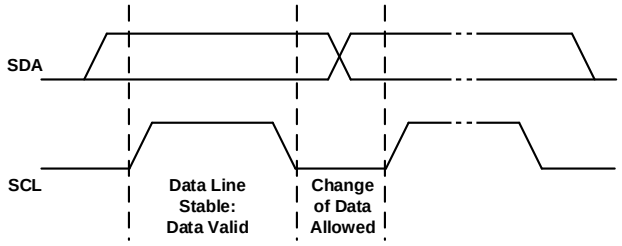


Figure 3: Bit Transfer on the I²C Bus

Start and Stop Conditions

The Start and Stop conditions are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The Start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The Stop condition is defined as the SDA signal transitioning from low to high while the SCL is high as shown in Figure 4.

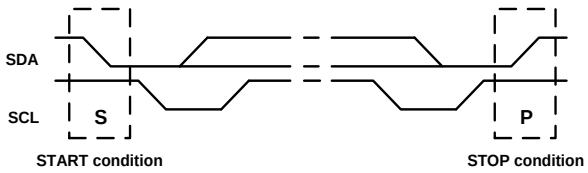


Figure 4: Start and Stop Conditions

Start and Stop conditions are generated always by the master. The bus is considered busy after the Start condition. The bus is considered free again after a minimum of 4.7µs after the Stop condition. The bus stays busy if a repeated Start (Sr) is generated instead of a Stop condition. The Start (S) and repeated Start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Data transfers follow the format shown in Figure 5. After the Start condition (S), a slave address is sent. This address is 7-bits long followed by an eighth bit, which is a data direction bit (R/W). A ‘0’ indicates a transmission (write), and a ‘1’ indicates a request for data (read). A data transfer is terminated always by a Stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated Start condition (Sr) and address another slave without first generating a stop condition.

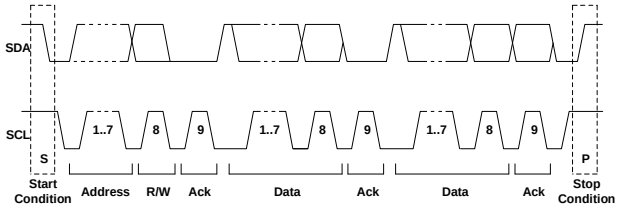


Figure 5: A Complete Data Transfer

Packet Error Checking (PEC)

The Packet Error Checking mechanism is employed to improve the communication reliability and robustness. Packet Error Checking, whenever applicable, is implemented by appending a Packet Error Code (PEC) at the end of each message transfer.

The PEC is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses and read/write bits). The PEC is appended to the message by the device that supplied the last data byte.

If PEC error occurs, I²C communication fails and is locked. Write 1 to register 0x09, bit7 to clear PEC error flag and recover I²C communication.

Write Sequence

The typical MPQ2022 write sequence requires a master's START condition, a valid slave address, a register index byte, a corresponding data byte, and ends with a PEC for a single data update.

After receipt of each byte, the MPQ2022 acknowledges by pulling the SDA line LOW during the HIGH period of a single clock pulse. A valid I²C address selects the MPQ2022. The MPQ2022 performs an update on the falling edge of the LSB byte.

Read Sequence

The typical MPQ2022 read sequence requires the five-byte long: Start with a master's START condition, then a valid slave address and followed by a register index byte. Different from the write sequence, a master's START condition comes again. And the bus direction then turns around with the re-broadcast of the slave address with bit "1" indicating a read cycle. The following fourth byte contains the data being returned by the MPQ2022. That byte value in the data byte reflects the value of the register index being queried before. Finally, the MPQ2022 sends PEC byte to end the Read Sequence.

I²C Update Sequence

The MPQ2022 requires a start condition, a valid I2C address, a register address byte, and a data byte for a single data update. After receipt of each byte, the MPQ2022 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I2C address selects the MPQ2022. The MPQ2022 performs an update on the falling edge of the LSB byte.

I²C Chip Address

The ADD pin can be used to program the I²C address through configuring the resistor value that connected between the ADD pin and ground. A 7.5μA current flows from ADD pin and generates a voltage on the ADD resistor. The MPQ2022 supports 7 addresses for up to 7 voltage rails by detecting the different voltage on ADD pin. Table 2 shows the resistor values for different I²C addresses.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by "0/1" to indicate write/read operation.

Table 2: I²C Address

Address	Resistor (kΩ,1%)	Voltage Window
21h	0	<200mV
22h	40.2	200mV – 400mV
23h	68	400mV – 600mV
24h	93.1	600mV – 800mV
25h	120	800mV – 1000mV
26h	147	1000mV – 1200mV
27h	>173 or floating	> 1200mV

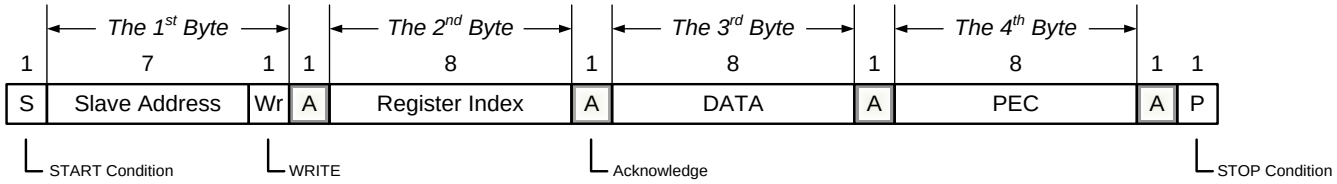


Figure 6: Write Sequence

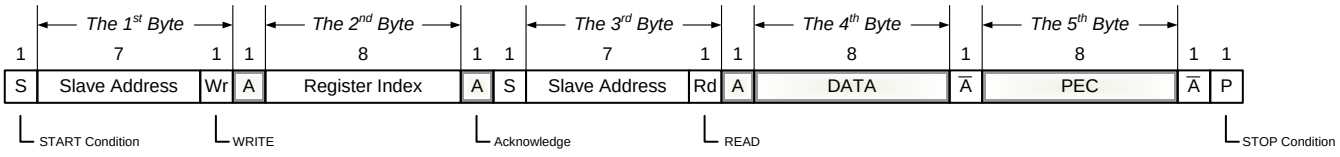


Figure 7: Read Sequence

DETAILED REGISTER BIT MAPPING

REGISTER SHORT NAME	R/W	ADD	D7	D6	D5	D4	D3	D2	D1	D0
DEVICE STATUS AND DIAGNOSTIC										
DEV_REV	R	0x00	SILLICON _INFO							
DEV_STAT	R	0x01	RSV	LDO_1 _ACTIVE	LDO_2 _ACTIVE	VOUT1_PG	VOUT2_PG	FT_ASSERT	I2C_ERR	POR
ERR _FLAG_1	R	0x02	VOUT_1_OV	VOUT_1_UV	VOUT_2_OV	VOUT_2_UV	RSV	RSV	LDO_1_StB	LDO_2_StB
ERR _FLAG_2	R	0x03	LDO_1_OC	LDO_2_OC	RSV	OT	RSV	RSV	RSV	RSV
DEV_CTRL	W/R	0x04	RSV	LDO_1_EN	LDO_2_EN	SHUTDOWN	ADC-EN	SOFT_RST	RSV	FAULT _HANDLE
MONITORING										
MON _VOUT_1	R	0x05	VOUT1_MON							
MON _VOUT_2	R	0x06	VOUT2_MON							
MON _IOUT_1	R	0x07	IOUT1_MON							
MON _IOUT_2	R	0x08	IOUT2_MON							
POWER MANAGEMENT										
SET_VOUT _1	W/R	0x09	I2C_REC	VOUT1_STEP	VOUT1_SET					
SET_VOUT _2	W/R	0x0A	POWER_SEQ	VOUT2_STEP	VOUT2_SET					
RSVD	W/R	0x0B	RSV							
RSVD	W/R	0x0C	RSV							
SET_PG_U VOV	W/R	0x0D	VOUT1_ OV_THR	VOUT1_ UV_THR	VOUT2 _OV_THR	VOUT2 _UV_THR	VOUT1_PG _H_THR	VOUT1_PG _L_THR	VOUT2_PG _H_THR	VOUT2_PG _L_THR
SET_IOUT_ LIM_1	W/R	0x0E	LDO1_TRC	LDO2_TRC	RSV	IOUT_1_OC_THR				
SET_IOUT_ LIM_2	W/R	0x0F	RSV	RSV	OC_MIN	IOUT_2_OC_THR				

REGISTER DESCRIPTION

DEV_REV *				Read only			Address: 0x00
DEVICE REVISION AND INFORMATION							POR/Soft Reset Value: N/A
D7	D6	D5	D4	D3	D2	D1	D0
SILLICON _INFO							
D[7:0]	SILLICON_INFO			Silicon information			

DEV_STAT				Read only			Address: 0x01
DEVICE STATUS							POR/Soft Reset Value: 00000000
D7	D6	D5	D4	D3	D2	D1	D0
RSV	LDO_1 _ACTIVE	LDO_2 _ACTIVE	VOUT1_PG	VOUT2_PG	FT _ASSERT	I2C_ERR	POR

D[7]	RSV	Reserved, always reads as 0
D[6]	LDO_1_ACTIVE	0: LDO 1 is NOT active
		1: LDO 1 is active
D[5]	LDO_2_ACTIVE	0: LDO 2 is NOT active
		1: LDO 2 is active
D[4]	VOUT1_PG	0: LDO 1 output voltage is NOT power good
		1: LDO 1 output voltage is power good
D[3]	VOUT2_PG	0: LDO 2 output voltage is NOT power good
		1: LDO 2 output voltage is power good
D[2]	FT_ASSERT	0: /FT pin is not asserted
		1: /FT pin is asserted (Active LOW)
D[1]	I2C_ERR	0: No I2C communication error
		1: I2C communication error occurred
D[0]	POR	0: No power on reset event
		1: Power on reset event occurred and finished

ERR_FLAG_1				Read only			Address: 0x02
DEVICE ERROR FALGS: UV OV							POR/Soft Reset Value: 00000000
D7	D6	D5	D4	D3	D2	D1	D0
VOUT_1_OV	VOUT_1_UV	VOUT_2_OV	VOUT_2_UV	VLDO_IN_OV	VLDO_IN_UV	LDO_1_StB	LDO_2_StB

D[7]	VOUT_1_OV	0: Clear to 0 when no over voltage on OUT1
		1: Over voltage detected on OUT1
D[6]	VOUT_1_UV	0: Clear to 0 when no under voltage on OUT1
		1: Under voltage detected on OUT1
D[5]	VOUT_2_OV	0: Clear to 0 when no over voltage on OUT2
		1: Over voltage detected on OUT2
D[4]	VOUT_2_UV	0: Clear to 0 when no under voltage on OUT2
		1: Under voltage detected on OUT2
D[3]	RSV	Reserved, always reads as 0
D[2]	RSV	Reserved, always reads as 0
D[1]	LDO_1_StB	0: Clear to 0 when no short-to-battery on LDO_1
		1: Short-to-battery detected on LDO_1
D[0]	LDO_2_StB	0: Clear to 0 when no short-to-battery on LDO_2
		1: Short-to-battery detected on LDO_2

ERR_FLAG_2				Read only			Address: 0x03
DEVICE ERROR FALGS: OC OT							POR/Soft Reset Value: 00000000
D7	D6	D5	D4	D3	D2	D1	D0
LDO_1_OC	LDO_2_OC	RSV	OT	RSV	RSV	RSV	RSV

D[7]	LDO_1_OC	0: Clear to 0 when no over current on OUT1
		1: Over current detected on OUT1
D[6]	LDO_2_OC	0: Clear to 0 when no over current on OUT2
		1: Over current detected on OUT2
D[5]	RSV	Reserved, always reads as 0
D[4]	OT	0: Clear to 0 when no over temperature
		1: Over temperature detected
D[3:0]	RSV	Reserved, always reads as 0

REGISTER DESCRIPTION *(continued)*

DEV_CTRL	Read and Write						Address: 0x04
DEVICE CONTROL							POR/Soft Reset Value: 01100001
D7	D6	D5	D4	D3	D2	D1	D0
RSV	LDO_1_EN	LDO_2_EN	SHUTDOWN	ADC-EN	SOFT_RST	RSV	FAULT _HANDLE

D[7]	RSV	Reserved, always reads as 0
D[6]	LDO_1_EN	0: LDO 1 is disabled 1: LDO 1 is enabled
D[5]	LDO_2_EN	0: LDO 2 is disabled 1: LDO 2 is enabled
D[4]	SHUTDOWN	0: No shutdown command 1: Device is forced shutdown
D[3]	ADC-EN	0: ADC is disable 1: ADC is enable
D[2]	SOFT_RST	0: No soft reset request 1: Soft reset is requested
D[1]	RSV	Reserved, always reads as 0
D[0]	FAULT_HANDLE	0: Latch mode 1: Auto retry mode after 100ms blanking time

MON_VOUT_1	Read only						Address: 0x05
MONITORED LDO1 OUTPUT VOLTAGE							POR/Soft Reset Value: 00000000
D7	D6	D5	D4	D3	D2	D1	D0
VOUT1_MON							
D[7:0]	VOUT1_MON	Record monitored OUT1 voltage by ADC, the value is refreshed each time read. Lsb=55mV; VOUT1_MON = D[7:0]*55mV. For example, D[7:0]=$(10100100)_2$ → $(164)_{10}$, then V_{OUT1} = 164*55mV = 9.02V.						

MON_VOUT_2	Read only						Address: 0x06
MONITORED LDO2 OUTPUT VOLTAGE							POR/Soft Reset Value: 00000000
D7	D6	D5	D4	D3	D2	D1	D0
VOUT2_MON							
D[7:0]	VOUT2_MON	Record monitored OUT2 voltage by ADC, the value is refreshed each time read. Lsb=55mV; VOUT2_MON = D[7:0]*55mV. For example, D[7:0]= $(10100100)_2$ → $(164)_{10}$, then V_{OUT2}= 164*55mV = 9.02V.						

MON_IOUT_1	Read only						Address: 0x07
MONITORED LDO1 OUTPUT CURRENT							POR/Soft Reset Value: 00000000
D7	D6	D5	D4	D3	D2	D1	D0
IOUT1_MON							
D[7:0]	IOUT1_MON	Record monitored OUT1 current by ADC, the value is refreshed each time read. Lsb=1.2mA; IOUT1_MON = D[7:0]*1.2mA. For example, D[7:0]=$(11111010)_2$ → $(250)_{10}$, then I_{OUT1}= 250*1.2mA = 300mA.						

MON_IOUT_2	Read only						Address: 0x08
MONITORED LDO2 OUTPUT CURRENT							POR/Soft Reset Value: 00000000
D7	D6	D5	D4	D3	D2	D1	D0
IOUT2_MON							
D[7:0]	IOUT2_MON	Record monitored OUT2 current by ADC, the value is refreshed each time read. Lsb=1.2mA; IOUT2_MON = D[7:0]*1.2mA. For example, D[7:0]=$(11111010)_2$ → $(250)_{10}$, then I_{OUT2}= 250*1.2mA = 300mA.						

REGISTER DESCRIPTION *(continued)*

SET_VOUT_1			Read and Write				Address: 0x09
LDO1 OUTPUT VOLTAGE SETTING							POR/Soft Reset Value: 01101000
D7	D6	D5	D4	D3	D2	D1	D0
I2C_REC	VOUT1_STEP	VOUT1_SET					
D[7]	I2C_REC	Recover I²C communication 0: default, no action 1: write '1' to recover I²C communication from locked status since PEC fault					
D[6]	VOUT1_STEP	Set OUT1 step voltage, default 200mV/step 0: 100mV 1: 200mV					
D[5:0]	VOUT1_SET	Set OUT1 voltage, Vout1=1V+ D[5:0]*step Default D[5:0]=$(101000)_2 \rightarrow (40)_{10}$, then default Vout1 = 1V+ 40*200mV = 9V					

SET_VOUT_2			Read and Write				Address: 0x0A
LDO2 OUTPUT VOLTAGE SETTING							POR/Soft Reset Value: 01101000
D7	D6	D5	D4	D3	D2	D1	D0
POWER_SEQ	VOUT2_STEP	VOUT2_SET					
D[7]	POWER_SEQ	0: OUT1 and OUT2 is powered simultaneously 1: OUT2 is delayed 100ms					
D[6]	VOUT2_STEP	Set OUT2 step voltage, default 200mV/step 0: 100mV 1: 200mV					
D[5:0]	VOUT2_SET	Set OUT2 voltage, Vout2=1V+ D[5:0]*step Default D[5:0]=$(101000)_2 \rightarrow (40)_{10}$, then default Vout1 = 1V+ 40*200mV = 9V					

SET_VPREBOOST			Read and Write				Address: 0x0B
RSVD							POR/Soft Reset Value: 01111000
D7	D6	D5	D4	D3	D2	D1	D0
RSVD							
D[7:0]	RSV	Reserved.					

SET_VPREBOOST_ON			Read and Write				Address: 0x0C
RSVD							POR/Soft Reset Value: 01001100
D7	D6	D5	D4	D3	D2	D1	D0
RSVD							
D[7:0]	RSV	Reserved.					

SET_PG_UVOV			Read and Write			Address: 0x0D	
POWER GOOD/LDO UV OV SETTINGS						POR/Soft Reset Value: 00000000	
D7	D6	D5	D4	D3	D2	D1	D0
VOUT1_OV_THR	VOUT1_UV_THR	VOUT2_OV_THR	VOUT2_UV_THR	VOUT1_PG_H_THR	VOUT1_PG_L_THR	VOUT2_PG_H_THR	VOUT2_PG_L_THR
D[7]	VOUT1_OV_THR	0:115% of set VOUT1 as over voltage threshold 1:120% of set VOUT1 as over voltage threshold					
D[6]	VOUT1_UV_THR	0:75% of set VOUT1 as under voltage threshold 1:80% of set VOUT1 as under voltage threshold					
D[5]	VOUT2_OV_THR	0:115% of set VOUT2 as over voltage threshold 1:120% of set VOUT2 as over voltage threshold					
D[4]	VOUT2_UV_THR	0:75% of set VOUT2 as under voltage threshold 1:80% of set VOUT2 as under voltage threshold					
D[3]	VOUT1_PG_H_THR	0: 105% of set voltage as the upper boundary of OUT1 PG threshold 1: 110% of set voltage as the upper boundary of OUT1 PG threshold					
D[2]	VOUT1_PG_L_THR	0: 90% of set voltage as the lower boundary of OUT1 PG threshold 1: 95% of set voltage as the lower boundary of OUT1 PG threshold					
D[1]	VOUT2_PG_H_THR	0: 105% of set voltage as the upper boundary of OUT2 PG threshold 1: 110% of set voltage as the upper boundary of OUT2 PG threshold					
D[0]	VOUT2_PG_L_THR	0: 90% of set voltage as the lower boundary of OUT2 PG threshold 1: 95% of set voltage as the lower boundary of OUT2 PG threshold					

REGISTER DESCRIPTION *(continued)*

SET_IOUT_LIM_1			Read and Write				Address: 0x0E
LDO1 CURRENT LIMIT THRESHOLD							POR/Soft Reset Value: 00010000
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO1-TRC	LDO2-TRC	RSV	IOUT_1_OC_THR				
D[7]	LDO1-TRC		0:LDO1 tracking mode disabled 1:LDO1 tracking mode enabled				
D[6]	LDO2-TRC		0:LDO2 tracking mode disabled 1:LDO2 tracking mode enabled				
D[5]	RSV		Reserved, always reads as 0				
D[4:0]	IOUT_1_OC_THR[4:0]		Set OUT1 overcurrent threshold; Lsb=6.25mA; Ilimit= D[4:0]*6.25mA+OC_MIN; OC_MIN is set by Reg0x0F[5] bit. Default D[4:0]=(10000)$_2$ → (16)$_{10}$, Ilimit = 16*6.25+300=400mA				

SET_IOUT_LIM_2			Read and Write				Address: 0x0F
LDO2 CURRENT LIMIT THRESHOLD							POR/Soft Reset Value: 00010000
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSV	RSV	OC_MIN	IOUT_2_OC_THR				
D[7:6]	RSV		Reserved				
D[5]	OC_MIN		Set minimum over current threshold for LDO1 and LDO2. Default 300mA. 0: 300mA 1: 100mA				
D[4:0]	IOUT_2_OC_THR[4:0]		Set OUT2 overcurrent threshold; Lsb=6.25mA; Ilimit= D[4:0]*6.25mA+OC_MIN; OC_MIN is set by Reg0x0F[5] bit. Default D[4:0]=(10000)$_2$ → (16)$_{10}$, Ilimit = 16*6.25+300=400mA				

APPLICATION INFORMATION

Selecting Input Capacitor

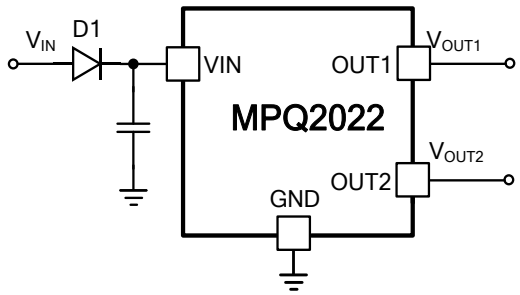
For efficient operation, place a ceramic capacitor between 1µF and 10µF of dielectric type (X5R or X7R) between the input pin and ground. Larger values in this range improve line transient response.

Selecting Output Capacitor

For stable operation, use a ceramic capacitor of type X5R or X7R between 4.7µF and 22µF. Larger values in this range improve load transient response and reduce noise. Output capacitors of other dielectric types may be used, but they are not recommended as their capacitance can deviate greatly from their rated value over temperature.

External Reverse Voltage Protection

In some situations, e.g. a backup battery is connected as MPQ2022 load, the output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is floating. Thus, the output voltage is higher than input voltage. Since the MPQ2022 PMOS pass element has a body diode, a current will conduct from the output to input and is not internally limited. It's possible that the IC will be damaged by this unlimited reverse current. To avoid this, it's recommended to place an external diode at input like below.



TYPICAL APPLICATION CIRCUITS

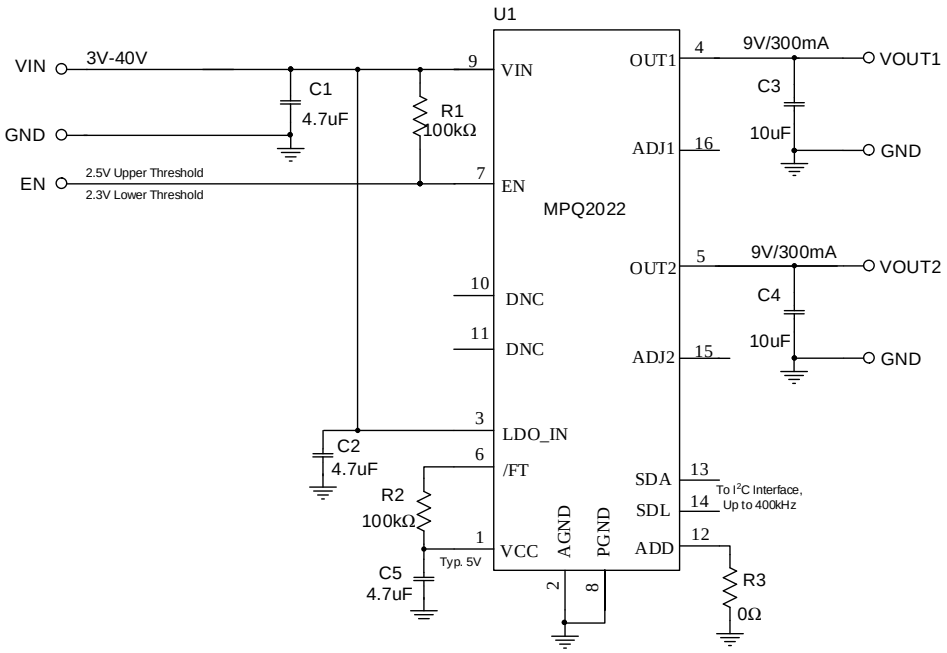
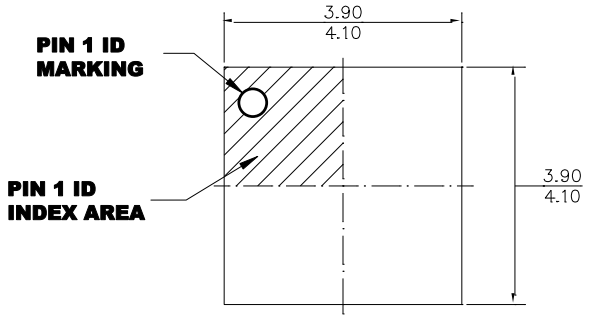


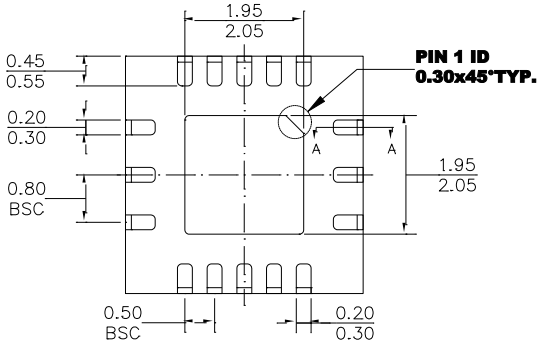
Figure 8: V_{OUT1}=9V, V_{OUT2}=9V

PACKAGE INFORMATION

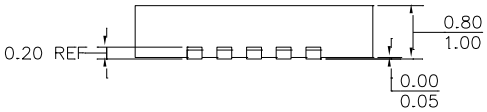
QFN-16 (4mmx4mm)
Wettable Flank



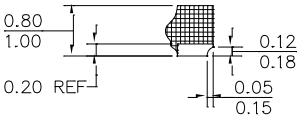
TOP VIEW



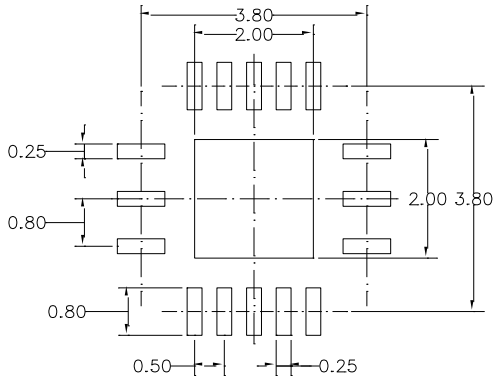
BOTTOM VIEW



SIDE VIEW



SECTION A-A

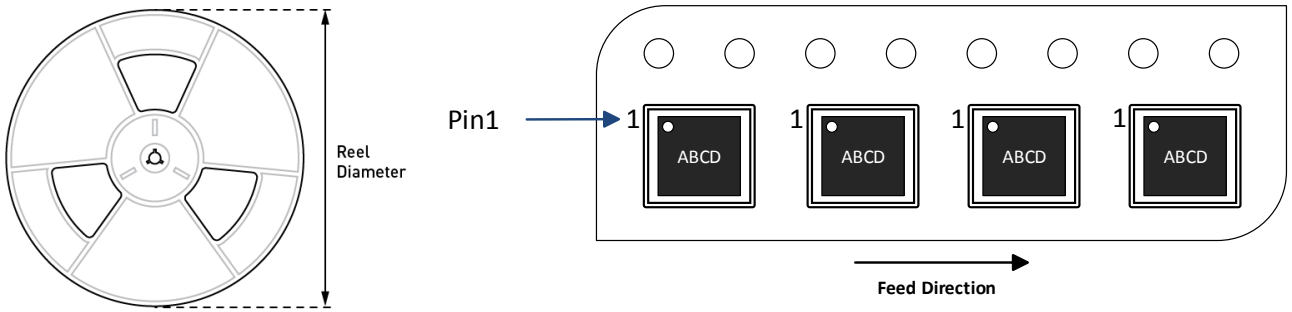


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantiy/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2022GRE-xxxx-AEC1-Z	QFN 4x4	5000	N/A	N/A	13in	12mm	8mm

单击下面可查看定价，库存，交付和生命周期等信息

>>MPS(芯源系统)