MP2762A

I²C-Controlled 6A Buck or Boost Charger with NVDC Power Managment and USB OTG for 2 Cells in Series Battery Applications

DESCRIPTION

The MP2762A is a highly integrated buck or boost charger IC with narrow voltage DC (NVDC) power path management and USB On-the-Go (OTG) for battery packs with two cells in series. All power MOSFETs are integrated to provide a compact system solution size.

The IC can accept a wide range of input voltages for charging, with a maximum of 21V. The device has two operating modes during the charging process: boost charging mode when the input voltage is below 5.75V, and buck charging mode when the input voltage exceeds 8.5V.

With the I²C interface, the MP2762A can be flexibly configured to set the parameters in both charging mode and OTG mode. Parameters include the input current limit, input voltage limit, charging current, battery-full voltage, and safety charge timer. It can also provide the operation status through status and fault registers.

To guarantee safe operation, the IC limits the die temperature to a preset value of 120°C. Other safety features include input over-voltage protection (OVP), battery OVP, system OVP, thermal shutdown, battery temperature protection, and a configured timer to prevent prolonged charging of a dead battery.

To comply with IMVP8 specifications, the IC provides three analog output pins for system power (PSYS), input current (IAM), and battery current (IBM). It also has a processor hot indication pin ($\overline{\text{PROCHOT}}$) for system power control.

The NVDC power path management regulates the system voltage within a narrow DC range to provide an optimized system bus voltage for the rails at the system bus. With this feature, the system can continue operating even when the battery is completely depleted or removed.

The MP2762A is available in a QFN-30 (4mmx5mm) package.

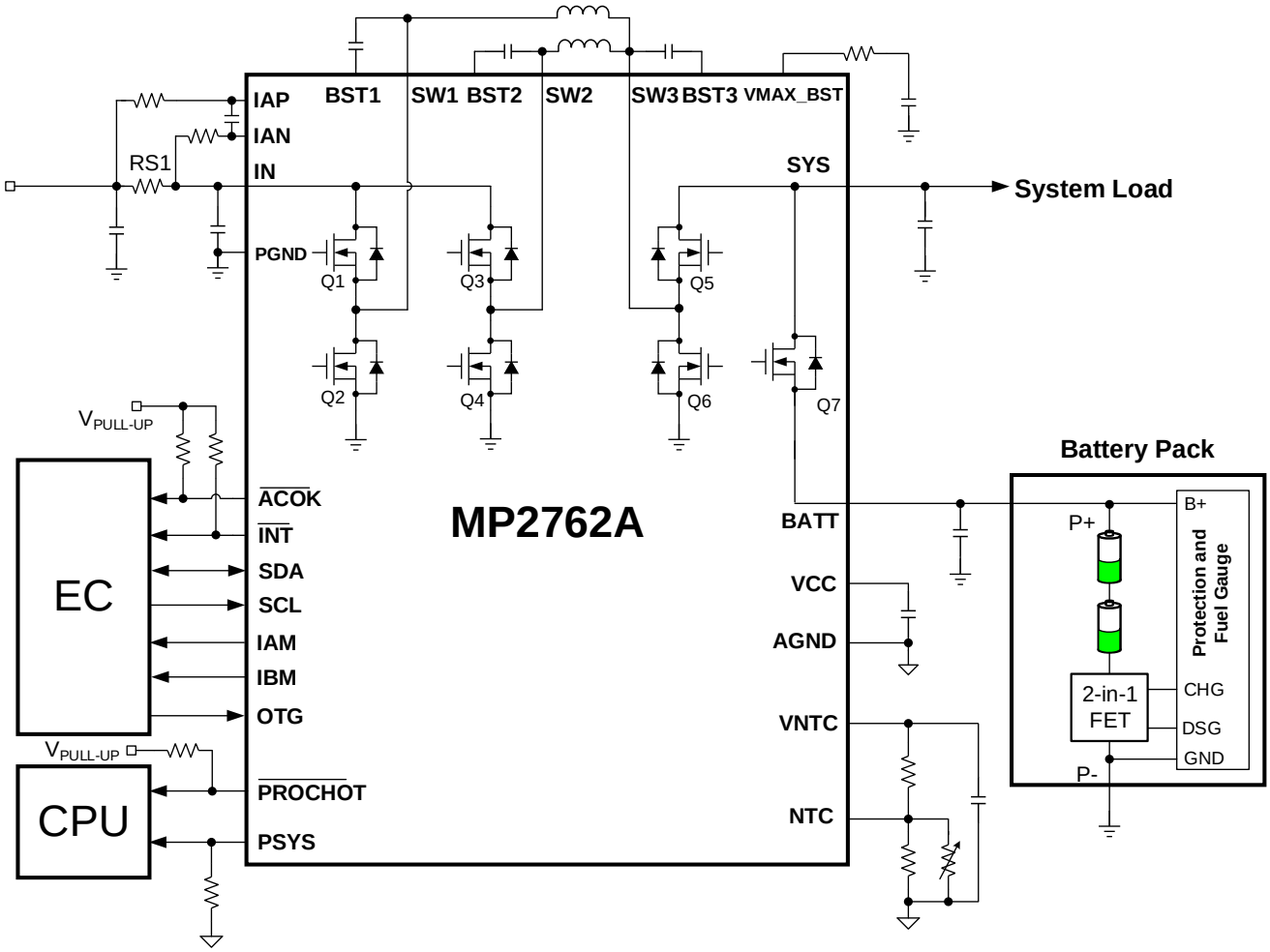
FEATURES

- Buck or Boost Charger for Battery Packs with Two Cells in Series
- NVDC Power Management
- All MOSFETs Integrated
- 4V to 21V Operation Voltage Range
- Up to 28V (20ns) Sustainable Input Voltage
- Dual-Phase Interleaving in Buck Charging Mode
- Configurable Input Voltage Limit
- Up to 6A Configurable Input Current Limit
- Up to 6A Configurable Charge Current
- Configurable Battery-Full Voltage Up to 9V
- System Power Indication via PSYS Pin
- Input Current and Battery Current Monitoring via IAM and IBM Pins
- Input Over-Voltage Protection (OVP)
- Battery Temperature Protection
- Battery Over-Voltage Protection (OVP)
- System Over-Voltage Protection (OVP)
- Configurable Safety Charge Timer
- Thermal Regulation and Thermal Shutdown
- 600kHz, 800kHz, and 1MHz Configurable Switching Frequency for Each Phase
- Input Power Source Status Indication Pin
- I²C Interface to Support Flexible Parameter Control
- Comprehensive Fault and Status Reporting in Register
- Up to 5V/3A USB On-the-Go (OTG)
- Configurable Output Current Limit OTG Mode
- Short-Circuit Protection (SCP) in OTG Mode
- Available in a QFN-30 (4mmx5mm) Package

APPLICATIONS

- Smartphones with Two Cells in Series
- Bluetooth Speakers
- Portable Gimbals

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2762AGV-xxxx**	QFN-30 (4mmx5mm)	*See Below*	1
EVKT-MP2762A	Evaluation Kit		

* For Tape & Reel, add suffix –Z (e.g. MP2762AGV-xxxx–Z).

** "xxxx" is the configuration code identifier for the register settings. For the default case, the number is "-0000." Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "-0000" code.

TOP MARKING

MPSYWW

M2762A

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M2762A: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-MP2762A

EVKT-MP2762A kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2762A-V-00A	MP2762A evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

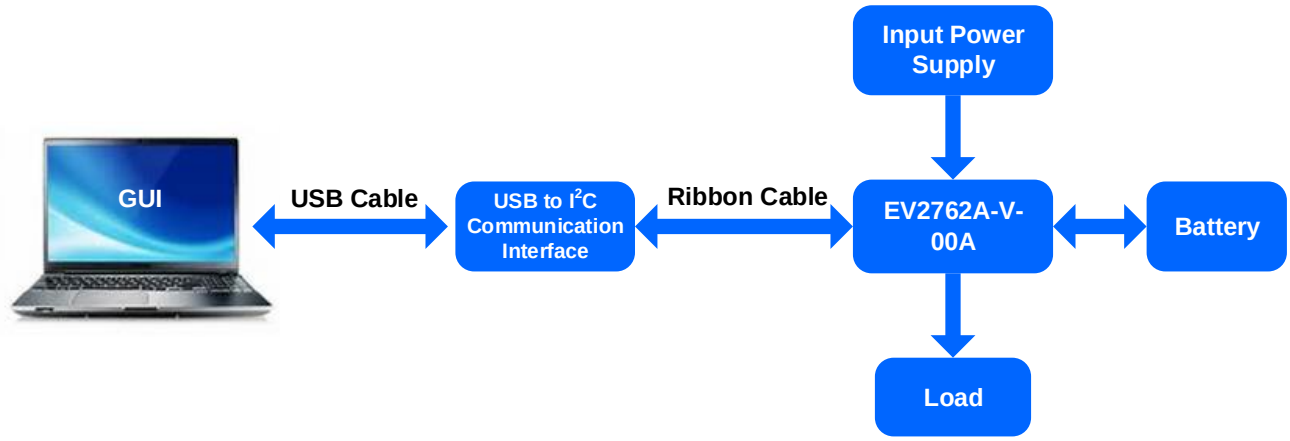
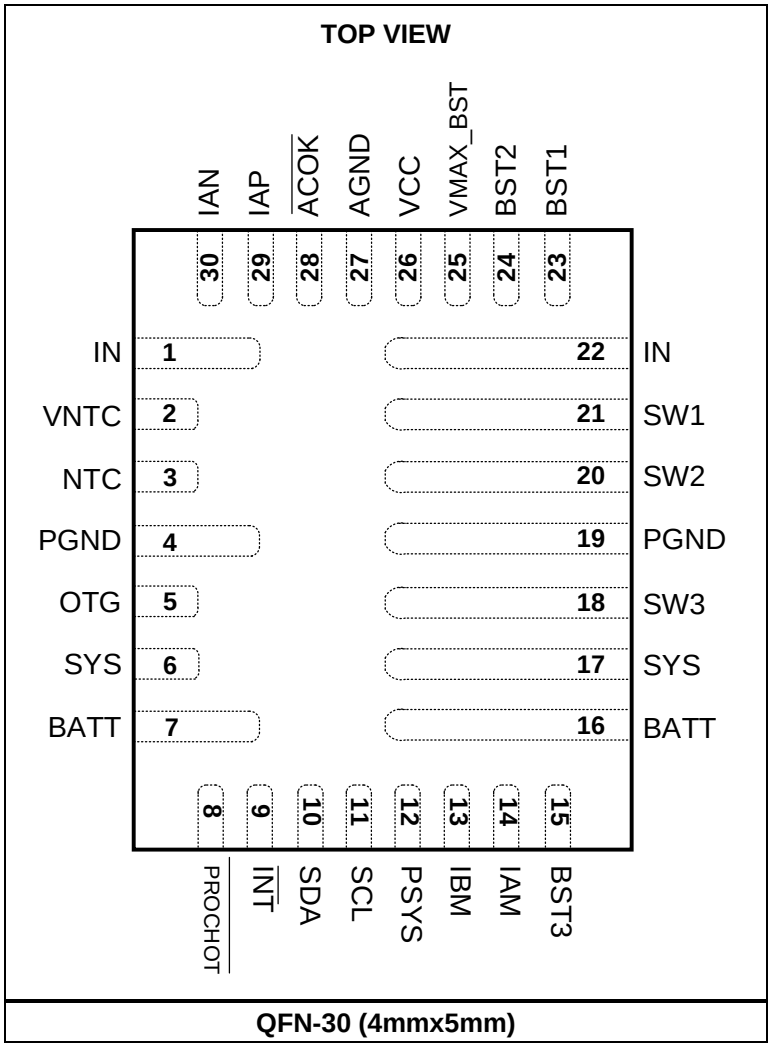


Figure 1: EVKT-MP2762A Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-30 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 22	IN	**Power input pin.** IN is the IC's power input from either an adapter or USB.
2	VNTC/ CMOUT	**NTC network pull-up voltage.** Pull-up voltage of the NTC comparator resistor divider for both the feedback and the reference. This pin can be also configured as an independent comparator output via the I²C interface.
3	NTC/ BATDET	**Negative temperature coefficient (NTC) thermistor input.** Connect a negative temperature coefficient thermistor from NTC to AGND. Program the hot and cold temperature window with a resistor divider from VNTC to NTC to AGND. Charging is suspended when NTC is out of its range. This pin also can be configured for the battery detection terminal by the I²C interface.
4, 19	PGND	**Power ground.**
5	OTG/ CMIN	**USB On-the-Go (OTG) enable control.** This pin can also be configured as the independent comparator input pin via the I²C interface. OTG is enabled via the internal register bit when this pin is configured to CMIN.
6, 17	SYS	**System output.** Connect a 5 x 22µF ceramic capacitor from SYS to PGND, and place it as close as possible to the IC.
7, 16	BATT	**Battery positive terminal.** Connect a 2 x 22µF ceramic capacitor from BATT to PGND, and place it as close as possible to the IC.
8	$\overline{\text{PROCHOT}}$	**Processor hot interrupt output.** This pin is an open-drain structure. It is pulled to AGND when the PROCHOT signal asserts, and floats when a PROCHOT event is not occurring. This pin must be pulled up externally.
9	$\overline{\text{INT}}$	**Open-drain interrupt output.** The $\overline{\text{INT}}$ pin can send the charging status and fault interruptions to the host. It must be pulled up externally.
10	SDA	**I²C interface data line**. Connect SDA to the logic rail through a 10kΩ resistor.
11	SCL	**I²C interface clock line**. Connect SCL to the logic rail through a 10kΩ resistor.
12	PSYS	**System power indication pin.** This pin outputs a current source that is proportional to the total system power.
13	IBM	**Battery current-sense output.** IBM outputs a voltage that is proportional to the battery charge current or battery discharger current.
14	IAM	**Input current-sense output.** IAM outputs a voltage that is proportional to the input current.
15	BST3	**Bootstrap for boost phase**. Connect a 470nF bootstrap capacitor between the BST3 and SW3 pins to form a floating supply across the power switch driver. This drives the power MOSFET's gate above the supply voltage.
18	SW3	**Boost phase switching node.**
20	SW2	**Buck phase 2 switching node.**
21	SW1	**Buck phase 1 switching node.**
23	BST1	**Bootstrap for buck phase 1**. Connect a 470nF bootstrap capacitor between the BST1 and SW1 pins to form a floating supply across the power switch driver. This drives the power MOSFET's gate above the supply voltage.
24	BST2	**Bootstrap for buck phase 2**. Connect a 470nF bootstrap capacitor between the BST2 and SW2 pins to form a floating supply across the power switch driver. This drives the power MOSFET's gate above the supply voltage.
25	VMAX_BST	**Charge pump output.** Connect a 100nF ceramic capacitor in series with a 100Ω resistor from VMAX_BST to PGND, and place it as close as possible to the IC.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
26	VCC	**VCC LDO output.** VCC can provide 3.6V/50mA for internal circuits, as well as the pull-up voltage for the open-drain pin. Connect a 10μF ceramic capacitor from VCC to AGND, and place it as close as possible to the IC.
27	AGND	**Analog ground.**
28	$\overline{\text{ACOK}}$	**Input power present indication.** This pin is an open-drain structure that must be pulled up externally.
29	IAP	**Input current-sense positive terminal.**
30	IAN	**Input current-sense negative terminal.**

ABSOLUTE MAXIMUM RATINGS (1)

IN, IAN, IAP to PGND (20ns) .....-0.3V to +28V
IN, IAN, IAP to PGND (DC) .....-0.3V to +26V
SYS to PGND .....-0.3V to +24V
VMAX_BST to PGND .....0V to 26V
BATT to PGND .....-0.3V to +24V
SW1/SW2 to PGND (20ns) .....-2V to +28V
SW1/SW2 to PGND (DC) .....-0.3V to +24V
SW3 to PGND.....-0.3V to +24V
BST1 to PGND .....SW1 to SW1 + 5V
BST2 to PGND .....SW2 to SW2 + 5V
BST3 to PGND .....SW3 to SW3 + 5V
All other pins to AGND.....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2)
..... 3.29W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 21V
Input current.....Up to 6A
Charge current.....Up to 6A
Discharge current via battery FET (DC)
.....Up to 14A
Battery voltage.....Up to 9V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-30 (4mmx5mm).....	38	8....	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 5.0V, V_{BATT} = 7.4V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input under-voltage lockout threshold	V_{IN_UVLO}	V_{IN} falling	3.45	3.68	3.87	V
Input under-voltage lockout hysteresis		V_{IN} rising		350		mV
Input under-voltage lockout recovery deglitch time		V_{IN} rising		30		ms
V_{IN} power-on reset (POR)	V_{IN_POR}	V_{IN} rising		3.17		V
V_{IN} POR hysteresis		V_{IN} falling		620		mV
Input over-voltage lockout threshold	V_{IN_OVLO}	V_{IN} rising	23	24	25	V
Input over-voltage lockout hysteresis		V_{IN} falling	1.55	1.66	1.78	V
DC/DC Converter						
Input shutdown current	I_{SHDN}	V_{IN} = 5V, Q1–Q6 are off			9.5	mA
		V_{IN} = 20V, Q1–Q6 are off			9.5	mA
VCC LDO output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 10mA	3.4	3.6	3.73	V
VCC LDO current limit	I_{VCC}	V_{IN} = 5V, V_{BATT} = 7.8V	50			mA
IN to SW1 N-channel MOSFET (Q1) on resistance	R_{ON_Q1}			16		mΩ
SW1 to PGND N-channel MOSFET (Q2) on resistance	R_{ON_Q2}			16		mΩ
IN to SW2 N-channel MOSFET (Q3) on resistance	R_{ON_Q3}			16		mΩ
SW2 to PGND N-channel MOSFET (Q4) on resistance	R_{ON_Q4}			16		mΩ
SW3 to SYS N-channel MOSFET (Q5) on resistance	R_{ON_Q5}			6		mΩ
SW3 to PGND N-channel MOSFET (Q6) on resistance	R_{ON_R6}			16		mΩ
SYS to BATT N-channel MOSFET (Q7) on resistance	R_{ON_Q7}			11		mΩ
Peak current limit for high-side N-channel MOSFET (Q1, Q3)	I_{HS_PK1}	Buck charging mode		8.3		A
Valley current limit for low-side N-channel MOSFET (Q2, Q4)	I_{LS_VL1}	Buck charging mode		6.5		A
Peak current limit for low-side N-channel MOSFET (Q6)	I_{LS_PK1}	Boost charging mode		10.2		A
Valley current limit for high-side N-channel MOSFET (Q5)	I_{HS_VL1}	Boost charging mode		7.8		A
Peak current limit for high-side N-channel MOSFET (Q5)	I_{HS_PK2}	Buck mode, OTG		8.2		A

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5.0V, V_{BATT} = 7.4V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Valley current limit for low-side N-channel MOSFET (Q6)	I_{LS_VL2}	Buck mode, OTG		9.1		A
Peak current limit for low-side N-channel MOSFET (Q2, Q4)	I_{LS_PK2}	Boost mode, OTG		6.5		A
Valley current limit for high-side N-channel MOSFET (Q1, Q3)	I_{HS_VL2}	Boost mode, OTG		8.1		A
Battery tracking regulation voltage	V_{TRACK}		25	100	230	mV
Minimum system regulation voltage	$V_{SYS\_REG\_MIN}$	REG07H, bits[5:4] = 01	6.87	7	7.11	V
Operating frequency	f_{SW}	REG0BH, bits[4:3] = 00		600		kHz
		REG0BH, bits[4:3] = 01		800		
		REG0BH, bits[4:3] = 10		1000		
System short circuit entry threshold		Boost charge, V_{SYS} falling, compare to V_{IN}	30	168	320	mV
System short circuit exit threshold		Boost charge, V_{SYS} rising, compare to V_{IN}	130	314	500	
Battery Charger						
Battery charge voltage regulation	V_{BATT_REG}	Depends on the I^2C setting, default (REG04H, bits[6:1] = 100111): 8.4V	8.337	8.4	8.463	V
Fast charge current	I_{CC}	I_{CC} = 6A, REG02H, bits[6:0] = 1111000	5.6	6	6.5	A
		I_{CC} = 3A, REG02H, bits[6:0] = 0111100	2.8	3	3.3	A
		I_{CC} = 2A, REG02H, bits[6:0] = 0101000	1.85	2	2.2	A
		I_{CC} = 1A, REG02H, bits[6:0] = 0010100	0.91	1	1.13	A
		I_{CC} = 0.5A, REG02H, bits[6:0] = 0001010	0.44	0.5	0.6	A
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	3.92	4	4.25	V
Trickle charge to pre-charge threshold hysteresis		V_{BATT} falling	450	550	650	mV
Trickle charge current	I_{TC}	V_{BATT} = 1V	60	100	190	mA
		V_{BATT} = 3V	130	188	240	mA
Pre-charge to fast charge rising threshold	V_{BATT_PRE}	REG07H, bits[5:4] = 01	6.87	7.0	7.11	V
		REG07H, bits[5:4] = 11	7.28	7.4	7.52	V
Pre-charge to fast charge falling threshold		REG07H, bits[5:4] = 01	6.66	6.8	6.9	V
		REG07H, bits[5:4] = 11	7.06	7.2	7.31	V

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5.0V, V_{BATT} = 7.4V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pre-charge current	I_{PRE}	V_{BATT} = 5V, REG03H, bits[7:4] = 0010	120	180	240	mA
		V_{BATT} = 5V, REG03, bits[7:4] = 0101	170	240	310	mA
		V_{BATT} = 5V, REG03H, bits[7:4] = 1010	400	540	720	mA
		V_{BATT} = 5V, REG03H, bits[7:4] = 1100	480	660	920	mA
		V_{BATT} = 5V, REG03H, bits[7:4] = 1111	600	840	1230	mA
Termination current	I_{TERM}	REG03H, bits[3:0] = 0001	30	145	280	mA
		REG03H, bits[3:0] = 0100	280	435	600	mA
		REG03H, bits[3:0] = 1111	1.3	1.5	1.75	A
Auto-recharge battery voltage threshold	V_{RECH}	Below the battery full voltage, REG04H, bit[0] = 1	150	210	270	mV
Charge termination deglitch time	t_{TERM_DGL}			1.7		sec
Battery over-voltage threshold	V_{BATT_OVP}	V_{BATT} rising, compare to V_{BATT_REG}		320		mV
Battery over-voltage threshold hysteresis				210		mV
Virtual diode entry threshold		V_{SYS} falling, V_{BATT} - V_{SYS}		25		mV
Virtual diode quit threshold		V_{SYS} rising, V_{SYS} - V_{BATT}		30		mV
Ideal diode forward voltage in supplement mode	V_{FWD}	10mA discharge current		30		mV
Battery over-current protection in discharge mode	I_{DSCHG_OC}	V_{IN} = 0V, V_{BATT} = 7.6V, OTG disabled, I_{SYS} rising	9			A
Input Voltage and Input Current Regulation						
Input current limit	I_{IN_LIM1}	REG00H, bits[6:0] = 0001010	410	470	530	mA
		REG00H, bits[6:0] = 0011110	1.4	1.49	1.57	A
		REG00H, bits[6:0] = 0111100	2.85	3	3.15	A
Input voltage clamp limit threshold	V_{IN_MIN}	REG01H, bits[7:0] = 00101101	4.28	4.5	4.72	V
		REG01H, bits[7:0] = 01010101	8.25	8.5	8.73	
		REG01H, bits[7:0] = 10010001	14.1	14.5	14.9	
Battery Temperature Protection (NTC JEITA)						
NTC low-temp rising voltage threshold	V_{COLD}	NTC pin voltage rising as a percentage of V_{NTC}	69	71.1	73.5	%

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5.0V, V_{BATT} = 7.4V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
NTC low-temp threshold hysteresis		NTC pin voltage falling		0.9		%
NTC cool-temp rising voltage threshold	V_{COOL}	NTC pin voltage rising as percentage of V_{NTC}, REG0AH, bits[1:0] = 01	66.5	68.9	71.5	%
NTC cool-temp threshold hysteresis		NTC pin voltage falling		1.3		%
NTC warm-temp falling voltage threshold	V_{WARM}	NTC pin voltage falling as percentage of V_{NTC}, REG0AH, bits[3:2] = 01	54	56.1	58.5	%
NTC warm-temp threshold hysteresis		NTC pin voltage rising		1.2		%
NTC hot-temp falling voltage threshold	V_{HOT}	NTC pin voltage falling as percentage of V_{NTC}	46	48.3	50.5	%
NTC hot-temp threshold hysteresis		NTC pin voltage rising		1.4		%
Thermal Regulation and Protection						
Thermal shutdown rising threshold (5)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (5)		T_J falling		20		°C
Thermal regulation point (5)	T_{J_REG}	Pre-charge stage, REG05H, bits[1:0] = 11		120		°C
Battery-Only Mode						
Battery leakage current	I_{BATT_Q}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, BATTFET on, REG0BH bits[1:0] = 00 to disable PROCHOT and PSYS/ADC functionality		40	60	μA
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, BATTFET on, REG0BH bits[1:0] = 01 to disable PSYS /ADC but enable PROCHOT functionality			490	
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, BATTFET on, REG0BH, bits[1:0] = 11 to enable both PSYS/ADC and PROCHOT functionality			2750	
Battery operation UVLO	V_{BATT_UVLO}	V_{BATT} falling		5.2		V
Battery operation UVLO hysteresis		V_{BATT} rising		560		mV
OTG Operation						
OTG short-circuit entry threshold		V_{IN} falling, compare to V_{SYS}	40	177	340	mV
OTG short-circuit exit threshold		V_{IN} rising, compare to V_{SYS}	160	335	520	mV

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5.0V, V_{BATT} = 7.4V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OTG over-voltage protection threshold	V_{OTG_OVP}	V_{BATT} = 7.4V, V_{IN_OTG} rising, as a percentage of OTG voltage setting, REG0DH, bits[5:4] = 00		125		%
OTG over-voltage protection threshold hysteresis		V_{IN_OTG} falling, as a percentage of OTG voltage setting		7.5		%
OTG output voltage	V_{IN_OTG}	I_{OTG} = 0A, REG06H, bits [6:0] = 0000111		5.1		V
OTG output voltage accuracy		As a percentage of V_{IN_OTG}, I_{OTG} = 0A	-2		+2	%
OTG under-voltage protection threshold	V_{OTG_UV}	V_{BATT} = 7.4V, V_{IN_OTG} falling, as a percentage of OTG voltage setting, REG0DH, bits[3:2] = 00		75		%
OTG under-voltage protection threshold hysteresis		V_{IN_OTG} rising, as a percentage of OTG voltage setting		7.5		%
OTG output current limit	I_{OLIM}	REG07H, bits[3:0] = 0110, V_{BATT} = 7.4V	1.075	1.43	1.735	A
		REG07H, bits[3:0] = 1100, V_{BATT} = 7.4V	2.59	2.93	3.27	A
IMVP Requirement						
Monitoring Function						
Input current indication gain	V_{IAM}	RS1 = 10mΩ		250		mV/A
Input current indication offset				100		mV
Battery current indication gain	V_{IBM}	Charging		125		mV/A
		Discharging		62.5		mV/A
Battery current indication offset		Charging		50		mV
		Discharging, I_{BATT} = 200mA		6.5		mV
System Power Monitor						
System power indicator full scale		256 steps		100		µA
Processor HOT Interruption						
System UV PROCHOT		REG0DH, bits[1:0] = 01, V_{SYS} falling		5.84		V
System UV PROCHOT hysteresis				160		mV
Battery discharge OC PROCHOT		REG0CH, bits[7:5] = 110, I_{BATT} increasing		12		A
Discharge OC PROCHOT deglitch time				25		µs
Input current OC PROCHOT		REG12H, bits[6:3] = 1010, I_{IN} increasing		8.2		A

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5.0V, V_{BATT} = 7.4V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
General Comparator						
General comparator reference		REG0CH, bit[0] = 0		1.22		V
General comparator hysteresis			40	110	180	mV
General comparator output open-drain MOSFET resistance				200		Ω
Battery Missing Detection						
Battery absent threshold				1.6		V
Battery absent hysteresis				10		mV
ADC Performance						
Sample rate				50		kHz
ADC resolution				10		bits
ADC reference				1.6		V
Logic I/O Pin Characteristics						
Logic low voltage threshold	V_L				0.4	V
Logic high voltage threshold	V_H		1.3			V
I²C Interface (SDA, SCL)						
Input high threshold level		V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level		V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level		I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Timer Specifications						
Digital clock	f_{DIG}	VCC LDO enabled	4.5	5	5.5	MHz
Watchdog timer	t_{WDT}	REG09H, bits[5:4] = 11		160		sec
Short circuit recovery time				25.6		ms
Trickle charge and pre-charge timer				1		hrs
Total charger timer	t_{TMR}			20		hrs

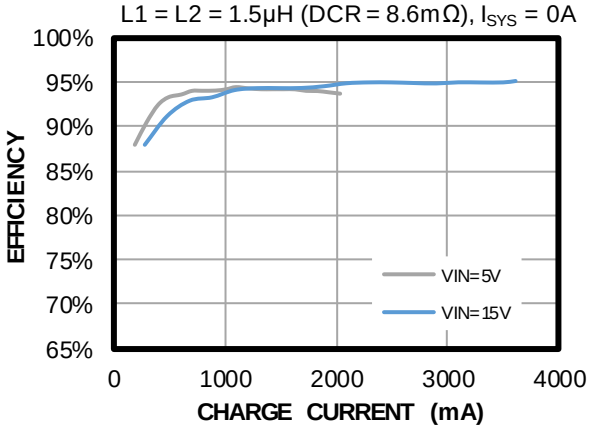
Note:

5) Guaranteed by design.

TYPICAL CHARACTERISTICS

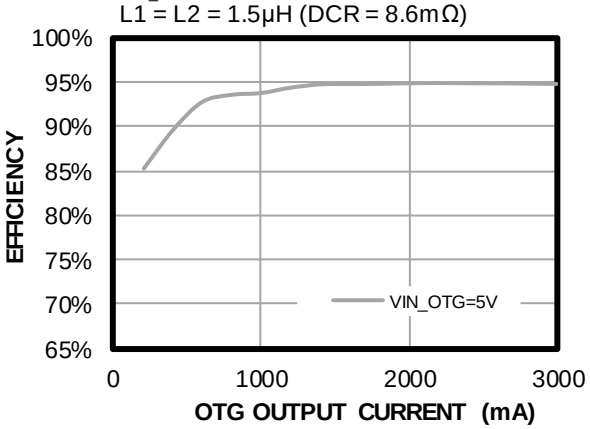
Charge Efficiency

V_{IN} = 5V/15V, V_{BATT} = 8V, f_{SW} = 600kHz, L1 = L2 = 1.5µH (DCR = 8.6mΩ), I_{SYS} = 0A



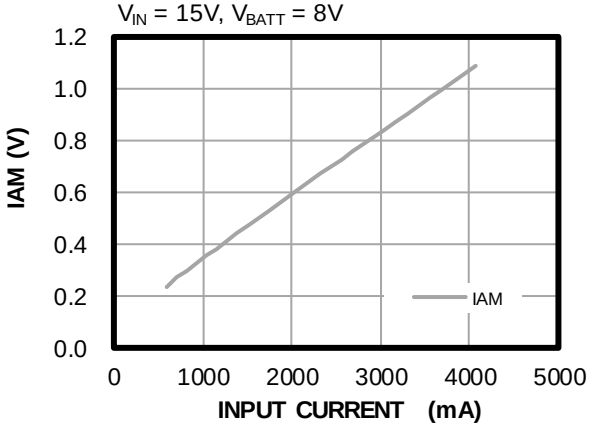
OTG Efficiency

V_{IN_OTG} = 5V, V_{BATT} = 8V, f_{SW} = 600kHz, L1 = L2 = 1.5µH (DCR = 8.6mΩ)



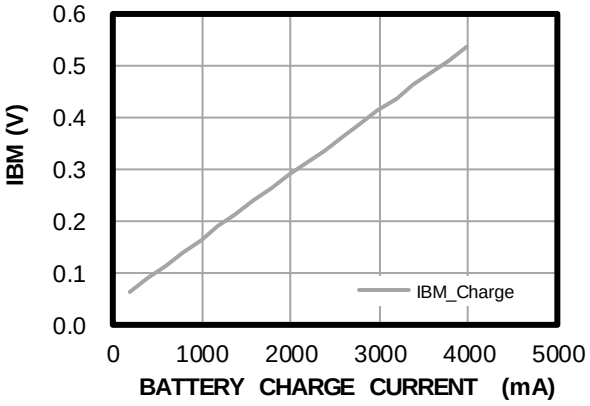
IAM vs. Input Current in Charge Mode

V_{IN} = 15V, V_{BATT} = 8V



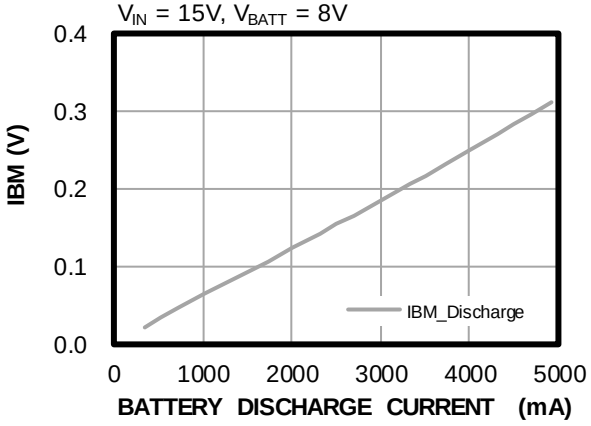
IBM vs. Battery Charge Current

V_{IN} = 15V, V_{BATT} = 8V



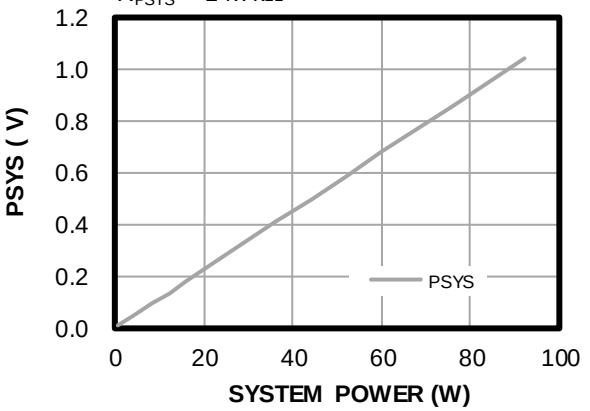
IBM vs. Battery Discharge Current

V_{IN} = 15V, V_{BATT} = 8V



PSYS vs. System Power

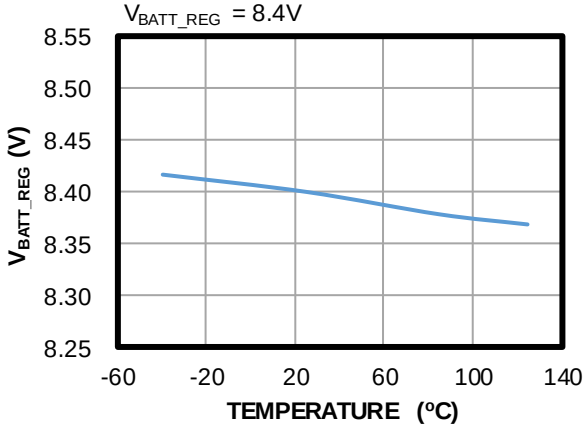
V_{IN} = 20V, V_{BATT} = 7.4V, I_{CHG} = 2A, R_{PSYS} = 14.7kΩ



TYPICAL CHARACTERISTICS *(continued)*

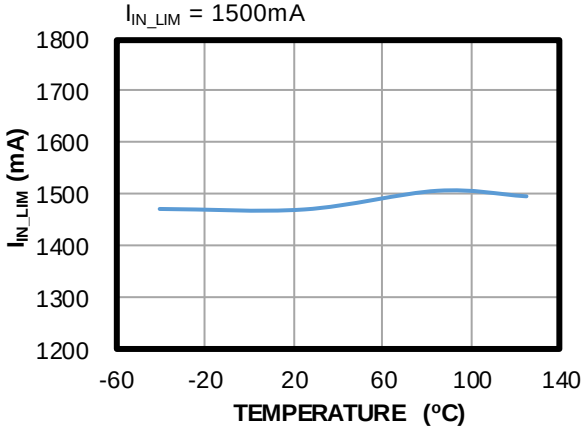
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 8.4V



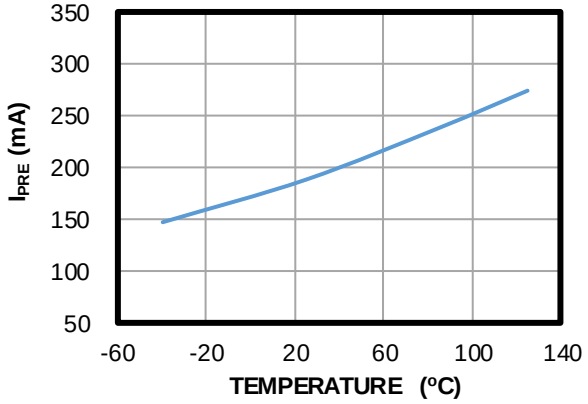
Input Current Limit vs. Temperature

I_{IN_LIM} = 1500mA



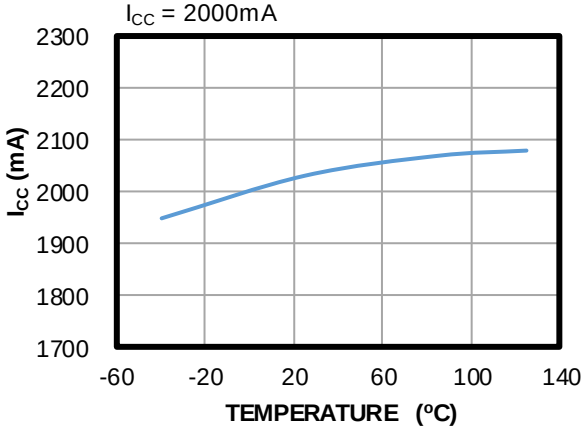
Pre-Charge Current vs. Temperature

I_{PRE} = 180mA



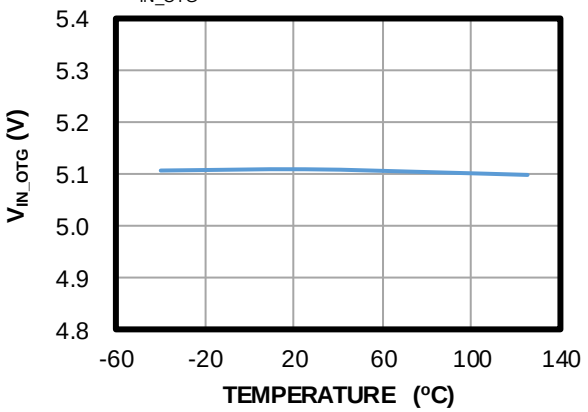
Fast Charge Current vs. Temperature

I_{CC} = 2000mA



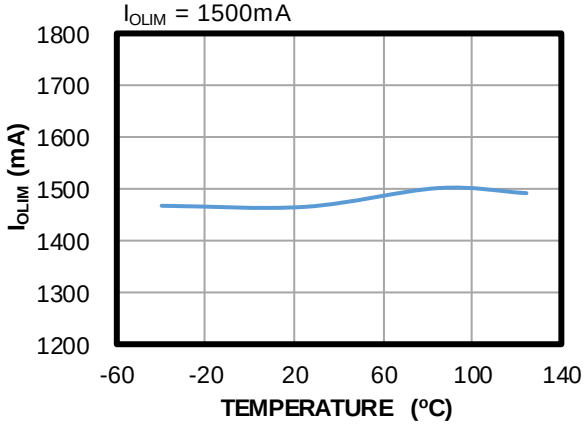
OTG Output Voltage vs. Temperature

V_{IN_OTG} = 5.1V



OTG Output Current Limit vs. Temperature

I_{OLIM} = 1500mA

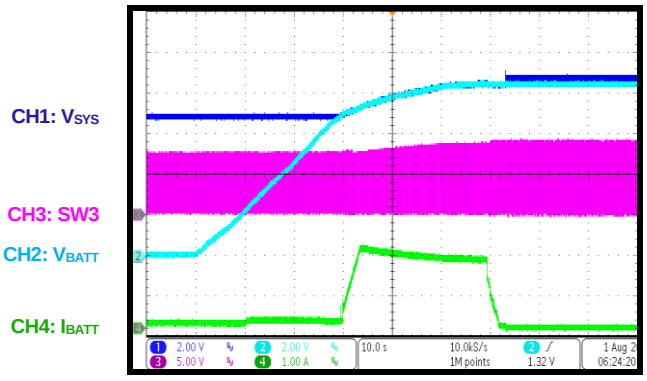


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L1 = L2 = 1.5µH, T_A = 25°C, unless otherwise noted.

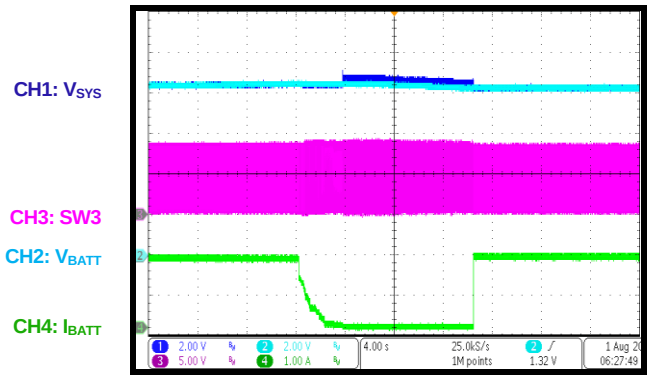
Battery Charge Curve

V_{IN} = 5V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



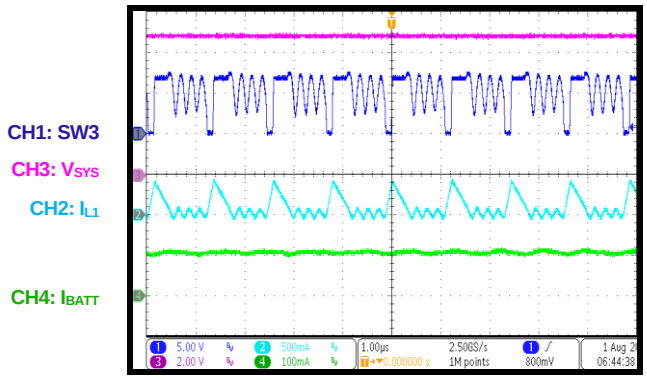
Auto-Recharge

V_{IN} = 5V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



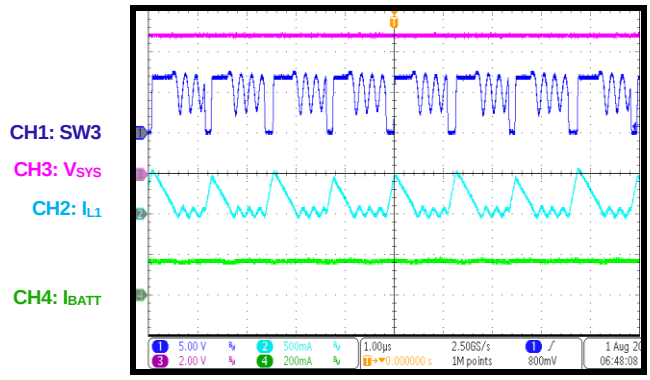
TC Charge Steady State

V_{IN} = 5V, V_{BATT} = 1V



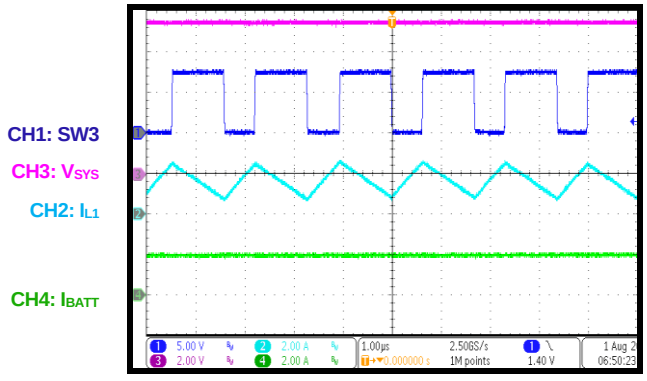
Pre-Charge Steady State

V_{IN} = 5V, V_{BATT} = 5.8V



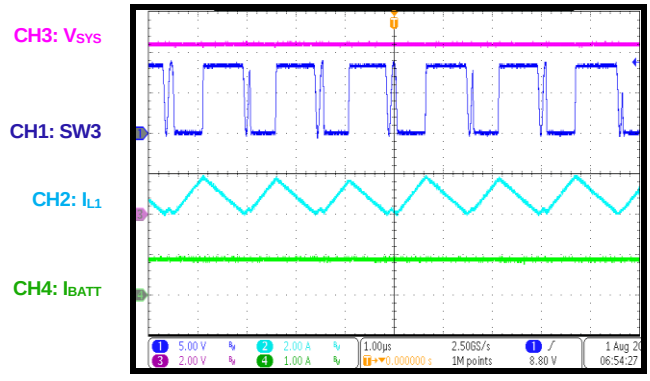
CC Charge Steady State

V_{IN} = 5V, V_{BATT} = 7.4V



CV Charge Steady State

V_{IN} = 5V, V_{BATT} = 8.4V

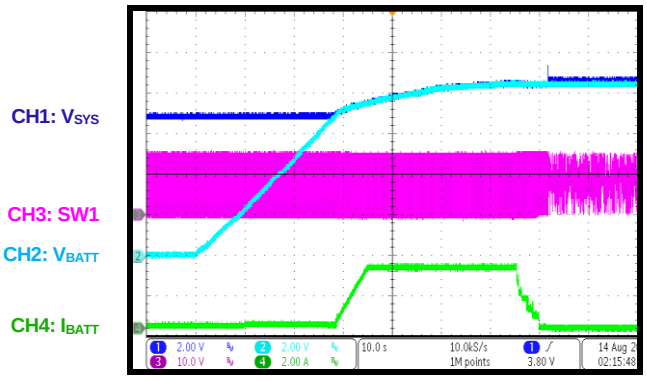


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L1 = L2 = 1.5µH, T_A = 25°C, unless otherwise noted.

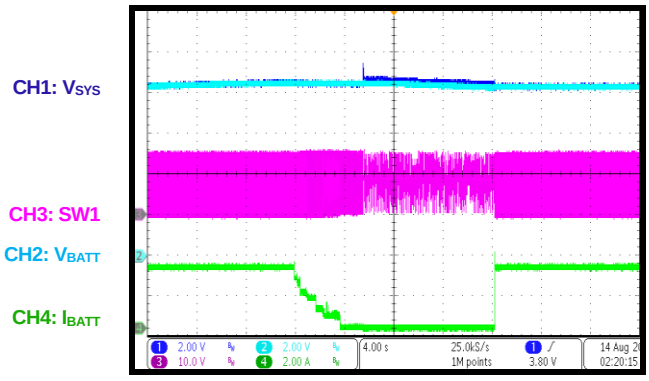
Battery Charge Curve

V_{IN} = 15V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



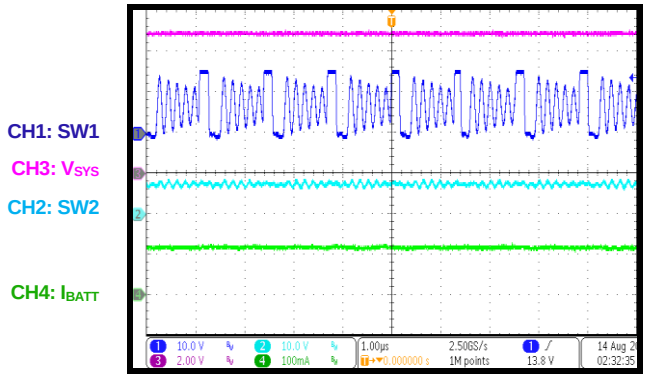
Auto-Recharge

V_{IN} = 15V, V_{BATT_PRE} = 6.8V, V_{BATT_REG} = 8.4V



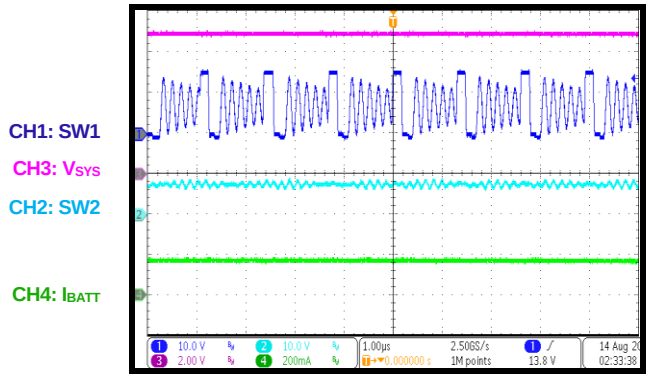
TC Charge Steady State

V_{IN} = 15V, V_{BATT} = 1V



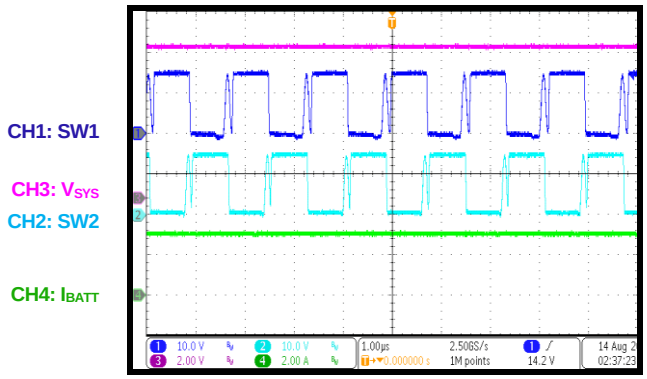
Pre-Charge Steady State

V_{IN} = 15V, V_{BATT} = 5.8V



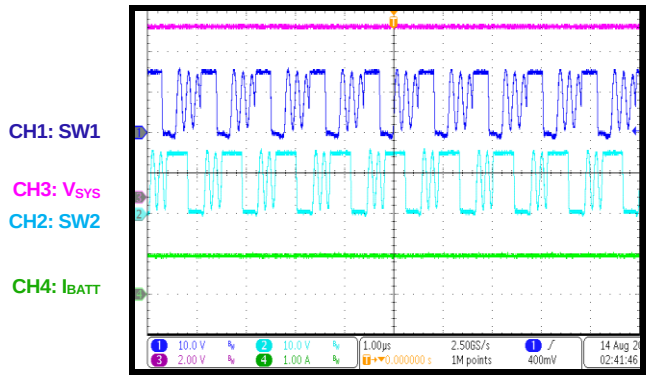
CC Charge Steady State

V_{IN} = 15V, V_{BATT} = 7.4V



CV Charge Steady State

V_{IN} = 15V, V_{BATT} = 8.4V

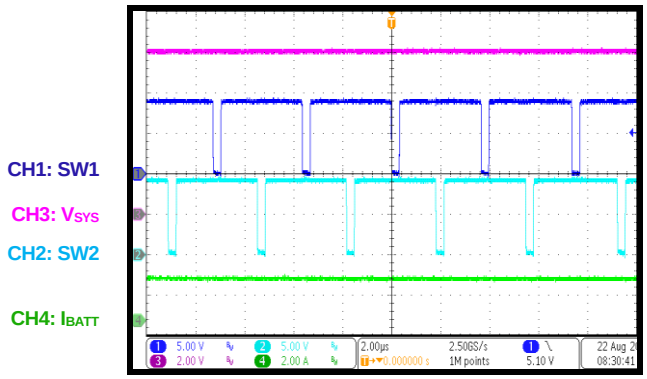


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L1 = L2 = 1.5µH, T_A = 25°C, unless otherwise noted.

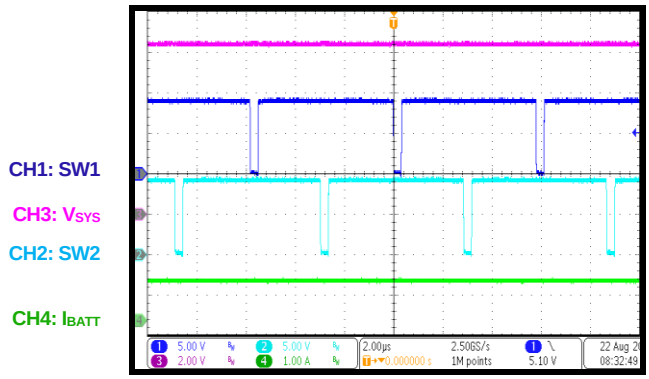
CC Charge Steady State

V_{IN} = 9V, V_{BATT} = 8V, I_{IN_LIM1} = I_{IN_LIM2} = 5A, I_{SYS} = 2A



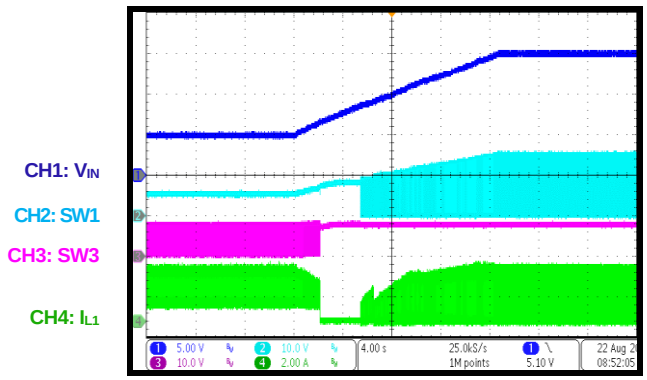
CV Charge Steady State

V_{IN} = 9V, V_{BATT} = 8.4V, I_{IN_LIM1}= I_{IN_LIM2} = 5A, I_{SYS} = 2A



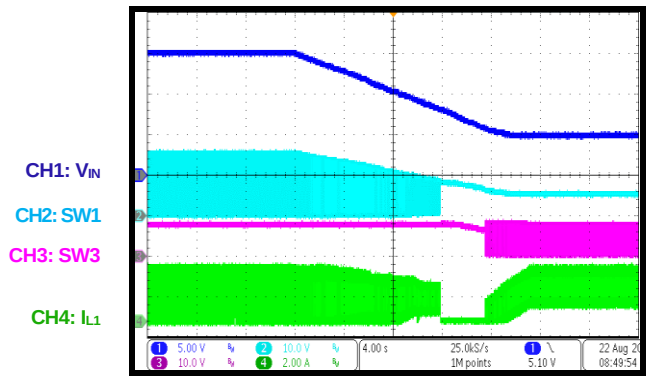
Boost-to-Buck Transition

V_{IN} = 5V to 15V, V_{BATT} = 7.4V



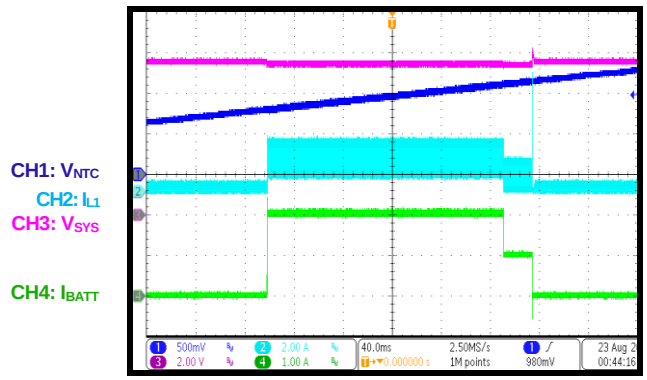
Buck-to-Boost Transition

V_{IN} = 15V to 5V, V_{BATT} = 7.4V



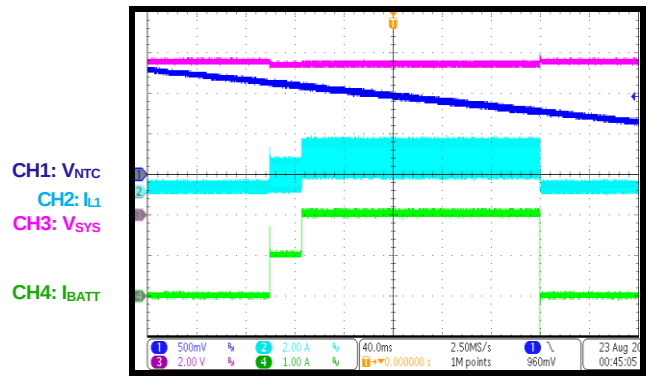
NTC

V_{IN} = 5V, V_{BATT} = 7.4V, temperature falling



NTC

V_{IN} = 5V, V_{BATT} = 7.4V, temperature rising

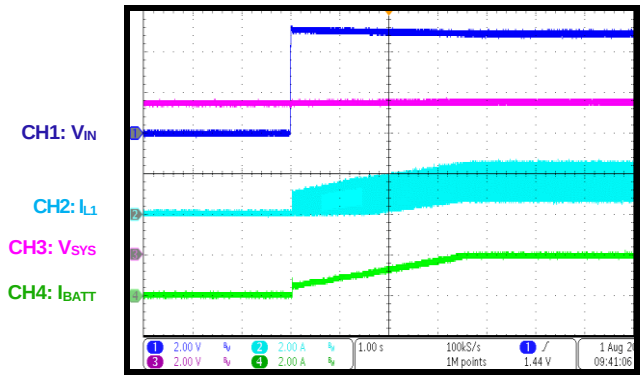


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L1 = L2 = 1.5µH, T_A = 25°C, unless otherwise noted.

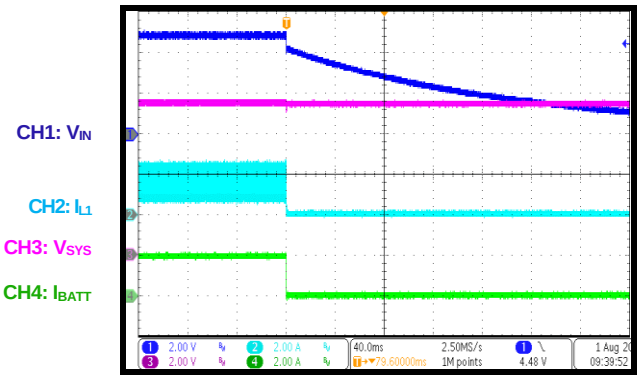
VIN Start-Up

V_{IN} = 5V, V_{BATT} = 7.4V



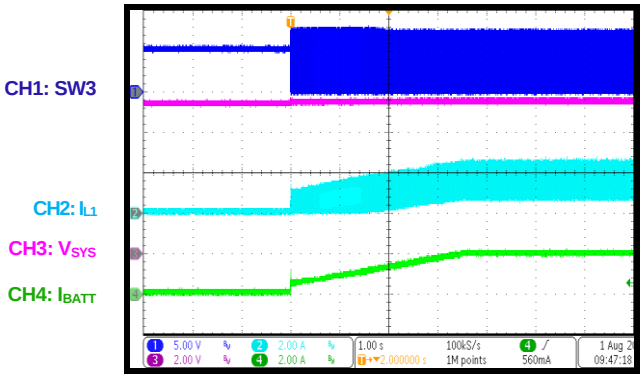
VIN Shutdown

V_{IN} = 5V, V_{BATT} = 7.4V



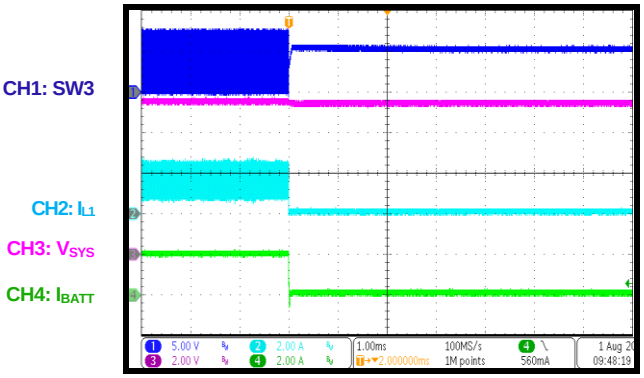
EN Start-Up

V_{IN} = 5V, V_{BATT} = 7.4V



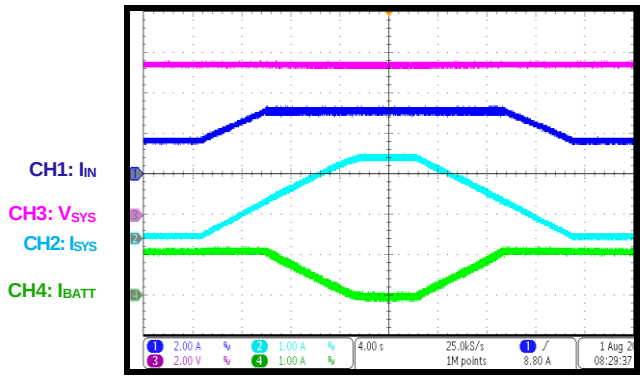
EN Shutdown

V_{IN} = 5V, V_{BATT} = 7.4V



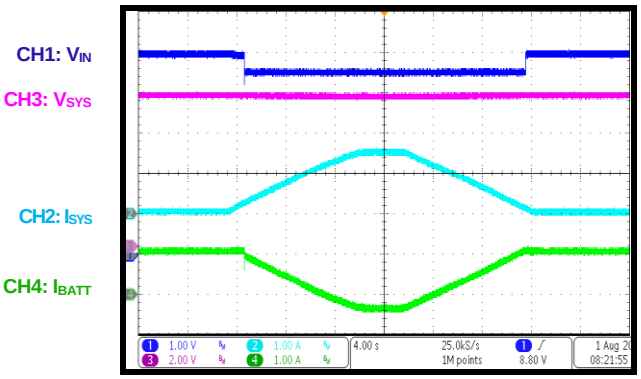
Input Current Limit

V_{IN} = 5V, V_{BATT} = 7.4V, I_{CHG} = 1A



Input Voltage Limit

V_{IN} = 5V (2A), V_{BATT} = 7.4V, I_{CHG} = 1A

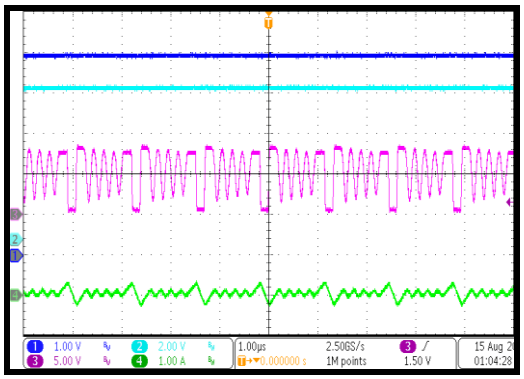


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_OTG} = 5V, V_{BATT} = 0V to 8.4V, I_{OLIM} = 3A, f_{SW} = 600kHz, L1 = L2 = 1.5µH, T_A = 25°C, unless otherwise noted.

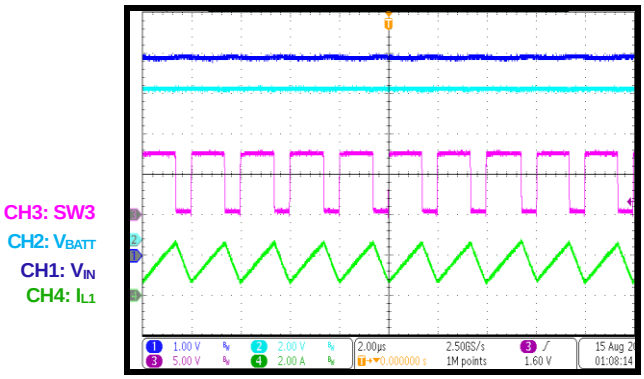
OTG Steady State

V_{BATT} = 7.4V, I_{OTG} = 0A



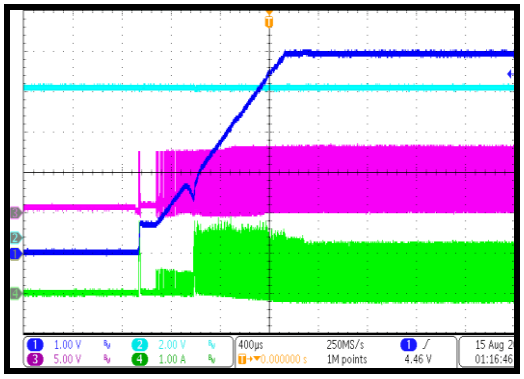
OTG Steady State

V_{BATT} = 7.4V, I_{OTG} = 3A



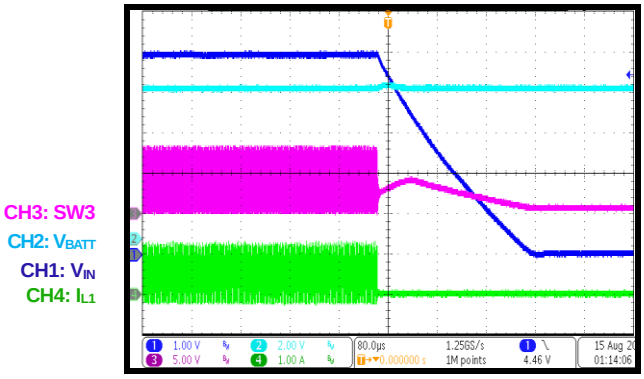
OTG EN Start-Up

V_{BATT} = 7.4V, I_{OTG} = 1A



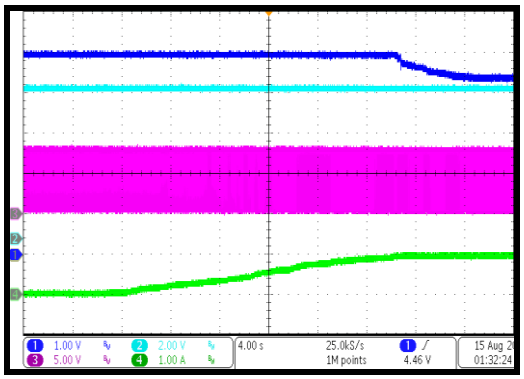
OTG EN Shutdown

V_{BATT} = 7.4V, I_{OTG} = 1A



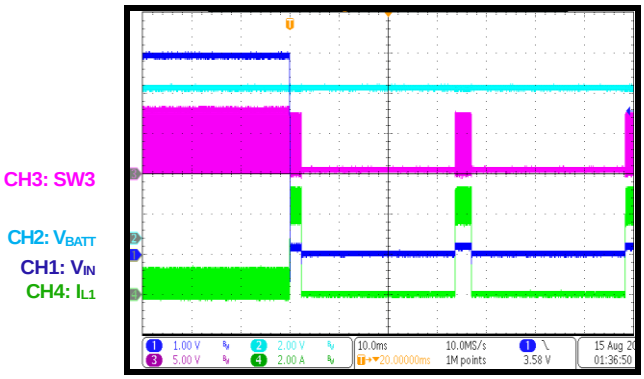
OTG Output Current Limit

V_{BATT} = 7.4V, I_{OLIM} = 1A



OTG SCP

V_{BATT} = 7.4V, I_{OTG} = 1A



FUNCTIONAL BLOCK DIAGRAM

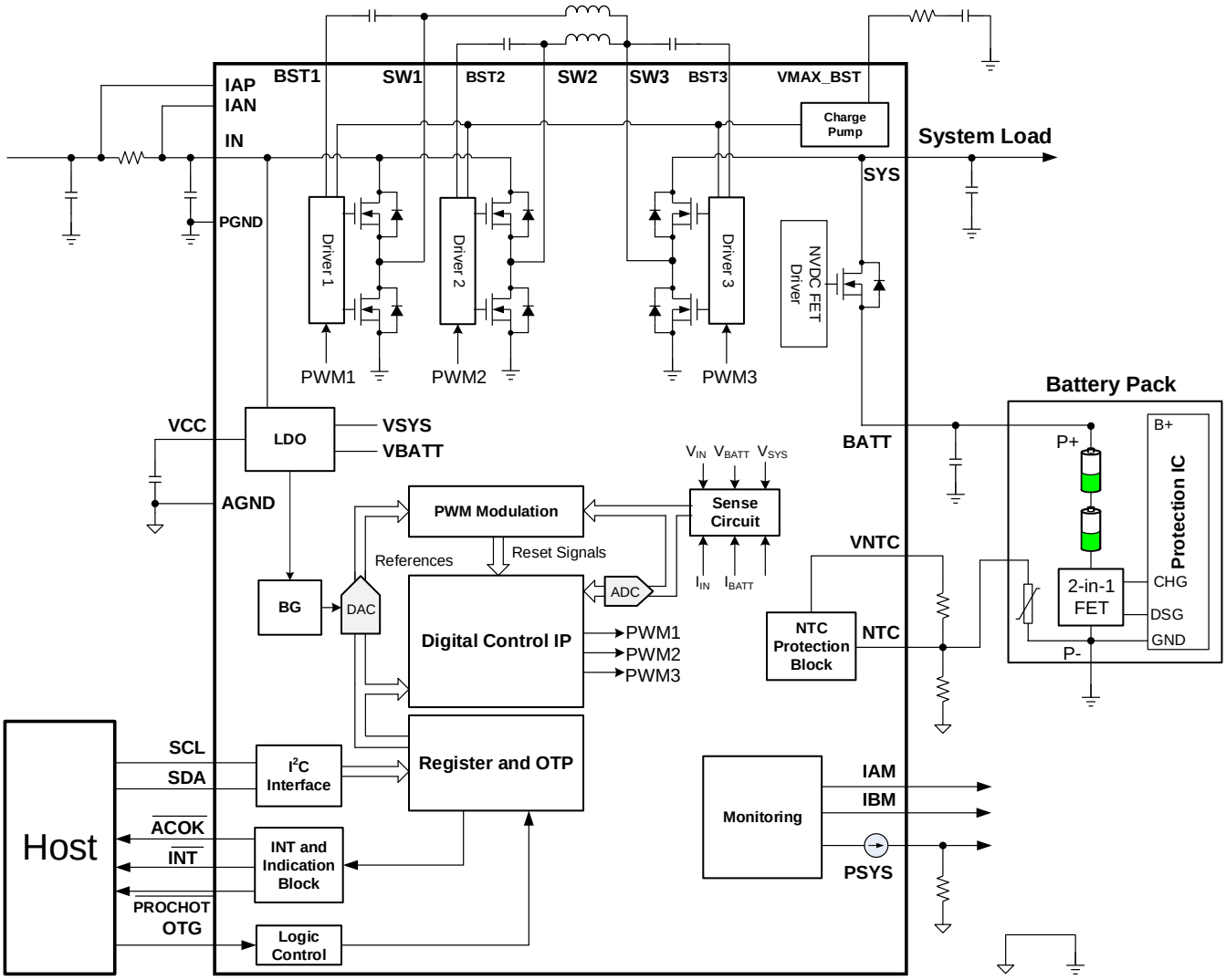


Figure 2: Functional Block Diagram

OPERATION

The MP2762A is a highly integrated buck or boost charger IC with narrow voltage DC (NVDC) power path management and USB On-the-Go (OTG) for battery packs with two cells in series. All power MOSFETs are integrated to provide a compact system solution size which is easy to use.

The IC can accept a wide range of input voltages (up to 21V) for charging, and it has two operating modes during the charging process: boost charging mode when the input voltage is below 5.75V, and buck charging mode when the input voltage exceeds 8.5V. In buck charging mode, there are two interleaving buck phases (Q1/Q2 and Q3/Q4) to allow for an inductor with a smaller profile while reducing the output current ripple (see Figure 3).

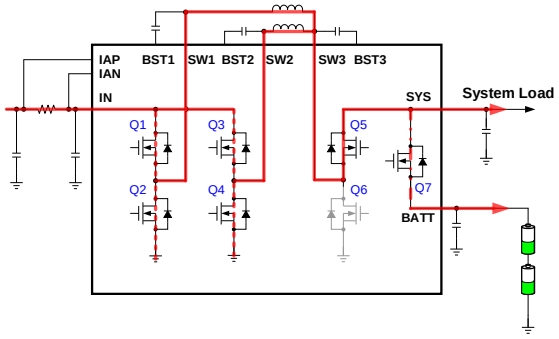


Figure 3: Power MOSFETs' State in Buck Charging Mode

In boost charge mode, two buck phases are in parallel (Q1/Q3) since the high-side MOSFET (HS-FET) is always on in each phase (see Figure 4).

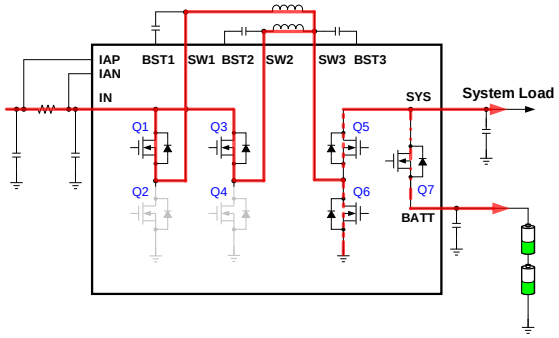


Figure 4: Power MOSFETs' State in Boost Charging Mode

The MP2762A can also provide a constant voltage (5V) at the input in USB OTG mode, and it utilizes a single-phase buck converter (Q5/Q6) to provide 5V/3A from the battery pack.

When the input is present, the device operates in charging mode. It automatically measures the battery voltage and charges the battery with four phases: constant current trickle charge, constant current pre-charge, constant current fast charge, and constant voltage charge. Other features include automatic charge termination and auto-recharge. This device also manages the input power, and meets the system's power demands with the integrated input current limit and minimum input voltage regulation function.

When the input is absent, the system is powered by the battery via the integrated battery FET (BATTFET). When the input is present but the input power is limited, the battery supplements the system along with the input.

The NVDC power path management regulates the system voltage within a narrow DC range to provide an optimized system bus voltage for the rails at the system bus. This allows the system to operate even when the battery is completely depleted or removed. When the input source current or voltage limit is reached, the power path management automatically reduces the charge current to meet the priority of the system's power requirements. If the system current increases when the charge current is reduced to zero, supplement mode allows the battery to power the system along with the input power supply.

Operation Modes

The MP2762A offers bidirectional operation modes: charging mode and On-the-Go (OTG) mode.

When the input is present, the device operates in charging mode. The DC/DC stage in the MP2762A operates as a buck or boost depending on the input voltage. Table 1 lists the DC/DC operation modes for different input voltages. When V_{IN} drops below 5.75V, the MP2762A operates as a boost charger with Q1 and Q3 always on. When V_{IN} exceeds 8.5V, the MP2762A operates as a buck charger for as long as V_{IN} exceeds V_{SYS} + 128mV, and Q5 remains on.

Table: 1 Operation Mode in Charging

V_{IN}	Boost Charge Mode	Buck Charge Mode
Rising	V_{IN} > 6.5V	V_{IN} > 8.5V
Falling	V_{IN} < 5.75V	V_{IN} < 8V

In charge mode, the MP2762A measures V_{IN} to automatically monitor the transition between buck and boost operation. When V_{IN} rises from 5V to 20V, the MP2762A charges the battery first in boost mode, then stops switching unless V_{IN} goes high enough for the device to operate in buck mode.

When the input is absent, the MP2762A powers the system from the battery through the integrated BATTFET (Q7). The MP2762A also provides a constant 5V voltage at the input terminal with I²C control or hardware pin control, which is called USB OTG mode (see Figure 5).

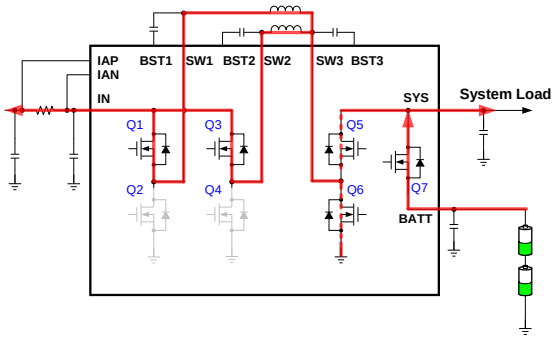


Figure 5: Power FETs State in OTG Mode

If the IC is not working in charging mode or on-the-go (OTG) mode, it enters battery-only mode. Several blocks can be disabled to optimize the battery quiescent current. The BATTFET can be turned off to further minimize the battery quiescent current.

VCC LDO Output

The VCC LDO supplies the internal bias circuits, as well as the HS-FET and LS-FET gate driver of the DC/DC converter. The pull-up rail of the open-drain outputs can also be connected to VCC as well. VCC has a 3.6V output and 50mA current capability.

VCC is supplied from either V_{IN} or V_{SYS}, depending on which has the higher value. When V_{IN} or V_{SYS} exceeds their respective UVLO threshold, then the sleep comparator, battery depletion comparator, and BATTFET driver are active. The I²C interface is ready for communication, and all the registers are reset to the default value. The host can access all the registers.

In charging mode, the internal VCC LDO is enabled when the following conditions are valid:

- V_{IN} > UVLO threshold
- Thermal shutdown is not occurring

Particularly when V_{IN} exceeds V_{IN_UVLO} in 5V boost charge mode, the VCC is powered by V_{SYS} after charge termination.

When the input is absent, the VCC LDO is powered by the battery.

Input Under-Voltage Lockout (UVLO) and Input Power-On Reset (POR)

The MP2762A has an input power-on reset (POR) voltage threshold. If V_{IN} drops below V_{IN_POR} and the battery is present, only the BATTFET block (charge pump, battery under-voltage lockout (UVLO), battery over-current protection (OCP)) and I²C continue to operate.

The MP2762A also has an input UVLO threshold. If V_{IN_POR} < V_{IN} < V_{IN_UVLO}, the internal control block reference, DAC, and ADC start to operate. However, the power stage is not ready until V_{IN} > V_{IN_UVLO}. Then the device can operate in buck or boost charging mode.

Input Power Status Reporting

The IC qualifies the voltage of the input source before start-up. The input source must meet the following requirements:

- V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}

Once the input power source meets the above conditions, the system status register (REG13H, bit[1]) asserts that the input power is good, and the buck or boost converter is ready to operate.

ACOK Indication

ACOK is an open-drain output pin indicating the presence of an adapter. It indicates the charger is operating normally by pulling ACOK to AGND under the following conditions:

- V_{IN} > V_{IN_UVLO}

NVDC Power Path Power Management

The MP2762A is designed as a charger with narrow voltage DC (NVDC) power path power management, which guarantees the priority of

the system power requirement under input plug-out or heavy load conditions (see Figure 6).

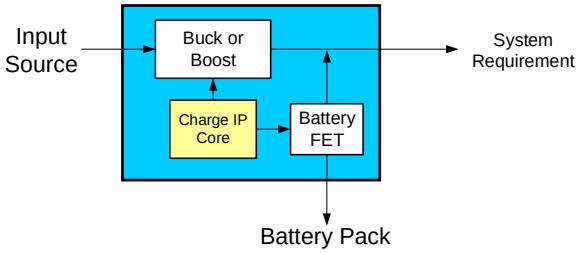


Figure 6: NVDC Power Path Management Structure

When $V_{BATT} > V_{BATT\_UVLO}$ and $V_{IN} < V_{IN\_UVLO}$, the MP2762A operates in battery-only mode. In this mode, the battery FET fully turns on to power the system using the battery.

When OTG is enabled, the battery supplies power to the input side via the buck or boost converter, as well as the system.

When $V_{IN\_OVLO} > V_{IN} > V_{IN\_UVLO}$, the input power supplies the system and charges the battery if charging is enabled. Due to the NVDC structure, V_{SYS} always tracks V_{BATT} when the battery FET is off, and $V_{BATT} > V_{BATT\_PRE}$ (see Figure 7). When $V_{BATT} > V_{BATT\_PRE}$ and charging is disabled, the minimum system voltage is regulated above V_{BATT} via V_{TRACK}.

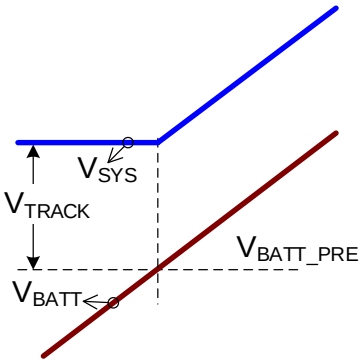


Figure 7: Battery Voltage Tracking

When charging is enabled and no charge fault occurs, the battery FET fully turns on once $V_{BATT} > V_{BATT\_PRE} + 140mV$ (see Figure 8).

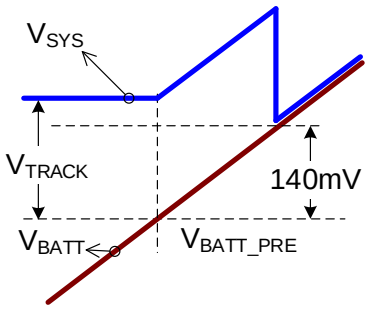


Figure 8: Switching Mode Fast Charging

Input Voltage Limit and Input Current Limit Regulation

To meet the maximum current limit for the USB specification and avoid overloading the adapter, the IC features both input current limiting and input voltage limiting.

If the preset input current limit exceeds the rating of the adapter, the backup input voltage limit loop works to prevent the input source from being overloaded.

IC Thermal Regulation

The IC continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset limit, the IC starts to reduce the charge current to prevent higher power dissipation.

Battery Supplement Mode

When the input current or input voltage limit loop operates, PWM control limits the power from the input. As a result, the system voltage and charge current decrease.

If the system power still increases and rises above the input power, the system voltage keeps falling. The charge current drops to 0A or becomes negative, which means the battery must start to discharge and supplement the system. This is called battery supplement mode. In this mode, the system load is powered by the battery and DC/DC converter simultaneously.

Virtual Diode Mode

In battery supplement mode, a virtual diode mode is designed into the IC to optimize the control transition between the battery FET and DC/DC converter. The battery FET enters virtual diode mode under the following conditions:

- $V_{IN} > V_{IN\_UVLO}$
- $V_{SYS} < V_{BATT}$ - 25mV

In virtual diode mode, the battery FET (BATTFET) operates as an ideal diode with a 30mV forward voltage (from the battery side to system side). When the system voltage is 25mV below the battery voltage, the gate drive of the battery FET is regulated to keep the battery FET's V_{DS} at about 30mV. As the discharge current increases, the battery FET obtains a stronger gate drive and a smaller $R_{DS(ON)}$ until the battery FET is fully on. The virtual diode exits when V_{SYS} exceeds V_{BATT} by 30mV due to the system's decreasing load current.

USB Suspended Mode

The IC has a USB suspended mode control bit to turn off the DC/DC converter and force the battery to power the system load, regardless of the input voltage status.

Charge Cycle

In charge mode, the IC has six control loops to regulate the input voltage, input current, charge current, charge voltage, system voltage, and device junction temperature.

The IC provides four main charging phases: constant current trickle charge, constant current pre-charge, constant current fast charge, and constant voltage charge. These phases are described below:

Phase 1 (constant current trickle charge): When the input power qualifies as a good power supply, the IC checks the battery voltage to decide if trickle current charging is required. If the battery voltage is below V_{BATT_TC}, a trickle charge current is applied to the battery.

Phase 2 (constant current pre-charge): When the battery voltage exceeds V_{BATT_TC}, the IC starts to safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle stops and a corresponding timeout fault signal is asserted. The pre-charge current can be configured via the I^2C (REG03H, bits[7:4]).

Phase 3 (constant current fast charge): If the battery voltage exceeds V_{BATT_PRE} set by REG07H, bits[5:4], the IC enters constant current charge (fast charge) phase. The fast charge current can be configured up to 6A via REG02H, bits[6:0].

Phase 4 (constant voltage charge): When the battery voltage rises to the battery-full voltage (V_{BATT_REG}) set via REG04H, bits[6:1], the charge current decreases due to battery voltage loop regulation.

The charge cycle is considered complete when the charge current reaches the battery-full termination threshold (I_{TERM}) set via REG03H, bits[3:0], as long as the termination function is enabled. If I_{TERM} is not reached before the safety charge timer expires (see the Safety Timer section on page 25), the charge cycle stops and the corresponding timeout fault signal is asserted.

Note that during the charging process, the actual charge current may be below the register setting due to the input current loop, input voltage loop, or thermal regulation. The thermal regulation loop reduces the charge current when the junction temperature exceeds the preset limit. The limit can be configured to be between 60°C and 120°C. The junction temperature regulation threshold can be set via REG05H, bits[1:0].

A new charge cycle starts when the following conditions are valid:

- The input power is re-plugged
- Battery charging is enabled by the I^2C
- No thermistor fault has occurred
- No battery over-voltage fault has occurred
- The BATTFET is not forced to turn off

Re-plugging the input power or toggling the battery charging control bit can restart a charge cycle, even if a fault has not occurred. The new charge cycle can start with any phase, which is determined by V_{BATT}.

Automatic Recharge

When charging is terminated, the battery may be discharged because of system consumption or the self-discharge function. When the battery voltage is discharged below the configurable recharge threshold, the IC automatically starts a new charging cycle. If the input power is valid, a manual restart is not required. The charging

safety timer resets when the auto-recharge cycle begins.

Battery Over-Voltage Protection (OVP)

The IC has battery over-voltage protection (OVP). If the battery voltage exceeds the battery OV threshold, charging stops and the battery FET turns off immediately. The system voltage is regulated at a value above V_{BATT} via V_{TRACK}.

Dual-Phase Operation

The MP2762A supports dual-phase operation in buck charging mode, so that each phase can supply half of the system load requirement. This optimizes the inductor's profile and thermal design. When I_{IN} < 0.4A, one of the phases can be disabled manually or automatically.

ADC Conversion and Multiplexer

The MP2762A integrates a 10-bit SAR ADC with 50ksps. In charge mode, the multiplexer measures the input voltage, input current, system voltage, battery voltage, and charge current. In OTG mode, the multiplexer measures the OTG output voltage, OTG output current, battery voltage, and current.

Safety Timer

The IC provides both a pre-charge and complete charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. If the battery voltage is below V_{BATT_PRE}, the total safety timer for both trickle charge and pre-charge is 1 hour. The complete charge safety timer includes a trickle charge and pre-charge timer. The user can configure a fast-charge safety timer through the I^2C. The safety timer feature can be disabled via the I^2C. The safety timer does not operate in discharge mode.

The safety timer is reset at the beginning of a new charging cycle. It can also be reset by sequentially writing 0 then 1 to REG08H, bit[4]. The following actions restart the safety timer:

- A new charge cycle begins
- Writing REG08H, bit[4] from 0 to 1 (charge enable)
- Writing REG09H, bit[3] from 0 to 1 (safety timer enable)

The IC can automatically adjust or suspend the timer when any fault occurs.

The timer is suspended when any of the following conditions occurs:

- The battery supplements the system
- System over-voltage protection (OVP)
- NTC hot or cold fault

If the input current limit, input voltage limit, or thermal regulation limit is reached, the remaining time of the timer can be doubled optionally. Once the condition is removed, the rest of timer operates normally. This function can be enabled or disabled by via the I^2C.

Impedance Compensation to Accelerate Charging

In the charging cycle, the constant voltage charging stage takes up large proportion of the total charging time. To accelerate the charging cycle, it is recommended to stay in the constant current charge stage for as long as possible.

The IC allows the user to compensate the intrinsic resistance of the battery by adjusting the charge-full voltage threshold according to the charge current and internal resistance. In addition, a maximum allowed regulated voltage is also set for safety reasons, calculated with Equation (1):

$$V_{BATT\_REG}* = V_{BATT\_REG} + Min(I_{CHG} x R_{BATT\_CMP}, V_{CLAMP}) \quad (1)$$

Where V_{BATT_REG}* is the real battery regulation voltage, V_{BATT_REG} is the charge-full voltage set via the REG04H, bits[6:1], and I_{CHG} is the real-time charge current.

Two-Level Input Current Limit

The input current limit can be set as two steps: I_{IN_LIM1} for the lower limit, and I_{IN_LIM2} for the higher limit. I_{IN_LIM2} can only last for t_2 and repeat once in t_1. Figure 9 shows the two current limit levels, as well as the time durations for t_2 and t_1.

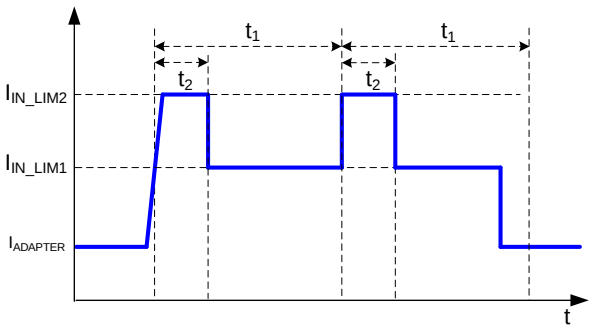


Figure 9: Two-Level Current Limit

The two-level current limit function is initiated when the input current is close to 100mA and below I_{IN_LIM1}. It starts at I_{IN_LIM2} for t_2, and then changes to I_{IN_LIM1} for t_1 before repeating the pattern. This fully utilizes the input adapter surge capability to extend the battery life.

I_{IN_LMT1} and I_{IN_LMT2} can be configured through I²C registers REG00H and REG0FH, respectively. t_2 and t_1 can be configured through I²C registers REG10H and REG11H, respectively.

System Power Monitor Analog Output (PSYS)

The IC has a PSYS pin to monitor the real-time system power in both charge mode and boost mode. The PSYS pin provides a current signal proportional to the total power consumed by the platform, and can be estimated with Equation (2):

$$P_{SYS} = K_{PSYS} x \left(V_{IN} x I_{IN} + V_{BATT} x I_{BATT} \right) \quad (2)$$

Where V_{IN} is the adapter voltage, I_{IN} is the adapter current, V_{BATT} is the battery voltage, and I_{BATT} is the battery discharging current. When the battery is charged, I_{BATT} is a negative value.

PSYS is an analog-controlled current source output that is proportional to the system power. The gain is 0.78μA/W. The MP2762A also has a 10-bit register to report the system power, with a resolution of 0.125W/bits. The PSYS function can be enabled or disabled through REG0BH, bits[1:0].

Current Monitoring (IAM/IBM)

The IC has an IBM pin to obtain the real-time battery current value in both charge mode and discharge mode. The IBM voltage (V_{IBM}) is a fraction of the charge current. It indicates the charge current flowing into and out of the battery during charge and discharge mode, respectively. V_{IBM} can be estimated with Equation (3):

$$V_{IBM} = I_{BATT} \times 0.125(V) \quad (3)$$

The IBM pin can report the charge current or discharge current depending on the I²C register setting. Similarly, the MP2762A also monitors the input current during the charging and discharging processes using the IAM pin, calculated with Equation (4):

$$V_{IAM} = I_{IN} \times 0.25(V) \quad (4)$$

The MP2762A also has registers to store the input current (REG1E~1FH), OTG current (REG22~23H), charge current (REG1A~1BH), and discharge current (REG28~29H). When the battery is charged in charge mode, the results in the OTG current and discharge current registers are set to 0. In OTG mode or battery supplement mode, the results in the input current and charge current registers are set to 0.

Processor Hot Interrupt (PROCHOT)

The IC continuously monitors the input current, battery discharge current, system voltage, input source presence, and whether the battery is present. The PROCHOT pin is pulled low if any of the following conditions occur:

- $I_{IN} > I_{IN\_OCP}$
- $I_{BAT} > I_{BAT\_DMAX}$
- $V_{SYS} < V_{SYS\_UV}$
- Adapter plug out
- Battery plug out
- Independent comparator has asserted

The thresholds for I_{IN_OCP}, I_{BAT_DMAX}, and V_{SYS_UV} are configurable through the I²C. To set the PROCHOT assertion threshold for adapter over-current conditions, write an ACProchot command to REG12H. If the adapter current exceeds the ACProchot threshold, the PROCHOT signal asserts after the debounce time. The signal latches on for a minimum time, which is configured by REG0EH (see Figure 10).

V_{SYS_UV} has two options for the debouncing time (10μs or 20μs), which can be set by REG0CH, bit[4]. Other triggering events have the same

debouncing time, which can also be set by REG0EH.

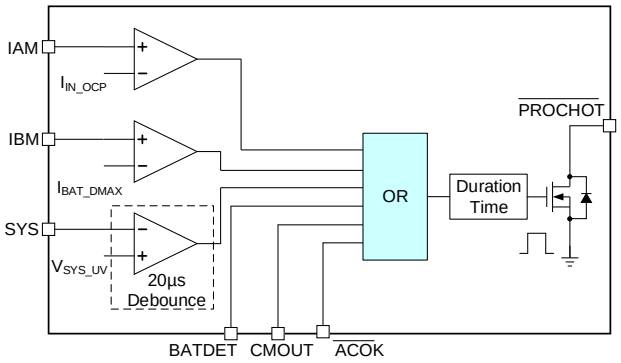


Figure 10: PROCHOT Events

Battery-Only Mode

When the input is absent and OTG mode is disabled, the battery FET fully turns on when V_{BATT} exceeds V_{BATT_UVLO}. The 10mΩ battery FET minimizes the conduction loss. The quiescent current of the IC is as low as 30µA. The low on resistance and low quiescent current help to extend the battery's runtime.

Light-Load Operation

Under light loads in buck mode, one of the phases can be disabled manually or automatically via the I²C. Light-load operation is designed to optimize the switching frequency. When the system current decreases, V_{SYS} rises and t_{ON} shortens. Then t_{OFF} is extended to keep the frequency constant. Finally, t_{OFF} reaches its limit and t_{ON} reaches the minimum on time. If the system voltage still increases, the on time is skipped once V_{SYS} exceeds 101% of V_{SYS_REG}. The threshold can be adjusted via REG31H, bits[1:0].

USB On-the-Go (OTG) Mode

In discharge mode, the regulated 5V/3A power is delivered from the battery to the IN pin through a single-phase buck converter.

The IC does not enter On-the-Go (OTG) mode if the battery is below the configurable battery UVLO threshold. This ensures that the battery is not drained. To enable buck mode, the input voltage at the IN pin must be below 1.0V.

OTG operation can be enabled when REG08H, bit[5] = 1, and the OTG pin is high. The USB OTG output current can be set between 0A and 3.75A via the I²C (REG07H, bits[3:0]). Buck mode is enabled when all of the following conditions are met:

- $V_{BATT} > V_{BATT\_UVLO}$ (5.2V)
- OTG REG08, bit[5] = 1
- A 30ms delay has completed
- The OTG pin is high
- $V_{IN} < 1V$

If V_{IN} does not exceed V_{OTG_UV} (set by REG0D, bits[3:2]) within 30ms while OTG is enabled, a buck fault is asserted, and buck mode is disabled until a command that enables OTG operation is reissued.

The IC also features output short-circuit protection and output over-voltage protection (OVP). If the load current approaches the OTG current-limit threshold (set by the I²C) while the IC runs in buck mode, the OTG output current loop dominates and the converter acts as a current source. If V_{BUS} falls below V_{OTG_UV} for more than 700µs, a buck fault is asserted. The buck is disabled and restarts after a 30ms delay time. Any fault during OTG buck operation sets the fault register (REG14, bit[6]) to 1.

When both charging and OTG buck mode are enabled, OTG buck mode takes priority.

The IC continuously monitors the voltage at the IN pin in OTG buck mode. If V_{BUS} exceeds V_{OTG_OV} (set by REG0D, bits[5:4]), the IC stops switching, and the corresponding fault register is set high to indicate the fault.

Thermal Shutdown Protection

Thermal shutdown protection is also active in OTG mode. If the junction temperature exceeds 150°C, the MP2762A enters thermal shutdown. It does not resume normal operation until the junction temperature drops below 120°C.

Host Mode and Default Mode

The IC is a host-controlled device. After power-on reset (POR), the IC starts in the watchdog timer expiration state, or its default mode. All registers revert to their default settings.

Any write to the IC is transmitted to host mode. All the device parameters can be configured by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG08H, bit[6] before the watchdog timer expires. The IC goes back to default mode once the watchdog timer expires.

The MP2762A has one-time programmable (OTP) memory to program the default value of certain registers after they are assembled.

I²C Interface

The IC uses an I²C-compatible interface for flexible charging parameter settings and instantaneous device status reporting. The I²C is a bidirectional, two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). The device can be considered a master or a slave when performing data transfers. The master is the device that initiates a data transfer on the bus and generates the clock signals to permit the transfer. At that time, any device addressed by the master is considered a slave.

The device operates as a slave device with address 5CH, and receives control inputs from the master device, such as a microcontroller or digital signal processor.

The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). Both SDA and SCL are connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. The SDA and SCL pins are open-drain.

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low. One clock pulse is generated for each data bit transferred (see Figure 11).

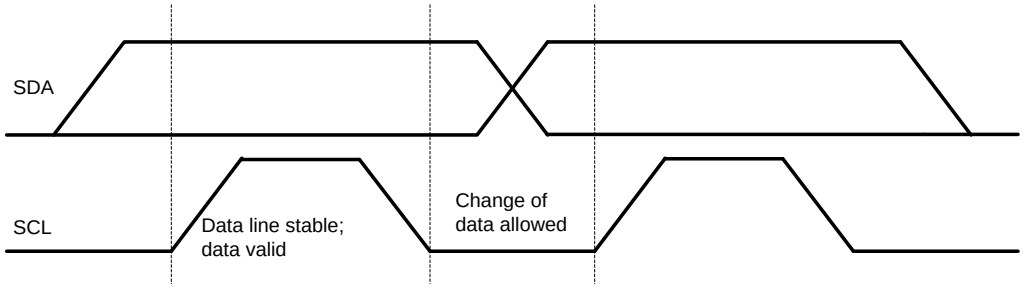


Figure 11: **Bit Transfer on the I²C Bus**

All the transactions begin with a start (S) and are terminated by a stop (P). A high-to-low transition on the SDA line while SCL is high defines a start command. A low-to-high transition on the SDA line when SCL is high defines a stop command. Start and stop commands are always generated by the master. The bus is considered busy after the start command, and is free after the stop command (see Figure 12).

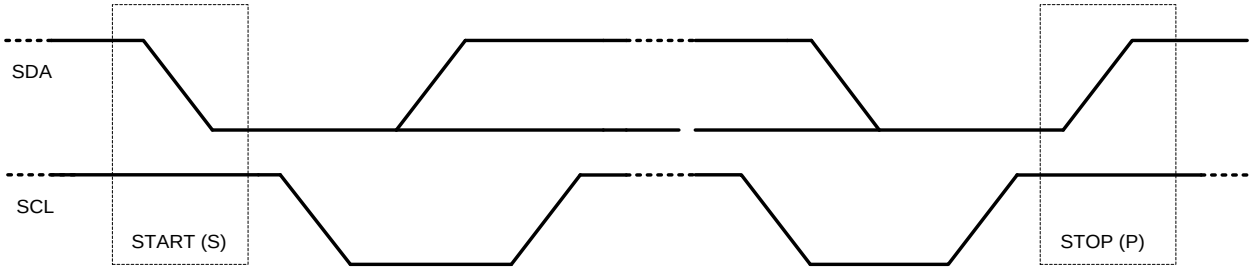


Figure 12: Start and Stop Conditions

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge (ACK) bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line (SCL) low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data, and SCL is released (see Figure 13).

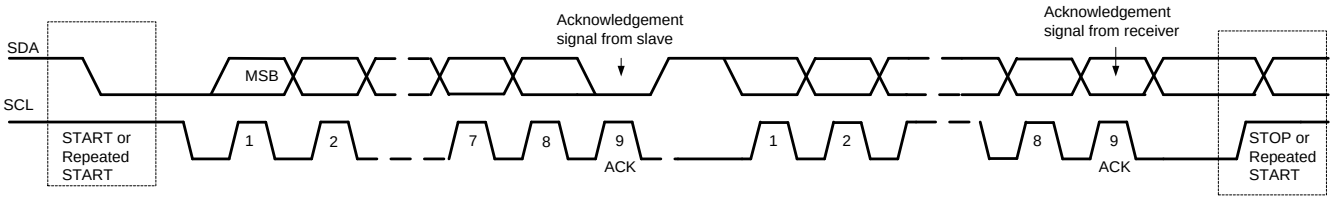


Figure 13: Data Transfer on the I²C BUS

The acknowledgement takes place after every byte. The acknowledge bit allows the receiver to signal to the transmitter that the byte was successfully received and that another byte may be sent. All clock pulses, including the acknowledge (9th) clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low. If it remains high during the 9th clock pulse, this is called a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer, or a repeated start command to start a new transfer.

After the process is initiated, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 14 shows the complete data transfer.

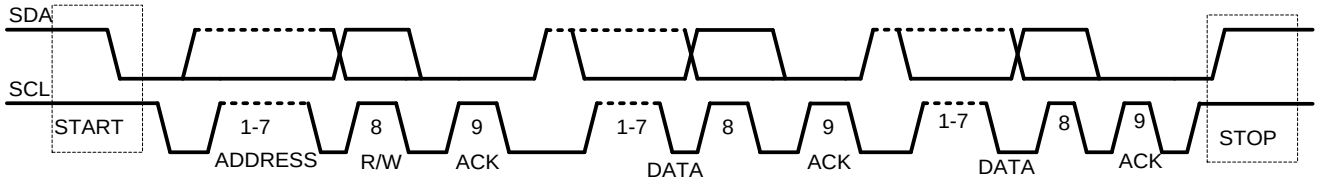


Figure 14: Complete Data Transfer

If the register address is not defined, the charger IC sends back NACK and reverts to its idle state.

Figure 15, Figure 16, Figure 17, and Figure 18 show examples of I²C processes.

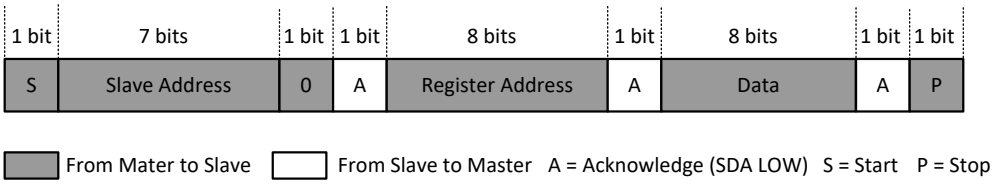


Figure 15: I²C Single Write

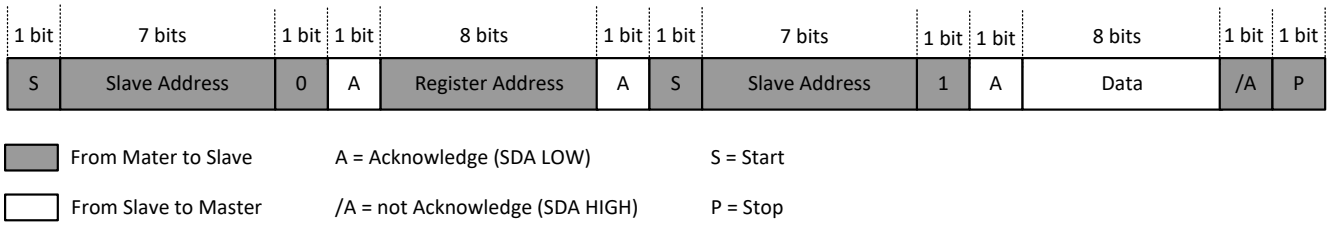


Figure 16: I²C Single Read

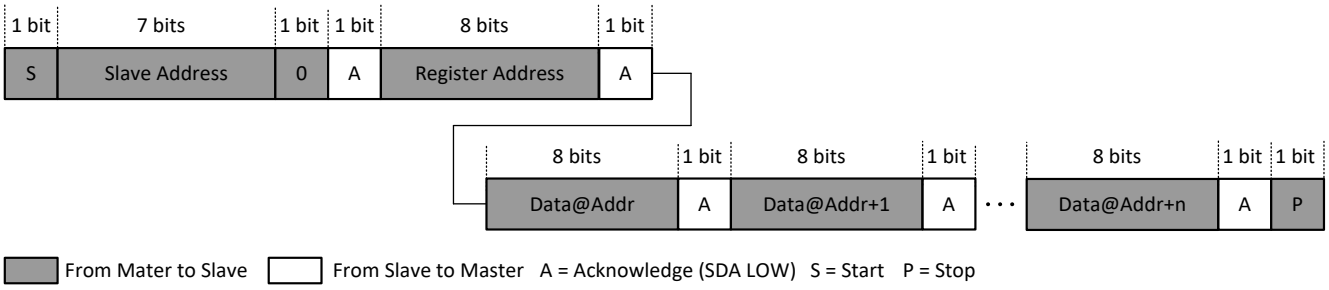


Figure 17: I²C Multi-Write

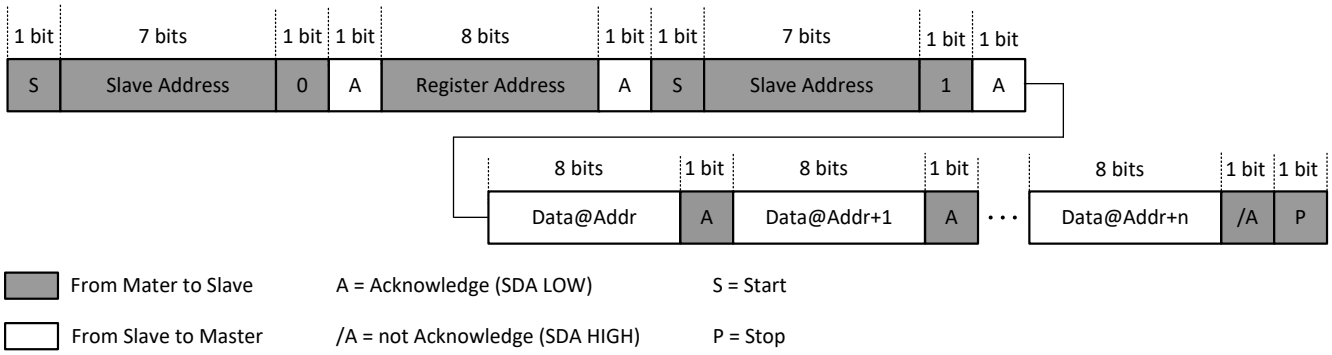


Figure 18: I²C Multi-Read

REGISTER MAP (Device Address: 5CH)

Register Name	Register Address	OTP	R/W	Description
REG00H	0x00	Yes	R/W	Input current limit 1 setting.
REG01H	0x01	Yes	R/W	Input voltage limit setting.
REG02H	0x02	Yes	R/W	Charge current setting.
REG03H	0x03	Yes	R/W	Pre-charge and termination current setting.
REG04H	0x04	Yes	R/W	Battery-full voltage and recharge threshold setting.
REG05H	0x05	No	R/W	Battery impedance compensation and junction temperature regulation.
REG06H	0x06	Yes	R/W	OTG voltage setting.
REG07H	0x07	Yes	R/W	Pre-charge threshold and OTG output current limit setting.
REG08H	0x08	Yes	R/W	Configuration register 0.
REG09H	0x09	Yes	R/W	Configuration register 1.
REG0AH	0x0A	No	R/W	Configuration register 2.
REG0BH	0x0B	Yes	R/W	Configuration register 3.
REG0CH	0x0C	Yes	R/W	Configuration register 4.
REG0DH	0x0D	Yes	R/W	System/OTG under-voltage and over-voltage setting.
REG0EH	0x0E	Yes	R/W	PROCHOT interrupt debounce time and duration time setting.
REG0FH	0x0F	Yes	R/W	Input current limit 2 setting.
REG10H	0x10	Yes	R/W	Input current limit 2 duration setting.
REG11H	0x11	Yes	R/W	Two-level input current limit period setting.
REG12H	0x12	Yes	R/W	Input OCP threshold for triggering PROCHOT.
REG13H	0x13	No	R	Status register.
REG14H	0x14	No	R	Fault register.
REG16~17H	0x16	No	R	ADC result for battery voltage.
REG18~19H	0x18	No	R	ADC result for system voltage.
REG1A~1BH	0x1A	No	R	ADC result for battery charge current.
REG1C~1DH	0x1C	No	R	ADC result for input voltage.
REG1E~1FH	0x1E	No	R	ADC result for input current.
REG20~21H	0x20	No	R	ADC result for OTG output voltage.
REG22~23H	0x22	No	R	ADC result for OTG output current.
REG24~25H	0x24	No	R	ADC result for junction temperature.
REG26~27H	0x26	No	R	ADC result for system power.
REG28~29H	0x28	No	R	ADC result for battery discharge current.
REG2BH	0x2B	Yes	R/W	Battery over-voltage protection deglitch time
REG2DH	0x2D	Yes	R/W	Battery voltage loop enable
REG30H	0x30	Yes	R/W	Battery pre-charge threshold option
REG31H	0x31	Yes	R/W	System voltage threshold for pulse skipping.
REG33H	0x33	Yes	R/W	INT mask for Hi-Z mode entry and exit.
REG36H	0x36	Yes	R/W	Analog frequency loop enable.
REG40~41H	0x40	No	R	ADC result for NTC voltage versus 1.6V reference voltage
REG48H	0x48	No	R	Hi-Z mode indication.

REG00H: Input Current Limit 1 Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	I_{IN_LIM1}[6]	0	Y	Y	R/W	3200mA.	These bits set the input current limit setting. (RS = 10mΩ) It has a 0mA offset, a 1.5A default, and a 0mA to 6.35A range via the one-time programmable memory (OTP).
5	I_{IN_LIM1}[5]	0	Y	Y	R/W	1600mA.	
4	I_{IN_LIM1}[4]	1	Y	Y	R/W	800mA.	
3	I_{IN_LIM1}[3]	1	Y	Y	R/W	400mA.	
2	I_{IN_LIM1}[2]	1	Y	Y	R/W	200mA.	
1	I_{IN_LIM1}[1]	1	Y	Y	R/W	100mA.	
0	I_{IN_LIM1}[0]	0	Y	Y	R/W	50mA.	

REG01H: Input Voltage Limit Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{IN_MIN}[7]	0	Y	Y	R/W	12800mV.	These bits set the input voltage limit threshold with a 4.5V default, and a 0V to 25.5V range via the OTP.
6	V_{IN_MIN}[6]	0	Y	Y	R/W	6400mV.	
5	V_{IN_MIN}[5]	1	Y	Y	R/W	3200mV.	
4	V_{IN_MIN}[4]	0	Y	Y	R/W	1600mV.	
3	V_{IN_MIN}[3]	1	Y	Y	R/W	800mV.	
2	V_{IN_MIN}[2]	1	Y	Y	R/W	400mV.	
1	V_{IN_MIN}[1]	0	Y	Y	R/W	200mV.	
0	V_{IN_MIN}[0]	1	Y	Y	R/W	100mV.	

REG02H: Charge Current Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	I_{CC}[6]	0	Y	Y	R/W	3200mA.	These bits set the charge current. It has a 0A offset, 0A to 6A range, and is set to 1A by default via the OTP.
5	I_{CC}[5]	0	Y	Y	R/W	1600mA.	
4	I_{CC}[4]	1	Y	Y	R/W	800mA.	
3	I_{CC}[3]	0	Y	Y	R/W	400mA.	
2	I_{CC}[2]	1	Y	Y	R/W	200mA.	
1	I_{CC}[1]	0	Y	Y	R/W	100mA.	
0	I_{CC}[0]	0	Y	Y	R/W	50mA.	

REG03H: Pre-Charge and Termination Current Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I_{PRE}[3]	0	Y	Y	R/W	0000: 180mA 0001: 180mA 0010: 180mA 0011: 180mA 0100: 180mA 0101: 240mA 0110: 300mA 0111: 360mA 1000: 420mA 1001: 480mA 1010: 540mA 1011: 600mA 1100: 660mA 1101: 720mA 1110: 780mA 1111: 840mA	These bits set the pre-charge current limit. It has a 0mA offset, and is set to 180mA by default via the OTP.
6	I_{PRE}[2]	0	Y	Y	R/W		
5	I_{PRE}[1]	1	Y	Y	R/W		
4	I_{PRE}[0]	1	Y	Y	R/W		
3	I_{TERM}[3]	0	Y	Y	R/W	800mA.	These bits set the termination current limit. It has a 0mA offset, 0mA to 1500mA range, and is set to 200mA by default via the OTP.
2	I_{TERM}[2]	0	Y	Y	R/W	400mA.	
1	I_{TERM}[1]	1	Y	Y	R/W	200mA.	
0	I_{TERM}[0]	0	Y	Y	R/W	100mA.	

REG04H: Battery-Full Voltage and Recharge Threshold Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	NA	Reserved.	Reserved.
6	V_{BATT_REG}[5]	1	Y	Y	R/W	800mV.	These bits set the charge-full voltage. It has a 7.425V offset, 7.425V to 9V range, and is set to 8.4V by default via the OTP.
5	V_{BATT_REG}[4]	0	Y	Y	R/W	400mV.	
4	V_{BATT_REG}[3]	0	Y	Y	R/W	200mV.	
3	V_{BATT_REG}[2]	1	Y	Y	R/W	100mV.	
2	V_{BATT_REG}[1]	1	Y	Y	R/W	50mV.	
1	V_{BATT_REG}[0]	1	Y	Y	R/W	25mV.	
0	V_{RECH_OS}	0	Y	Y	R/W	0: 200mV 1: 400mV	This bit sets the battery recharge threshold offset. It has a 200mV offset set via the OTP.

REG05H: Battery Impedance Compensation and Junction Temperature Regulation

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	R_{BATT}[2]	0	Y	Y	R/W	100mΩ.	These bits set the IR compensation resistor for each cell. It has a 0mΩ to 175mΩ range, and is set to 0mΩ by default.
6	R_{BATT}[1]	0	Y	Y	R/W	50mΩ.	
5	R_{BATT}[0]	0	Y	Y	R/W	25mΩ.	
4	V_{CLAMP}[2]	0	Y	Y	R/W	120mV.	These bits set the IR compensation resistor clamp for each cell (above the charge voltage limit). It has a 0mV offset, a 0mV to 210mV range, and is set to 0mV by default.
3	V_{CLAMP}[1]	0	Y	Y	R/W	60mV.	
2	V_{CLAMP}[0]	0	Y	Y	R/W	30mV.	
1	T_{REG}[1]	1	Y	Y	R/W	00: 60°C 01: 80°C 10: 100°C 11: 120°C	These bits set the thermal regulation threshold. It has a 120°C default, and is only for the BATTFET linear charge loop.
0	T_{REG}[0]	1	Y	Y	R/W		

REG06H: OTG Voltage Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	V_{IN_OTG}[2]	0	Y	Y	R/W	000: 4.75V	These bits set the OTG voltage. It is set to 4.75V by default via the OTP.
5	V_{IN_OTG}[1]	0	Y	Y	R/W		
4	V_{IN_OTG}[0]	0	Y	Y	R/W		
3	$V_{IN\_OTG\_OS}$[3]	0	Y	Y	R/W	400mV.	These bits set the secondary OTG voltage. It is set to 250mV by default via the OTP.
2	$V_{IN\_OTG\_OS}$[2]	1	Y	Y	R/W	200mV.	
1	$V_{IN\_OTG\_OS}$[1]	0	Y	Y	R/W	100mV.	
0	$V_{IN\_OTG\_OS}$[0]	1	Y	Y	R/W	50mV.	

REG07H: Pre-Charge Threshold and OTG Output Current Limit Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.

5	V_{BATT_PRE}[1]	0	Y	Y	R/W	Option1: 00: 5.8V 01: 6.0V 10: 6.2V 11: 6.4V Option2: 00: 6.6V 01: 6.8V 10: 7.4V 11: 7.2V	These bits set the battery pre-charge threshold. It is set to 6.8V by default via the OTP. The option is set by REG30H, bit[3].
4	V_{BATT_PRE}[0]	1	Y	Y	R/W		
3	I_{OTG}[3]	0	Y	Y	R/W	2000mA.	These bits set the OTG current limit. It has a 0mA offset, a 0mA to 3.75A range, and is set to 1A by default via the OTP.
2	I_{OTG}[2]	1	Y	Y	R/W	1000mA.	
1	I_{OTG}[1]	0	Y	Y	R/W	500mA.	
0	I_{OTG}[0]	0	Y	Y	R/W	250mA.	

REG08H: Configuration Register 0

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	REG_RST	0	Y	Y	R/W	0: Keep current register setting 1: Reset to the default register value and reset the safety timer	This bit sets the register reset setting. It is set to 0 by default. It resets to 0 after the register is reset.
6	WTD_RST	0	Y	Y	R/W	0: Normal 1: Reset	This bit sets the I^2C watchdog timer reset. It is set to 0 by default. It resets to 0 after the register is reset.
5	OTG_EN	0	Y	Y	R/W	0: Disable OTG 1: Enable OTG	This bit configures the OTG mode configuration. It is set to 0 to by default. OTG_EN will over-ride charge enable function.
4	CHG_EN	1	Y	Y	R/W	0: Charge disabled (only turn off BATTFET) 1: Charge enabled	This bit configures the charge mode. It is set to 1 by default. OTG_EN overrides the CHG_EN enable function. It can be configured via the OTP.
3	SUSP_EN	0	Y	Y	R/W	0: Disable SUSP mode 1: Enable SUSP mode (only turn off DC/DC)	This bit configures suspend mode. It is set to 0 by default.

2	NTC_ GCOMP_ SEL	1	Y	Y	R/W	0: The OTG/CMIN pin acts as CMIN, the VNTC/CMOUT pin acts as CMOUT, and the NTC/BATDET pin acts as BATDET 1: The OTG/CMIN pin acts as OTG, the VNTC/CMOUT pin acts as VNTC, and the NTC/BATDET pin acts as NTC	This bit selects the NTC and OTG pin functions. It is set to 1 by default. When the OTG pin is selected as the independent input, the internal OTG pin is pulled high for OTG mode. It can be configured via the OTP.
1	BATTFET_E N	1	Y	Y	R/W	0: Disable charging or discharge 1: Enable charging or discharge	This bit configures the BATTFET. It is set to 1 by default.
0	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.

REG09H: Configuration Register 1

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	EN_TERM	1	Y	Y	R/W	0: Disabled 1: Enabled	This bit enables charging termination. It is set to 1 by default.
5	WTD[1]	0	Y	Y	R/W	00: Disable timer 01: 40s 10: 80s 11: 160s	This bit sets the I^2C watchdog timer. They are set to 00 by default, and can be configured via the OTP.
4	WTD[0]	0	Y	Y	R/W		
3	EN_TMR	1	Y	Y	R/W	0: Disabled 1: Enabled	This bit enables the charging safety timer (both the pre-charge timer and complete charge cycle timer). It is set to 1 by default via the OTP.
2	CHG_TMR [1]	1	Y	Y	R/W	00: 5 hours 01: 8 hours 10: 12 hours 11: 20 hours	This bit sets the fast-charge timer. They are set to 10 by default via the OTP.
1	CHG_TMR [0]	0	Y	Y	R/W		

0	TMR2X_EN	0	Y	Y	R/W	0: The safety timer is not doubled during input DPM or thermal regulation 1: The safety timer is doubled during input DPM and thermal regulation	This bit sets the safety timer during DPM and thermal regulation. It is set to 0 by default.

REG0AH: Configuration Register 2

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	JEITA_ISET	0	Y	Y	R/W	0: 50% 1: 20%	This bit sets the JEITA low-temperature current. It is set to 0 by default. It is a percentage of the value set by REG02, bits[6:0]. This bit is only valid when REG0A, bits[5:4] = 00.
6	JEITA_ VSET	0	Y	Y	R/W	0: Set the charge voltage to V_{BATT_REG} - 150mV 1: Set the charge voltage to V_{BATT_REG} - 300mV	This bit sets the JEITA high-temperature voltage. It is set to 0 by default. It is only valid when REG0A, bits[5:4] = 00.
5	NTC_CTRL [1]	1	Y	Y	R/W	00: JEITA 01/10: Standard 11: Disabled	These bits set the NTC protection type. They are set to 11 by default.
4	NTC_CTRL [0]	1	Y	Y	R/W		
3	NTC_WARM [1]	0	Y	Y	R/W	00: 58.3% (40°C) 01: 56.1% (45°C) 10: 53.7% (50°C) 11: 51.3% (55°C)	This bit is set to 01 by default.
2	NTC_WARM [0]	1	Y	Y	R/W		
1	NTC_COOL [1]	1	Y	Y	R/W	00: 70.7% (0°C) 01: 69.7% (5°C) 10: 68.6% (10°C) 11: 67.3% (15°C)	These bits are set to 10 by default.
0	NTC_COOL [0]	0	Y	Y	R/W		

REG0BH: Configuration Register 3

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
5	IBM_CFG	0	N	N	R/W	0: Reflect the battery discharge current 1: Reflect the battery charge current	This bit configures the battery current monitor. It is set to 0 by default.
4	SW_FREQ [1]	0	N	N	R/W	00: 600kHz 01: 800kHz 10: 1000kHz 11: Invalid	These bits set the switching frequency. They are set to 00 by default via the OTP.
3	SW_FREQ [0]	0	N	N	R/W		
2	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
1	PROCHOT/ PSYS_CFG [1]	0	N	N	R/W	00: Disable PROCHOT and PSYS functionality (lowest quiescent current) 01: Enable PROCHOT and disable PSYS (middle quiescent current, since part of the circuit is enabled) 10/11: Enable PROTHOT and PSYS	These bits set the function setting in battery-only mode. They are set to 00 by default via the OTP.
0	PROCHOT/ PSYS_CFG [0]	0	N	N	R/W		

REG0CH: Configuration Register 4

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	DSCHG_OC _PROCHOT [2]	1	N	N	R/W	000: 0A 001: 2A 010: 4A 011: 6A 100: 8A 101: 10A 110: 12A 111: 14A	These bits set the battery discharging over-current threshold for PROCHOT assertion. They are set to 110 by default via the OTP.
6	DSCHG_OC _PROCHOT [1]	1	N	N	R/W		
5	DSCHG_OC _PROCHOT [0]	0	N	N	R/W		
4	VSYS PROCHOT TDB	0	N	N	R/W	0: 10µs 1: 20µs	This bit sets the VSYS under-voltage (UV) trigger PROCHOT debounce time. It is set to 0 by default via the OTP.

3	VIRTUAL_ DIODE_EN	0	N	N	R/W	0: Disabled 1: Enabled	This bit sets the ideal diode mode when an adapter is absent. It is set to 0 by default via the OTP.
2	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
1	INDEPEN DENT_ COMPAR ATOR_CFG	0	N	N	R/W	0: PROCHOT does not assert 1: PROCHOT asserts	This bit sets the PROCHOT assertion when the independent comparator outputs low. It is set to 0 by default via the OTP.
0	INDEPEN DENT_ COMPAR ATOR_REF ERENCE	0	N	N	R/W	0: 1.2V 1: 2.1V	This bit sets the independent comparator reference. It is set to 0 by default via the OTP.

REG0DH: System/OTG Under-Voltage and Over-Voltage Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
5	V_{OTG_OV}/ V_{SYS_OV}[1]	0	N	N	R/W	00: 125% 01: 120% 10: 115% 11: 110%	These bits set the OTG over-voltage (OV) and system OV threshold. It is a percentage of the OTG voltage, and is set to 00 by default via the OTP.
4	V_{OTG_OV}/ V_{SYS_OV}[0]	0	N	N	R/W		
3	V_{OTG_UV}/ V_{SYS_UV}[1]	0	N	N	R/W	00: 75% 01: 80% 10: 85% 11: 90%	These bits set the OTG under-voltage lockout (UVLO) voltage and system UVLO voltage. It is a percentage of the OTG voltage, and is set to 00 by default via the OTP.
2	V_{OTG_UV}/ V_{SYS_UV}[0]	0	N	N	R/W		
1	SYS_UV_P ROCHOT[1]	0	N	N	R/W	00: 5.6V 01: 5.8V 10: 6.0V 11: 6.2V	These bits set the low system voltage PROCHOT assertion threshold. They are set to 01 by default via the OTP.
0	SYS_UV_P ROCHOT[0]	1	N	N	R/W		

REG0EH: PROCHOT Interrupt Debounce Time and Duration Time Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{DEB}[2]	0	N	N	R/W	000: 100µs 001: 200µs 010: 300µs 011: 400µs 100: 500µs 101: 600µs 110: 700µs 111: 800µs	These bits set the time before the following assert: ACProchot, DCProchot, input absent, battery absent and independent comparator output trigger PROCHOT. They are set to 001 by default via the OTP.
6	t_{DEB}[1]	0	N	N	R/W		
5	t_{DEB}[0]	1	N	N	R/W		
4	t_{DUR}[3]	0	N	N	R/W	1600µs.	These bits set the duration time for the PROCHOT signal once it is asserted. It has a 200µs offset, and is set to 400µs by default via the OTP.
3	t_{DUR}[2]	0	N	N	R/W	800µs.	
2	t_{DUR}[1]	0	N	N	R/W	400µs.	
1	t_{DUR}[0]	1	N	N	R/W	200µs.	
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Reserved.

REG0FH: Input Current Limit 2 Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	I_{IN_LIM2}[6]	0	N	N	R/W	3200mA.	These bits set the second input current limit (RS1 = 10mΩ). It has a 0mA offset, 0mA to 6.35A range, and is set to 1.5A by default via the OTP.
5	I_{IN_LIM2}[5]	0	N	N	R/W	1600mA.	
4	I_{IN_LIM2}[4]	1	N	N	R/W	800mA.	
3	I_{IN_LIM2}[3]	1	N	N	R/W	400mA.	
2	I_{IN_LIM2}[2]	1	N	N	R/W	200mA.	
1	I_{IN_LIM2}[1]	1	N	N	R/W	100mA.	
0	I_{IN_LIM2}[0]	0	N	N	R/W	50mA.	

REG10H: Input Current Limit 2 Duration Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{MAX}[6]	0	N	N	R/W	12800µs.	These bits set the second input current limit duration. (RS1 = 10mΩ) It has a 100µs offset, 100µs to 25.6ms range, and is set to 700µs by default via the OTP.
6	t_{MAX}[5]	0	N	N	R/W	6400µs.	
5	t_{MAX}[4]	0	N	N	R/W	3200µs.	
4	t_{MAX}[3]	0	N	N	R/W	1600µs.	
3	t_{MAX}[2]	0	N	N	R/W	800µs.	
2	t_{MAX}[1]	1	N	N	R/W	400µs.	
1	t_{MAX}[0]	1	N	N	R/W	200µs.	
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Reserved.

REG11H: Two-Level Input Current Limit Period Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{PERIOD}[6]	0	N	N	R/W	12800µs.	These bits set the total time duration of for the second and first input current limit (RS1 = 10mΩ). It has a 200µs offset, 200µs to 25.6ms range, and is set to 0000 111 (1600µs) by default via the OTP.
6	t_{PERIOD}[5]	0	N	N	R/W	6400µs.	
5	t_{PERIOD}[4]	0	N	N	R/W	3200µs.	
4	t_{PERIOD}[3]	0	N	N	R/W	1600µs.	
3	t_{PERIOD}[2]	1	N	N	R/W	800µs.	
2	t_{PERIOD}[1]	1	N	N	R/W	400µs.	
1	t_{PERIOD}[0]	1	N	N	R/W	200µs.	
0	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.

REG12H: Input OCP Threshold for Triggering PROCHOT

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	I_{IN_OCP}[3]	1	N	N	R/W	6400mA.	These bits set the input over-current threshold. PROCHOT is triggered when the input current exceeds this threshold. It has a 700mA offset, and a 11.9A default via the OTP.
5	I_{IN_OCP}[2]	1	N	N	R/W	3200mA.	
4	I_{IN_OCP}[1]	1	N	N	R/W	1600mA.	
3	I_{IN_OCP}[0]	0	N	N	R/W	800mA.	
2	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.

1	DIG_SKIP_EN	1	N	N	R/W	0: Disabled 1: Enabled	When this bit is 1, digital skip mode is enabled to skip PWM when the load is light for all loops. Set by the OTP.
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Reserved.

REG13H: Status Register

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	BATT_UVLO	0	N/A	N/A	R	0: Battery voltage UVLO has not occurred 1: Battery voltage UVLO has occurred	This bit indicates the battery voltage under-voltage lockout (UVLO) status. It is set to 0 by default.
6	VSYS_UV	0	N/A	N/A	R	0: The system does not have a UV condition 1: The system has a UV condition	This bit indicates an under-voltage (UV) condition, which triggers short-circuit protection. It is set to 0 by default.
5	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
4	PPM_STAT	0	N/A	N/A	R	0: No DPM 1: VINDPM or INDPM	This bit indicates the power path management status. It is set to 0 by default.
3	CHG_STAT[1]	0	N/A	N/A	R	00: Not charging 01: Pre-charge 10: Fast charging or trickle charge 11: Charge termination	These bits indicate the charging status. They are set to 00 by default.
2	CHG_STAT[0]	0	N/A	N/A	R		
1	ACOK	0	N/A	N/A	R	0: V_{IN} not power good 1: V_{IN} power good	This bit indicates the power good status. It is set to 0 by default.
0	VSYS_STAT	0	N/A	N/A	R	0: In VSYSMIN regulation 1: Not in VSYSMIN regulation	This bit indicates the VSYS regulation status. It is set to 0 by default.

REG14H: Fault Register

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG_FAULT	0	N/A	N/A	R	0: Normal operation 1: The watchdog timer has expired	This bit indicates whether a watchdog fault has occurred. It is set to 0 by default.
6	OTG_FAULT	0	N/A	N/A	R	0: Normal operation 1: VBUS is overloaded, or VBUS over-voltage protection (OVP) has occurred	This bit indicates whether an OTG mode fault has occurred. It is set to 0 by default.
5	CHG_FAULT [1]	0	N/A	N/A	R	00: Normal operation 01: Input over-voltage protection (OVP) has occurred 10: Thermal shutdown has occurred 11: The safety timer has expired	These bits indicate whether a charge fault has occurred. They are set to 00 by default. If several faults occur, it goes in the following order: 01, 10, then 11.
4	CHG_FAULT [0]	0	N/A	N/A	R		
3	BATT_FAULT	0	N/A	N/A	R	0: Normal operation 1: Battery over-voltage protection (OVP) has occurred	This bit indicates whether a battery fault has occurred. It is set to 0 by default.
2	NTC_FAULT [2]	0	N/A	N/A	R	000: Normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot	These bits indicate whether an NTC fault has occurred. They are set to 000 by default.
1	NTC_FAULT [1]	0	N/A	N/A	R		
0	NTC_FAULT [0]	0	N/A	N/A	R		

REG16~17H: ADC Battery Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{BATT}[9]	N/A	N/A	N/A	R	6400mV.	These bits indicate the ADC conversion of the battery voltage.
14	V_{BATT}[8]	N/A	N/A	N/A	R	3200mV.	
13	V_{BATT}[7]	N/A	N/A	N/A	R	1600mV.	
12	V_{BATT}[6]	N/A	N/A	N/A	R	800mV.	
11	V_{BATT}[5]	N/A	N/A	N/A	R	400mV.	
10	V_{BATT}[4]	N/A	N/A	N/A	R	200mV.	
9	V_{BATT}[3]	N/A	N/A	N/A	R	100mV.	
8	V_{BATT}[2]	N/A	N/A	N/A	R	50mV.	
7	V_{BATT}[1]	N/A	N/A	N/A	R	25mV.	
6	V_{BATT}[0]	N/A	N/A	N/A	R	12.5mV.	

5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG18~19H: ADC System Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{SYS}[9]	N/A	N/A	N/A	R	6400mV.	These bits indicate the ADC conversion of the system voltage.
14	V_{SYS}[8]	N/A	N/A	N/A	R	3200mV.	
13	V_{SYS}[7]	N/A	N/A	N/A	R	1600mV.	
12	V_{SYS}[6]	N/A	N/A	N/A	R	800mV.	
11	V_{SYS}[5]	N/A	N/A	N/A	R	400mV.	
10	V_{SYS}[4]	N/A	N/A	N/A	R	200mV.	
9	V_{SYS}[3]	N/A	N/A	N/A	R	100mV.	
8	V_{SYS}[2]	N/A	N/A	N/A	R	50mV.	
7	V_{SYS}[1]	N/A	N/A	N/A	R	25mV.	
6	V_{SYS}[0]	N/A	N/A	N/A	R	12.5mV.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG1A~1BH: ADC Battery Charge Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{CHG}[9]	N/A	N/A	N/A	R	6400mA.	These bits indicate the ADC conversion of the charge current.
14	I_{CHG}[8]	N/A	N/A	N/A	R	3200mA.	
13	I_{CHG}[7]	N/A	N/A	N/A	R	1600mA.	
12	I_{CHG}[6]	N/A	N/A	N/A	R	800mA.	
11	I_{CHG}[5]	N/A	N/A	N/A	R	400mA.	
10	I_{CHG}[4]	N/A	N/A	N/A	R	200mA.	
9	I_{CHG}[3]	N/A	N/A	N/A	R	100mA.	
8	I_{CHG}[2]	N/A	N/A	N/A	R	50mA.	
7	I_{CHG}[1]	N/A	N/A	N/A	R	25mA.	
6	I_{CHG}[0]	N/A	N/A	N/A	R	12.5mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG1C~1DH: ADC Input Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{IN}[9]	N/A	N/A	N/A	R	12800mV.	These bits indicate the ADC conversion of the input voltage.
14	V_{IN}[8]	N/A	N/A	N/A	R	6400mV.	
13	V_{IN}[7]	N/A	N/A	N/A	R	3200mV.	
12	V_{IN}[6]	N/A	N/A	N/A	R	1600mV.	
11	V_{IN}[5]	N/A	N/A	N/A	R	800mV.	
10	V_{IN}[4]	N/A	N/A	N/A	R	400mV.	
9	V_{IN}[3]	N/A	N/A	N/A	R	200mV.	
8	V_{IN}[2]	N/A	N/A	N/A	R	100mV.	
7	V_{IN}[1]	N/A	N/A	N/A	R	50mV.	
6	V_{IN}[0]	N/A	N/A	N/A	R	25mV.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG1E~1FH: ADC Input Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{IN}[9]	N/A	N/A	N/A	R	3200mA.	These bits indicate the ADC conversion of the input current.
14	I_{IN}[8]	N/A	N/A	N/A	R	1600mA.	
13	I_{IN}[7]	N/A	N/A	N/A	R	800mA.	
12	I_{IN}[6]	N/A	N/A	N/A	R	400mA.	
11	I_{IN}[5]	N/A	N/A	N/A	R	200mA.	
10	I_{IN}[4]	N/A	N/A	N/A	R	100mA.	
9	I_{IN}[3]	N/A	N/A	N/A	R	50mA.	
8	I_{IN}[2]	N/A	N/A	N/A	R	25mA.	
7	I_{IN}[1]	N/A	N/A	N/A	R	12.5mA.	
6	I_{IN}[0]	N/A	N/A	N/A	R	6.25mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG20~21H: ADC OTG Output Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{IN_OTG}[9]	N/A	N/A	N/A	R	12800mV.	These bits indicate the ADC conversion of the OTG voltage 5V to 12.5mV/LSB. For all others, 25mV/LSB.
14	V_{IN_OTG}[8]	N/A	N/A	N/A	R	6400mV.	
13	V_{IN_OTG}[7]	N/A	N/A	N/A	R	3200mV.	
12	V_{IN_OTG}[6]	N/A	N/A	N/A	R	1600mV.	
11	V_{IN_OTG}[5]	N/A	N/A	N/A	R	800mV.	
10	V_{IN_OTG}[4]	N/A	N/A	N/A	R	400mV.	
9	V_{IN_OTG}[3]	N/A	N/A	N/A	R	200mV.	
8	V_{IN_OTG}[2]	N/A	N/A	N/A	R	100mV.	
7	V_{IN_OTG}[1]	N/A	N/A	N/A	R	50mV.	
6	V_{IN_OTG}[0]	N/A	N/A	N/A	R	25mV.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG22~23H: ADC OTG Output Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{OTG}[9]	N/A	N/A	N/A	R	3200mA.	These bits indicate the ADC conversion of the OTG current.
14	I_{OTG}[8]	N/A	N/A	N/A	R	1600mA.	
13	I_{OTG}[7]	N/A	N/A	N/A	R	800mA.	
12	I_{OTG}[6]	N/A	N/A	N/A	R	400mA.	
11	I_{OTG}[5]	N/A	N/A	N/A	R	200mA.	
10	I_{OTG}[4]	N/A	N/A	N/A	R	100mA.	
9	I_{OTG}[3]	N/A	N/A	N/A	R	50mA.	
8	I_{OTG}[2]	N/A	N/A	N/A	R	25mA.	
7	I_{OTG}[1]	N/A	N/A	N/A	R	12.5mA.	
6	I_{OTG}[0]	N/A	N/A	N/A	R	6.25mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG24~25H: ADC Junction Temperature Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	TJ[9]	N/A	N/A	N/A	R	512	These bits indicate the ADC conversion of the IC junction temperature sense. T_J = 903 - 2.578 x T(°C).
14	TJ[8]	N/A	N/A	N/A	R	256	
13	TJ[7]	N/A	N/A	N/A	R	128	
12	TJ[6]	N/A	N/A	N/A	R	64	
11	TJ[5]	N/A	N/A	N/A	R	32	
10	TJ[4]	N/A	N/A	N/A	R	16	
9	TJ[3]	N/A	N/A	N/A	R	8	
8	TJ[2]	N/A	N/A	N/A	R	4	
7	TJ[1]	N/A	N/A	N/A	R	2	
6	TJ[0]	N/A	N/A	N/A	R	1	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG26~27H: ADC System Power Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	P_{SYS}[9]	N/A	N/A	N/A	R	64W.	These bits indicate the ADC conversion of the system power.
14	P_{SYS}[8]	N/A	N/A	N/A	R	32W.	
13	P_{SYS}[7]	N/A	N/A	N/A	R	16W.	
12	P_{SYS}[6]	N/A	N/A	N/A	R	8W.	
11	P_{SYS}[5]	N/A	N/A	N/A	R	4W.	
10	P_{SYS}[4]	N/A	N/A	N/A	R	2W.	
9	P_{SYS}[3]	N/A	N/A	N/A	R	1W.	
8	P_{SYS}[2]	N/A	N/A	N/A	R	0.5W.	
7	P_{SYS}[1]	N/A	N/A	N/A	R	0.25W.	
6	P_{SYS}[0]	N/A	N/A	N/A	R	0.125W.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG28~29H: ADC Battery Discharge Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{BATT_DSG}[9]	N/A	N/A	N/A	R	6400mA.	These bits indicate the ADC conversion of the battery discharge current.
14	I_{BATT_DSG}[8]	N/A	N/A	N/A	R	3200mA.	
13	I_{BATT_DSG}[7]	N/A	N/A	N/A	R	1600mA.	
12	I_{BATT_DSG}[6]	N/A	N/A	N/A	R	800mA.	
11	I_{BATT_DSG}[5]	N/A	N/A	N/A	R	400mA.	
10	I_{BATT_DSG}[4]	N/A	N/A	N/A	R	200mA.	
9	I_{BATT_DSG}[3]	N/A	N/A	N/A	R	100mA.	
8	I_{BATT_DSG}[2]	N/A	N/A	N/A	R	50mA.	
7	I_{BATT_DSG}[1]	N/A	N/A	N/A	R	25mA.	
6	I_{BATT_DSG}[0]	N/A	N/A	N/A	R	12.5mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG2BH: Battery Over-Voltage Protection Deglitch Time

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	VBATT_ OVP_DGL	1	N	N	R/W	0: 200μs 1: 0μs	This bit is set to 1 by default via the OTP.

REG2DH: Battery Voltage Loop Enable

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	VBATT_ LP_EN	1	N	N	R/W	0: Disabled 1: Enabled	This bit is set to 1 by default.

REG30H: Battery Pre-charge Threshold Option

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	VBATT_PR E_SEL	1	N	N	R/W	0: Option1 1: Option2	This bit is set to 1 by default via the OTP.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG31H: System Voltage Threshold for Pulse Skipping

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	VSYS_SKIP [1]	1	N	N	R/W	00: 102% 01: 103% 10: 104% 11: 101%	These bits are set to 11 by default via the OTP.
0	VSYS_SKIP [0]	1	N	N	R/W		

REG33H: INT Mask for Hi-Z Mode Entry and Exit

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	HIZ_INT_ MASK	1	N	N	R/W	0: Masked 1: Not masked	This bit configures the INT output for Hi-Z mode entry and exit. It is set to 1 by default via the OTP.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG36H: Analog Frequency Loop Enable

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	FS_LOOP_	0	N	N	R/W	0: Disable the analog	When the analog

	EN					frequency loop 1: Enable the analog frequency loop	frequency loop is disabled, an alternative t_{OFF} calculation is used to calibrate the switching frequency.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG40~41H: ADC Result for NTC voltage

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
14	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
13	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
12	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
11	NTC [11]	N/A	N/A	N/A	R	2048	These bits indicate the ADC conversion of the NTC voltage versus the reference voltage (1.6V). The real NTC voltage is NTC [11:0] x 1.6V/4096.
10	NTC [10]	N/A	N/A	N/A	R	1024	
9	NTC [9]	N/A	N/A	N/A	R	512	
8	NTC 8]	N/A	N/A	N/A	R	256	
7	NTC [7]	N/A	N/A	N/A	R	128	
6	NTC [6]	N/A	N/A	N/A	R	64	
5	NTC [5]	N/A	N/A	N/A	R	32	
4	NTC [4]	N/A	N/A	N/A	R	16	
3	NTC [3]	N/A	N/A	N/A	R	8	
2	NTC [2]	N/A	N/A	N/A	R	4	
1	NTC [1]	N/A	N/A	N/A	R	2	
0	NTC [0]	N/A	N/A	N/A	R	1	

REG48H: Hi-Z Mode Indication (DC/DC Switcher is Off)

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	HI-Z MODE	0	N/A	N/A	R	0: Buck charge or boost charge mode 1: Hi-Z mode	This bit indicates the state of the DC/DC operation.

APPLICATION INFORMATION

Selecting the Input Current-Sense Filter

The MP2762A has an input current loop to limit the output current drawn from the USB port. An external current-sense resistor is required to sense the average input current. The input current sensed through IAP/IAN covers the ripple current and improves the input current accuracy and loop stability.

Figure 19 shows a recommended application that can filter noise.

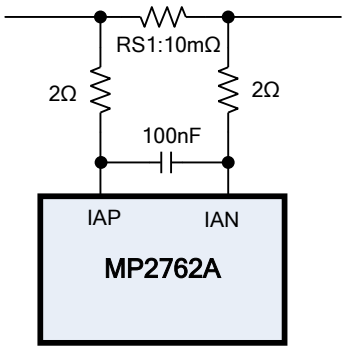


Figure 19: Input Current-Sense Filter

Selecting the Input Capacitor

The input capacitor from the typical application circuit absorbs the maximum ripple current from the PWM converter (see Figure 22 on page 56). The worst-case RMS ripple current is half of the output current when the duty cycle is 50% in buck mode, estimated with Equation (5):

$$I_{CIN\_RMS} = I_{SYS} x \frac{\sqrt{V_{SYS} x (V_{IN} - V_{SYS})}}{V_{IN}} \quad (5)$$

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended to be the input decoupling capacitor, and should be placed as close as possible to IN and PGND. Their voltage rating must exceed the normal input voltage level. A capacitor with a minimum 25V rating is recommended for input voltages between 19V and 20V.

Selecting the VMAX_BST Output Capacitor

The MP2762A has an integrated charge pump to power the high-side MOSFET (HS-FET) driver. An external output capacitor must be placed between the VMAX_BST pin and PGND to act as an output capacitor for the integrated charge pump. In addition to the charge pump output, several other paths can supplement the output capacitor (see Figure 20). To limit the inrush current flowing into the capacitor during input power or battery hot insertion, place an additional 100Ω resistor in series with the charge pump output capacitor.

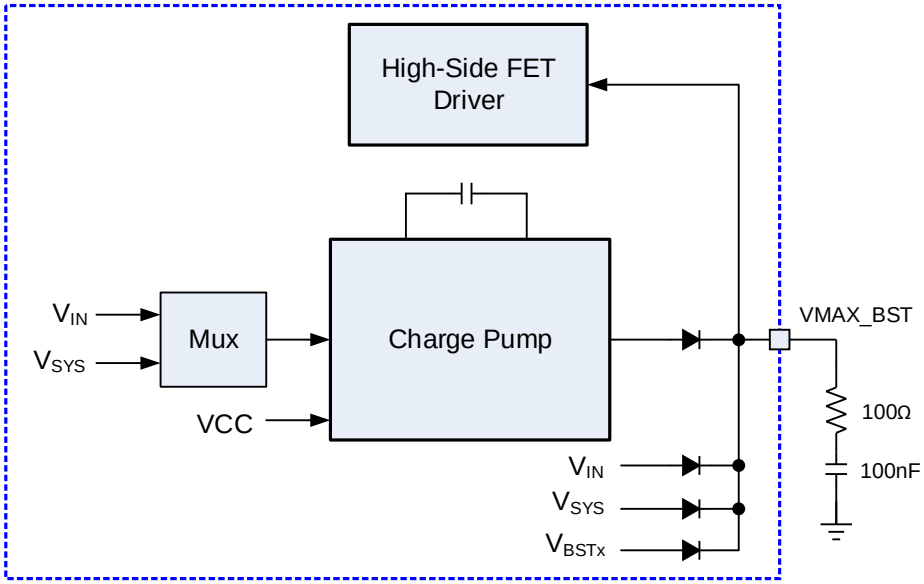


Figure 20: VMAX_BST Circuit Diagram

VCC Decoupling Capacitor

VCC is an internal LDO output. An external 10µF decoupling capacitor must be placed between VCC and AGND.

INT and PROCHOT Pull-Up

Both the $\overline{INT}$ and $\overline{PROCHOT}$ pins are open-drain outputs that interrupt operation if any status or faults occurs. To deliver high logic, these pins must be pulled up to an external power source by 10kΩ to 100kΩ resistors.

NTC Sense Resistive Divider

In real applications, an external thermistor (negative temperature coefficient) is placed close to the battery to sense the battery's temperature. The MP2762A measures the battery temperature by monitoring the voltage ratio between the NTC and VNTC pins (see Figure 21). Every temperature corresponds to a voltage ratio. The MP2762A has four temperature thresholds to satisfy JEITA requirements.

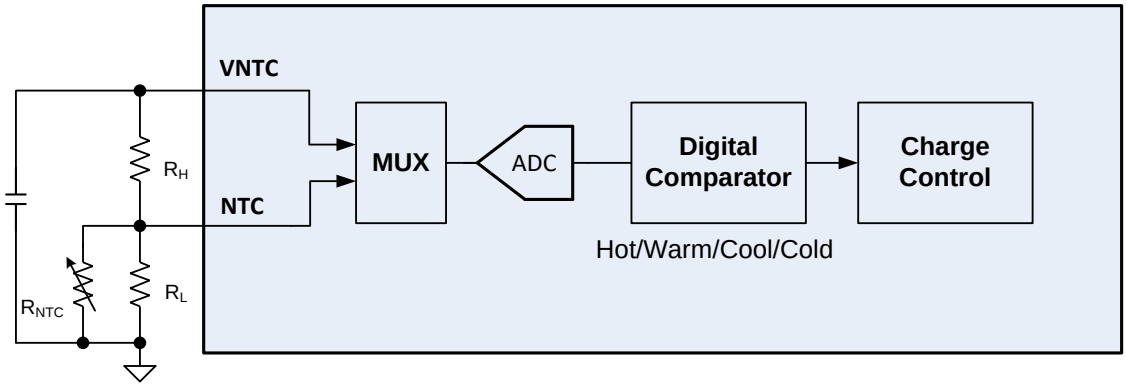


Figure 21: Temperature Sensing

For a given NTC thermistor, the NTC hot and cold temperature points can be calculated with Equation (6) and Equation (7), respectively:

$$\frac{\frac{R_L x R_{NTC\_HOT}}{R_L + R_{NTC\_HOT}}}{R_H + \frac{R_L x R_{NTC\_HOT}}{R_L + R_{NTC\_HOT}}} = \frac{V_{HOT}}{V_{VNTC}} \quad (6)$$

$$\frac{\frac{R_L x R_{NTC\_COLD}}{R_L + R_{NTC\_COLD}}}{R_H + \frac{R_L x R_{NTC\_COLD}}{R_L + R_{NTC\_COLD}}} = \frac{V_{COLD}}{V_{VNTC}} \quad (7)$$

Where R_{NTC_HOT} is the thermistor value at the expected hot temperature protection point, and R_{NTC_COLD} is the thermistor value at the expected cold temperature protection point. V_{HOT} / V_{VNTC} and V_{COLD} / V_{VNTC} are 48.3% and 71.1%, respectively.

Assume the expected hot and cold temperature thresholds are 60°C and 0°C. Using a 104AT thermistor as an example, the thermistor values are:

- R_{NTC_COLD} = 390.3kΩ
- R_{NTC_HOT} = 19.72kΩ

R_H and R_L can be calculated with Equation (6) and Equation (7). R_H = 13.79kΩ and R_L = 37.15kΩ.

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor offers a smaller size, but results in higher ripple current, magnetic hysteresis losses, and output capacitance. The inductor ripple current should not exceed 30% of the maximum load current under worst-case conditions.

The MP2762A has three options for the switching frequency. A higher switching frequency allows the use of smaller inductor and capacitor values. The inductor saturation current should be higher than the load current plus half the ripple current. The MP2762A supports interleaving dual-phase operation, which reduces the output current ripple. This allows a smaller inductor to be used, which balances DCR and size. The recommended inductors are based on a 50% current ripple.

The inductor ripple current in buck operation depends on the input voltage, duty cycle, switching frequency, and inductance. The inductance can be calculated with Equation (8):

$$L=\frac{V_{IN}-V_{SYS}}{\Delta I_L} x \frac{V_{SYS}}{V_{IN} x f_{SW}} \quad (8)$$

The inductor's peak current can be calculated with Equation (9):

$$I_{PEAK}=I_{LOAD(MAX)} x \left(1+\frac{\Delta I_L}{2}\right) \quad (9)$$

Where V_{IN} is the input voltage, V_{SYS} is the system voltage, f_{SW} is the switching frequency, and ΔI_L is the expected inductor current ripple.

Table 2 lists how to select the inductance based on different voltages in buck mode.

Table 2: Inductance Values for Buck Mode

Specs	Inductance Selection				
V_{IN}	Calculations	L_{MIN}	L	I_{SAT}	DCR (mΩ)
9V	$L=\frac{V_{IN}-V_{SYS}}{\Delta I_L} x \frac{V_{SYS}}{V_{IN} x f_{SW}}$ ΔI_L = 0.5 x I_{SYS} = 3A f_{SW} = 800kHz	0.65µH	1.5µH	>6.7	<20
12V		1.2µH	1.5µH	>7.1	<20
15V		1.5µH	1.5µH	>7.5	<20
20V		2.0µH	2.2µH	>7.4	<20

When the MP2762A operates in boost mode, the required inductance can be estimated with Equation (10):

$$L=\frac{V_{IN} x (V_{SYS}-V_{IN})}{V_{SYS} x f_{SW} x \Delta I_L} \quad (10)$$

The peak current of the inductor can be estimated with Equation (11):

$$I_{PEAK}=I_{IN(MAX)} x \left(1+\frac{\Delta I_L}{2}\right) \quad (11)$$

Table 3 lists how to select the inductance based on different voltages in boost mode.

Table 3: Inductance Values for Boost Mode

Specs	Inductance Selection				
V_{IN}	Calculations	L_{MIN}	L	I_{SAT}	DCR (mΩ)
5V	$L=\frac{V_{IN} x (V_{SYS}-V_{IN})}{V_{SYS} x f_{SW} x \Delta I_L}$ ΔI_L = 0.5 x I_{IN} = 2.5A f_{SW} = 800kHz	1.1µH	1.5µH	>7	<20

A 1.5µH inductor with a >7.5A saturation current is recommended for most specifications. However, for applications that allow for a higher ripple current, a lower-value inductor can be used to reduce PCB size.

Selecting the System Capacitor

The output capacitor (C_{SYS}) from the typical application circuit is parallel to the SYS load (see Figure 22 on page 56). C_{SYS} absorbs the high-frequency switching ripple current and smooths the output voltage. Its impedance must be below that of the system load to ensure that it absorbs the ripple current.

Ceramic capacitors are recommended for their low ESR and small size, which allows the ESR of the output capacitor to be ignored.

The output voltage ripple can be estimated with Equation (12):

$$\frac{\Delta V_{SYS}}{V_{SYS}}=\frac{1-\frac{V_{SYS}}{V_{IN}}}{8 x C_{SYS} x f_{SW} x L} \quad (12)$$

The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage. Assume that ±0.2% output ripple voltage should be obtained CCM mode.

Then C_{SYS} can be estimated with Equation (13):

$$C_{SYS} = \frac{1-\frac{V_{SYS}}{V_{IN}}}{8xf_{SW}xLx\frac{\Delta V_{SYS}}{V_{SYS}}} \quad (13)$$

Based on Equation (13), C_{SYS} must be 44µF.

To further improve loop stability, use a minimum 60µF capacitor. For an output capacitor, the recommended ceramic capacitor is 25V, with X7R or X5R dielectrics.

PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A 4-layer or greater PCB is recommended. For the best performance, refer to Figure 22 and follow the guidelines below:

1. The VMAX_BST capacitor should be connected to PGND. Place one 100Ω resistor in series with the VMAX_BST capacitor.
2. Connect AGND to PGND to each decoupling capacitor via a single-point connection.
3. Connect SW2 to BST2, and place a BST capacitor directly on top of BST2. The internal path for BST2 is longer than BST1, so the two phases require additional leverage.
4. Place the VCC capacitor close to the VCC and AGND pins.
5. A Kelvin connection is required for the input current-sense resistor.
6. Place capacitors between VIN and PGND, as close as possible.
7. For the input current sense, use CM and DM filters.

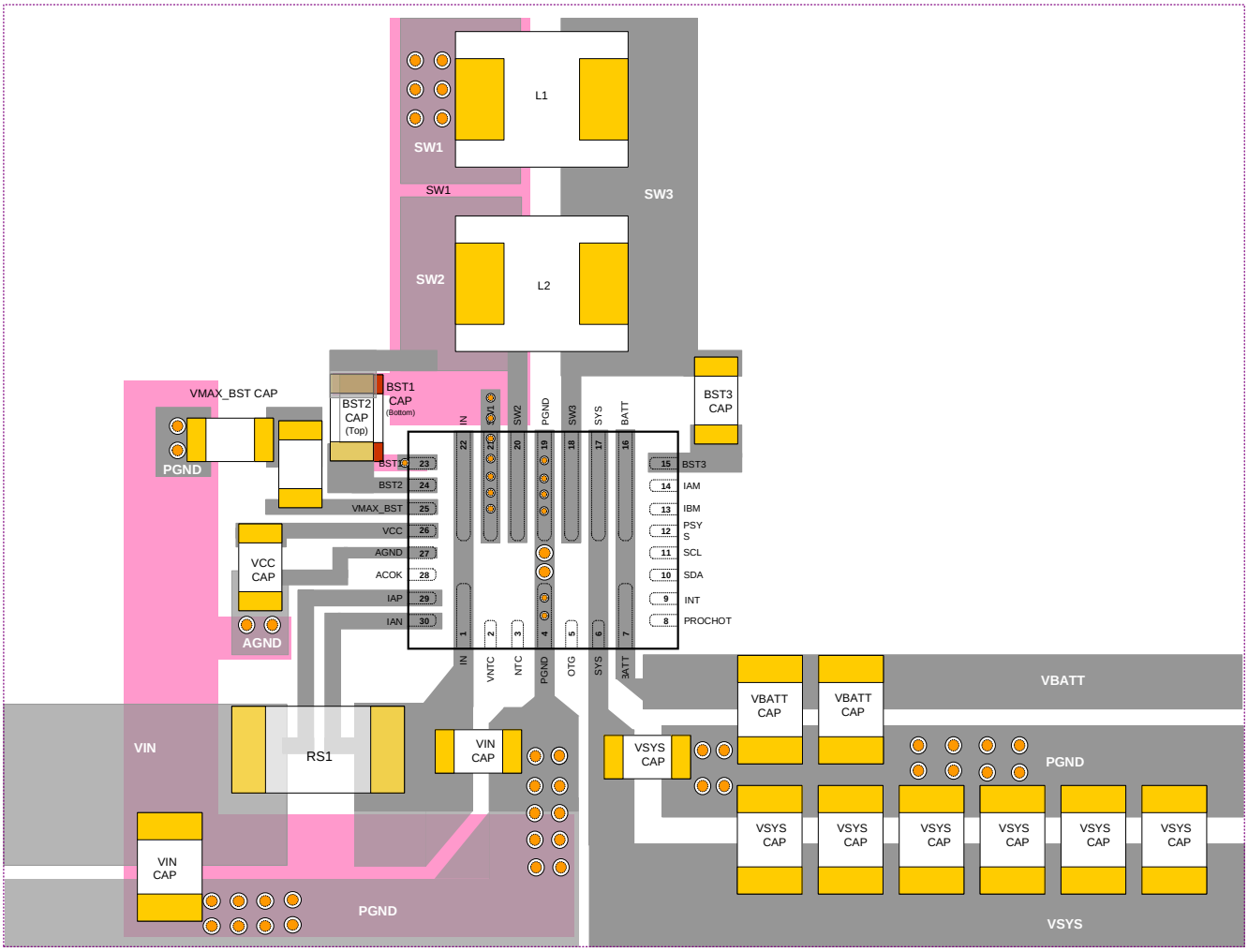


Figure 22: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

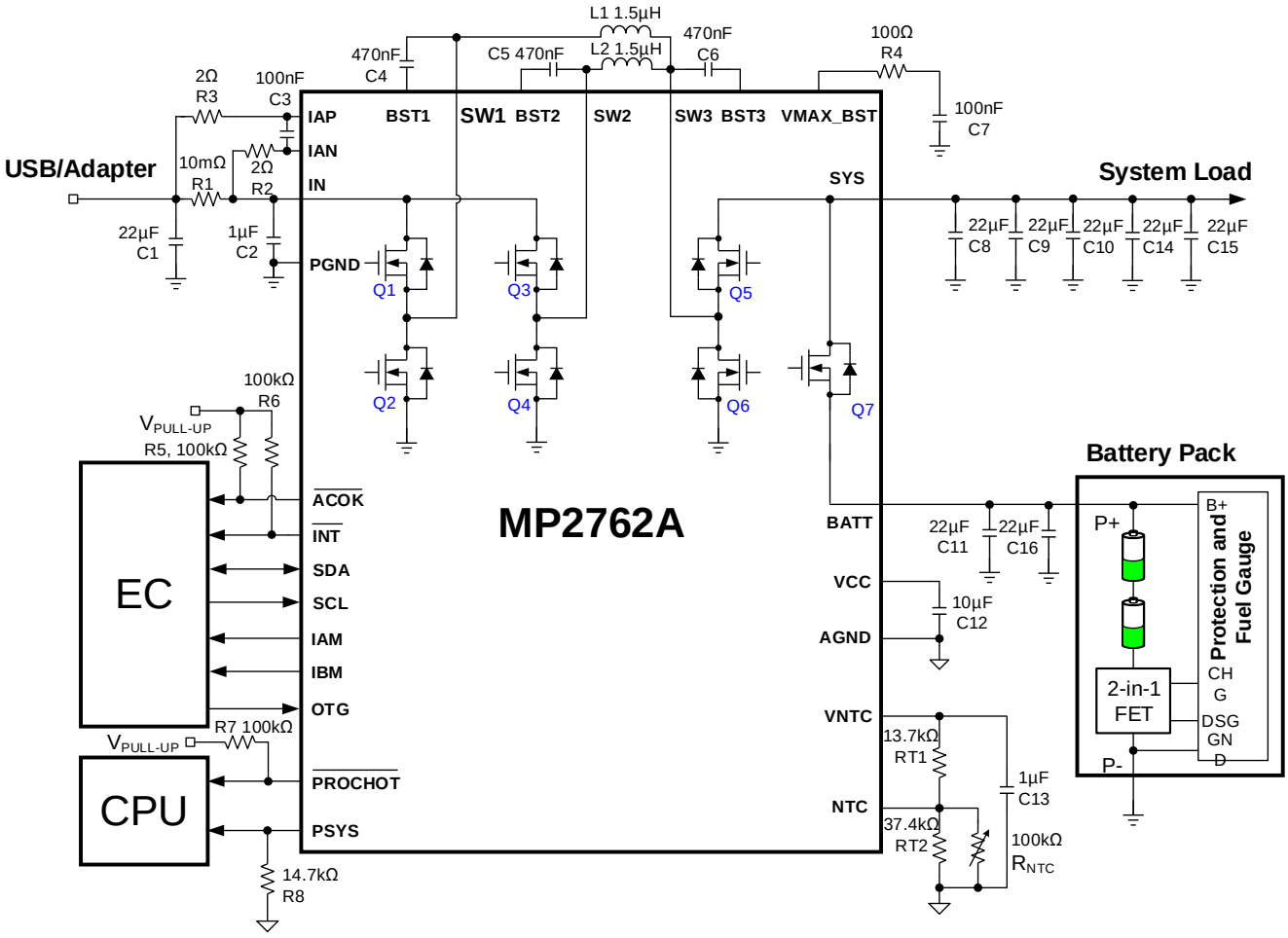


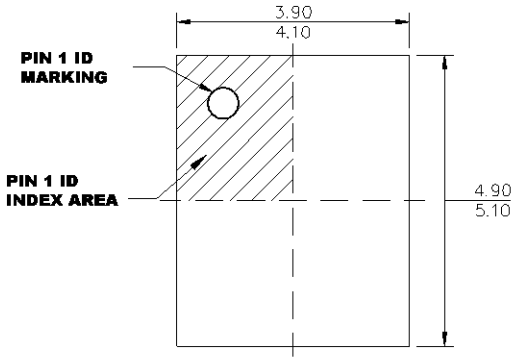
Figure 23: Typical Application Circuit

Table 4: Key BOM for Figure 23

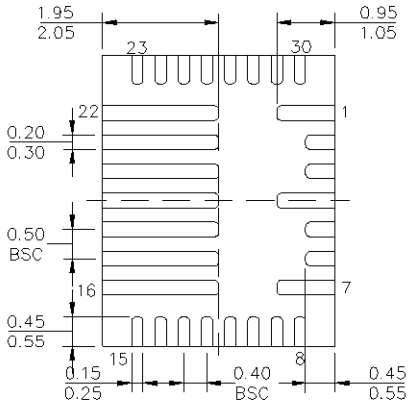
Qty	Ref	Value	Description	Package	Manufacturer
8	C1, C8, C9, C10, C11, C14, C15, C16	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C2	1µF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C3	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
3	C4, C5, C6	470nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C7	100nF	Ceramic capacitor, 50V, X5R or X7R	0603	Any
1	C12	10µF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	R1	10mΩ	Film resistor, 1%	1206	Any
2	R2, R3	2Ω	Film resistor, 1%	0603	Any
1	R4	100Ω	Film resistor, 1%	0603	Any
1	RT1	13.7kΩ	Film resistor, 1%	0603	Any
1	RT2	37.4kΩ	Film resistor, 1%	0603	Any
2	L1, L2	1.5µH	Inductor, 1.5µH, low DCR, I_{SAT} >7A	SMD	Any

PACKAGE INFORMATION

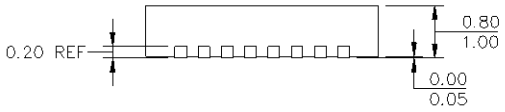
QFN-30 (4mmx5mm)



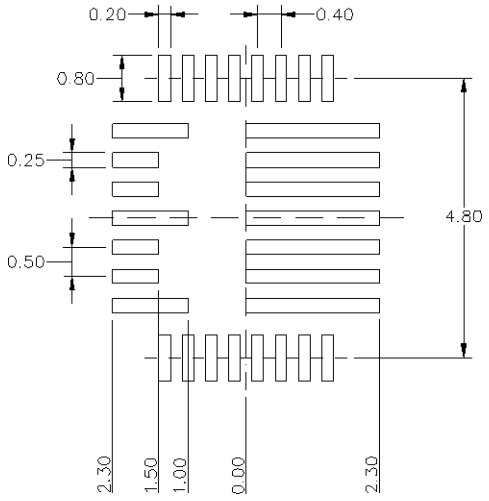
TOP VIEW



BOTTOM VIEW



SIDE VIEW

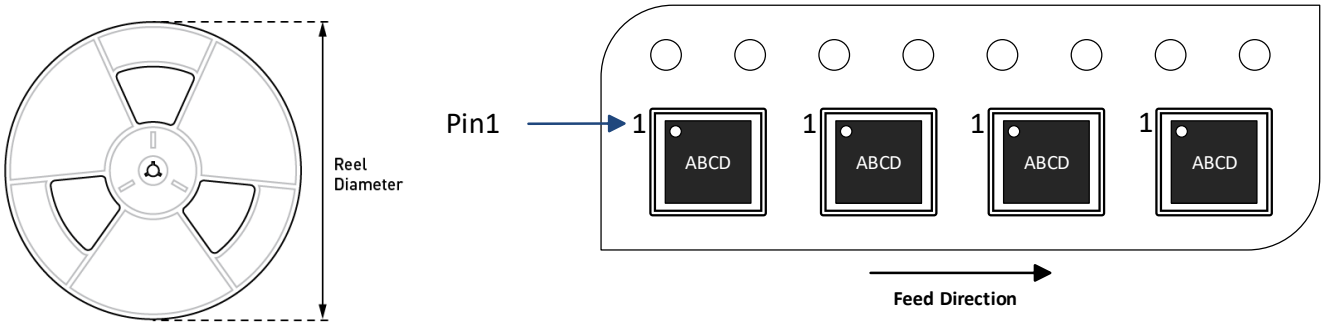


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,4 AND PIN7 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERN OF PIN16~22 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2762AGV-xxxx–Z	QFN-30 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	12/11/2020	Initial Release	-

单击下面可查看定价，库存，交付和生命周期等信息

>>MPS(芯源系统)