GT25C08

Automotive (A2)

SPI

8K Bits EEPROM

GT25C08

Table of Contents

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1. Features

- Serial Peripheral Interface (SPI) Compatible
  — Supports Mode 0 (0,0) and Mode 3 (1,1)
- Wide-voltage Operation
  — V_{CC} = 2.5V to 5.5V
- Low power CMOS
  — Standby current: ≤2 μA (5.5V)
  — Operating current: ≤3 mA (5.5V)
- Operating frequency: 20 MHz (5.5V)
- Memory organization: 8Kb (1,024 x 8)
- Byte and Page write (up to 32 bytes)
  — Partial page write allowed

- Block Write Protection
  — Protect 1/4, 1/2, or Entire Array
- Self timed write cycle: 5 ms (max.)
- High-reliability
  — Endurance: 1 million cycles
  — Data retention: 100 years
- Compliant with automotive standard AEC-Q100 grade 2
- Packages (8-pin): SOIC, TSSOP
- Lead-free, RoHS, Halogen free, Green

2. General Description

The GT25C08 is a standard electrically erasable programmable read only memory (EEPROM) product that utilizes standard Serial Peripheral Interface (SPI) for communications. The GT25C08 contains a memory array of 8K bits (1,024x 8), which is organized in 32 bytes per page. This EEPROM operates in a wide voltage range from 2.5V to 5.5V, which fits most application. The device provides low-power operations and low standby current. The product is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC and TSSOP.

The functionalities of the GT25C08 are optimized for most applications, such as consumer electronics, wireless, telecommunication, industrial, medical, instrumentation, commercial and others, where low-power and low-voltage are vital. This product has a compatible SPI interface: Chip-Select ($\overline{CS}$), Serial Data In (SI), Serial Data Out (SO) and Serial Clock (SCK) for high-speed communication. Furthermore, a Hold feature via $\overline{HOLD}$ pin allows the device entering into a suspended state whenever

necessary and resuming the communication without re-initializing the serial sequence. A Status Register facilitates a flexible write protection mechanism and device status monitoring.

In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is implemented. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into Standby mode. This should also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the V_{CC} is within its operating level.

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3. Functional Block Diagram
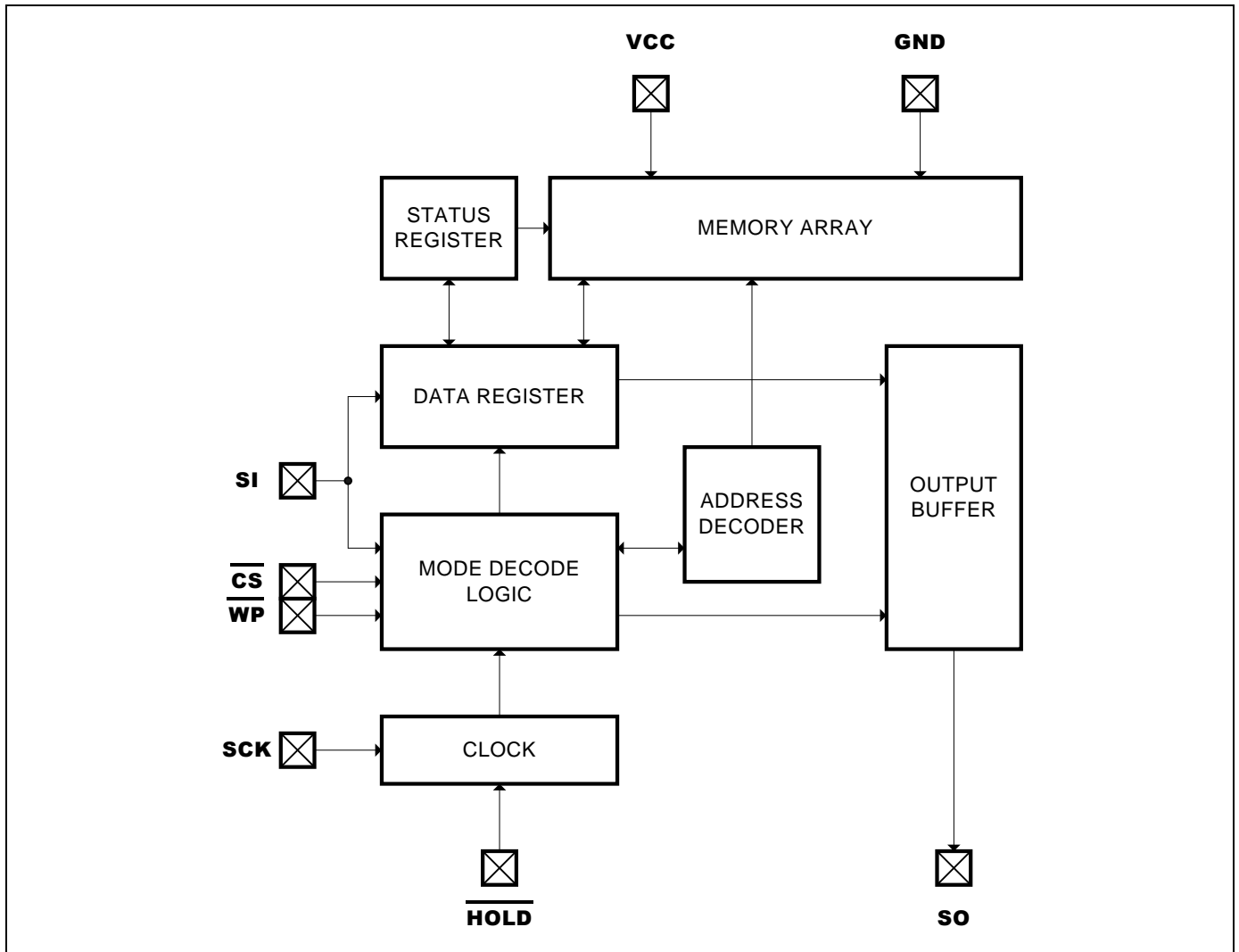
Serial Interface Description

Master:	The device that provides a clock signal.
Slave:	GT25C08.
Transmitter/Receiver:	The GT25C08 has both data input (SI) and data output (SO).
MSB	MSB (Most Significant Bit) is the first bit being transmitted or received.
Op-Code:	Operational instruction code typically sent to the GT25C08 is the first byte of information transmitted after $\overline{CS}$ is Low. If the Op-Code is a valid instruction as listed in Table 5.3, then it will be decoded appropriately. It is prohibited to send an invalid Op-Code.

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4. Pin Configuration

4.1 8-Pin SOIC and TSSOP

Top View

```
        ___
        CS  |1      8| Vcc
             ___
        SO  |2      7| HOLD
        ___
        WP  |3      6| SCK
       GND  |4      5| SI
```
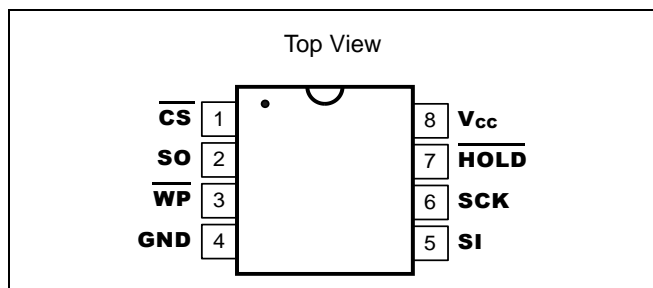
4.2 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	$\overline{CS}$	I	Chip Select
2	SO	O	Serial Data Output
3	$\overline{WP}$	I	Write Protect Input
4	GND	-	Ground
5	SI	I	Serial Data Input
6	SCK	I	Serial Clock
7	$\overline{HOLD}$	I	Hold function
8	V_{CC}	-	Supply Voltage

4.3 Pin Descriptions

Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is used to enable or disable the device. Upon power-up, $\overline{CS}$ must follow the supply voltage. When the device is ready for instruction input, this signal requires a High-to-Low transition. Once $\overline{CS}$ is stable at Low, the device is enabled. Then the master and slave can communicate among each other through SCK, SI, and SO pins. Upon completion of transmission, $\overline{CS}$ must be driven to High in order to stop the operation or start the internal write operation. And the device will enter into standby mode, unless an internal write operation is in progress. During this mode, SO becomes high impedance.

Serial Clock (SCK)

Under the SPI modes (0, 0) and (1, 1), this clock signal provides synchronization between the master and GT25C08. Typically, Op-Codes, addresses and data are latched from SI at the rising edge of SCK, while data from SO are clocked out at the falling edge of SCK.

Serial Data Input (SI)

Data Input pin.

Serial Data Output (SO)

Data output pin.

Write Protect ($\overline{WP}$)

This active Low input signal is utilized to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being modified. To activate the Hardware Write Protection, $\overline{WP}$ must be Low simultaneously when WPEN is set to 1.

Hold ($\overline{HOLD}$)

This feature is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). The $\overline{HOLD}$ signal transitions must occur only when SCK is Low and be held stable during SCK transitions. Connecting $\overline{HOLD}$ to High disables this feature. Figure. 5-8 shows Hold timing.

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5. Device Operation

5.1 Status Register

The Status Register accessible by the user consists of 8-bits data for write protection control and write status. It becomes Read-Only under any of the following conditions:

Hardware Write Protection is enabled or WEN is set to 0. If neither is true, it can be modified by a valid instruction.

Table 5.1: Status Register

Bit	Symbol	Name	Description
0	$\overline{RDY}$	Ready	When $\overline{RDY}$ = 0, device is ready for an instruction. When $\overline{RDY}$ = 1, device is busy. As busy, device only accepts Read Status Register command.
1	WEN	Write Enable	This represents the write protection status of the device. When WEN = 0, Status Register and entire array cannot be modified, regardless the setting of WPEN, $\overline{WP}$ pin or block protection. Write Enable command (WREN) can be used to set WEN to 1. Upon power-up stage, WEN is reset to 0.
2	BP0	Block Protect Bit	Despite of the status on WPEN, $\overline{WP}$ or WEN, BP0 and BP1 configure any combinations of the four blocks being protected (Table 5.2). They are non-volatile memory and programmed to 0 by factory.
3	BP1	Block Protect Bit	
4	X	Don't Care	Values can be either 0 or 1, but are not retained. Mostly always 0, except during write operation.
5	X	Don't Care	
6	X	Don't Care	
7	WPEN	Write Protect Enable	This bit can be utilized to enable Hardware Write Protection, together with $\overline{WP}$ pin. If enabled, Status Register becomes read-only. However, the memory array is not protected by this mode. Hardware Write Protection requires the setting of $\overline{WP}$ = 0 and WPEN = 1. Otherwise, it is disabled. WPEN cannot be altered from 1 to 0 if $\overline{WP}$ is already set to Low. (Table 5.4 for write protection)

Note: During internal write cycles, bits 0 to 7 are temporarily 1's.

Table 5.2: Block Protection by BP0 and BP1

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	300h-3FFh
2 (1/2)	1	0	200h-3FFh
3 (All)	1	1	000h-3FFh

5.2 Op-Code Instructions

The operations of the GT25C08 are controlled by a set of instruction Op-Codes (Table 5.3) that are clocked-in serially via SI pin. To initiate an instruction, the chip select ($\overline{CS}$) must be Low. Subsequently, each Low-to-High transition of the clock (SCK) will latch a stable level from SI. After the 8-bit Op-Code, it may continue to latch-in an address and/or data from SI accordingly, or to output data from SO. During data output, data are latched out at the falling edge of SCK. All communications start with MSB first. Upon the transmission of the last bit but prior to any following Low-to-High transition on SCK, $\overline{CS}$ must be brought to High in order to end the transaction and start the operation. The device will enter into Standby Mode after the operation is completed.

Table 5.3: Instruction Op-Codes[1,2,3]

Name	Op-Code	Operation	Address	Data (SI)	Data (SO)
WREN	0000 X110	Set Write Enable Latch	-	-	-
WRDI	0000 X100	Reset Write Enable Latch	-	-	-
RDSR	0000 X101	Read Status Register	-	-	D_7-D_0 -
WRSR	0000 X001	Write Status Register	-	D_7-D_0	-
READ	0000 X011	Read Data from Array	A_{15}-A_0	-	D_7-D_0, ...
WRITE	0000 X010	Write Data to Array	A_{15}-A_0	D_7-D_0, ...	-

Notes: [1] X = Don't care bit. However, it is recommended to be "0".

[2] Some address bits may be don't care (Table 5.5).

[3] It is strongly recommended that an appropriate format of Op-Code must be entered. Otherwise, it may cause unexpected phenomenon to be occurred. Nevertheless, it is illegal to input invalid any Op-Code.

5.3 Write Enable

When V_{CC} is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR) or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a Write Enable (WREN) instruction is necessary to set WEN to 1 (Figure. 5-2).

5.4 Write Disable

The device can be completely protected from modification by resetting WEN to 0 through the Write Disable (WRDI) instruction (Figure. 5-3).

5.5 Read Status Register

The Read Status (RDSR) instruction reviews the status of Write Protect Enable, Block Protection setting (Table 5.2), Write Enable state and $\overline{RDY}$ status. RDSR is the only instruction accepted when a write cycle is underway. It is recommended that the status of Write Enable and $\overline{RDY}$ be checked, especially prior to an attempted modification of data. These 8 bits information can be repeatedly output on SO after the initial Op-Code (Figure. 5-4).

5.6 Write Status Register

The Write Status Register (WRSR) instruction allows the user to choose a Block Protection setting and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1 and are not stored in the Status Register. WRSR will be ignored unless both following conditions are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled (Table 5.4). Except for $\overline{RDY}$ status, the values in the Status Register remain unchanged until the moment when the write cycle is completed and the register is updated. Note that WPEN can be changed from 1 to 0 only if $\overline{WP}$ is already set High. Once completed, WEN is reset for complete chip write protection (Fig. 5-5).

5.7 Read Data

This instruction includes an Op-Code and 16-bit address, then results the selected data to be shifted out from SO.

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Following the first data byte, additional sequential data can be output. If the data byte of the last address is initially output, then address will rollover to the first address in the array, and the output could loop indefinitely. At any time, a rising $\overline{CS}$ signal ceases the operation (Figure. 5-6).

5.8 Write Data

The WRITE instruction contains an Op-Code, a 16-bit address and the first data byte. Additional data bytes may be supplied sequentially after the first byte. Each WRITE instruction can affect up to 32 bytes of data in a page. Each page has a starting address XXXXXXXX XXX00000 and an ending address XXXXXXXX XXX11111. After the last byte of data in a page is input, the address rolls over to the

beginning of the same page. If more than 32 bytes of data is input during a single instruction, then only the last 32 bytes will be retained, but the initial data will be overwritten.

The contents of the array defined by Block Protection cannot be modified as long as that block configuration is selected. The contents of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction is initiated prior to WRITE. Once Write operation is completed, WEN is reset for complete chip write protection (Figure. 5-7). Besides, Hardware Write Protection has no affect on the memory array.

Table 5.4: Write Protection

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

Table 5.5: Address Key

Name	GT25C08
A_N	A_9-A_0
Don't Care Bit	A_{15}-A_{10}

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5.9. Diagrams
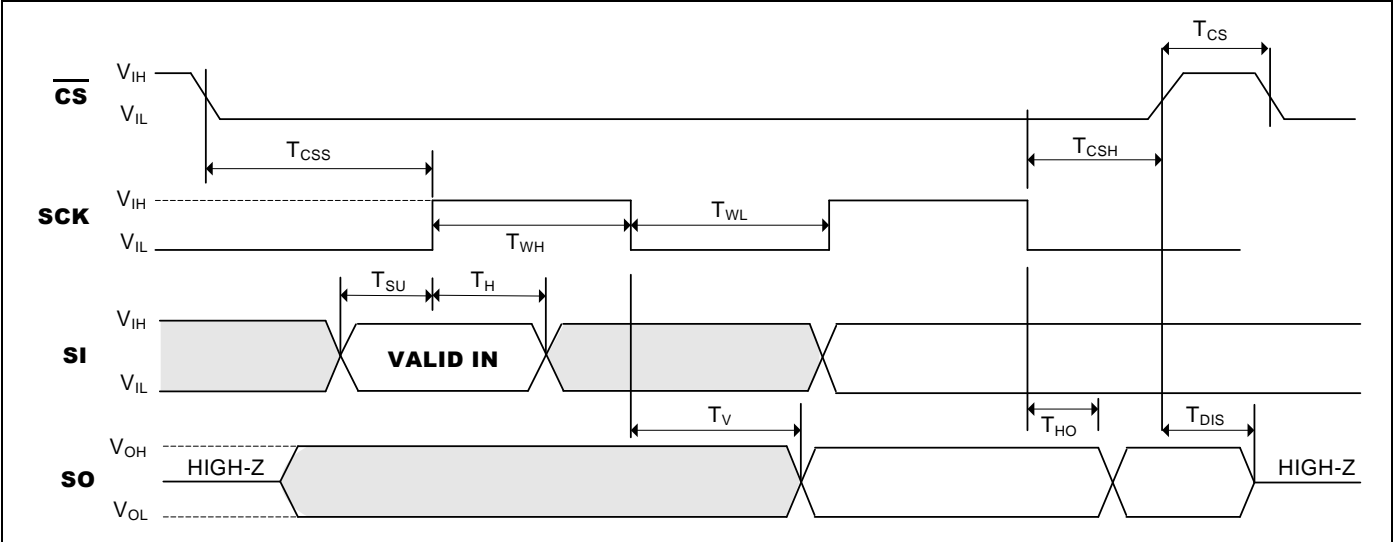
Figure 5-1. Synchronous Data Timing
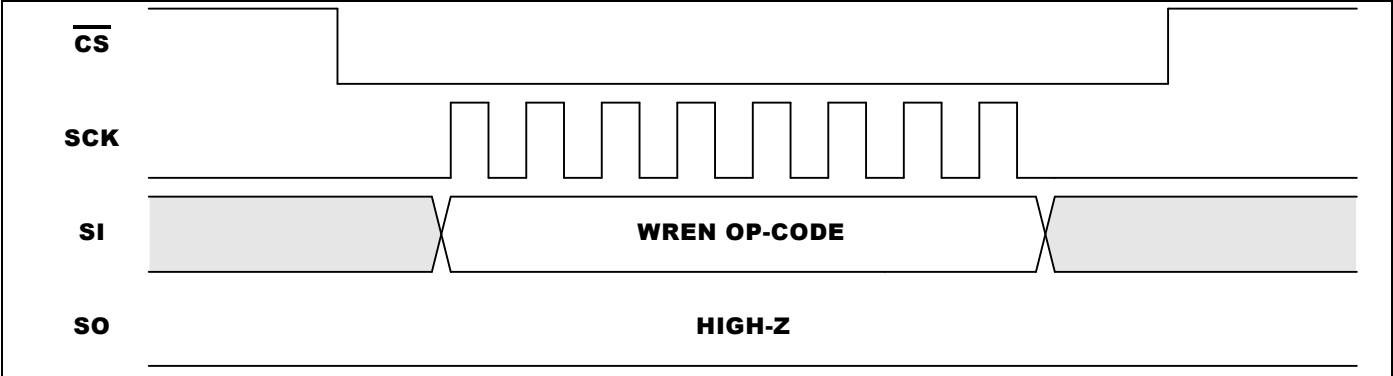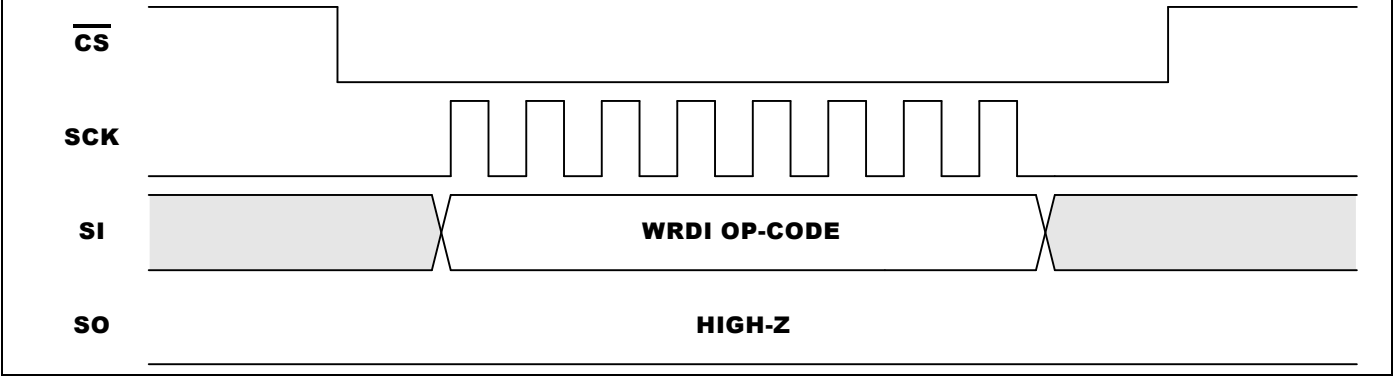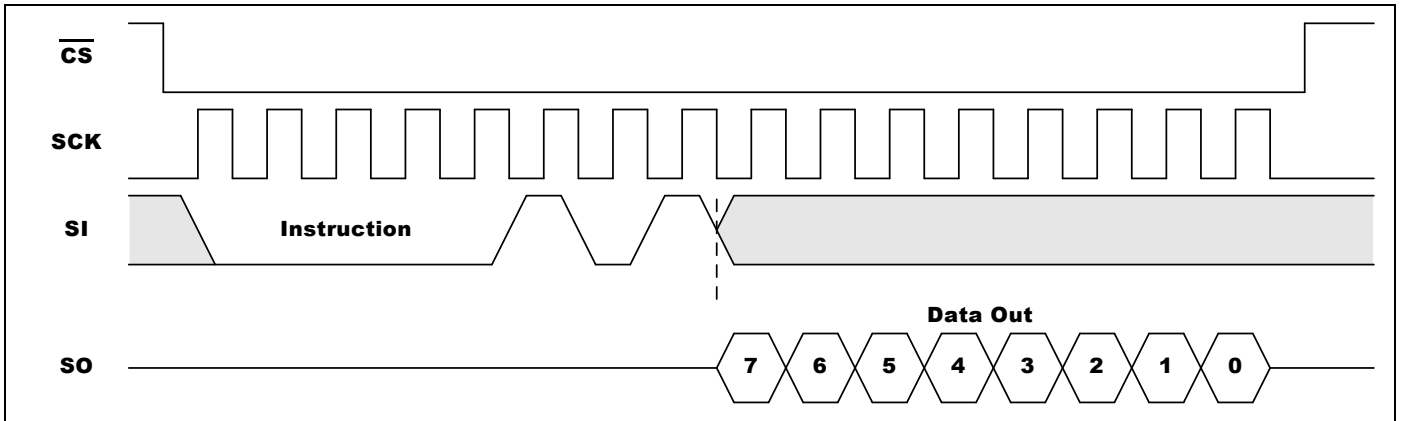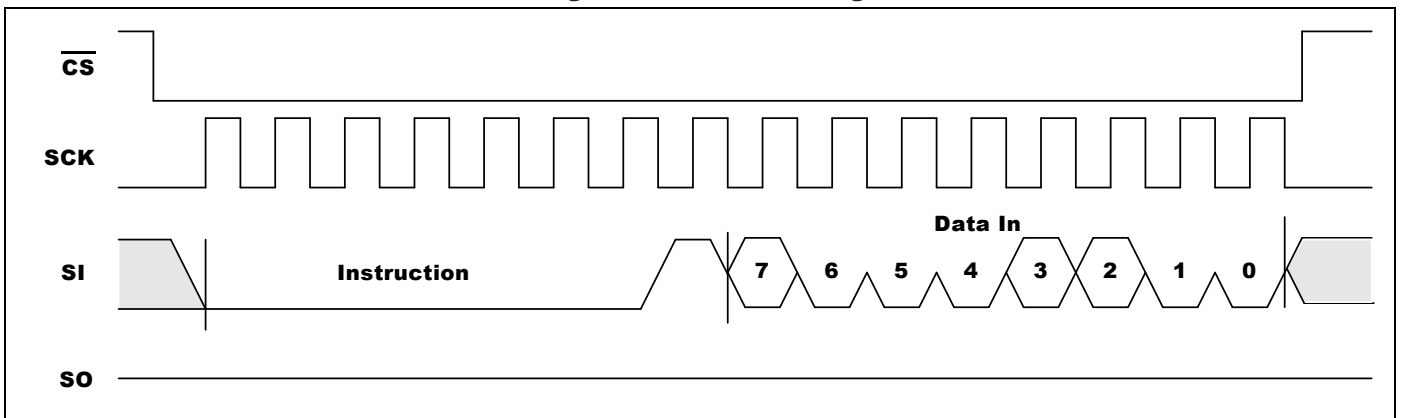

Figure 5-2. WREN Timing

Figure 5-3. WRDI Timing

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Figure 5-4. RDSR Timing

Figure 5-5. WRSR Timing

Figure 5-6. READ Timing

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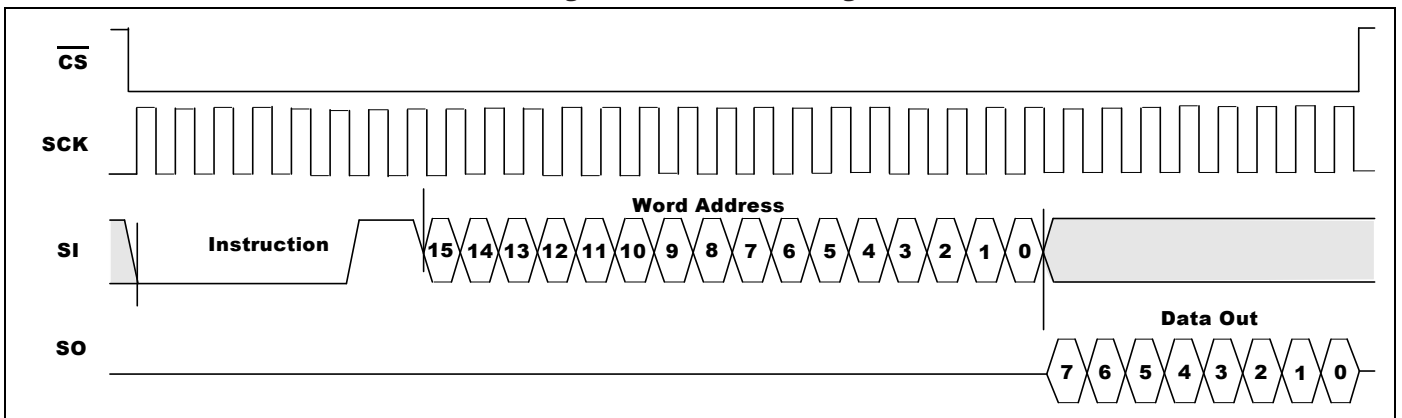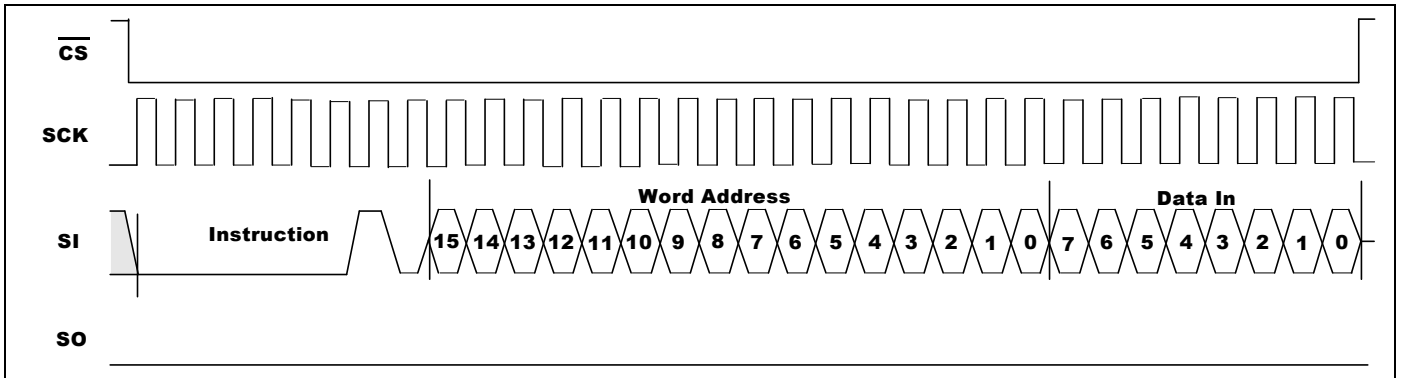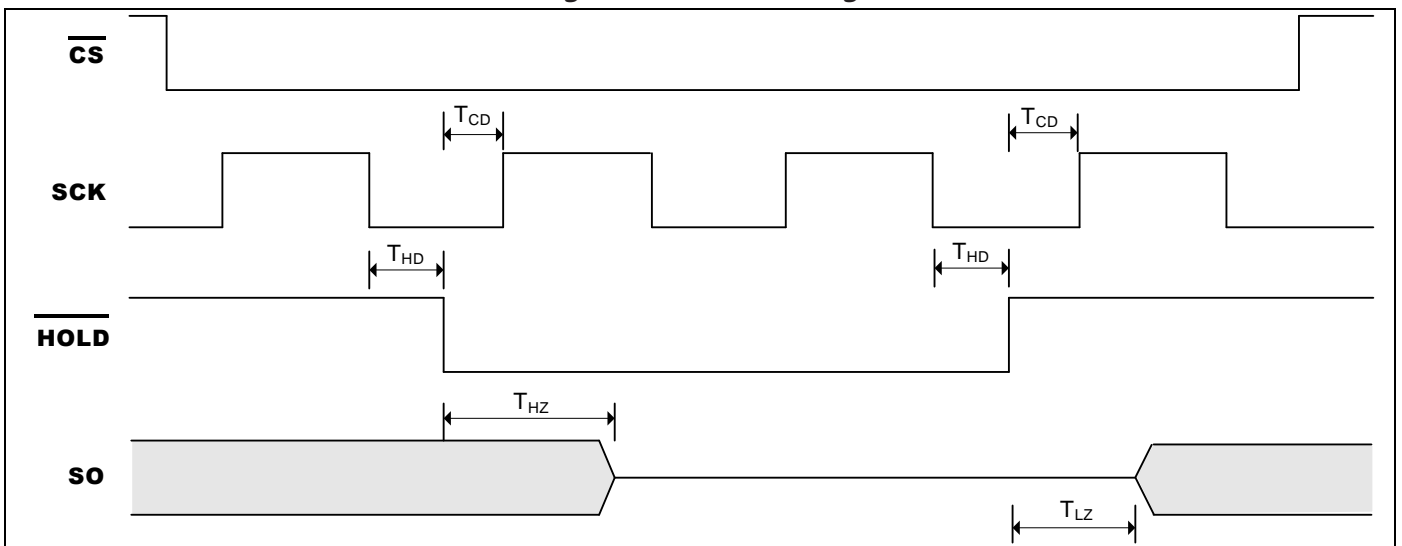10/19

Figure 5-7. WRITE Timing

Figure 5-8. HOLD Timing

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6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to V_{CC} + 1	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 1	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive Grade 2	–40°C to +105°C	2.5V to 5.5V

6.3 Reliability

Ambient Temperature (TA)	Symbol	Parameter	Min.	Unit
Ta=+25°C	End	Endurance	1 million	Program / Erase Cycles
	DR	Data Retention	100	Years

6.4 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V

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6.5 DC Electrical Characteristic

Automotive: T_A = −40˚C to +105˚C, V_{CC} = 2.5V ~ 5.5V

Symbol	Parameter	V_{CC}	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage			2.5	5.5	V
V_{IH}	Input High Voltage			0.7* V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage			-0.3	0.3* V_{CC}	V
I_{LI}	Input Leakage Current		V_{IN} = 0V To V_{CC}	-2	2	µA
I_{LO}	Output Leakage Current		V_{OUT} = 0V To V_{CC}, $\overline{CS}$ = V_{CC}	-2	2	µA
V_{OH}	Output High Voltage	2.5	I_{OH} = -0.4mA	0.8*V_{CC}	—	V
		5.5	I_{OH} = -2 mA	0.8*V_{CC}	—	V
V_{OL}	Output Low Voltage	2.5	I_{OL} = 1.5 mA	—	0.4	V
		5.5	I_{OL} = 2 mA	—	0.4	V
I_{CC}	Operating Current	2.5	Read/Write at 10 MHz, SO=Open	—	2	mA
		5.5	Read/Write at 20 MHz, SO=Open	—	3	mA
I_{SB}	Standby Current	2.5	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—	1	µA
		5.5	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—	2	µA

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6.6 AC Electrical Characteristic

Automotive: T_A = −40°C to +105°C, Supply voltage = 2.5V to 5.5V

Symbol	Parameter[1]	2.5V≤V_{CC}<4.5V		4.5V≤V_{CC}≤5.5V		Unit
		Min.	Max.	Min.	Max.	
F_{SCK}	SCK Clock Frequency	0	10	0	20	MHz
T_{RI}	Input Rise Time	—	1	—	1	µs
T_{FI}	Input Fall Time	—	1	—	1	µs
T_{WH}	SCK High Time	40	—	20	—	ns
T_{WL}	SCK Low Time	40	—	20	—	ns
T_{CS}	$\overline{CS}$ High Time	50	—	25	—	ns
T_{CSS}	$\overline{CS}$ Setup Time	50	—	25	—	ns
T_{CSH}	$\overline{CS}$ Hold Time	50	—	25	—	ns
T_{SU}	Data In Setup Time	10	—	5	—	ns
T_H	Data In Hold Time	10	—	5	—	ns
T_{HD}	$\overline{HOLD}$ Setup Time	10	—	5	—	ns
T_{CD}	$\overline{HOLD}$ Hold Time	10	—	5	—	ns
T_V[2]	Output Valid	0	40	0	20	ns
T_{HO}	Output Hold Time	0	—	0	—	ns
T_{LZ}	$\overline{HOLD}$ to Output Low Z	0	50	0	25	ns
T_{HZ}	$\overline{HOLD}$ to Output High Z	—	80	—	40	ns
T_{DIS}	Output Disable Time	—	80	—	40	ns
T_{WC}	Write Cycle Time	—	5	—	5	ms

Notes: [1] The parameters are characterized but not 100% tested.

[2] C_L = 30pF (typical)

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7. Ordering Information

Automotive Grade: -40°C to +105°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
2.5V to 5.5V	GT25C08-3GLA2-TR	150-mil SOIC
	GT25C08-3ZLA2-TR	3 x 4.4 mm TSSOP

*

1. Contact Giantec Sales Representatives for availability and other package information.

2. The product is packed in tape and reel "-TR" (4K per reel), except UDFN is 5K per reel.

3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.

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8. Top Markings

8.1 SOIC Package
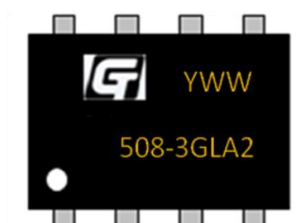
G: Giantec Logo

508-3GLA2: GT25C08-3GLA2-TR

YWW: Date Code, Y=year, WW=week

8.2 TSSOP Package
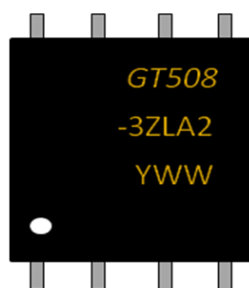
GT: Giantec Logo

508-3ZLA2: GT25C08-3ZLA2-TR

YWW: Date Code, Y=year, WW=week

9. Package Information

9.1 SOIC

8L 150mil SOIC Package Outline

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:

1. Controlling Dimension:MM

2. Dimension D and E1 do not include Mold protrusion

3. Dimension b does not include dambar protrusion/intrusion.

4. Refer to Jedec standard MS-012

5. Drawing is not to scale

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9.2 TSSOP

8L 3x4.4mm TSSOP Package Outline

Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.4 BSC			0.252 BSC		
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

10. Revision History

Revision	Date	Descriptions
A0	Nov. 2015	Initial version

单击下面可查看定价，库存，交付和生命周期等信息

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