High Speed 10MBit/s Logic Gate Optocouplers

Description

The UMW 6N137 optocoupler consists of a 850 nm AlGaAS LED, optically coupled to a very high speed integrated photo-detector logic gate withastrobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5mA will provide a minimum output sink current of 13mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10kV/μs. The UMW 6N137 has a minimum CMR of 5kV/μs.

Features

- Very high speed – 10 MBit/s
- Superior CMR – 10 kV/μs
- Double working voltage-480V
- Fan-out of 8 over -40℃ to +85℃
- Logic gate output
- Strobable output
- Wired OR-open collector
- UL approved: UL1577, file No. E492440

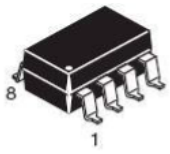
Truth Table (Positive Logic)

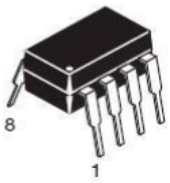
Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Applications

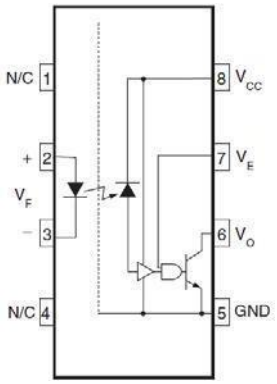
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

Package Outlines





Schematics



Absolute Maximum Ratings (T_A = 25℃ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-55 to +125	℃
T_{OPR}	Operating Temperature	-40 to +85	℃
T_{SOL}	Lead Solder Temperature (for wave soldering only)	260 for 10 sec	℃
EMITTER			
I_F	DC/Average Forward Input Current	50	mA
V_E	Enable Input Voltage Not to Exceed V_{CC} by more than 500mV	5.5	V
V_R	Reverse Input Voltage	5.0	V
P_I	Power Dissipation	100	mW
DETECTOR			
V_{CC} (1 minute max)	Supply Voltage	7.0	V
I_O	Output Current	50	mA
V_O	Output Voltage	7.0	V
P_O	Collector Output	85	mW

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. We do not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
I_{FL}	Input Current, Low Level	0	250	μA
I_{FH}	Input Current, High Level	*6.3	15	mA
V_{CC}	Supply Voltage, Output	4.5	5.5	V
V_{EL}	Enable Voltage, Low Level	0	0.8	V
V_{EH}	Enable Voltage, High Level	2.0	V_{CC}	V
T_A	Low Level Supply Current	-40	+85	℃
N	Fan Out (TTL load)		8	

Note: *6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less.

Electro-optical Characteristics (T_A= 0 to 70 ℃ unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
EMITTER						
V_F	Input Forward Voltage	I_F = 10mA, T_A = 25 ℃		1.4	1.8 1.75	V
B_{VR}	Input Reverse Breakdown Voltage	I_R = 10 μA	5.0			V
C_{IN}	Input Capacitance	V_F = 0, f = 1MHz		60		pF
$\Delta V_F/\Delta T_A$	Input Diode Temperature Coefficient	I_F = 10mA		-1.4		mV/°C
DETECTOR						
I_{CCH}	High Level Supply Current	V_{CC} = 5.5V, I_F = 0mA, V_E = 0.5V		7	10	mA
I_{CCL}	Low Level Supply Current	V_{CC} = 5.5V, I_F = 10mA		9	13	mA
I_{EL}	Low Level Enable Current	V_{CC} = 5.5V, V_E = 0.5V		-0.8	-1.6	mA
I_{EH}	High Level Enable Current	V_{CC} = 5.5V, V_E = 2.0V		-0.6	-1.6	mA
V_{EH}	High Level Enable Voltage	V_{CC} = 5.5V, I_F = 10mA	2.0			V
V_{EL}	Low Level Enable Voltage	V_{CC} = 5.5V, I_F = 10mA (3)			0.8	V

Switching Characteristics (T_A -40 ℃ to +85 ℃, V_{CC}= 5V, I_F= 7.5mA unless otherwise specified)

Symbol	AC Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
T_{PLH}	Propagation Delay Time to Output HIGH Level	R_L = 350 Ω, T_A = 25 ℃ C_L=15pF (4)(Fig. 12)	20	45	75 100	ns
T_{PHL}	Propagation Delay Time to Output LOW Level	T_A = 25 ℃ (5) R_L = 350 Ω, C_L= 15pF (Fig. 12)	25	45	75 100	ns
$\|T_{PHL} - T_{PLH}\|$	Pulse Width Distortion	(R_L = 350 Ω, C_L=15pF (Fig. 12)		3	35	ns
t_r	Output Rise Time (10–90%)	R_L = 350 Ω, C_L = 15pF (6) (Fig. 12)		50		ns
t_f	Output Rise Time (90–10%)	R_L = 350 Ω, C_L = 15pF (7) (Fig. 12)		12		ns
t_{ELH}	Enable Propagation Delay Time to Output HIGH Level	I_F = 7.5mA, V_{EH} = 3.5V, R_L = 350Ω, C_L = 15pF (8) (Fig. 13)		20		ns
t_{EHL}	Enable Propagation Delay Time to Output LOW Level	I_F = 7.5mA, V_{EH} = 3.5V, R_L = 350Ω, C_L = 15pF (9) (Fig. 13)		20		ns
$\|CM_H\|$	Common Mode Transient Immunity (at Output HIGH Level)	T_A = 25 ℃, $\|V_{CM}\|$ = 50V (Peak), I_F = 0mA, V_{OH} (Min.) = 2.0V, R_L = 350Ω(10) (Fig. 14)	5000	10000		V/μs
$\|CM_L\|$	Common Mode Transient Immunity (at Output LOW Level)	R_L = 350Ω, I_F = 7.5mA, V_{OL} (Max.) = 0.8V, T_A = 25 ℃ (11) (Fig. 14)	5000	10000		V/μs

Electrical Characteristics (Continued)

Transfer Characteristics (T_A = -40 to +85 ℃ unless otherwise specified)

Symbol	DC Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{OH}	HIGH Level Output Current	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250 μA, V_E = 2.0V(2)			100	μA
V_{OL}	LOW Level Output Current	V_{CC} = 5.5V, I_F = 5mA, V_E = 2.0V, I_{CL} = 13mA(2)		0.35	0.6	V
I_{FT}	Input Threshold Current	V_{CC} = 5.5V, V_O = 0.6V, V_E = 2.0V, I_{OL} = 13mA		3	5	mA

Isolation Characteristics (T_A = -40 ℃ to +85 ℃ unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, T_A = 25 ℃, t = 5s, V_{I-O} = 3000 VDC(12)			10*	μA
V_{ISO}	Withstand Insulation Test Voltage	RH < 50%, T_A = 25° C, I_{I-O} ≤ 2 μA, t = 1 min.(12)	2500			V_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500V(12)		10^{12}		Ω
C_{I-O}	Capacitance (Input to Output)	f = 1MHz(12)		0.6		pF

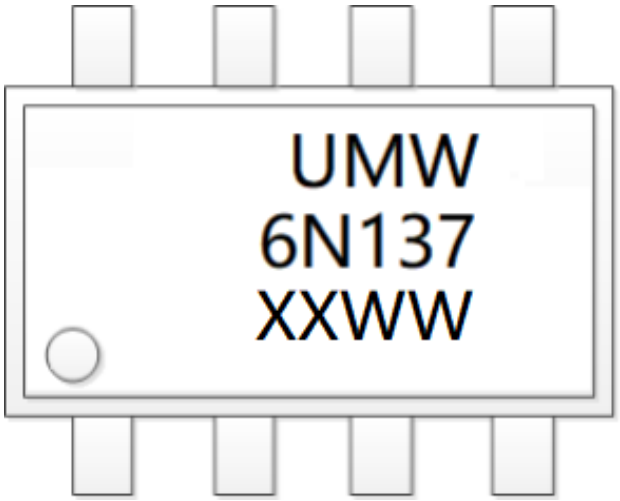
* All Typicalsat VCC = 5V

* TA = 25 ℃

* Note:

1. The V_{CC} supply to each optoisolator must be bypassed by a 0.1 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. One channel.
3. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
4. t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
5. t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
6. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
7. tf – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
8. t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
9. t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
10. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT}> 2.0V). Measured in volts per microsecond (V/μs).
11. CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT}< 0.8V). Measured in volts per microsecond (V/μs).
12. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Marking



- "XX" denotes YEAR;
- "WW" denotes WEEK

Order Code

Order Code	Description	Base qty
UMW 6N137M	Iron frame, DIP, Halogen/lead -free	2250/BOX
UMW 6N137S	Copper frame,SOP-8,Halogen -free	1000/REEL

Typical Performance Curves

Fig.1 Low Level Output Voltage vs. Ambient Temperature

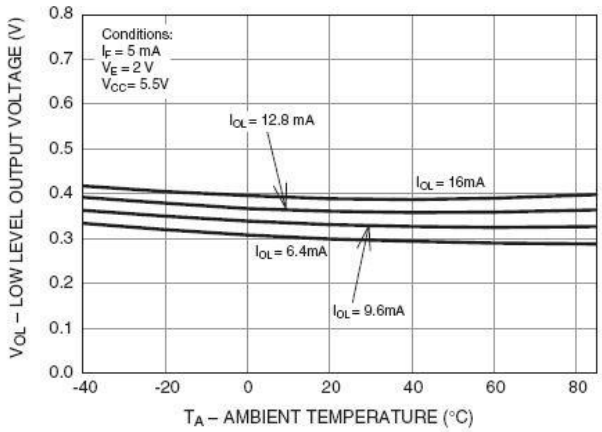


Fig. 2 Input Diode Forward Voltage vs. Forward Current

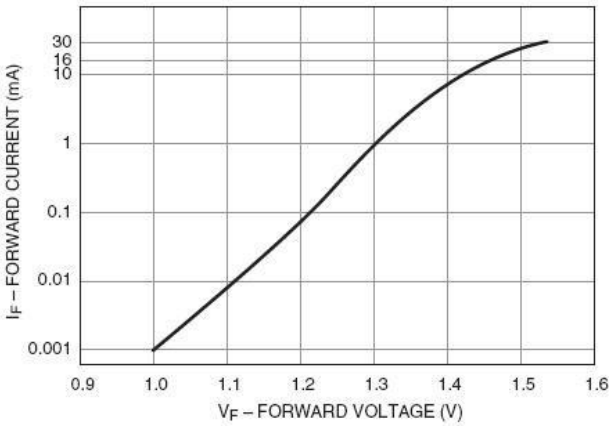


Fig.3 Switching Time vs. Forward Current

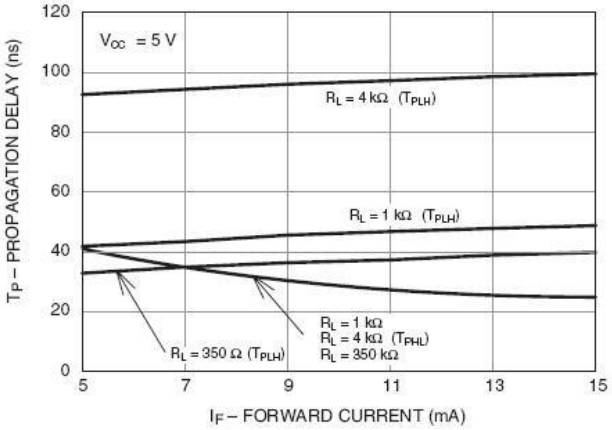


Fig. 4 Low Level Output Current vs. Ambient Temperature

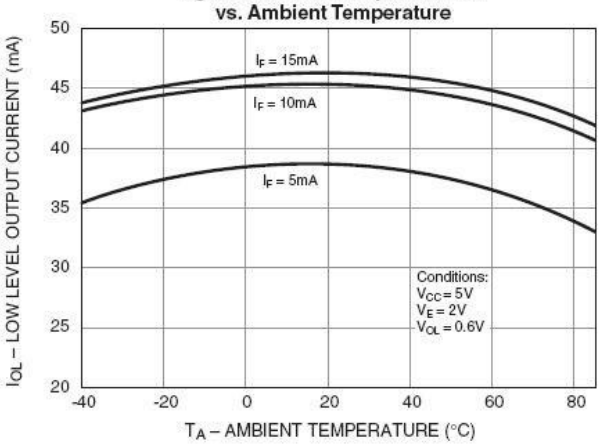


Fig. 5 Input Threshold Current vs. Ambient Temperature

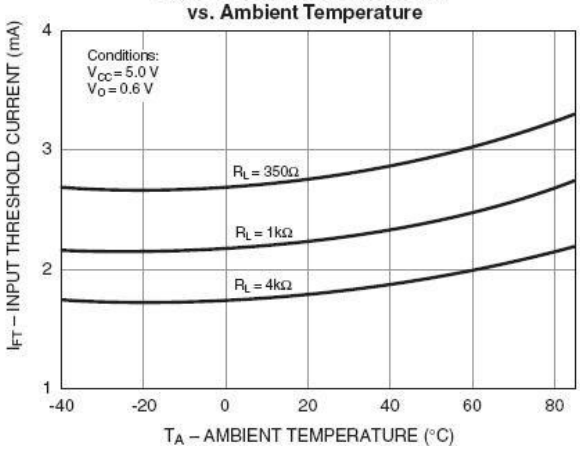
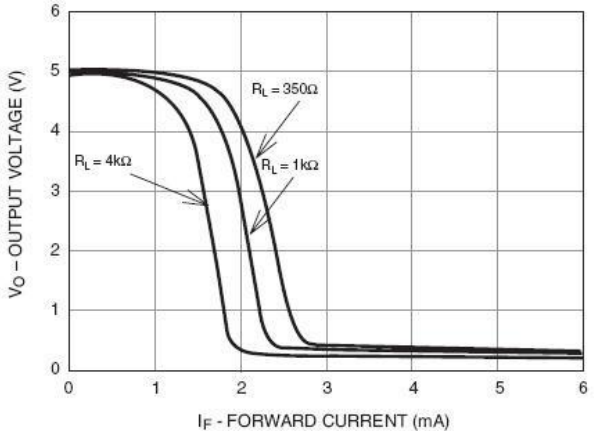


Fig. 6 Output Voltage vs. Input Forward Current



Typical Performance Curves (Continued)

Fig. 7 Pulse Width Distortion vs. Temperature

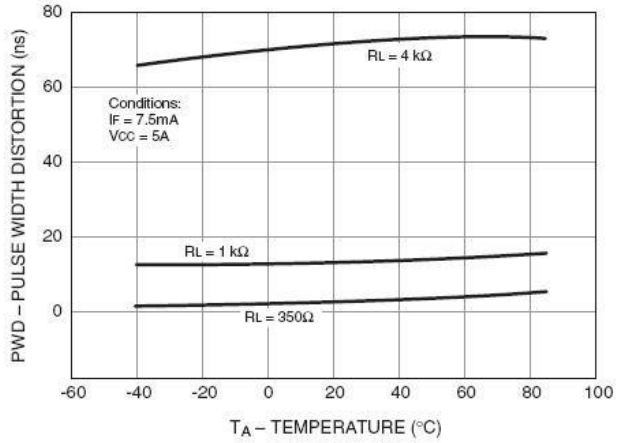


Fig. 8 Rise and Fall Time vs. Temperature

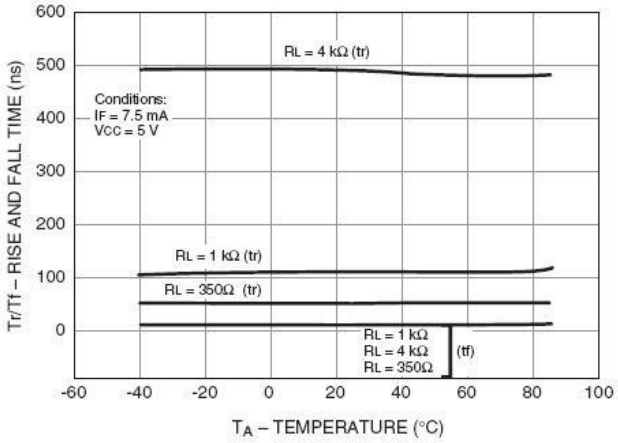


Fig. 9 Enable Propagation Delay vs. Temperature

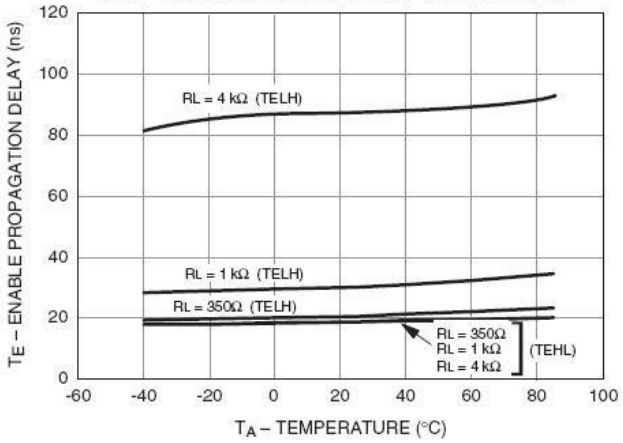


Fig. 10 Switching Time vs. Temperature

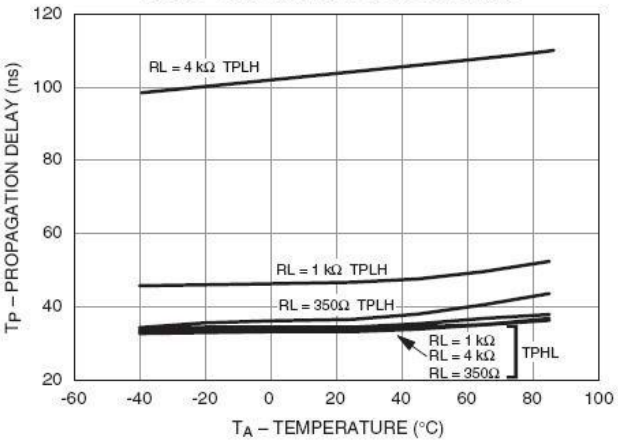
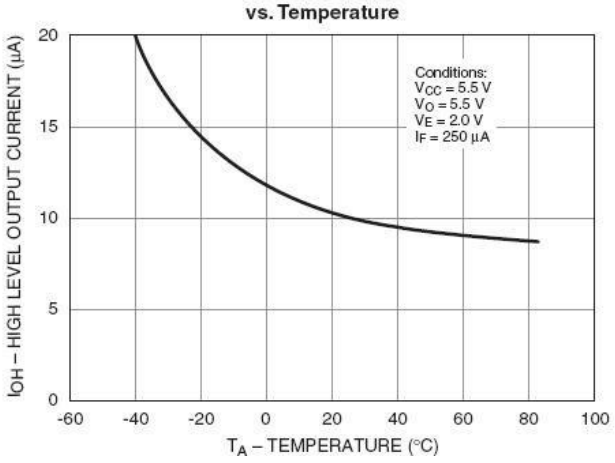


Fig. 11 High Level Output Current vs. Temperature



Test Circuits

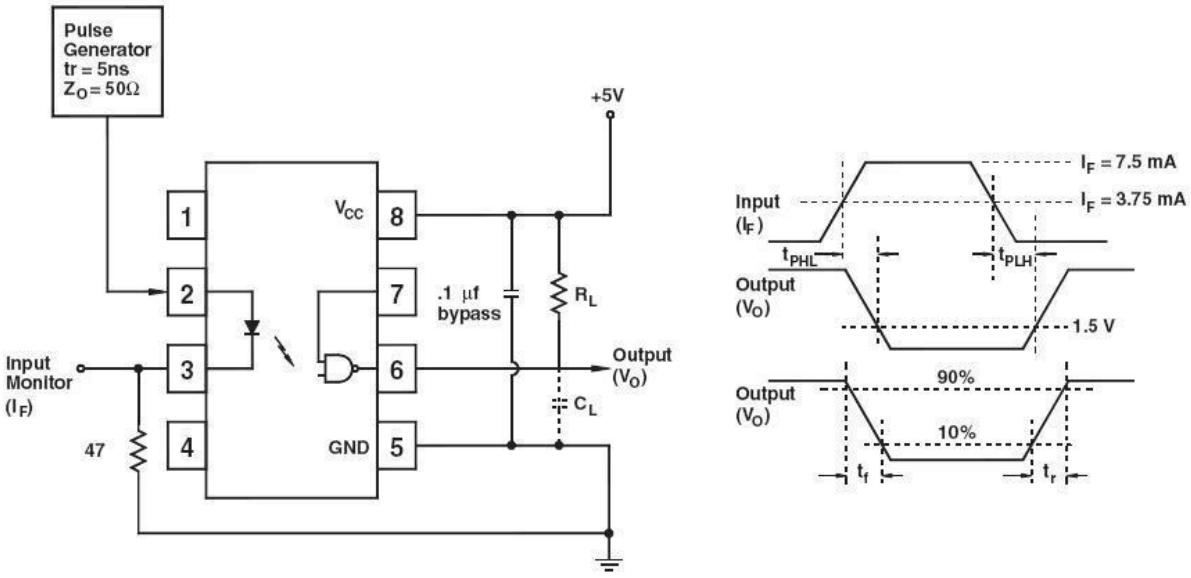


Fig. 12 Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r and t_f

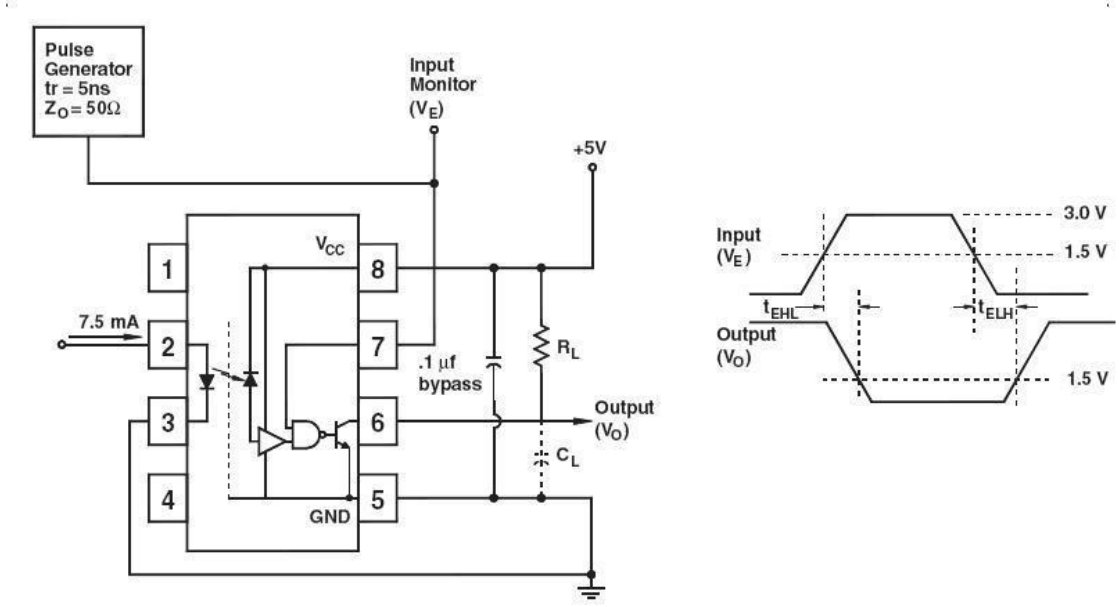


Fig. 13 Test Circuit t_{EHL} and t_{ELH}

Test Circuits (Continued)

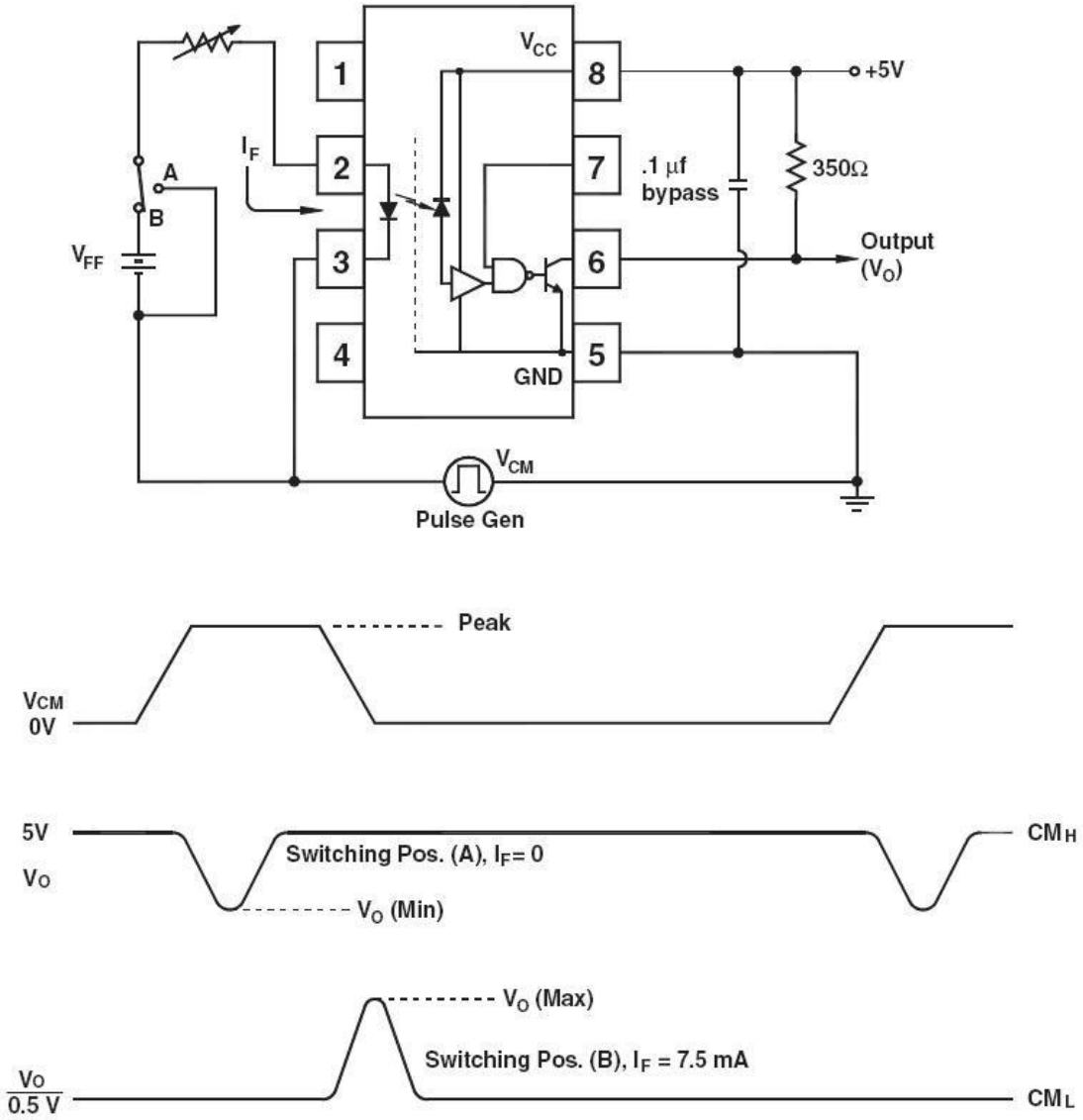
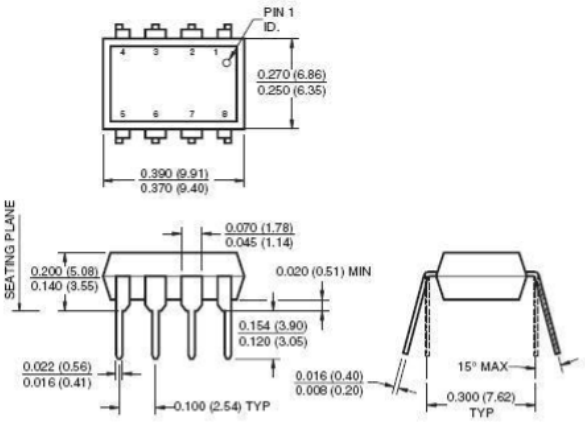


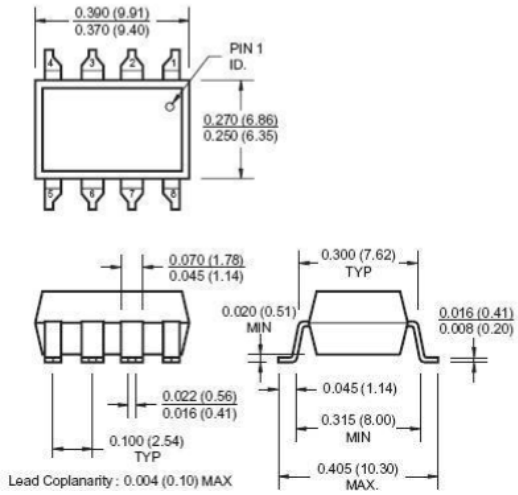
Fig. 14 Test Circuit Common Mode Transient Immunity

Package Dimensions

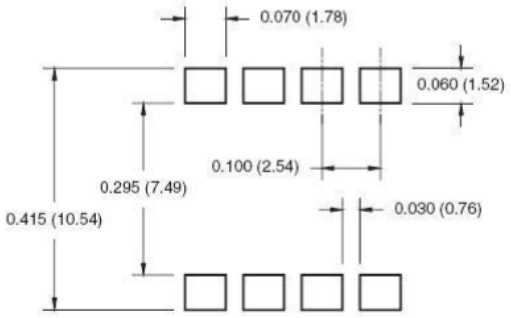
Through Hole



Surface Mount



8-Pin DIP – Land Pattern



Note: All dimensions are in inches (millimeters)

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)