LVDS Interface LSI LVDS Transmitter for Automotive

BU92T101-M

General Description

BU92T101-M LVDS transmitter operates from 15MHz to 174MHz wide clock frequency range, and 35 bits data of parallel LVCMOS level inputs (R/G/B 30 bits and VSYNC, HSYNC, DE, CNTL1, CNTL2) are converted to 5 channels of LVDS data stream. Data is transmitted seven times (x7) stream and reduce cable number by 3(1/3).

BU92T101-M has low swing mode to be able to expect further low power and low EMI.

Features

- AEC-Q100 Qualified ^(Note 1)
- LVDS Maximum Data Rate is 1.218Gbps/Channel
- LVDS Transmitter Support Wide Frequency Range from 15MHz up to 174MHz (☆) ^(Note 2)
- Support Reduced Swing LVDS Output for Low EMI
- Support Input Clock Edge Select Function
- Support Power Down Mode

(Note 1) Grade2

(Note 2) (1/2): Special Characteristics

Key Specifications

.	Power Supply Voltage : VDD	3.0V to 3.6V
	LVDD	3.0V to 3.6V

- CLKIN Input Frequency: 15MHz to 174MHz LVDS Output Frequency: 15MHz to 174MHz
- Operating Temperature Range: -40°C to +105°C

Package

HTQFP64AV

W(Typ) x D(Typ) x H(Max)

12.00mm x 12.00mm x 1.00mm



Applications

- Car Navigation System
- CID (Center Information Display)
- HUD (Head Up Display)

Block Diagram

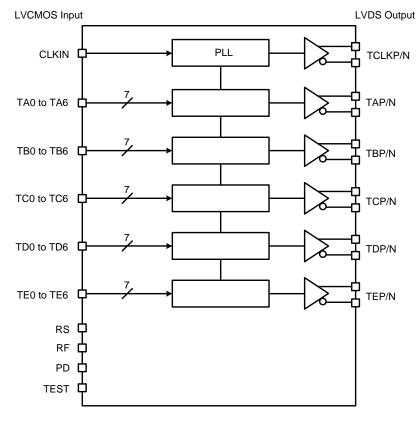


Figure 1. Block Diagram

OProduct structure : Silicon monolithic integrated circuit OThis product has no designed protection against radioactive rays

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TSZ02201-0L2L0H500900-1-2 25.Oct.2017 Rev.001

Pin Configuration

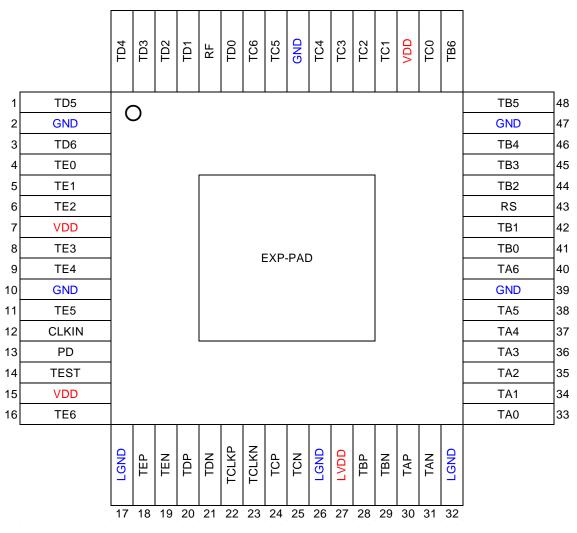


Figure 2. Pin Configuration (TOP VIEW)

Pin Descriptions

Pin No.	Pin Name	Туре	Descriptions
30,31	TAP, TAN	LVDS OUT	
28,29	TBP, TBN	LVDS OUT	_
24,25	TCP, TCN	LVDS OUT	LVDS data
20,21	TDP, TDN	LVDS OUT	
18,19	TEP, TEN	LVDS OUT	
22,23	TCLKP, TCLKN	LVDS OUT	LVDS clock
33,34,35,36, 37,38,40	TA0, TA1, TA2, TA3, TA4, TA5, TA6	LVCMOS IN	
41,42,44,45, 46,48,49	TB0, TB1, TB2, TB3, TB4, TB5, TB6	LVCMOS IN	
50,52,53,54, 55,57,58	TC0, TC1, TC2, TC3, TC4, TC5, TC6	LVCMOS IN	LVCMOS pixel data
59,61,62,63, 64,1,3	TD0, TD1, TD2, TD3, TD4, TD5, TD6	LVCMOS IN	
4,5,6,8, 9,11,16	TE0, TE1, TE2, TE3, TE4, TE5, TE6	LVCMOS IN	
12	CLKIN	LVCMOS IN	LVCMOS clock
13	PD	LVCMOS IN	Power down H: Normal operation L: Power down (All LVDS output signals are Hi-Z)
43	RS	LVCMOS IN	LVDS output swing mode select H: Normal swing (350mV) L: Reduced swing (200mV)
60	RF	LVCMOS IN	Input clock edge select (Refer to Figure 5) H: Rising edge L: Falling edge
14	TEST	LVCMOS IN	Test mode enable with internal pull down resistor Connect to GND directly H: Vendor test mode L: Normal operation
27	LVDD	Power	Power Supply for LVDS
7,15, 51	VDD	Power	Power Supply for I/O
17,26,32	LGND	Ground	Ground for LVDS
2,10,39,47,56	GND	Ground	Ground for I/O
-	EXP-PAD	-	Must tie to ground

I/O Equivalence Circuit

Туре	Circuit Type	Applied Pins
LVDS OUT	Pin	TAP, TAN, TBP, TBN, TCP, TCN, TDP, TDN, TEP, TEN, TCLKP, TCLKN
LVCMOS IN		TA0, TA1, TA2, TA3, TA4, TA5, TA6, TB0, TB1, TB2, TB3, TB4, TB5, TB6, TC0, TC1, TC2, TC3, TC4, TC5, TC6, TD0, TD1, TD2, TD3, TD4, TD5, TD6, TE0, TE1, TE2, TE3, TE4, TE5, TE6, CLKIN
LVCMOS IN	Pin	PD, RS,
LVCMOS IN	Pin	RF
LVCMOS IN	Pin RDN	TEST

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage	V _{DD}	-0.3 to +4.5	V	For VDD, LVDD
Input Voltage	Vin	-0.3 to V _{DD} +0.3	V	V _{DD} +0.3 < 4.5V
Storage Temperature Range	Tstg	-55 to +125	°C	
Maximum Junction Temperature	Tjmax	125	°C	

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 3)

Parameter		Thermal Res	Unit		
Farameter	Symbol	1s ^(Note 5)	2s2p ^(Note 6)	Unit	
HTQFP64AV					
Junction to Ambient	θյΑ	63.4	14.9	°C/W	
Junction to Top Characterization Parameter ^(Note 4)	Ψ_{JT}	2	1	°C/W	

(Note 3) Based on JESD51-2A(Still-Air)

Footprints and Traces

(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package. (Note 5) Using a PCB board based on JESD51-3.

35µm

(NOLE 5) USING A FCB DUALU DASEU	011 JESD31-3.				
Layer Number of Measurement Board	Material	Board Size			
Single	FR-4	114.3mm x 76.2mm x	1.57mmt		
Тор					
Copper Pattern	Thickness				
Footprints and Traces	70µm				
(Note 6) Using a PCB board based	on JESD51-5, 7	-			
Layer Number of	Material	Board Size		Thermal	Via
Measurement Board	Material	Board Bize	Board Size		
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt		1.20mm	
Тор		2 Internal Layers		Bott	or
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Patter	n

74.2mm x 74.2mm

(Note 7) This thermal via connects with the copper pattern of all layers.

70µm

Thermal Via(Note 7)

Bottom

74.2mm x 74.2mm

Diameter

Φ0.30mm

Thickness

70µm

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit	Conditions
i arameter	Symbol	Min	Тур	Max	Unit	Conditions
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	For VDD, LVDD
Operating Temperature Range	Tj	-40	+25	+105	°C	
Operating Frequency	fın	15	-	174	MHz	
Operating Frequency	fouт	15	-	174	MHz	

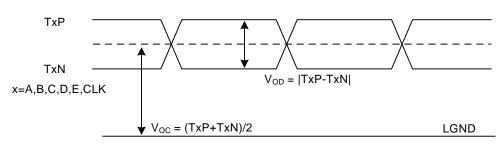
Electrical Characteristics

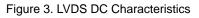
DC Electrical Characteristics

	<u> </u>	able 1. LVCM	OS DC Specific	cations		
Demonster	Symbol	Limit				Conditions
Parameter	Symbol	Min	Тур	Max	- Unit	Conditions
High Level Input Voltage	Vін	V _{DD} x0.7	-	Vdd	V	All LVCMOS IN Pins
Low Level Input Voltage	VIL	GND	-	V _{DD} x0.3	V	All LVCMOS IN Pins
Hysteresis Voltage	Vн	-	600	-	mV	The PD, RS, TEST Pin
Input Leakage Current	lız	-10	-	+10	μA	0V≤V _{IN} ≤V _{DD} (Except the TEST Pin)
Pull Down Resistor	Rdn	35	50	65	kΩ	The TEST Pin

Table 2. LVDS DC Specifications

Parameter	Symbol	Limit			Unit	Conditions	
	Symbol	Min	Тур	Max	Offic	Conditions	
Differential Output Voltage	Vod	250	350	450	mV	R∟=100Ω (Refer to	RS=H
Differential Output Voltage	VOD	140	200	300	mV	Figure 3, 4)	RS=L
Change in V _{OD} Between Complementary Output States	ΔV_{OD}	-	-	35	mV	R∟=100Ω (Refer to Figure 3, 4)	
Common Mode Voltage	Voc	1.125	1.25	1.375	V		
Change in V _{OC} Between Complementary Output States	ΔV_{OC}	-	-	35	mV		
Output Short Circuit Current	los	-	100	150	mA	LVDS Transmitter Pin Force=0V	
Output Tri-state Current	loz	-10	-	+10	μA	PD=L LVDS Transr Pin Force=0	





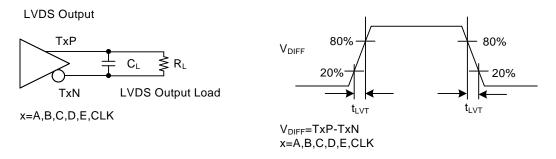
AC Electrical Characteristics

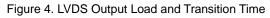
Table 3. Switching Characteristics (R_L =100 Ω , C_L =5pF)

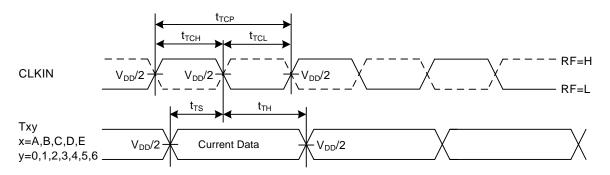
						Canditiana	
Parameter	Symbol	Min	Тур	Max	Unit	Conditions	
CLKIN Input Frequency (☆)	fın	15	-	174	MHz	(Note 8)	
CLKIN Input Period	t _{TCP}	5.75	-	66.6	ns		
CLKIN High Time	t _{тсн}	0.35t _{TCP}	0.5t _{TCP}	0.65t _{TCP}	ns		
CLKIN Low Time	t⊤c∟	0.35t _{TCP}	0.5ttcp	0.65t _{TCP}	ns	(Refer to Figure 5)	
LVCMOS Data Setup Time to CLKIN	tтs	0.8	-	-	ns		
LVCMOS Data Hold Time from CLKIN	tтн	0.8	-	-	ns		
LVDS Clock Output Frequency (☆)	fout	15	-	174	MHz	(Note 8)	
LVDS Clock Output Period	t _{TCOP}	5.75	-	66.6	ns	(Refer to Figure 6)	
LVDS Transition Time	t∟∨⊤	-	-	0.5	ns	(Refer to Figure 4)	
Differential Output Setup Time	t TSUP	-	-	120	ps	fout=174MHz	
Differential Output Hold Time	t _{THLD}	-	-	120	ps	f _{OUT} =174MHz	
Output Data Position 1	t _{TOP1}	- t _{THLD}	0	+ t _{TSUP}	ns		
Output Data Position 0	t _{TOP0}	$\frac{t_{TCOP}}{7}$ - tthld	t _{TCOP} 7	$\frac{t_{TCOP}}{7}$ + tTSUP	ns		
Output Data Position 6	t _{TOP6}	$2\frac{t_{TCOP}}{7}$ - tthld	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7}$ + tTSUP	ns		
Output Data Position 5	t _{TOP5}	$3\frac{t_{TCOP}}{7}$ - tthld		$3\frac{t_{TCOP}}{7}$ + tTSUP	ns	(Refer to Figure 6)	
Output Data Position 4	t _{TOP4}	$4 \frac{t_{\text{TCOP}}}{7} - t_{\text{THLD}}$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7}$ + tTSUP	ns		
Output Data Position 3	tторз	$5\frac{t_{TCOP}}{7}$ - tthld	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7}$ + tTSUP	ns		
Output Data Position 2	t _{TOP2}	$6 \frac{t_{TCOP}}{7} - t_{THLD}$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7}$ + t_{TSUP}	ns		
Input Modulation Frequency	f _{IMOD}	30	-	250	kHz		
Input Modulation Ratio	r _{IMOD}	-2.0	-	+2.0	%		

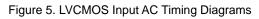
(Note 8) (☆): Special Characteristics

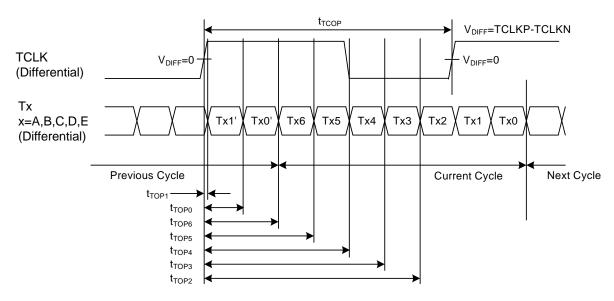
AC Timing Diagrams

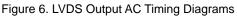












BU92T101-M

Supply Current

Table 4. Supply Current (R_L=100Ω, C_L=5pF)

Demonstern	Currents of	Limit			l lecit			
Parameter	Symbol	Min	Тур	Max	Unit		Conditions	
Supply Current Worst Case Pattern		-	70	95	mA	RS=L	f _{IN} =f _{OUT} =90MHz	
	Ітссw	-	100	130	mA	(200mV)	f _{IN=fout=} 174MHz	
(Refer to Figure 7)		-	88	115	mA	RS=H	f _{IN} =f _{OUT} =90MHz	
		-	118	150	mA	(350mV)	fin=fout=174MHz	
Power Down Current	vn Current ITCCS - 5 8 mA PD=L All LVCI			Pixel Data, Clock Pins=L				

LVCMOS Input

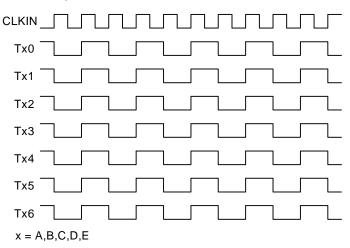


Figure 7. Worst Case Pattern (Maximum Power Condition)

Timing Chart

Power Supply Timing

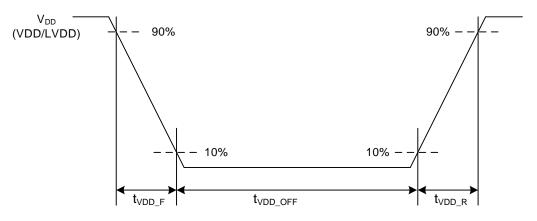


Figure 8. Power Supply Rise and Fall Timing

Table	5	Power	Supply	Timing
Table	υ.	1 0 100	ouppiy	rinning

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
V _{DD} Rise Time	t _{VDD_R}	-	-	10	ms	
V _{DD} Fall Time	t_{VDD_F}	-	-	10	ms	
V _{DD} Off Time	t _{VDD_OFF}	100	-	-	ms	

Reset Release Timing

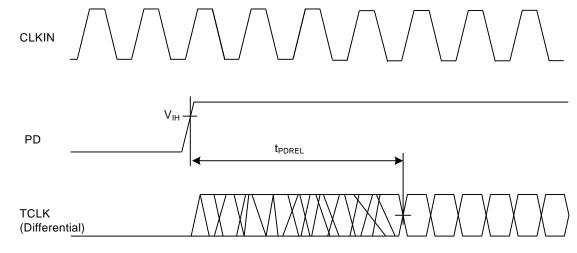


Figure 9. Reset Release Timing

Table 6. Reset Release Timing

g						
Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Output Stable Time	t PDREL	-	-	10	ms	

Application Examples

Typical Application Example

LVCMOS Parallel Data Input:

35 Bits (R/G/B 30 Bits, HSYNC, VSYNC, DE, CNTL1, CNTL2) Input Clock Edge: Falling Edge (RF=L) LVDS Output Swing: 350mV (RS=H)

LVDS Data Output:

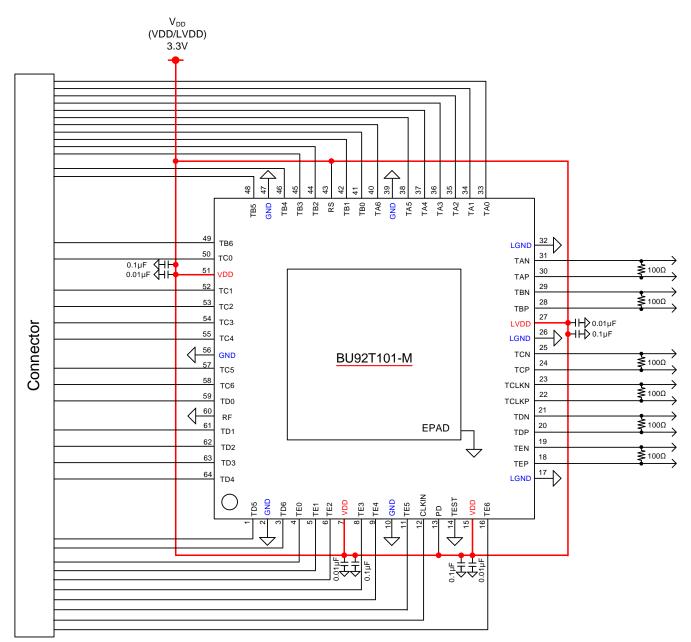


Figure 10. Application Example (1)

SOC

Application Examples - continued

BU92T101-M Connect with LVDS Receiver

 BU92T101-M (LVDS Transmitter)

 LVCMOS Parallel Data Input:

 33 Bits (R/G/B 30 Bits, HSYNC, VSYNC, DE)

 Input Clock Edge: Falling Edge (RF=L)

 LVDS Data Output:

 LVDS Output Swing: 350mV (RS=H)

BU16002KVT (LVDS Receiver) LVDS Data Input: LVCMOS Data Output:

(Need Termination Resistor on PCB) 33 Bits (R/G/B 30 Bits, HSYNC, VSYNC, DE) Output Clock Edge: Falling Edge (RF=L)

LVDS Data Mapping:

JEIDA Format (10Bit)

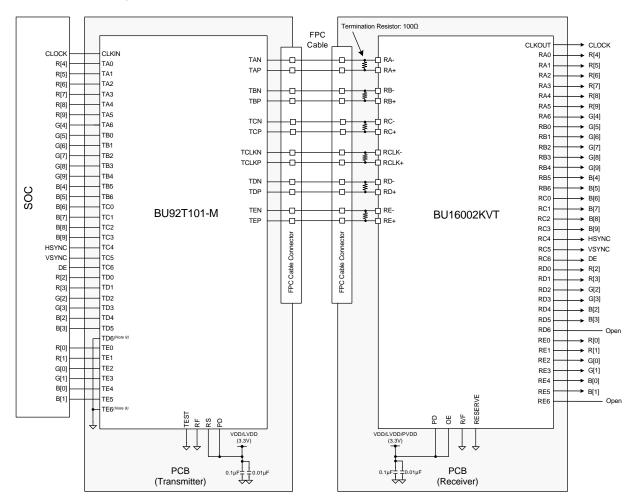


Figure 11. Application Example (2)

(Note 9) LVCMOS pixel data pins unused are recommended to connect to GND.

Application Examples - continued

BU92T101-M Connect with LVDS Repeater

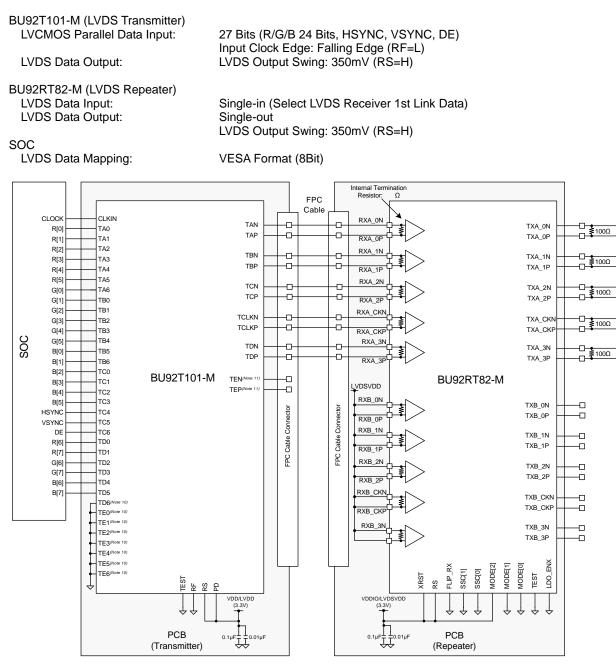


Figure 12. Application Example (3)

(Note 10) LVCMOS pixel data pins unused are recommended to connect to GND. (Note 11) LVDS pins unused should be open.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

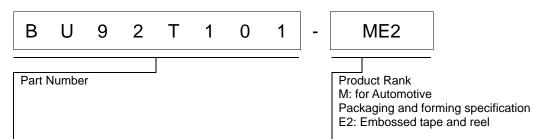
11. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

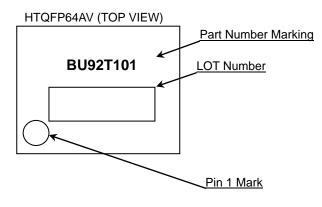
12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

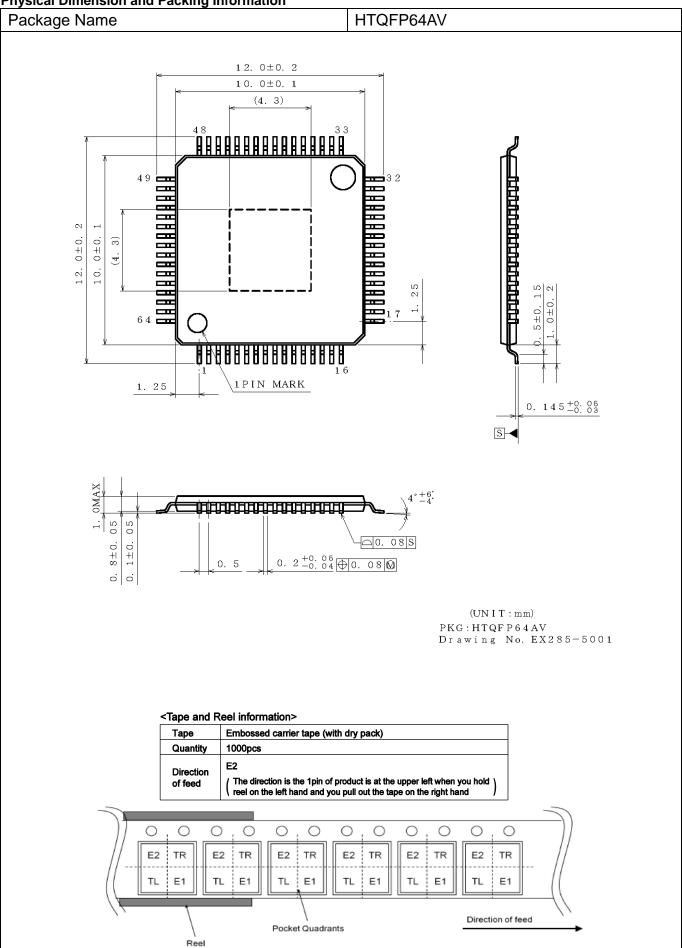
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
25.Oct.2017	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applica	ions
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JAPAN	USA	EU	CHINA
CLASSI	CLASSⅢ	CLASS II b	CLASSII
CLASSⅣ	CLASSI	CLASSⅢ	CLASSII

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:

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[b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
- 2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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