2PAI SEMICONDUCTOR

Enhanced ESD, 5.0 kV rms, 2Mbps Triple-Channel Digital Opto-Couplers

Data Sheet **π131S6XR**

FEATURES

- Ultra-low power consumption (2Mbps): 0.80mA /Channel
- Maximum data rate: 2Mbps
- High common-mode transient immunity: 250 kV/µs
- High robustness to radiated and conducted noise
- Isolation voltages: AC 5000Vrms
- High ESD rating:
  - ESDA/JEDEC JS-001-2017
  - Human body model (HBM) ±8kV
- Safety and regulatory approvals (Pending)：
  - UL certificate number:
    - 5000Vrms for 1 minute per UL 1577
  - VDE certificate number:
    - DIN V VDE V 0884-11 (VDE V 0884-11):2017-01
    - V_{IORM} = 1200V peak
  - CQC certification per GB4943.1-2011
- 2.5 V to 5.5 V level translation
- Wide temperature range: -40°C to 125°C
- 10-Lead, RoHS-compliant WB SSOIC-10 package

APPLICATIONS

- General-purpose multichannel isolation
- Industrial field bus isolation
- Isolation Industrial automation systems
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control

GENERAL DESCRIPTION

The π1xxxxxR is a 2PaiSemi digital Opto-Coupler product family that includes over hundreds of digital isolator products. By using maturated standard semiconductor CMOS technology and 2PaiSemi ***iDivider®*** technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The π1xxxxxR digital Opto-Coupler data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 5.0 kV rms and the data rate from DC up to 200Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 2.5 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

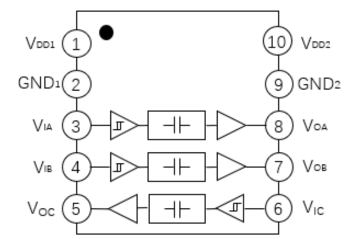

Figure 1.π131S6XR functional Block Diagram

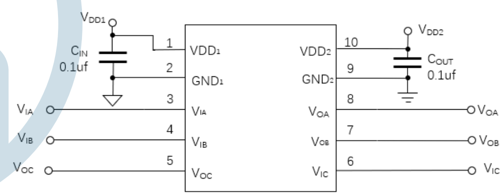

Figure 2.π131S6XR Typical Application Circuit

Rev.1.1

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PIN CONFIGURATIONS AND FUNCTIONS

Table 1.π131S6XR Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{IC}	Logic Input C.
7	V_{OB}	Logic Output B.
8	V_{OA}	Logic Output A.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	V_{DD2}	Supply Voltage for Isolator Side 2.

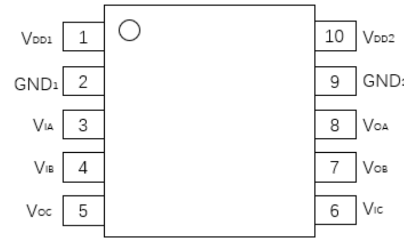


Figure 3.π131S6XR Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Table 2.Absolute Maximum Ratings[4]

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC})[1]	−0.5 V to V_{DDx} + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC})[1]	−0.5 V to V_{DDx} + 0.5 V
Average Output Current per Pin[2] Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Average Output Current per Pin[2] Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients Immunity[3]	−300 kV/µs to +300 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[2] See *Figure 4* for the maximum rated current values for various temperatures.

[3] See *Figure 12* for Common-mode transient immunity (CMTI) measurement.

[4] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 3.Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	2.5		5.5	V
High Level Input Signal Voltage	V_{IH}	0.6*V_{DDx}[1]		V_{DDx}[1]	V
Low Level Input Signal Voltage	V_{IL}	0		0.3*V_{DDx}[1]	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Maximum Data Rate		0		2	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 4.π131S6XR Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low V_{Ox} Output[1]	Default High V_{Ox} Output[1]	Test Conditions /Comments
Low	Powered[2]	Powered[2]	Low	Low	Normal operation
High	Powered[2]	Powered[2]	High	High	Normal operation
Open	Powered[2]	Powered[2]	Low	High	Default output
Don't Care[4]	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	

Notes:

[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

[2] Powered means $V_{DDx} \geq 2.4$ V

[3] Unpowered means $V_{DDx} < 2.0$V

[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.

[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 18us.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 5.Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2}$ =2.5V_{DC}±3% or 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			0.5	us	Within pulse width distortion (PWD) limit
Maximum Data Rate		2			Mbps	Within PWD limit
Propagation Delay Time[1,4]	t_{pHL}, t_{pLH}		0.28	0.5	us	The different time between 50% input signal to 50% output signal 50% @ 5V_{DC} supply
			0.29	0.5	us	@ 3.3V_{DC} supply
			0.30	0.5	us	@ 2.5V_{DC} supply
Pulse Width Distortion[4]	PWD	0	1	10	ns	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
		0	1	10	ns	@ 3.3V_{DC} supply
		0	1	10	ns	@ 2.5V_{DC} supply
Part to Part Propagation Delay Skew[4]	t_{PSk}			150	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V_{DC} supply
				150	ns	@ 3.3V_{DC} supply
				150	ns	@ 2.5V_{DC} supply
Channel to Channel Propagation Delay Skew[4]	t_{CSK}		0	50	ns	The max amount propagation delay time differs between any two output channels in the single device @ 5V_{DC} supply.
			0	50	ns	@ 3.3V_{DC} supply
			0	50	ns	@ 2.5V_{DC} supply
Output Signal Rise/Fall Time[4]	t_r/t_f		1.5		ns	See *Figure 9*
Common-Mode Transient Immunity[3]	CMTI		250		kV/µs	$V_{IN} = V_{DDx}{}^2$ or 0V, V_{CM} = 1000 V.
ESD (HBM - Human body model)	ESD		±8		kV	

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See *Figure 10*.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.
[3] See *Figure 12* for Common-mode transient immunity (CMTI) measurement.
[4] t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal， t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 6.DC Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} =2.5V_{DC}±3% or 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	V_{IT+}		0.5*V_{DDx}[1]	0.6*V_{DDx}[1]	V	
Falling Input Signal Voltage Threshold	V_{IT-}	0.3* V_{DDx}[1]	0.35* V_{DDx}[1]		V	
High Level Output Voltage	V_{OH} [1]	V_{DDx} − 0.1	V_{DDx}		V	−20 μA output current
		V_{DDx} − 0.2	V_{DDx} − 0.1		V	−2 mA output current
Low Level Output Voltage	V_{OL}		0	0.1	V	20 μA output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	I_{IN}	−10	0.5	10	μA	0 V ≤ Signal voltage ≤ V_{DDX}[1]
V_{DDx}[1] Undervoltage Rising Threshold	V_{DDxUV+}	2.1	2.25	2.4	V	
V_{DDx}[1] Undervoltage Falling Threshold	V_{DDxUV-}	2.0	2.1	2.25	V	
V_{DDx}[1] Hysteresis	V_{DDxUVH}		0.15		V	

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 7.Quiescent Supply Current

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} =2.5V_{DC}±3% or 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 10 pF, unless otherwise noted.

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
π131S6XR	$I_{DD1 (Q)}$		0.83	0.97	mA	5V_{DC}	Input is same with default output
	$I_{DD2 (Q)}$		1.34	1.6	mA		
	$I_{DD1 (Q)}$		1.24	1.61	mA		Input is not same with default output
	$I_{DD2 (Q)}$		1.69	2.41	mA		
	$I_{DD1 (Q)}$		0.81	0.95	mA	3.3V_{DC}	Input is same with default output
	$I_{DD2 (Q)}$		1.32	1.58	mA		
	$I_{DD1 (Q)}$		1.21	1.5	mA		Input is not same with default output
	$I_{DD2 (Q)}$		1.66	2.19	mA		
	$I_{DD1 (Q)}$		0.78	0.95	mA	2.5V_{DC}	Input is same with default output
	$I_{DD2 (Q)}$		1.30	1.58	mA		
	$I_{DD1 (Q)}$		1.17	1.45	mA		Input is not same with default output
	$I_{DD2 (Q)}$		1.63	2.12	mA		

Table 8.Total Supply Current vs. Data Throughput (C_L = 10 pF)

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 2.5V_{DC}±3% or 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 10 pF, unless otherwise noted.

Parameter	Symbol	50Kbps			150Kbps			2Mbps			Unit	Supply voltage
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
π131S6XR	I_{DD1}		1.04	1.29		1.04	1.29		1.20	1.50	mA	5V_{DC}
	I_{DD2}		1.53	2		1.54	2		1.84	2.34	mA	
	I_{DD1}		1.01	1.23		1.02	1.23		1.11	1.24	mA	3.3V_{DC}
	I_{DD2}		1.5	1.89		1.51	1.89		1.70	1.90	mA	
	I_{DD1}		0.96	1.2		0.97	1.2		1.03	1.21	mA	2.5V_{DC}
	I_{DD2}		1.47	1.85		1.48	1.85		1.63	1.86	mA	

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 9.Insulation Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration

Minimum External Air Gap (Clearance)	L (CLR)	⩾8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	⩾8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		⩾21	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN EN 60112 (VDE 0303-11):2010-05
Material Group		II		IEC 60112:2003 + A1:2009

PACKAGE CHARACTERISTICS

Table 10.Package Characteristics

Parameter	Symbol	Typical Value	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{IO}	10^{11}	Ω	
Capacitance (Input to Output)[1]	C_{IO}	1.5	pF	@1MHz
Input Capacitance[2]	C_I	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}	45	°C/W	Thermocouple located at center of package underside

Notes:

[1]The device is considered a 2-terminal device; WB SSOIC-10 Pin1~Pin5 are shorted together as the one terminal, and WB SSOIC-10 Pin6~Pin10 are shorted together as the other terminal.

[2]Testing from the input signal pin to ground.

REGULATORY INFORMATION

See Table 11 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 11.Regulatory

Regulatory	π131S6XR
UL	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 5000V rms Isolation Voltage File (pending)
VDE	DIN V VDE V 0884-11 (VDE V 0884-11):2017-01[2] Basic insulation, V_{IORM} = 1200 V peak, V_{IOSM} = 5000 V peak File (pending)
CQC	Certified under CQC11-471543-2012 and GB4943.1-2011 Basic insulation at 845 V rms (1200 V peak) working voltage Reinforced insulation at 422 V rms (600 V peak) File (pending)

Notes:

[1] In accordance with UL 1577, each π131S6XR is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-11, each π131S6XR is proof tested by ≥1800V peak for 1 sec.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

These digital Opto-Couplers are suitable for basic electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 12.VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms			I to IV	

For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to III I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Rated Isolation Working Voltage		V_{IOWM}	1200	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1800	V peak
Input to Output Test Voltage, Method A		$V_{pd\,(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.3 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1560	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1440	V peak
Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	V_{IOTM}	7071	V peak
Surge Isolation Voltage Basic	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 6500\ V_{PK}$	V_{IOSM}	5000	V peak
Surge Isolation Voltage Reinforced	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	V_{IOSM}	/	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see *Figure 4*)			
Maximum Safety Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.14	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

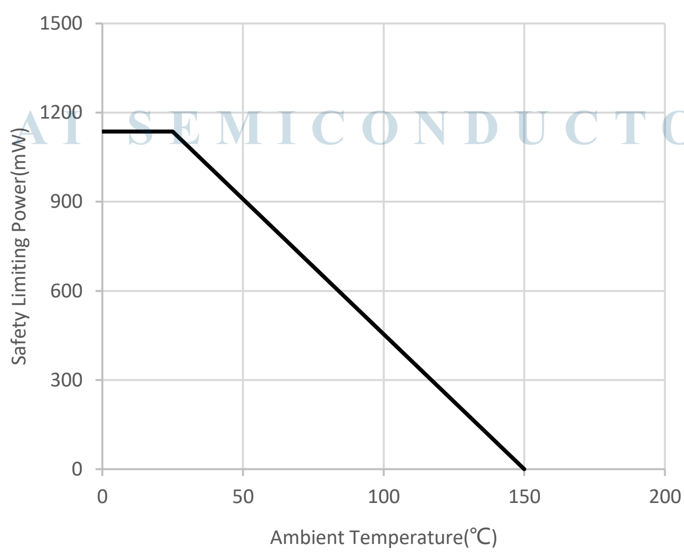


Figure 4.Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE

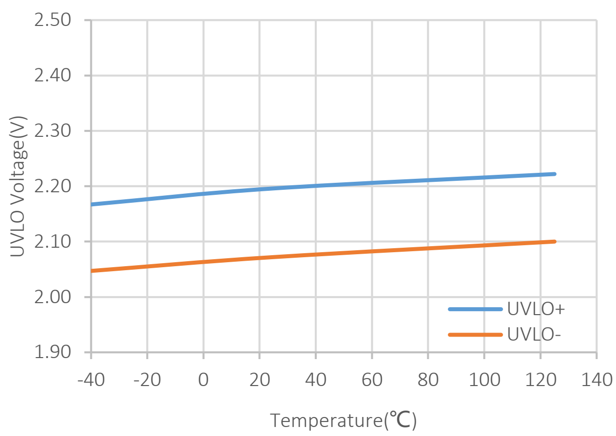


Figure 5.UVLO vs. Temperature

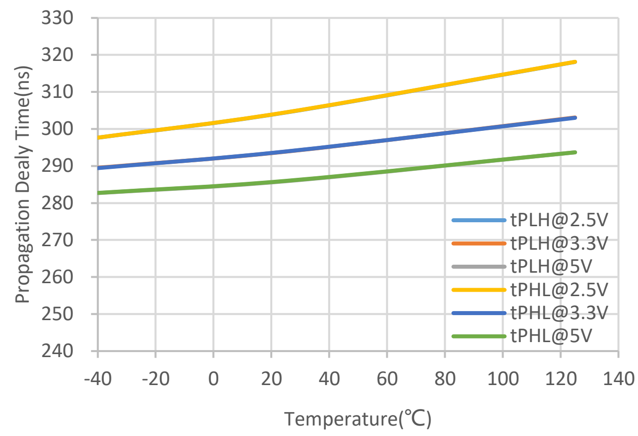


Figure 6.Propagation Dealy Time vs. Temperature

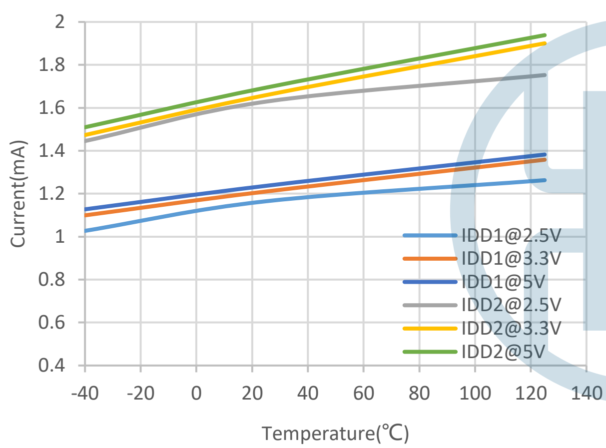


Figure 7. Quiescent Supply Current with 0V input vs. Temperature

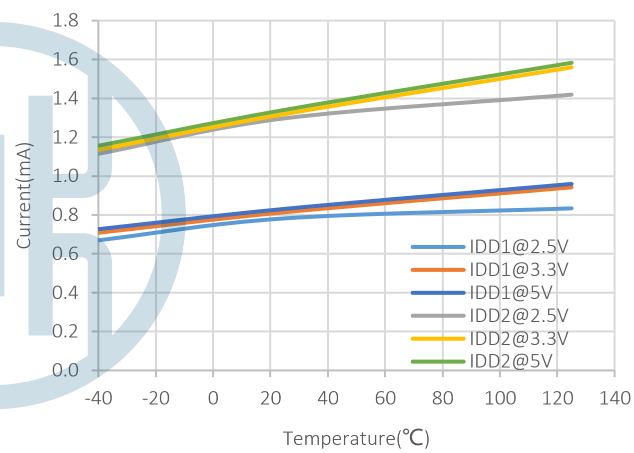


Figure 8. Quiescent Supply Current with VDDx input vs. Temperature

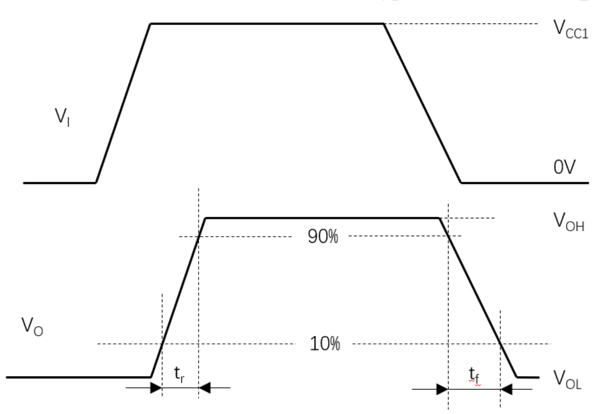


Figure 9.Transition time waveform measurement

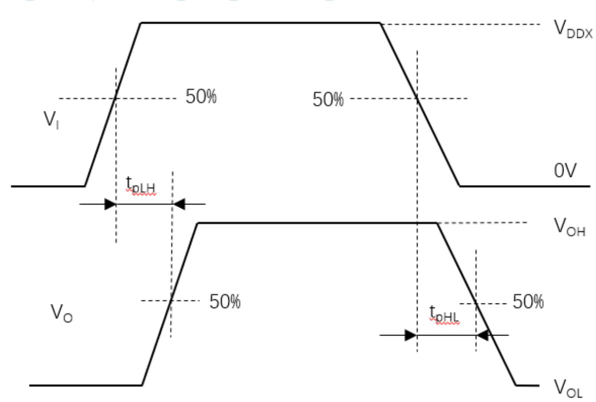


Figure 10.Propagation delay time waveform measurement

APPLICATIONS INFORMATION

OVERVIEW

The π1xxxxxR are 2PaiSemi digital Opto-Couplers product family based on 2PaiSemi unique ***iDivider®*** technology. Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, ***iDivider®*** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using maturated standard semiconductor CMOS technology and the innovative ***iDivider®*** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The π1xxxxxR digital Opto-Coupler data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 5.0 kV rms and the data rate from DC up to 200Mbps (see the Ordering Guide).

The π131S6XR are the outstanding 2Mbps triple-channel digital Opto-Couplers with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation. The devices operate with the supply voltage on either side ranging from 2.5 V to 5.5 V, offering voltage translation of 2.5 V and 5 V logic.

The π131S6XR have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 2.5 V to 5.5 V, offering voltage translation of 2.5 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between VDD1 and GND1 and between VDD2 and GND2. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1μF and 10μF. The user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy, or in order to enhance the anti ESD ability of the system.

Figure 11.Recommended Printed Circuit Board Layout

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

CMTI MEASUREMENT

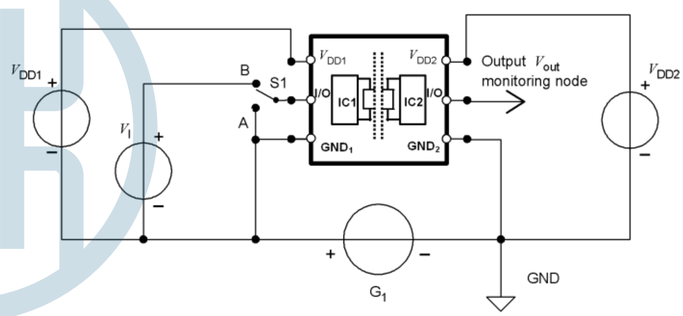
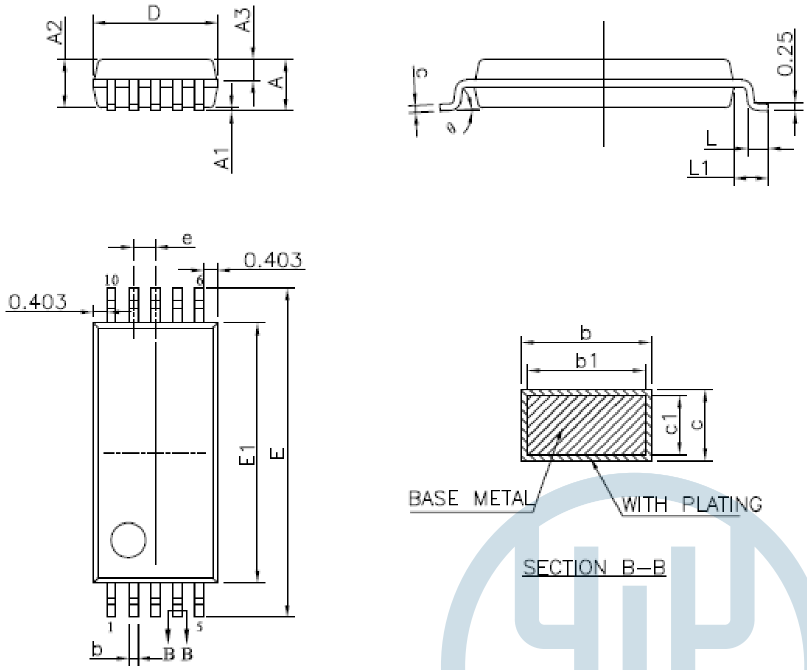


Figure 12.Common-mode transient immunity (CMTI) measurement

To measure the Common-Mode Transient Immunity (CMTI) of π1xxxxx isolator under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions, The common-mode pulse generator (G_1) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse (V_{CM}) and the maximum common-mode slew rates (dV_{CM}/dt) can be applied to π1xxxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of π1xxxxx isolator and shall be capable of providing positive transients as well as negative transients.

OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.65
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.55	0.60	0.65
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	3.50	3.60	3.70
E	9.30	9.50	9.70
E1	7.40	7.50	7.60
e	0.635BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 13.10-Lead wide body SSOIC Package

Land Patterns

The below figure illustrates the recommended land pattern details for the π131S6XR in a 10-Lead wide body SSOIC. The table below lists the values for the dimensions shown in the illustration.

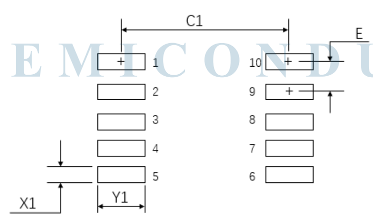


Figure 14. 10-Lead wide body SSOIC Land Pattern

Table 13. 10-Lead wide body SSOIC Land Pattern Dimensions

Dimension	Feature	Value	Unit
C1	Pad column spacing	8.9	mm
E	Pad row pitch	0.635	mm
X1	Pad width	0.4	mm
Y1	Pad length	1.5	mm

Note：

1.This land pattern design is based on IPC -7351 for Density Level B (Median Land Protrusion).

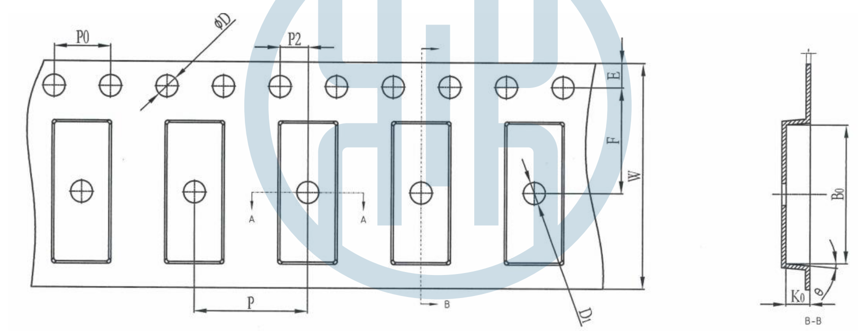
2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

Top Marking

Line 1	πxxxxxxx=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXX, no special meaning

Figure 15.Top marking

REEL INFORMATION



Items	Size(mm)
E	1.75±0.10
F	7.50±0.10
P_2	2.00±0.05
D	1.55±0.05
D_1	1.55±0.05
P_0	4.00±0.10
$10P_0$	40.0±0.20

Items	Size(mm)
W	16.00±0.10
P	8.00±0.10
A_0	3.90±0.10
B_0	9.90±0.10
K_0	1.80±0.10
t	0.30±0.02
θ	5°TYP

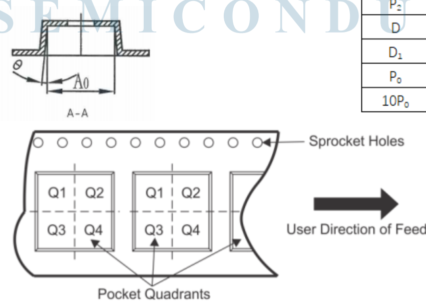


Figure 16.Reel information

ORDERING GUIDE

Table 14.Ordering guide

Model Name [1]	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	MSL Peak Temp [2]	MOQ/ Quantity per reel [3]
π131S61R	−40~125°C	2	1	5	High	WB SSOIC-10	Level-3-260C-168 HR	4000
π131S60R	−40~125°C	2	1	5	Low	WB SSOIC-10	Level-3-260C-168 HR	4000

Note：

1. Pai1xxxxxx is equals to π1xxxxxx in the customer BOM

2. MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

3. MOQ, minimum ordering quantity.

PART NUMBER NAMED RULE

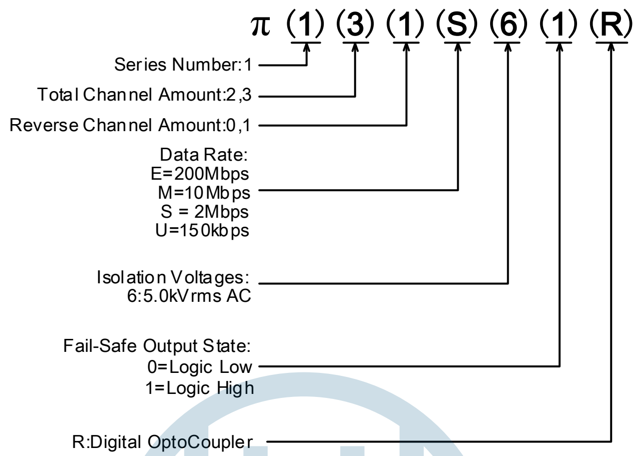


Figure 17. Part number named rule

Notes:
Pai1xxxxxx is equals to π1xxxxx in the customer BOM

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REVISION HISTORY

Revision	Date	Page	Change Record
Rev.1.0	2021/11/17	All	Initial version
Rev.1.1	2022/01/17	Page1	Update the general description
		Page 3	Update the table 5
		Page 5	Update the table 12

