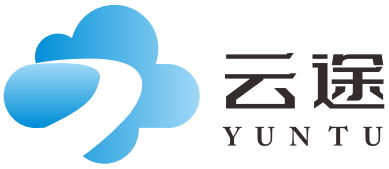

YTM32B1ME0x Product Brief

support YTM32B1ME0xG0MLQT, YTM32B1ME0xG0MLLT, YTM32B1ME0xG0MLHT

Document Number: REV 1.0

2021/12/6

Contents

Revision history

Rev.No.	Date	Substantive Change(s)
1.0	2021/12/6	Initial release

1 Ordering parts

Product	Memory		Package	
Part number	Flash(KB)	SRAM(KB)	Pin count	Package
YTM32B1ME05G0MLQT	1024	128	144	LQFP
YTM32B1ME04G0MLQT	512	64	144	LQFP
YTM32B1ME03G0MLQT	256	32	144	LQFP
YTM32B1ME05G0MLLT	1024	128	100	LQFP
YTM32B1ME04G0MLLT	512	64	100	LQFP
YTM32B1ME03G0MLLT	256	32	100	LQFP
YTM32B1ME05G0MLHT	1024	128	64	LQFP
YTM32B1ME04G0MLHT	512	64	64	LQFP
YTM32B1ME03G0MLHT	256	32	64	LQFP

2 Introduction

YTM32B1ME0x series provide the highly scalable portfolio of ARM® Cortex®-M33 MCUs in the automotive industry. With 2.7 ~ 5.5 V supply and focus on exceptional EMC/ESD robustness, YTM32B1ME0x series devices are well suited to a wide range of applications in electrical harsh environments, and are optimized for cost-sensitive applications offering low pin-count option.

The YTM32B1ME0x series offers a broad range of memory, peripherals and package options. They share common peripherals and pin counts allowing developers to migrate easily within an MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the YTM32B1ME0x series for their end product platforms, maximizing hardware and software reuse and reducing time-to-market.

Following are the general features of the YTM32B1ME0x series MCUs.

- 32-bit ARM Cortex-M33 with FPU and DSP, up to 120 MHz
- Up to 1 MB Program Flash memory and 256 KB Data flash with ECC support
- Up to 128 KB SRAM
  - Supporting ECC feature
  - There are two 16KB SRAM which supports data retention in powerdown mode
- 32 bytes register file which supports data retention in powerdown mode
- Integrated clock architecture with on-chip fast IRC 96 MHz, slow IRC 12 MHz, fast OSC 40 MHz, slow OSC 32 KHz and a PLL 120 MHz
- Power Control Unit (PCU) with internal regulators capable of supporting multiple power modes including:
  - Active
  - Sleep
  - Deepsleep
  - Standby
  - Powerdown
- support up to 32 WKU pins to wake up powerdown mode
- 16 DMA channels with 128 hardware trigger sources
- Human-machine interface

  - Up to 126 general-purpose input/output (GPIO)
  - External interrupt
- Analog modules providing precision mixed-signal capabilities, including:
  - two 12-bit, 2Msps SAR ADCs
  - On-chip Analog Comparator (ACMP) with 8-bit DAC
  - 1.89mV/℃ temperature sensor
- Timers
  - one Timer (TMR)
  - one 4-channel Periodic Timer (pTMR)
  - one Low Power Timer (lpTMR)
  - six Enhanced Timer (eTMR)
  - one Real-Time Clock (RTC)
  - one Programmable Trigger Unit (PTU)
- Serial communication interfaces
  - six FlexCAN modules with FD
  - six LINFlexD modules
  - six SPI modules
  - three I2C modules
- I/O supporting 2.7 V to 5.5 V supply
- Wide operating voltage ranges (2.7 - 5.5 V) with fully functional flash memory program/erase/read operations
- Temperature range:
  - Ambient operating temperature: -40℃ ~ 125℃
  - Junction operating temperature: -40℃ ~ 150℃
- Security and Safety features are supported as follow:
  - Cyclic Redundancy Checker (CRC)
  - Hardware Cryptography Unit (HCU) which supports AES/SM4/SHA
  - True Random Number Generator (TRNG)
  - Clock Monitor Unit (CMU)
  - Watchdog (WDG)
  - External watchdog (EWDG)
  - MPU for dynamic task protection (16 regions)
  - Peripheral Protection Unit (PPU)
  - Interrupt Monitor (INTM)
  - ECC Management Unit (EMU)
- Debug functionality
  - Joint Test Action Group (JTAG)
  - Serial Wire Debug (SWD)
- Package options
  - 144-pin LQFP
  - 100-pin LQFP
  - 64-pin LQFP

The YTM32B1ME0x MCU portfolio is supported by a highly comprehensive set of development tools and software. The enablement package includes: YTMicroelectronics Software Development Kit (SDK), graphical configuration tool, as well as broad support from IAR Systems, MDK, GCC and other partners.

3 Block diagram

The following figure shows an overall block diagram of the device.

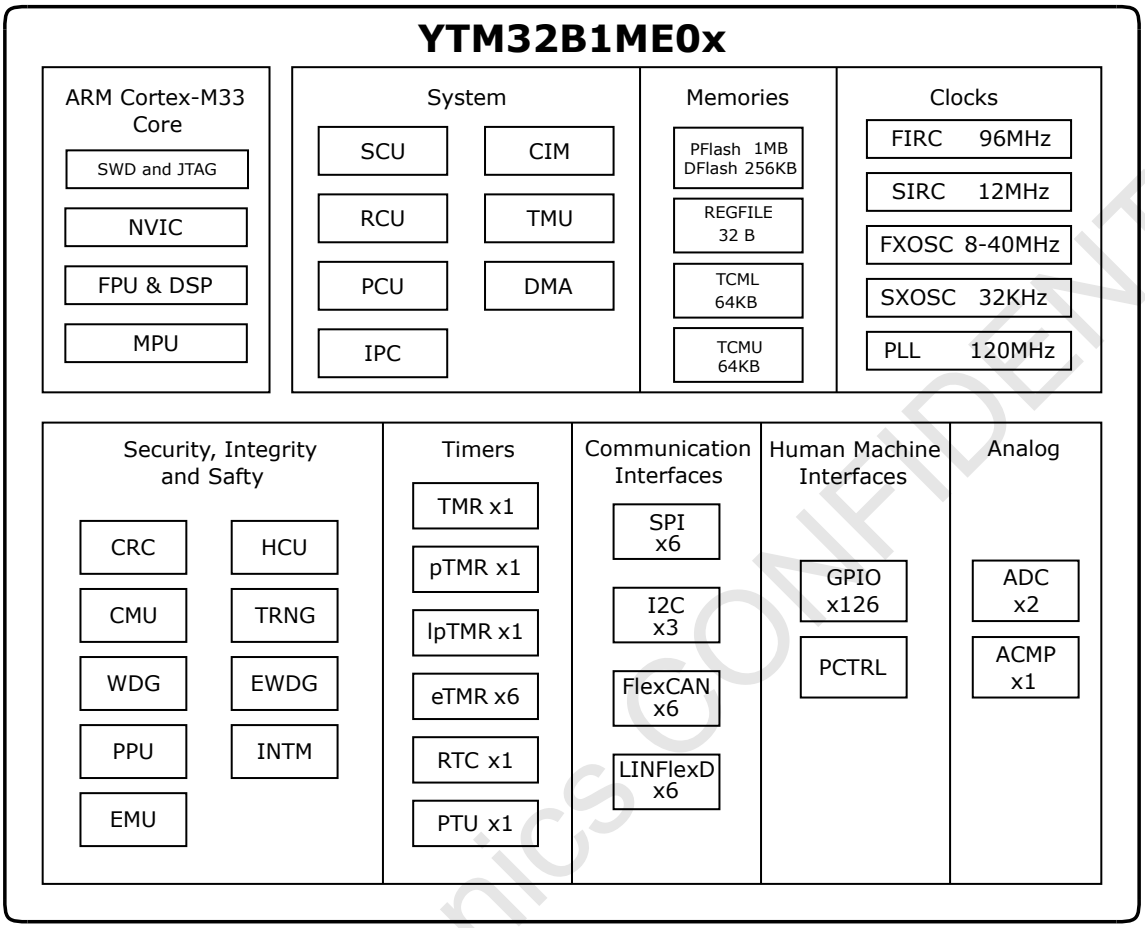

Figure 1: YTM32B1ME0x block diagram

4 Pinmux definition

4.1 Pinmux table

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document.

Table 3: Pinmux Table

144 LQFP	100 LQFP	64 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	-	PTE_16	-	PTE_16	-	SPI2_SIN	eTMR2_CH7	eTMR4_FLT0	-	TRGMUX_OUT7
2	2	-	PTE_15	-	PTE_15	-	SPI2_SCK	eTMR2_CH6	eTMR4_FLT1	-	TRGMUX_OUT6
3	3	1	VDD11	VDD11	-	-	-	-	-	-	-
4	4	2	VDD25	VDD25	-	-	-	-	-	-	-
5	5	3	PTE_11	-	PTE_11	SPI2_PCS0	LPTMR0_ALT1	eTMR2_CH5	LINFlex3_TX	ETM_TRACE_D0	TRGMUX_OUT5
6	6	4	PTE_10	-	PTE_10	SCU_CLKOUT	SPI2_PCS1	eTMR2_CH4	LINFlex3_RX	-	TRGMUX_OUT4
7	7	-	PTE_13	-	PTE_13	eTMR4_CH5	SPI2_PCS2	eTMR2_FLT0	-	-	-
8	8	5	PTE_5	-	PTE_5	TCLK_IN2	eTMR2_QD_PHA	eTMR2_CH3	CAN0_TX	-	EWDG_IN
9	9	6	PTE_4	-	PTE_4	ETM_TRACE_D1	eTMR2_QD_PHB	eTMR2_CH2	CAN0_RX	-	EWDG_OUT_b

144 LQFP	100 LQFP	64 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
10	-	-	PTA_25	-	PTA_25	eTMR5_CH0	-	-	-	-	-
11	10	7	VDD	VDD	-	-	-	-	-	-	-
12	-	-	VSS	VSS	-	-	-	-	-	-	-
13	11	8	VDDA	VDDA	-	-	-	-	-	-	-
14	12	9	VREFH	VREFH	-	-	-	-	-	-	-
15	13	-	VREFL	VREFL	-	-	-	-	-	-	-
16	14	10	VSS	VSS	-	-	-	-	-	-	-
17	15	11	PTB_7	EXTAL	PTB_7	I2C0_SCL	-	SPI3_SCK	eTMR4_FLT3	-	TRGMUX_OUT2
18	16	12	PTB_6	XTAL	PTB_6	I2C0_SDA	-	SPI3_SIN	eTMR4_FLT2	-	TRGMUX_OUT1
19	-	-	PTA_26	-	PTA_26	eTMR5_CH1	SPI1_PCS0	SPI0_PCS0	-	-	-
20	17	-	PTE_14	-	PTE_14	eTMR0_FLT1	-	eTMR2_FLT1	-	-	-
21	18	13	PTE_3	-	PTE_3	eTMR0_FLT0	SPI1_SIN	eTMR2_FLT0	SPI3_SOUT	TRGMUX_IN6	ACMP0_OUT
22	-	-	PTA_27	-	PTA_27	eTMR5_CH2	SPI1_SOUT	LINFlex0_TX	CAN0_TX	-	-
23	19	-	PTE_12	-	PTE_12	eTMR0_FLT3	LINFlex2_TX	eTMR5_FLT0	SPI3_PCS0	-	-
24	-	-	PTA_28	-	PTA_28	eTMR5_CH3	SPI1_SCK	LINFlex0_RX	CAN0_RX	-	-
25	20	-	PTD_17	-	PTD_17	eTMR0_FLT2	LINFlex2_RX	eTMR5_FLT1	-	-	-
26	-	-	PTA_29	-	PTA_29	eTMR5_CH4	-	LINFlex2_TX	SPI1_SIN	-	-
27	-	-	PTA_30	-	PTA_30	eTMR5_CH5	LINFlex2_RX	SPI0_SOUT	-	-	-
28	21	14	PTD_16	EXTAL32	PTD_16	eTMR0_CH1	CAN4_TX	SPI0_SIN	ACMP0_ACTIVE	ETM_TRACE_D2	ETM_TRACE_CLKOUT
29	22	15	PTD_15	XTAL32	PTD_15	eTMR0_CH0	CAN4_RX	SPI0_SCK	-	ETM_TRACE_D3	-
30	23	16	PTE_9	-	PTE_9	eTMR0_CH7	SPI1_SCK	I2C2_SDA	-	-	-
31	-	-	VSS	VSS	-	-	-	-	-	-	-
32	-	-	VDD	VDD	-	-	-	-	-	-	-
33	-	-	PTA_31	-	PTA_31	eTMR5_CH6	-	SPI0_PCS1	-	-	-
34	24	-	PTD_14	-	PTD_14	eTMR2_CH5	LINFlex1_TX	-	SPI5_PCS3	-	SCU_CLKOUT
35	25	-	PTD_13	-	PTD_13	eTMR2_CH4	LINFlex1_RX	-	SPI5_PCS2	-	RTC_CLKOUT
36	-	-	PTB_18	ADC0_SE16	PTB_18	eTMR5_CH7	-	SPI1_PCS1	-	-	-
37	-	-	PTB_20	ADC0_SE17	PTB_20	LINFlex3_TX	-	-	I2C1_SDA	-	-
38	-	-	PTB_21	ADC0_SE18	PTB_21	LINFlex3_RX	-	-	I2C1_SCL	-	-
39	26	17	PTE_8	ACMP0_IN3	PTE_8	eTMR0_CH6	-	I2C2_SCL	SPI3_PCS1	-	-
40	27	18	PTB_5	-	PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	SCU_CLKOUT	TRGMUX_IN0	-
41	28	19	PTB_4	-	PTB_4	eTMR0_CH4	SPI0_SOUT	-	-	TRGMUX_IN1	-
42	29	20	PTC_3	ADC0_SE11 ACMP0_IN4	PTC_3	eTMR0_CH3	CAN0_TX	LINFlex0_TX	SPI4_PCS0	-	-
43	30	21	PTC_2	ADC0_SE10 ACMP0_IN5	PTC_2	eTMR0_CH2	CAN0_RX	LINFlex0_RX	SPI4_SCK	ETM_TRACE_CLKOUT	-
44	31	22	PTD_7	ACMP0_IN6	PTD_7	LINFlex2_TX	eTMR0_CH3	eTMR2_FLT3	SPI4_SIN	ETM_TRACE_D0	-
45	32	23	PTD_6	ACMP0_IN7	PTD_6	LINFlex2_RX	eTMR0_CH2	eTMR2_FLT2	SPI4_SOUT	-	-
46	33	24	PTD_5	-	PTD_5	eTMR2_CH3	LPTMR0_ALT2	eTMR2_FLT1	SPI4_PCS1	TRGMUX_IN7	-
47	34	-	PTD_12	-	PTD_12	eTMR2_CH2	-	ETM_TRACE_D1	SPI5_SIN	-	-
48	35	-	PTD_11	-	PTD_11	eTMR2_CH1	eTMR2_QD_PHA	ETM_TRACE_D2	SPI5_SOUT	-	-
49	36	-	PTD_10	-	PTD_10	eTMR2_CH0	eTMR2_QD_PHB	ETM_TRACE_D3	SPI5_SCK	SCU_CLKOUT	-
50	37	-	VSS	VSS	-	-	-	-	-	-	-
51	38	-	VDD	VDD	-	-	-	-	-	-	-
52	39	25	PTC_1	ADC0_SE9	PTC_1	eTMR0_CH1	SPI2_SOUT	CAN3_TX	-	eTMR1_CH7	-
53	40	26	PTC_0	ADC0_SE8	PTC_0	eTMR0_CH0	SPI2_SIN	CAN3_RX	-	eTMR1_CH6	-
54	41	-	PTD_9	-	PTD_9	LINFlex4_TX	-	eTMR2_FLT3	-	eTMR1_CH5	-
55	42	-	PTD_8	-	PTD_8	LINFlex4_RX	-	eTMR2_FLT2	-	eTMR1_CH4	-
56	43	27	PTC_17	ADC0_SE15	PTC_17	eTMR1_FLT3	CAN2_TX	SPI4_PCS0	eTMR2_CH1	-	-
57	44	28	PTC_16	ADC0_SE14	PTC_16	eTMR1_FLT2	CAN2_RX	SPI4_SCK	eTMR2_CH0	-	-
58	-	-	PTB_22	ADC0_SE19	PTB_22	-	-	-	LINFlex1_TX	-	-
59	45	29	PTC_15	ADC0_SE13	PTC_15	eTMR1_CH3	SPI2_SCK	SPI4_SIN	LINFlex4_TX	TRGMUX_IN8	-
60	-	-	PTB_23	ADC0_SE20	PTB_23	-	LINFlex1_RX	-	-	-	-

144 LQFP	100 LQFP	64 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
61	46	30	PTC_14	ADC0_SE12	PTC_14	eTMR1_CH2	SPI2_PCS0	SPI4_SOUT	LINFlex4_RX	TRGMUX_IN9	-
62	-	-	PTB_25	ADC0_SE21	PTB_25	-	-	SPI4_PCS1	SPI2_PCS0	-	-
63	47	31	PTB_3	ADC0_SE7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA	-	TRGMUX_IN2	-
64	-	-	PTB_27	ADC0_SE22	PTB_27	eTMR5_FLT2	-	-	SPI2_SOUT	-	-
65	-	-	PTB_28	ADC0_SE23	PTB_28	eTMR5_FLT3	-	-	SPI2_SIN	-	-
66	-	-	VSS	VSS	-	-	-	-	-	-	-
67	-	-	VDD	VDD	-	-	-	-	-	-	-
68	48	32	PTB_2	ADC0_SE6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB	-	TRGMUX_IN3	-
69	-	-	PTB_29	-	PTB_29	-	-	-	SPI2_SCK	-	-
70	49	-	PTC_13	-	PTC_13	eTMR3_CH7	eTMR2_CH7	-	-	-	-
71	50	-	PTC_12	-	PTC_12	eTMR3_CH6	eTMR2_CH6	-	-	-	-
72	-	-	PTC_19	-	PTC_19	-	-	-	SPI2_PCS1	-	-
73	-	-	PTC_23	-	PTC_23	SPI0_SCK	-	-	-	-	-
74	51	-	PTC_11	-	PTC_11	eTMR3_CH5	eTMR4_CH2	CAN5_TX	-	TRGMUX_IN10	-
75	52	-	PTC_10	-	PTC_10	eTMR3_CH4	-	CAN5_RX	-	TRGMUX_IN11	-
76	-	-	PTC_27	-	PTC_27	eTMR4_CH4	-	-	-	-	-
77	53	33	PTB_1	ADC0_SE5	PTB_1	LINFlex0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	eTMR4_CH5	-
78	54	34	PTB_0	ADC0_SE4	PTB_0	LINFlex0_RX	SPI0_PCS0	LPTMR0_ALT3	CAN0_RX	eTMR4_CH6	-
79	-	-	PTC_28	-	PTC_28	eTMR4_CH7	-	-	-	-	-
80	55	35	PTC_9	-	PTC_9	LINFlex1_TX	eTMR1_FLT1	eTMR5_CH0	CAN4_TX	SPI5_PCS1	-
81	56	36	PTC_8	-	PTC_8	LINFlex1_RX	eTMR1_FLT0	eTMR5_CH1	CAN4_RX	SPI5_PCS0	-
82	-	-	PTC_29	-	PTC_29	eTMR5_CH2	-	-	-	-	-
83	57	37	PTA_7	ADC0_SE3	PTA_7	eTMR0_FLT2	eTMR5_CH3	RTC_CLKIN	I2C2_SCL	SPI5_SCK	-
84	-	-	PTC_30	-	PTC_30	eTMR5_CH4	-	-	-	-	-
85	58	38	PTA_6	ADC0_SE2	PTA_6	eTMR0_FLT1	SPI1_PCS1	eTMR5_CH5	I2C2_SDA	SPI5_SIN	-
86	-	-	PTC_31	-	PTC_31	eTMR5_CH6	-	-	-	-	-
87	59	39	PTE_7	-	PTE_7	eTMR0_CH7	eTMR3_FLT0	-	-	SPI5_SOUT	-
88	-	-	PTD_18	ADC1_SE16	PTD_18	eTMR5_CH7	-	CAN5_TX	-	-	-
89	-	-	PTD_19	ADC1_SE17	PTD_19	-	-	CAN5_RX	-	-	-
90	60	40	VSS	VSS	-	-	-	-	-	-	-
91	61	41	VDD	VDD	-	-	-	-	-	-	-
92	62	-	PTA_17	-	PTA_17	eTMR0_CH6	eTMR3_FLT0	EWDG_OUT_b	eTMR5_FLT0	-	-
93	63	-	PTB_17	-	PTB_17	eTMR0_CH5	SPI1_PCS3	eTMR5_FLT1	-	-	-
94	64	-	PTB_16	ADC1_SE15	PTB_16	eTMR0_CH4	SPI1_SOUT	-	-	-	-
95	65	-	PTB_15	ADC1_SE14	PTB_15	eTMR0_CH3	SPI1_SIN	-	-	-	-
96	66	-	PTB_14	ADC1_SE9	PTB_14	eTMR0_CH2	SPI1_SCK	-	-	-	-
97	67	42	PTB_13	ADC1_SE8	PTB_13	eTMR0_CH1	eTMR3_FLT1	CAN2_TX	-	-	-
98	68	43	PTB_12	ADC1_SE7	PTB_12	eTMR0_CH0	eTMR3_FLT2	CAN2_RX	-	-	-
99	-	-	PTD_22	ADC1_SE18	PTD_22	eTMR4_FLT2	-	-	-	-	-
100	69	44	PTD_4	ADC1_SE6	PTD_4	eTMR0_FLT3	eTMR3_FLT3	-	-	SPI5_PCS2	-
101	70	45	PTD_3	ADC1_SE3	PTD_3	eTMR3_CH5	SPI1_PCS0	I2C1_SCL	CAN5_TX	TRGMUX_IN4	NMI_b
102	71	46	PTD_2	ADC1_SE2	PTD_2	eTMR3_CH4	SPI1_SOUT	I2C1_SDA	CAN5_RX	TRGMUX_IN5	-
103	-	-	PTD_23	ADC1_SE19	PTD_23	eTMR4_FLT3	-	-	-	-	-
104	72	47	PTA_3	ADC1_SE1	PTA_3	eTMR3_CH1	I2C0_SCL	EWDG_IN	-	LINFlex0_TX	-
105	73	48	PTA_2	ADC1_SE0	PTA_2	eTMR3_CH0	I2C0_SDA	EWDG_OUT_b	-	LINFlex0_RX	-
106	-	-	PTD_24	ADC1_SE20	PTD_24	-	-	-	-	-	-
107	74	-	PTB_11	-	PTB_11	eTMR3_CH3	LINFlex5_TX	-	-	-	-
108	75	-	PTB_10	-	PTB_10	eTMR3_CH2	LINFlex5_RX	-	-	-	-
109	76	-	PTB_9	-	PTB_9	eTMR3_CH1	-	-	-	-	-
110	-	-	PTD_27	ADC1_SE21	PTD_27	eTMR5_FLT2	-	-	-	-	-
111	77	-	PTB_8	-	PTB_8	eTMR3_CH0	-	-	-	-	-
112	-	-	PTD_28	ADC1_SE22	PTD_28	eTMR5_FLT3	-	-	-	-	-

144 LQFP	100 LQFP	64 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
113	78	49	PTA_1	ADC0_SE1 ACMP0_IN1	PTA_1	eTMR1_CH1	LINFlex5_TX	-	eTMR1_QD_PHA	-	TRGMUX_OUT0
114	-	-	PTD_29	ADC1_SE23	PTD_29	-	-	-	-	-	-
115	79	50	PTA_0	ADC0_SE0 ACMP0_IN0	PTA_0	eTMR2_CH1	LINFlex5_RX	-	eTMR2_QD_PHA	-	TRGMUX_OUT3
116	-	-	PTD_30	-	PTD_30	-	-	-	-	-	-
117	80	51	PTC_7	ADC1_SE5	PTC_7	LINFlex1_TX	CAN1_TX	eTMR3_CH3	-	eTMR1_QD_PHA	-
118	81	52	PTC_6	ADC1_SE4	PTC_6	LINFlex1_RX	CAN1_RX	eTMR3_CH2	-	eTMR1_QD_PHB	-
119	82	-	PTA_16	ADC1_SE13	PTA_16	eTMR1_CH3	SPI1_PCS2	-	-	-	-
120	83	-	PTA_15	ADC1_SE12	PTA_15	eTMR1_CH2	SPI0_PCS3	SPI2_PCS3	-	-	-
121	84	53	PTE_6	ADC1_SE11	PTE_6	SPI0_PCS2	-	eTMR3_CH7	-	ETM_TRACE_D2	ETM_TRACE_CLKOUT
122	85	54	PTE_2	ADC1_SE10	PTE_2	SPI0_SOUT	LPTMR0_ALT3	eTMR3_CH6	-	ETM_TRACE_D3	-
123	86	-	VSS	VSS	-	-	-	-	-	-	-
124	87	-	VDD	VDD	-	-	-	-	-	-	-
125	-	-	PTE_19	-	PTE_19	-	-	-	-	-	-
126	-	-	PTE_20	-	PTE_20	eTMR4_CH0	-	-	-	-	-
127	88	-	PTA_14	-	PTA_14	eTMR0_FLT0	eTMR3_FLT1	EWDG_IN	-	eTMR1_FLT0	-
128	-	-	PTE_21	-	PTE_21	eTMR4_CH1	-	-	-	-	-
129	-	-	PTE_22	-	PTE_22	eTMR4_CH2	-	-	-	-	-
130	89	55	PTA_13	-	PTA_13	eTMR1_CH7	CAN1_TX	SPI3_PCS0	-	eTMR2_QD_PHA	-
131	-	-	PTE_23	-	PTE_23	eTMR4_CH3	-	-	-	-	-
132	-	-	PTE_24	-	PTE_24	eTMR4_CH4	CAN2_TX	-	-	-	-
133	-	-	PTE_25	-	PTE_25	eTMR4_CH5	CAN2_RX	-	-	-	-
134	90	56	PTA_12	-	PTA_12	eTMR1_CH6	CAN1_RX	SPI3_SCK	-	eTMR2_QD_PHB	-
135	91	57	PTA_11	-	PTA_11	eTMR1_CH5	-	SPI3_SIN	ACMP0_ACTIVE	-	-
136	92	58	PTA_10	-	PTA_10	eTMR1_CH4	-	SPI3_SOUT	-	-	JTAG_TDO_SWD_SWO
137	93	59	PTE_1	-	PTE_1	SPI0_SIN	-	-	SPI1_PCS0	eTMR1_FLT1	-
138	94	60	PTE_0	-	PTE_0	SPI0_SCK	TCLK_IN1	-	SPI1_SOUT	eTMR1_FLT2	-
139	95	61	PTC_5	-	PTC_5	eTMR2_CH0	RTC_CLKOUT	SPI3_PCS1	-	eTMR2_QD_PHB	JTAG_TDI
140	96	62	PTC_4	ACMP0_IN2	PTC_4	eTMR1_CH0	RTC_CLKOUT	-	EWDG_IN	eTMR1_QD_PHB	JTAG_TCK_SWD_CLK
141	97	63	PTA_5	-	PTA_5	CAN3_TX	TCLK_IN1	-	-	-	RESET_b
142	98	64	PTA_4	-	PTA_4	CAN3_RX	-	ACMP0_OUT	EWDG_OUT_b	-	JTAG_TMS_SWD_IO
143	99	-	PTA_9	-	PTA_9	LINFlex2_TX	SPI2_PCS0	-	eTMR3_FLT2	eTMR1_FLT3	eTMR4_FLT0
144	100	-	PTA_8	-	PTA_8	LINFlex2_RX	SPI2_SOUT	-	eTMR3_FLT3	eTMR4_FLT1	-

4.2 Pin assignment

The following diagrams are supported packages of YTM32B1ME0x series chip

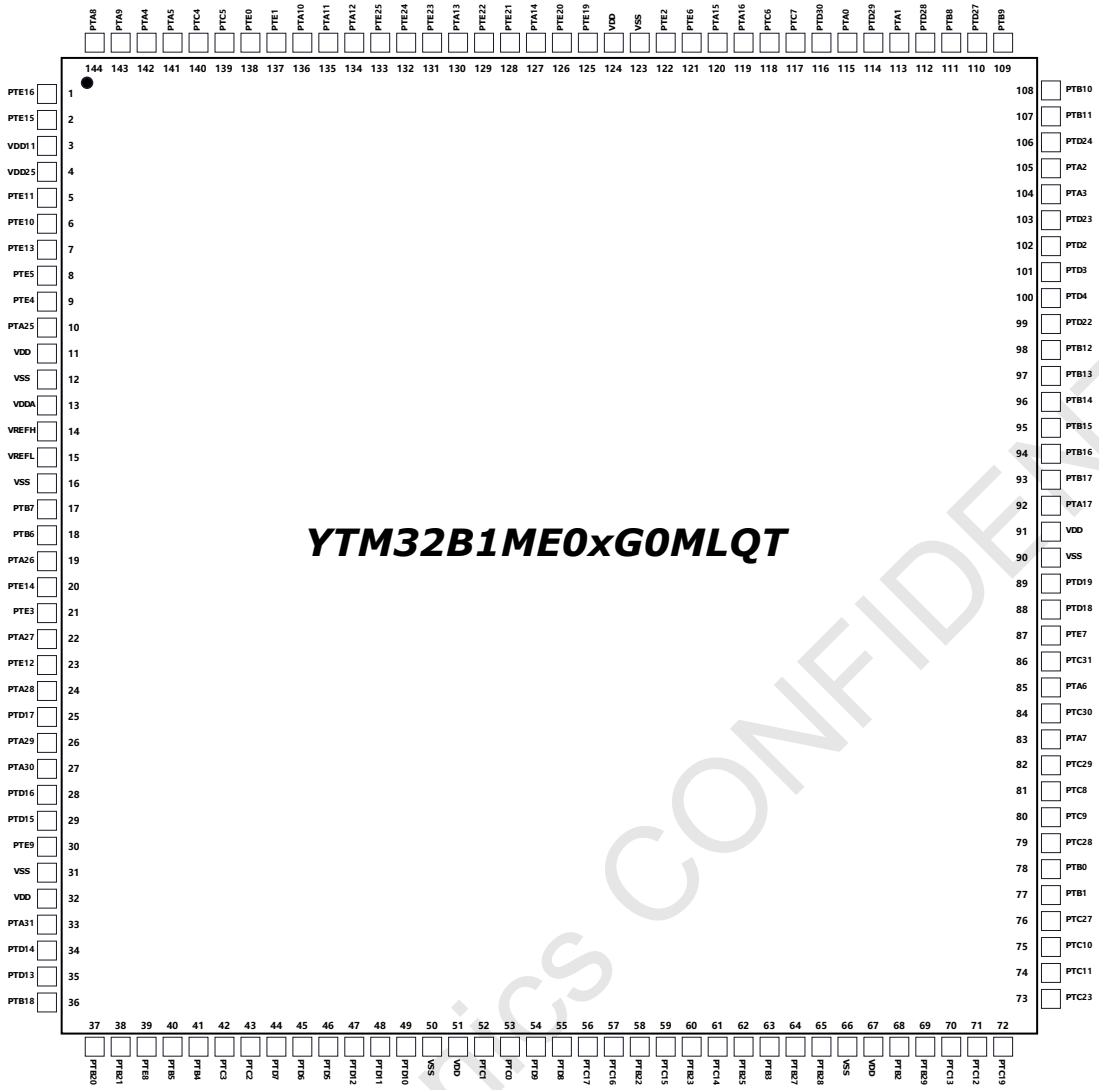

Figure 2: 144-pin LQFP package

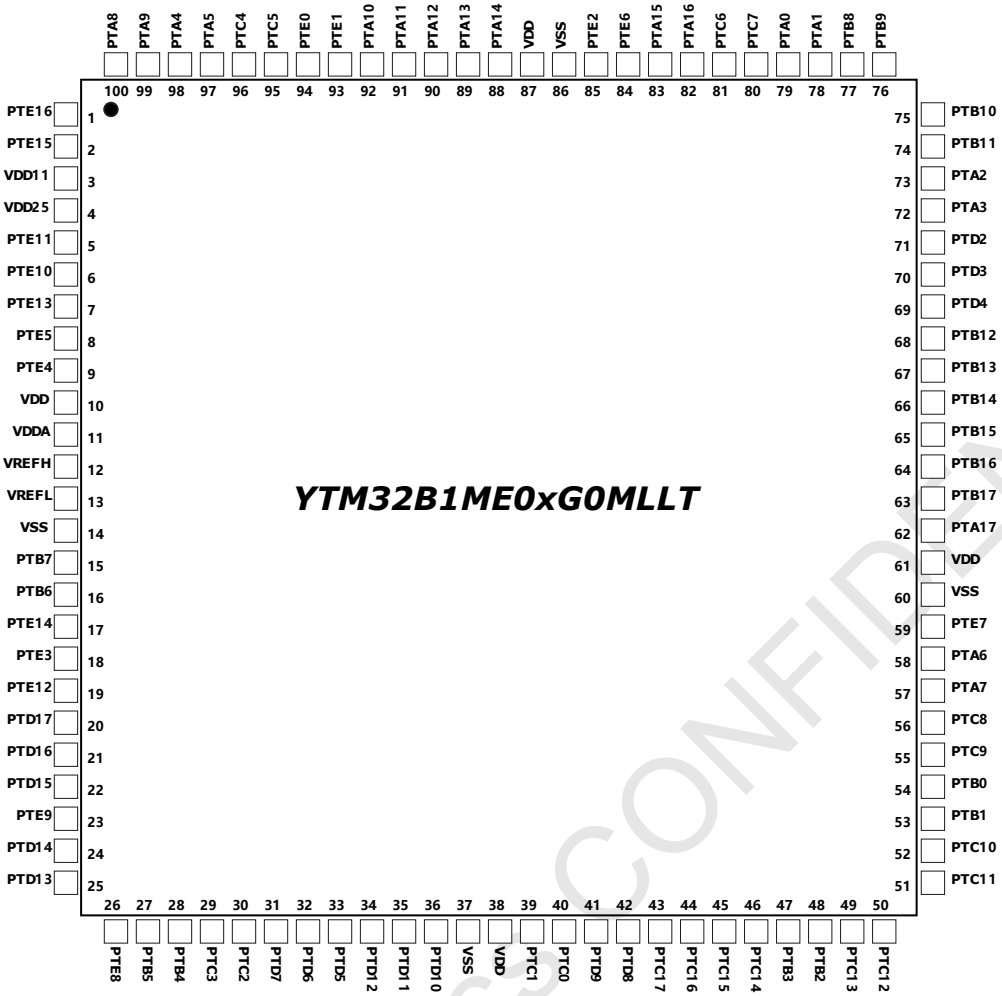

Figure 3: 100-pin LQFP package

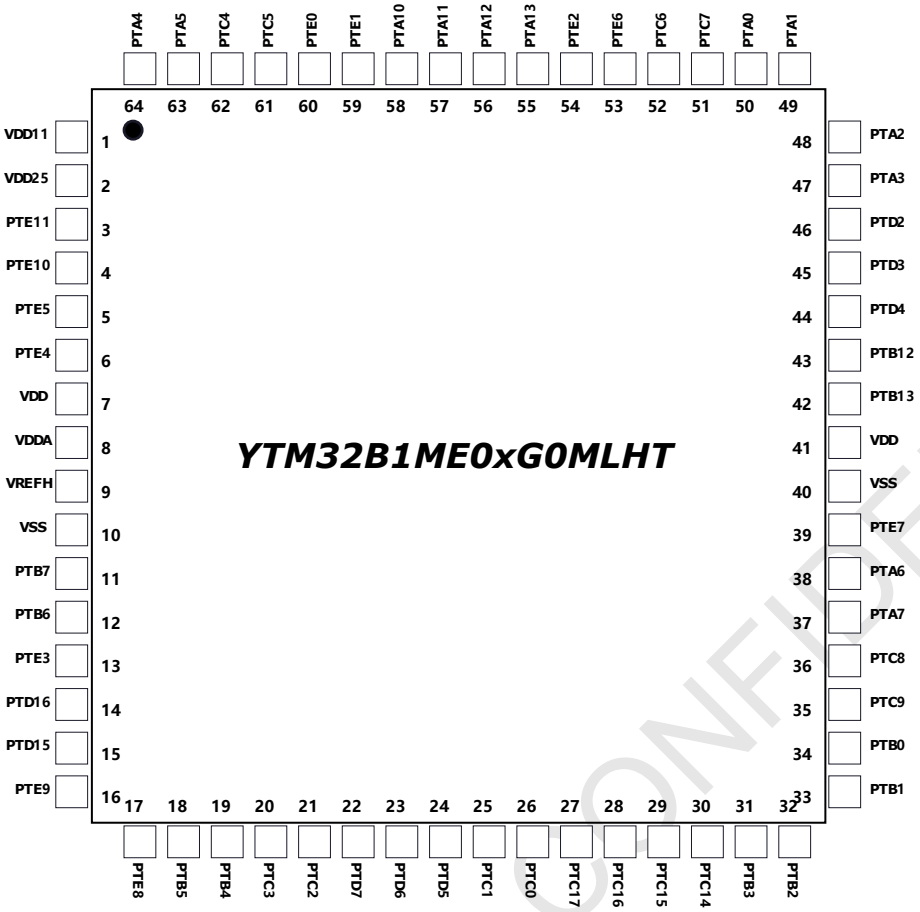

Figure 4: 64-pin LQFP package

5 Features

5.1 Memory and package options

The following table summarizes the memory and package options for the YTM32B1ME0x family.

Table 4: YTM32B1ME0x Family Summary

Family	Performance(MHz)	Memory		Package		
		Flash(MB)	SRAM(KB)	144 LQFP	100 LQFP	64 LQFP
YTM32B1ME0x	120	1.25	128	+	+	+

5.2 Part numbers and packaging

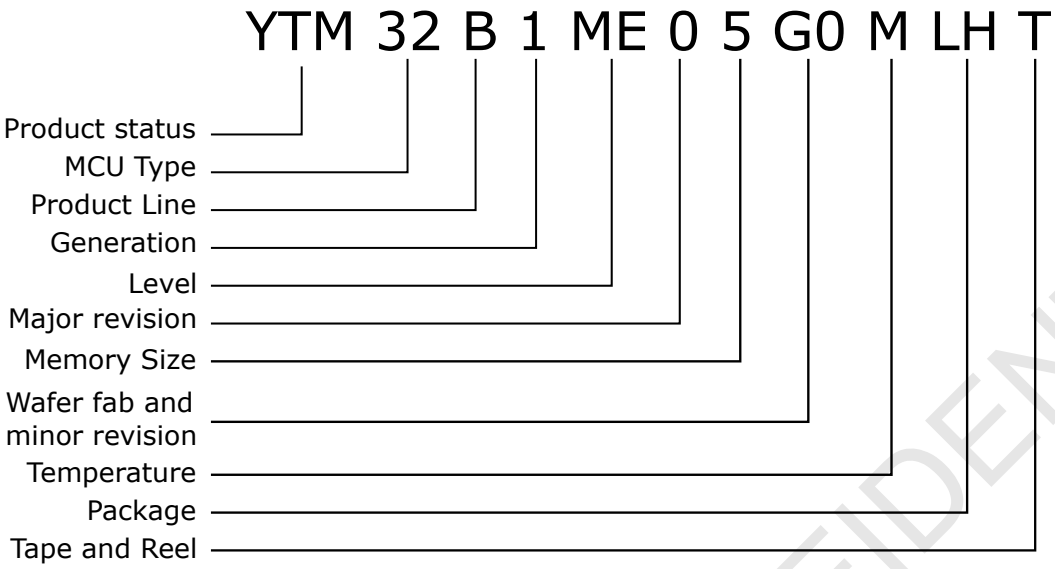

Figure 5: 64-pin part numbers diagram

Table 5: Part number field description

<table>
<tr><th>Field</th><th>Description</th><th colspan="6">Values</th></tr>
<tr><td>YTM</td><td>Product Status</td><td colspan="6">YTM: Qualified
PTM: Prototype</td></tr>
<tr><td>32</td><td>MCU Type</td><td colspan="6">32: 32-bit</td></tr>
<tr><td>B</td><td>Product Line</td><td colspan="6">B: General
D: Dashboard
P: Powertrain
V: Vision
N: Network</td></tr>
<tr><td>1</td><td>Generation</td><td colspan="6">1st generation product</td></tr>
<tr><td>Mx</td><td>Level</td><td colspan="6">Hx: High end
Mx: Middle end
Lx: Low end</td></tr>
<tr><td>0</td><td>Major revision</td><td colspan="6">1st revision</td></tr>
<tr><td rowspan="5">4</td><td rowspan="5">Memory Size</td><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr>
<tr><td>H</td><td>2M</td><td>4M</td><td>6M</td><td>8M</td><td>-</td></tr>
<tr><td>M</td><td>64K</td><td>128K</td><td>256K</td><td>512K</td><td>1M</td></tr>
<tr><td>L</td><td>8K</td><td>16K</td><td>32K</td><td>64K</td><td>-</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>G0</td><td>Wafer Fab and Revision</td><td colspan="6">Hx: HHGrace
Gx: Global Foundry
Tx: TSMC
Sx: SMIC</td></tr>
<tr><td>M</td><td>Ambient Temperature</td><td colspan="6">C: -40℃~85℃
V: -40℃~105℃
M: -40℃~125℃
W: -40℃~150℃</td></tr>
<tr><td rowspan="7">LH</td><td rowspan="7">Package</td><td>Pins</td><td colspan="2">LQFP</td><td>QFN</td><td colspan="2">BGA</td></tr>
<tr><td>32</td><td colspan="2">LE</td><td>FM</td><td colspan="2">-</td></tr>
<tr><td>48</td><td colspan="2">LF</td><td>-</td><td colspan="2">-</td></tr>
<tr><td>64</td><td colspan="2">LH</td><td>-</td><td colspan="2">-</td></tr>
<tr><td>100</td><td colspan="2">LL</td><td>-</td><td colspan="2">MH</td></tr>
<tr><td>144</td><td colspan="2">LQ</td><td>-</td><td colspan="2">-</td></tr>
<tr><td>176</td><td colspan="2">LU</td><td>-</td><td colspan="2">-</td></tr>
<tr><td>T</td><td>Tape and Reel</td><td colspan="6">T: Trays/Tubes
R: Tape and Reel</td></tr>
</table>

5.3 Module-by-module feature list

The following sections describe the high-level module features for YTM32B1ME0x device.

5.3.1 Core modules

5.3.1.1 ARM Cortex-M33 core

The features of the ARM Cortex-M33 core module are listed below.

- ARM Cortex M33 core running up to 120 MHz
- ARM core M33 with 1.5 DMIPS/MHz

- On-core MPU for dynamic task protection (16 regions)
- Single cycle 32 x 32 bits multiply
- 3-stage pipeline, thumb-2 technology
- Digital Signal Processor (DSP)
- Single Precision Floating Point Unit (SPFPU), IEEE 754 compliant
- Support for the instruction trace option:
  - Embedded Trace Macrocell (ETM)
- Binary compatible instruction set with the ARM Cortex M7

5.3.1.2 Nested Vectored Interrupt Controller (NVIC)

The features of the Nested Vectored Interrupt Controller (NVIC) module are listed below.

- Up to 192 interrupt sources
- Includes a single non-maskable interrupt

5.3.1.3 Debug Controller

The features of the Debug Controller module are listed below.

- 2-pin serial wire debug (SWD) provides external debugger interface
- Support JTAG port
- Support ITM(Instruction Trace Macrocell): S/W Instrumentation Messaging + Simple Data Trace Messaging + Watchpoints Messaging
- Support ETM(Embedded Trace Macrocell): Used for instruction trace
- Support DWT(Data and Address Watchpoints): 4 data and address watchpoints

5.3.2 Memories and memory interfaces

5.3.2.1 Embedded Flash Module (EFM)

The features of the Embedded Flash Module (EFM) module are listed below.

- 1MB PFlash with 8-bit ECC includes 2 blocks, block size is 512KB, sector size is 2KB
- 256KB DFlash with 8-bit ECC includes 1 block, block size is 256KB, sector size is 1KB
- There are 3 NVR sectors with 8-bit ECC that includes secured AES key storage, One-Time-Program, and Security control, each sector is 1KB
- Protection scheme against accidental program or erase operations
- Optional interrupt on command completion and status update
- Program and erase operations do not require any special power sources other than the normal VDD supply

5.3.2.2 TCML/TCMU (SRAM)

The features of the TCML/TCMU (SRAM) module are listed below.

- 64KB TCML and 64KB TCMU
- Support ECC feature
- Two regions of 16KB SRAM which supports data retention in powerdown mode

5.3.2.3 Register File (REGFILE)

The features of the Register File (REGFILE) module are listed below.

- 32 bytes regfile which supports data retention in powerdown mode

5.3.3 System modules

5.3.3.1 System Clock Unit (SCU)

The features of the System Clock Unit (SCU) module are listed below.

- SCU provides system clock dividers to generate core clock, fast bus clock and slow bus clock.
- SCU provides glitch free switcher to select system clock source
- Fast internal RC oscillator(FIRC)
  - Up to 96MHz
  - Default system boot clock source
  - Support trim for temperature and process
  - Can be selected as PLL reference clock
- Slow internal RC oscillator(SIRC)
  - Can be selected as system clock source
  - Always on unless it is forced to be disabled in standby mode and powerdown mode
  - Support trim for temperature and process
- Fast crystal oscillator(FXOSC)
  - Support 8 ~ 40MHz crystal
  - Can be selected as PLL reference clock
  - Can be selected as system clock source
  - Support bypass mode
- Slow crystal oscillator(SXOSC)
  - 32KHz real time oscillator
  - Can’t be selected as system clock
  - Provides accurate clock to watchdog(WDG) and real time clock(RTC)
  - Support bypass mode
- Phase-locked loop(PLL)
  - Up to 120 MHz
  - Contain voltage-controlled oscillator(VCO)
  - Support selectable reference clock
  - Contain Frequency lock detector
  - Can be select as system clock source

5.3.3.2 Chip Integration Module (CIM)

The features of the Chip Integration Module (CIM) module are listed below.

- ADC/ACMP trigger selection
- Software trigger generation
- eTMR external clock and fault selection
- FPU interrupt enable
- System device identification (ID)
- Flash memory and system RAM size configuration

- Package configuration
- FlexCAN FD feature configuration

5.3.3.3 Reset Controller Unit (RCU)

The features of the Reset Controller Unit (RCU) module are listed below.

- Record the reset sources of most recent resets
- Configurable filter for reset pin
- Reset pin filter can work in all power modes

5.3.3.4 Trigmux Unit (TMU)

The features of the Trigmux Unit (TMU) module are listed below.

- Allow software to select the trigger sources for peripherals as trigger sources
- Support up to 12 trigger input pads and up to 8 trigger output pads

5.3.3.5 Power Control Unit (PCU)

The features of the Power Control Unit (PCU) module are listed below.

- Combination of internal and external voltage regulator options, offering a variety of power modes
- Active POR providing brown-out detect
- Low voltage reset for all system relevant power domains (LVR)
- Low voltage detect (LVD) and high voltage detect (HVD) as indication for software

5.3.3.6 Direct Memory Access (DMA)

The features of the Direct Memory Access (DMA) module are listed below.

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
  - Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
  - Address increase/decrease/not change selectable
- Up to 16 DMA channels
  - Fix priority and round-robin arbitration
  - Support channel to channel link
- Software/Hardware trigger
- Up to 128 peripheral hardware triggers
- Internal data FIFO for data transfer
- Support update DMA transfer information from system memory after transfer complete

5.3.3.7 IP Controller (IPC)

The features of the IP Controller (IPC) module are listed below.

- Peripheral Bus clock enable
- IPC clock source selection as follows
  - FIRC 96 MHz
  - SIRC 12 MHz

  - FXOSC 8 ~ 40 MHz
  - SXOSC 32 KHz
- IPC clock divide values from 1 to 16

5.3.4 Communication interfaces

5.3.4.1 Serial Peripheral Interface (SPI)

The features of the Serial Peripheral Interface (SPI) module are listed below.

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support single line mode
- Support Master and slave mode
- Support Transmit/Receive via DMA

5.3.4.2 Inter-Integrated Circuit (I2C)

The features of the Inter-Integrated Circuit (I2C) module are listed below.

- Support standard, fast and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBus mode
- Support multi-master arbitration and synchronization
- Support Master and slave clock stretching
- Transmit/Receive FIFO (Master only)
- Analog and digital filter on both SCL and SDA pins
- Support Transmit/Receive via DMA

5.3.4.3 Flexible Controller Area Network (FlexCAN)

The features of the Flexible Controller Area Network (FlexCAN) module are listed below.

- Full implementation of the CAN FD protocol and CAN Specification 2.0, Part B
  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32, or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Legacy Rx FIFO with storage capacity for up to 6 CAN frames and automatic internal pointer handling with DMA support
- Full-featured Enhanced Rx FIFO with storage capacity for up to 20 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability

- Flexible message buffers, totaling 64 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer with an optional external time tick or high-resolution 32-bit on-chip timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-power modes, with programmable wakeup on bus activity or matching with received frames (Pretended Networking)
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Legacy Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Legacy Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 ID Filter Table elements
- Powerful Enhanced Rx FIFO ID filtering, capable of matching incoming IDs against either 64 extended or 128 standard ID filter elements with three filtering schemes: mask + filter, range, and two filters without mask
- 100% backward compatibility with previous FlexCAN version
- Supports detection and correction of errors in memory read accesses. Each byte of FlexCAN memory is associated to 5 parity bits. The error correction mechanism ensures that in this 13-bit word, errors in one bit can be corrected (correctable errors) and errors in 2 bits can be detected but not corrected (non-correctable errors).
- Supports Pretended Networking functionality in low-power modes: Deepsleep mode

5.3.4.4 Local Interconnect Network (LINFlexD)

The features of the Local Interconnect Network (LINFlexD) module are listed below.

- LINFlexD common features in both LIN and UART mode:
  - Fractional baud rate generator
  - Three operating modes for power saving and configuration registers lock
    - Initialization
    - Normal

        - Sleep
    - Test mode: Loop Back
    - Maskable interrupts
- LIN mode features include:
    - Support for LIN protocol versions 1.3, 2.0, 2.1 and 2.2
    - Bit rates up to 20 Kbit/s (LIN protocol)
    - Master/slave modes
    - Classic and enhanced checksum calculation and check
    - Single 8-byte buffer or FIFO for transmission/reception
    - Timeout management
    - Identifier filters
    - DMA interface
    - Support for 16 identifiers
    - Master mode with autonomous message handling
    - Wakeup event on dominant bit detection
    - True LIN field state machine
    - Advanced LIN error detection
    - Header, response and frame timeout
    - Slave mode
        - Autonomous header handling
        - Autonomous transmit/receive data handling
    - Identifier filters for autonomous message handling in slave mode
    - Separate clock for baud rate calculation
- UART mode features include:
    - Full-duplex communication
    - Separate clock for baud rate calculation
    - 7/8 bits data, parity
    - 1/2/3 stop bits
    - 12-bit + parity reception
    - 4-byte buffer for reception; 4-byte buffer for transmission
    - 12-bit counter for timeout management
    - The maximum baud rate achievable is ipg_baud_clk/4 Mbit/s
    - For bit rate $\leq$ ipg_baud_clk/16 Mbit/s
        - 16 times oversampling
        - 3:1 majority voting
    - For ipg_baud_clk/16 Mbit/s $<$ bit rate $\leq$ ipg_baud_clk/8 Mbit/s
        - Reduced oversampling programmable by software
        - 3:1 majority voting for reduced oversampling of 8 samples per bit
    - For ipg_baud_clk/8 Mbit/s $<$ bit rate $\leq$ ipg_baud_clk/4 Mbit/s
        - Reduced oversampling programmable by software
        - 1:1 voting for all reduced oversampling of 4, 5 and 6 samples per bit

5.3.5 Analog

5.3.5.1 Analog-to-Digital Converter (ADC)

The features of the Analog-to-Digital Converter (ADC) module are listed below.

- Contain two ADC instances
    - ADC0 supports up to 31 analog input channels
    - ADC1 supports up to 24 analog input channels

- Support 12-bit, 10-bit, 8-bit, and 6-bit single-ended configurable resolution
- Up to 2Msps for 12-bit resolution conversion performance
- Support DMA and conversion result FIFO with watermark
- Support multiple conversion modes
  - Single mode
  - Continuous mode
  - Discontinuous mode
- Support software/hardware trigger for ADC start conversion
- Support two low power modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support interrupt generate
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
- Support work and wake up when the chip under low power mode

5.3.5.2 Analog Comparator (ACMP)

The features of the Analog Comparator (ACMP) module are listed below.

- Up to 8 channels
- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode:
  - Common mode
  - Sample mode
  - Window mode
  - Continuous mode
    - one-shot mode
    - loop mode
- All channels can be used to execute automatic comparison
- Support digital filter, the filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- Functional in all power mode
- Support independent 8-bit DAC output to the comparator
- Support several interrupts
  - For common/sample/window mode
    - Generate interrupt on rising-edge, falling-edge or both edges of the comparator output
  - For continuous mode
    - Generate interrupt when the comparison results don’t match with expectations
- Interrupt can generate without any clock except in continuous mode

- A comparison event can be selected to trigger DMA transfer

5.3.6 Timer

5.3.6.1 Timer (TMR)

The features of the Timer (TMR) module are listed below.

- One 32-bit count-up timer with an 8-bit prescaler
- Four 32-bit compare channels
- An independent interrupt source for each channel
- Ability to stop the timer in debug mode

5.3.6.2 Periodic Timer (pTMR)

The features of the Periodic Timer (pTMR) module are listed below.

- Timers can generate interrupts
- Four channels of 32-bit timers, each timer has independent timeout period
- Ability to stop in debug mode
- Support chain mode to connect multiple timer to a longer timer

5.3.6.3 Low Power Timer (lpTMR)

The features of the Low Power Timer (lpTMR) module are listed below.

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

5.3.6.4 Enhanced Timer (eTMR)

The features of the Enhanced Timer (eTMR) module are listed below.

This chip contains 6 eTMRs (eTMR0, eTMR1, eTMR2, eTMR3, eTMR4, eTMR5), features of them can be divided into common features and individual features.

The common features of all eTMRs are listed below:

- Configurable initial and final counter values
- Contain 8 channels
- Support two clock sources
  - Bus clock
  - External clock
- Support 7-bits clock prescaler
- Support three channel modes
  - PWM mode
    - Independent mode for each channel
    - Complementary mode for each pair of channels
      - All channels support independent deadtime insertion

        - Support dithering
        - Channel output control (initialization, software control, mask control, double switch control, fault control)
            - Support 4 fault input sources
            - Support fault input from TMU or pad
            - Support fault input polarity control
            - Support fault input filter
            - Support fault input stretch
            - Support fault event generated by combinational logic
        - Relevant registers have buffer registers and support loading mechanism
    - Output Compare mode
        - The output can be configured to set, clear or toggle on match point
    - Input Capture mode
        - Support rising edges, falling edges or dual edges capture
        - Support input filter with a prescaler
        - Support capture test mode
        - Support pulse width measure
- Support generating triggers
    - Output triggers with adjustable pulse width on match point
    - Output pulse with adjustable width by PWM
- Polarity control is available for each channel
- Support GTB (Global Time Base)
- Support several interrupts
    - Channel interrupt (capture interrupt and compare interrupt)
    - Counter overflow interrupt
    - Fault event interrupt
- Support DMA
- Support counter running under debug mode

The individual features are listed below:

- Counter
    - eTMR3 has a 32-bit counter
    - Other eTMRs have a 16-bit counter
- eTMR1 and eTMR2 support quadrature decoder mode
    - Contain a independent 16-bit counter with a clock prescaler
    - Support 4 up-down counting modes
    - Support phase A and phase B input filter
    - Support quadrature decoder counter overflow interrupt
- eTMR0 and eTMR3 support modulated output
- eTMR2 supports hall sensor input
- eTMR1 and eTMR2 support input from ACMP

5.3.6.5 Real-Time Clock (RTC)

The features of the Real-Time Clock (RTC) module are listed below.

- RTC clock source:
    - SXOSC
    - RTC_CLKIN
- 32-bit seconds counter with overflow flag and optional interrupt
- Configurable 32-bit alarm

- 16-bit prescaler with compensation that can correct errors
- Register write protection
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt
- Lock support of register access for control and alarm register

5.3.6.6 Programmable Trigger Unit (PTU)

The features of the Programmable Trigger Unit (PTU) module are listed below.

- 8 Configurable PTU channels for ADC hardware trigger
- Each trigger output can be enabled/disabled independently
- Configurable delay trigger output
- Support Back-to-Back Mode
- Support Bypass of trigger delay
- Support software trigger source
- Support Continuous Mode
- Optional interrupt of counter and sequence error
- Support pulse out

5.3.7 Human machine interface

5.3.7.1 General-Purpose Input/Output (GPIO)

The features of the General-Purpose Input/Output (GPIO) module are listed below.

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Port Input Disable register
- Pin interrupts
  - Interrupt flag and enable registers for each pin, functional in all digital pinmux modes
  - Support for interrupt or DMA request
  - Support for edge sensitive (rising, falling, both) or level sensitive (low, high) configured per pin
  - Asynchronous wake-up in low-power mode except powerdown mode

5.3.7.2 Port Control (PCTRL)

The features of the Port Control (PCTRL) module are listed below.

- Individual pull control fields with pull-up, pulldown and pull-disable support
- Individual drive strength field supporting high and low drive strength
- Individual mux control field supporting analog or pin disabled, GPIO and up to 7 chip-specific digital functions
- Individual passive filter field supporting enable and disable passive filter for specific input

5.3.8 Security, Integrity and Safety

5.3.8.1 Cyclic Redundancy Check (CRC)

The features of the Cyclic Redundancy Check (CRC) module are listed below.

- The following CRC polynomials are implemented:
  - CRC4 (CRC-ITU):
    $X^4 + X + 1$
  - CRC16 (CRC-CCITT):
    $X^{16} + X^{12} + X^5 + 1$
  - CRC32 (CRC-ethernet):
    $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable initial seed
- Optional bit-swap in one byte is available for input data
- Optional bit-swap in one word is available for output data
- Optional bit-inversion is available for output data
- 8/16/32-bit access for CRC input data

5.3.8.2 Hardware Cryptography Unit (HCU)

The features of the Hardware Cryptography Unit (HCU) module are listed below.

- Support 128-bit, 192-bit and 256-bit key length
- Support both encryption and decryption
- Support secure hardware key and flexible software key
- Support several engines
  - AES (ECB, CBC, CTR, CCM, CMAC)
  - SM4 (ECB)
  - SHA (SHA-256, SHA-384)
- All data is in big-endian format
- Support 1-bit, 8-bit and 16-bit data swap
- Size of input/output FIFO is up to 32*32 bits
- Support DMA transport between chip memory and input/output FIFO
- Support operation done interrupt
- Clock gating strategy is used for engine core when input/output FIFO is not ready

5.3.8.3 Clock Monitor Unit (CMU)

The features of the Clock Monitor Unit (CMU) module are listed below.

- SCU contains 4 CMU blocks
- CMU monitors slow bus clock, FIRC, FXOSC and PLL clock
- FXOSC or SIRC clock can be selected as reference clock of CMU
- CMU can detect frequency out of range, loss of checked clock and loss of reference clock

5.3.8.4 True Random Number Generator (TRNG)

The features of the True Random Number Generator (TRNG) module are listed below.

- Generate a 256-bit entropy
- Monobit limit test
- Long run test
- 1 ring OSC with clock checker
- 3 interrupt sources

5.3.8.5 Watchdog (WDG)

The features of the Watchdog (WDG) module are listed below.

- 32-bit countdown timer
- selectable SXOSC/SIRC clock source
- Support regular or window servicing mode
- Support reset request or interrupt for first timeout
- Master access protection
- Hard and soft configuration lock bits
- Support fixed key for dog feeding

5.3.8.6 External Watchdog (EWDG)

The features of the External Watchdog (EWDG) module are listed below.

- Independent LPO_CLK clock source
- selectable SXOSC/SIRC clock source
- Programmable time-out period specified in terms of number of EWDG clock cycles.
- Windowed refresh option
- Provides robust check that program flow is faster than expected.
- Programmable window.
- Refresh outside window leads to assertion of EWDG_OUT_b.
- Robust refresh mechanism
- Write values of 0xA8 and 0x6C to EWDG Refresh Register within 15 peripheral bus clock cycles.
- One output port, EWDG_OUT_b, when asserted is used to reset or place the external circuit into safe mode.
- One Input port, EWDG_in, allows an external circuit to control the assertion of the EWDG_OUT_b signal.

5.3.8.7 Peripheral Protection Unit (PPU)

The features of the Peripheral Protection Unit (PPU) module are listed below.

- Write access for the module under protection can be restricted to the supervisor mode only
- Maximum 1KB register slot size of module under protection
- Multiple ways are present to set the lock bits
- Once the lock bits are set, the registers could be protected from modification

5.3.8.8 Interrupt Monitor (INTM)

The features of the Interrupt Monitor (INTM) module are listed below.

- Up to 4 programmable monitors
- Programmable monitored interrupt source per monitor
- Programmable 24-bit latency counter per monitor
- Programmable 24-bit counter threshold per monitor
- Timer expired status bit per monitor
- One overall interrupt acknowledge for all monitors
- One overall enable for all monitors

5.3.8.9 ECC Management Unit (EMU)

The features of the ECC Management Unit (EMU) module are listed below.

- Two channels to ECC injection and report: TCML and TCMU
- Two-stage enable mechanism to ECC injection and ECC report
- Location and correction or non-correction error can be injected
- ECC error interrupt under each enable register's control
- The register keep the last ECC error data

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