AC7325 Datasheet

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Document Revision History

Revision	Date	Author	Description
1.0	2019-11-15	Autochips	Initial Version
1.1	2020-05-22	Autochips	1. Update Figure 10-4 2. Input impedance typ value change to 50kΩ

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1 General Feature List

The AC7325 is a 4X45W power amplifier, which uses a complementary DMOS output stage based on BCD process and intended for automotive applications. It has a high efficiency mode with full I²C-bus controlled start-up diagnostics. AC7325 can operate at low voltage, making this amplifier suitable for start-stop operation.

Thanks for the new high efficiency mode using a new switch technique, the dissipation is more than 65 % less than standard class AB solutions when used for front and rear correlated audio signals. Dissipation is less than standard BTL when used for uncorrelated (delayed) audio signals between front and rear. AC7325 also has been designed to be very robust against several kinds of misconnections.

- BCD technology and MOSFET output power stage.
- New high efficiency mode optimizing the uncorrelated signal.
- More High efficiency mode selection.
- Operate in 3.3 V and 5 V compliant I²C-bus modes.
- Four hardware-selectable I²C-bus addresses.
- Independent selectable soft mute of front and rear channels.
- Clipping detect with selectable threshold: 2 %, 5 % or 10 %.
- Selectable thermal pre-warning.
- Capable to operate down to 6V (“start stop”).
- Speaker fault Diagnostic.
- Load detection during start-up diagnostics: open, short, normal.
- Selectable AC load (tweeter) diagnostic: low and high current mode.
- Offset detection.
- Thermal-, clipping- or load fault information (short load or to VCC or to ground) can be indicated on pin DIAG.
- Safe operation when ground/VCC missing.
- All amplifier outputs protection against short to ground, power and across load.
- All pins ok with short-circuit to ground.
- Temperature controlled gain reduction
- Selectable 7.5 V or 6 V minimum battery voltage operation.
- Overvoltage protection (safe on load-dump up to VCC = 50 V) with overvoltage pre-warning at 16 V.

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2 Quick Reference Data

Table 2-1 Quick Reference Data

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VCC	Operating supply voltage	RL=4Ω	6	14.4	18	V
I_q	Quiescent current	no load	-	250	350	mA
Po	Output power	RL = 4Ω; VCC = 14.4 V; maximum power; Vi = 2 VRMS square wave	37	40	-	W
		RL = 4Ω; VCC = 15.2 V; maximum power; Vi = 2 V RMS square wave	41	45	-	W
		RL=4Ω; VCC=14.4V; THD=1%	18	20	-	W
		RL=4Ω; VCC=14.4V; THD=10%	23	25	-	W
THD	Total harmonic	Po = 1 W to 12 W; fi = 1 kHz; RL = 4Ω; BTL mode	-	0.01	0.1	%
		Po = 4 W; fi = 1 kHz; RL = 4Ω; high efficiency mode	-	0.03	-	%
Vn(o)	Output noise voltage	filter 20 Hz to 22 kHz;	-	40	60	μV
CT	Cross talk	F=1kH, Rg=600Ω	60	70	-	dB
		F=10kHz, Rg=600 Ω	55	70	-	dB
GV	Voltage gain	-	25	26	27	dB
BW	Power bandwidth	-	-	-	100	kHz
ΔVo	Output voltage variation	Pop during switch-on and switch-off, high efficiency mode				
		From off to mute and mute to off	-	7.5	-	mV
		From mute to on and on to mute (soft mute)	-	7.5	-	mV

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3 System Block Diagram

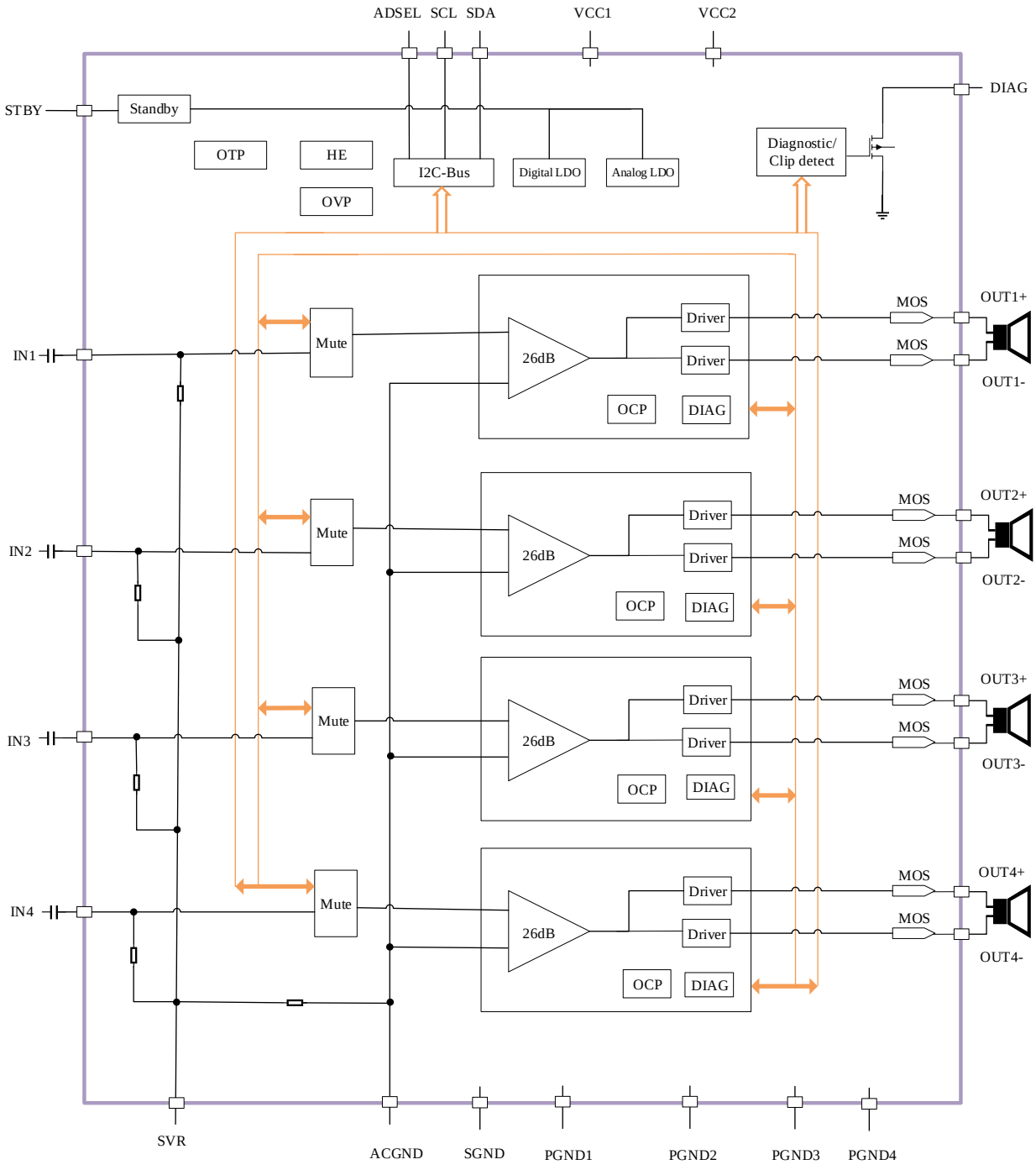

Figure 3-1 AC7325 block diagram

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4 Pin Information

4.1 Pinning

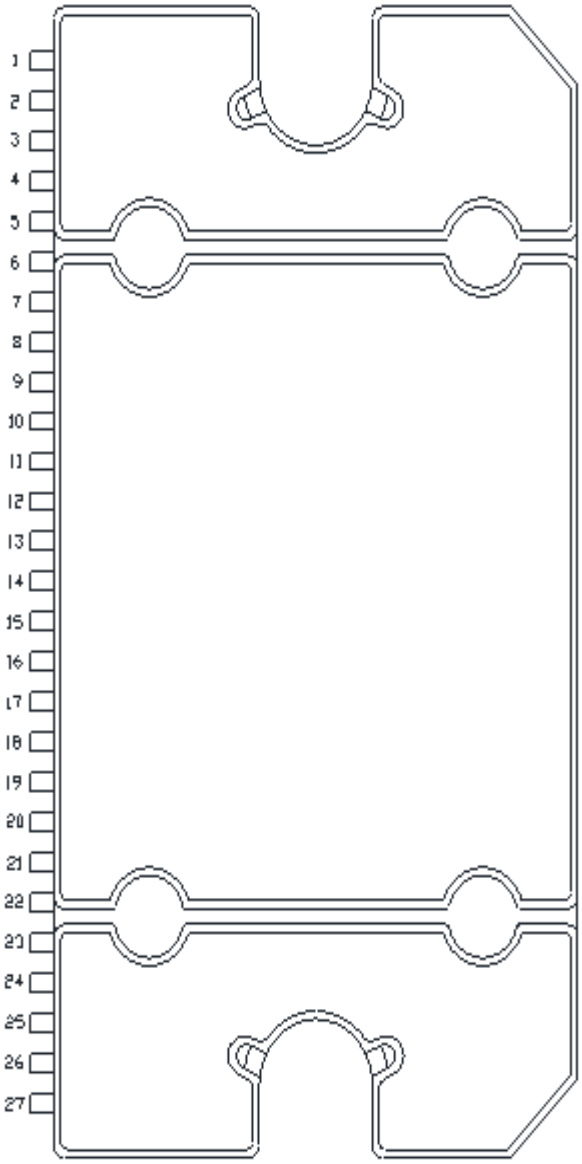

Figure 4-1 AC7325 Pinning

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4.2 Pin description

Table 4-1 Pin description

Symbol	Pin	Description
ADSEL	1	I²C-bus address select pin
STBY	2	Standby pin
PGND2	3	Channel 2 power ground
OUT2-	4	Channel 2 output- (left rear)
DIAG	5	Diagnostic and clip detection output
OUT2+	6	Channel 2 output+ (left rear)
VCC1	7	Power supply voltage1
OUT1-	8	Channel 1 output- (left front)
PGND1	9	Channel 1 power ground
OUT1+	10	Channel 1 output+ (left front)
SVR	11	SVR pin
IN1	12	Input pin channel 1
IN2	13	Input pin channel 2
SGND	14	Signal ground pin
IN4	15	Input pin channel 4
IN3	16	Input pin channel 3
ACGND	17	AC ground
OUT3+	18	Channel 3 output+ (right front)
PGND3	19	Channel 3 power ground
OUT3-	20	Channel 3 output- (right front)
VCC2	21	Power supply voltage2
OUT4+	22	Channel 4 output+ (right rear)
SCL	23	I²C-bus clock pin
OUT4-	24	channel 4 output- (right rear)
PGND4	25	Channel 4 power ground
SDA	26	I²C-bus data pin
TAB	27	Heatsink connection, must be connected to ground

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5 Thermal Characteristics

Table 5-1 Thermal Characteristics

Symbol	Parameter	Max.	Unit
FZIP27			
Rth(j-c)	Thermal resistance from junction to case	1	K/W

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6 Limiting Values

Table 6-1 Limiting values

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	Operating	6	18	V
		Non-operating	–1	+50	V
		Load dump protection	-	50	V
I_{OCP}	Output protection current		-	5.5	A
Tj(max)	Maximum junction temperature		-	150	°C
T_{stg}	Storage temperature		–55	+150	°C
T_{amb}	Ambient temperature	Suitable heatsink to ensure T_j does not exceed 150 °C	–40	+105	°C
V(prot)	Output protection voltage	Output short-circuit voltage	-	V_{CC}	V
Vi(max)	maximum input voltage	RMS value	-	5	V
V_{max}	SCL and SDA max voltage		0	6.5	V
	SVR, ACGND and DIAG max voltage		0	10	V
ESD	HBM			8K	V
	CDM	Corner pin		750	V
	CDM	All others pin		500	V

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7 Characteristics

Table 7-1 Characteristics

T_{amb} = 25 °C; V_{cc} = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = 40 °C to +150 °C; functionality is guaranteed for V_{cc} < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage behavior						
VCC	Operating supply voltage	R_L=4	6	14.4	18	V
I_q	Quiescent current	no load	-	250	300	mA
Ioff	Off-state current	V_{STBY} = 0.4 V	-	1	10	μA
V_o	Output voltage	DC	6.8	7.2	7.6	V
Vcc_mute	Low voltage mute	Vcc rising				
		IB4[D0] = 1	7.0	7.7	8.1	V
		IB4[D0] = 0	5.4	5.7	6.2	V
		Vcc falling				
		IB4[D0] = 1	6.5	7.2	7.7	V
		IB4[D0] = 0	5.2	5.5	5.9	V
Vth_mute	Low voltage mute threshold	IB4[D0] = 1	0.1	0.5	0.8	V
		IB4[D0] = 0	0.1	0.3	0.7	V
Vcc_ovwarn	Vcc high voltage warning	Vcc rising	15.2	16	16.9	V
		Vcc falling	14.4	15.2	16.2	V
		Threshold	-	0.8	-	V
Vovp	Vcc overvoltage protection	Vcc rising	18	20	22	V
VPOR	Vcc power-on reset voltage	Vcc falling	-	3.1	4.5	V
V_o_offset	Output offset voltage	Amplifier on	-75	0	+75	mV
Voltage of STBY pin						
VSTBY	Voltage on pin STBY	Off mode			0.8	V
		Operating mode	2.5	-	Vcc	V
Turn on/off, mute timing						
T_{wake}	Wake-up time	Time after wake-up by STBY pin	-	7	10	ms
Td_mute_off	Mute off delay time	time from amplifier start to 10% output	-	150	-	ms
Tamp_on	Amplifier on time	time from amplifier start to	-	150	-	ms

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		amplifier on; 90 % of output				
Toff	Amplifier switch-off time	time to DC output voltage < 0.1 V	-	100	200	ms
Td(mute-on)	Delay time from mute to on	10% to 90% output	-	20	45	ms
Td(soft_mute)	Soft mute delay time	90% to 10 % output	-	20	45	ms
Td(fast_mute)	Fast mute delay time	90% to 10% output	-	0.4	1	ms
I²C interface						
VIL	LOW-level input voltage	Pins SCL and SDA	-	-	1.5	V
VIH	HIGH-level input voltage	Pins SCL and SDA	2.3	-	5.5	V
VOL	LOW-level output voltage	Pin SDA; IL = 5 mA	-	-	0.4	V
FSCL	SCL clock frequency			400		kHz
RADSEL	resistance on pin ADSEL	I²C-bus address				
		A[6:0] = 1101 010	9.9	10	10.1	kΩ
		A[6:0] = 1101 111	29.7	30	30.3	kΩ
		A[6:0] = 1101 110	99	100	101	kΩ
		A[6:0] = 1101 101	500			kΩ
Turn on diagnostics						
Tsudiag	Start-up diagnostic time	No load; IB1[D1] = 1	50	130	250	ms
RL_DIAG	Load diagnostic threshold	Short load			1.5	Ω
		Normal load	3.2	-	20	Ω
		Open load	80	-	-	Ω
Amplifier diagnostics						
VL_DIAG	Low-level output voltage on DIAG pin	I_{DIAG} = 1 mA	-	-	0.3	V
VOD	Output offset threshold		1.0	1.3	2.0	V
THDclip	Clip detection threshold of THD	Vcc>10V				
		IB2[D7:D6] = 00	-	2	-	%
		IB2[D7:D6] = 01	-	5	-	%
		IB2[D7:D6] = 10	-	10	-	%
Tj_warn	High temperature warning	IB3[D4] = 0	127	137	147	°C
		IB3[D4] = 1	109	119	129	°C
Tj_mute	High temperature mute start			154		°C

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Tj_shutdown	High temperature shutdown		169			°C
Io_acload	Output peak current	AC load detect peak current				
		IB4[D1] = 1	500	-	-	mA
		IB4[D1] = 0	275	-	-	mA
		AC load not detect peak current				
		IB4[D1] = 1	-	-	250	mA
		IB4[D1] = 0	-	-	100	mA
Amplifier performance						
P_o	Output power	R_L=4; Vcc=14.4V; THD=1%	20	-	-	W
		R_L=4; Vcc=14.4V; THD=10%	25	-	-	W
P_{o_MAX}	Output max power	R_L=4; Vcc=14.4V; V_i = $2V_{RMS}$ square wave	37	40	-	W
		R_L=4; Vcc=15.2V; V_i = $2V_{RMS}$ square wave	41	45	-	W
THD	Total harmonic distortion	P_o=1 W to 12 W; f_i=1 kHz; R_L=4; BTL mode	-	0.01	0.1	%
		P_o=1 W; f_i=1 kHz; R_L=4; BTL mode	-	0.01	0.1	%
		P_o=4 W; f_i=1 kHz; R_L=4; High efficiency mode		0.03	0.1	%
Crosstalk	Channel separation	High efficiency mode				
		f_i=1 kHz	-65	-80		dB
		f_i=10 kHz	-55	-65		dB
PSRR	Power supply ripple rejection	f_i = 1 kHz;	-55	-70	-	dB
V_{pop}	Output voltage variation	Pop during turn on and turn off				
		from off to mute and mute to off	-	7.5	-	mV
		from mute to on and on to mute (soft mute)	-	7.5	-	mV
		from off to on and on to off	-	7.5	-	mV

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Amplifier performance						
Vnoise	Output noise voltage	20 Hz to 22 kHz				
		BTL mode	-	40	60	μV
		High efficiency mode	-	40	60	μV
Gain	Voltage gain	Differential out	25	26	27	dB
Z_i	Input impedance		-	50	-	kΩ
Amute	Mute attenuation		-	-90	-	dB
Bandwidth	Power bandwidth		-	-	100	kHz
CL(crit)	Critical load capacitance	No oscillation; R_L between 4 to open load; C_L from all outputs to GND	20	-	-	nF

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8 I²C-bus Bytes

AC7325 I²C_SLAVE is used to control and diagnose the amplifier. I²C_SLAVE write operation is used to update IB (instruction bytes) registers. I²C_SLAVE read operation is used to send DB (diagnostic bytes) registers information to the host. There are 5 bytes IB and DB registers.

8.1 I²C instruction bytes

Table 8-1 Instruction byte IB1

Bit	Description
D7	0 = Disable CD function when Vcc<10V 1 = Enable CD function when Vcc<10V
D6	-
D5	-
D4	-
D3	-
D2	0 = Disable AC load diagnostic 1 = Enable AC load diagnostic
D1	0 = Disable start-up diagnostics 1 = Enable start-up diagnostics
D0	0 = Turn off amplifier 1 = Turn on amplifier

Table 8-2 Instruction byte IB2

Bit	Description
D7	00 = CD function threshold set to 2 % 01 = CD function threshold set to 5 % 10 = CD function threshold set to 10 % 11 = Disable CD function
D6	
D5	0 = Temperature information output to pin DIAG 1 = No temperature information output to pin DIAG
D4	0 = Shorts information output to pin DIAG 1 = No shorts information output to pin DIAG
D3	-
D2	0 = No soft mute on CH1 and CH3 1 = Soft mute on CH1 and CH3

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D1	0 = No soft mute on CH2 and CH4 1 = Soft mute on CH2 and CH4
D0	0 = No fast mute on all CHs 1 = Fast mute on all CHs

Table 8-3 Instruction byte IB3

Bit	Description
D7	-
D6	-
D5	-
D4	0 = Temperature warning set to T= 160ºC 1 = Temperature warning set to T= 135ºC
D3	-
D2	-
D1	-
D0	-

Table 8-4 Instruction byte IB4

Bit	Description
D7	-
D6	0 = Fast mute during shut-down via pin STBY 1 = Slow mute during shut-down via pin STBY
D5	0 = No 16 V overvoltage warning output to pin DIAG 1 = 16 V overvoltage warning output to pin DIAG
D4	0 = DC load information on bits DBx[D5:D4] 1 = AC load information on bits DBx[D5:D4]
D3	-
D2	-
D1	0 = AC load diagnostic set to low current threshold 1 = AC load diagnostic set to high current threshold
D0	0 = LV mute set to 5.5 V 1 = LV mute set to 7.2 V

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Table 8-5 Instruction byte IB5

Bit	Description
D7	0 = Disabled high efficiency mode 1 = Enable high efficiency mode
D6D5	00 = Set high efficiency mode in all 4 channels 10 = Set high efficiency mode in 2 * 2 channels 01 = Set high efficiency mode in CH1 & CH2 11 = Set high efficiency mode in CH3 & CH4
D4	-
D3	-
D2	-
D1	-
D0	-

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8.2 I²C data bytes

Table 8-6 Data byte DB1

Bit	Description
D7	0 = No temperature pre-warning 1 = Temperature pre-warning has triggered
D6	0 = No speaker fault detected on CH2 1 = Speaker fault detected on CH2
D5	If bit IB4[D4] = 1: 0 = No AC-load detected on CH2 1 = AC-load detected on CH2 If bit IB4[D4] = 0: 00 = Normal load detected on CH2 01 = - 10 = Open load detected on CH2 11 = DC-load detected not valid on CH2
D4	-
D3	0 = No shorted load detected on CH2 1 = Shorted load detected on CH2
D2	0 = No output offset detected on CH2 1 = Output offset detected on CH2
D1	0 = No short to supply detected on CH2 1 = Short to supply detected on CH2
D0	0 = No short to ground detected on CH2 1 = Short to ground detected on CH2

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Table 8-7 Data byte DB2

Bit	Description
D7	0 = No POR 1 = POR has triggered
D6	0 = No speaker fault detected on CH4 1 = Speaker fault detected on CH4
D5	If bit IB4[D4] = 1: 0 = No AC-load detected on CH4 1 = AC-load detected on CH4 If bit IB4[D4] = 0: 00 = Normal load detected on CH4 01 = - 10 = Open load detected on CH4 11 = DC-load detected not valid on CH4
D4	-
D3	0 = No shorted load detected on CH4 1 = Shorted load detected on CH4
D2	0 = No output offset detected on CH4 1 = Output offset detected on CH4
D1	0 = No short to supply detected on CH4 1 = Short to supply detected on CH4
D0	0 = No short to ground detected on CH4 1 = Short to ground detected on CH4

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Table 8-8 Data byte DB3

Bit	Description
D7	0 = No over temperature protection 1 = Over temperature protection has triggered
D6	0 = No speaker fault detected on CH1 1 = Speaker fault detected on CH1
D5	If bit IB4[D4] = 1: 0 = No AC-load detected on CH1 1 = AC-load detected on CH1 If bit IB4[D4] = 0: 00 = Normal load detected on CH1 01 = - 10 = Open load detected on CH1 11 = DC-load detected not valid on CH1
D4	-
D3	0 = No shorted load detected on CH1 1 = Shorted load detected on CH1
D2	0 = No output offset detected on CH1 1 = Output offset detected on CH1
D1	0 = No short to supply detected on CH1 1 = Short to supply detected on CH1
D0	0 = No short to ground detected on CH1 1 = Short to ground detected on CH1

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Table 8-9 Data byte DB4

Bit	Description
D7	0 = No overvoltage warning 1 = Overvoltage warning has triggered
D6	0 = No speaker fault detected on CH3 1 = Speaker fault detected on CH3
D5	If bit IB4[D4] = 1: 0 = No AC-load detected on CH3 1 = AC-load detected on CH3 If bit IB4[D4] = 0: 00 = Normal load detected on CH3 01 = - 10 = Open load detected on CH3 11 = DC-load detected not valid on CH3
D4	-
D3	0 = No shorted load detected on CH3 1 = Shorted load detected on CH3
D2	0 = No output offset detected on CH3 1 = Output offset detected on CH3
D1	0 = No short to supply detected on CH3 1 = Short to supply detected on CH3
D0	0 = No short to ground detected on CH3 1 = Short to ground detected on CH3

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Table 8-10 Data byte DB5

Bit	Description
D7	0 = No undervoltage 1 = Undervoltage has triggered
D6	0 = No overvoltage protection 1 = Overvoltage protection has triggered
D5	0 = System not busy with start-up diagnostics 1 = System busy with start-up diagnostics
D4	0 = Vcc above 7.5 V 1 = Vcc below 7.5 V
D3	0 = Vcc above 10 V 1 = Vcc below 10 V
D2	0 = No undervoltage protection 1 = Undervoltage protection has triggered
D1	-
D0	0 = Amplifier off 1 = Amplifier on

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9 Functional Description

AC7325 is a four channels BTL audio power amplifier for car audio. It can work when battery voltage is as low as 6 V being so suitable for the start stop function. If battery drops below 6 V, the amplifier will mute without audible plops and can play automatically when the battery voltage back to 6V or above.

During amplifier turns on, the built-in diagnostics can be used to detect the load status. The status of each channel can be read separately. Any abnormal state such as open load, short load, load fault content, output DC offset, short to ground, and short to Vcc can be detected and reported by I^2C.

AC7325 is protected against overvoltage, short-circuit, over temperature, and miss of ground or Vcc connections. The high temperature warning and clip detect threshold can be programmed by the I^2C-bus.

There are 4 selectable I^2C addresses that can be decided by a resistor connected to ADSEL pin and ground.

The high efficiency mode can reduce the conduction impedance and the dissipation. Comparing with standard bridge connection, working in HE mode will save power up to 65%.

9.1 Turn on and turn off sequence

STBY pin is 3.3V and 5V compatible. RC cells at STBY pin have to be always used in order to smooth the transition for preventing any audible noise.

The capacitor on SVR sets the turn on and turn off time. It helps to have pop free transitions. Its minimum recommended value is 10uF. Increasing the SVR capacitor value also increases the turn on and turn off time. This capacitor also contributes to power supply voltage ripple rejection. In order to reduce the turn on time, the impedance of SVR charging circuit is decreased to a low value until mute release. To keep device working continuously when the battery falls down (start stop), SVR is set as VCC/4 to make sure the device can fully operate, only the maximum output power is reduced according to the available voltage supply.

The amplifier is turned on with IB1[D0]=1, the capacitor on the SVR is charged and SVR rises. Then the amplifier output rises to half power supply with output muted until SVR rises to a specific level. When the amplifier output has risen to the specific level, the mute state will be held when the I^2C-bus bits are set to mute and will be released when the I^2C-bus bits are set to unmute..

During turn on until mute is released, speaker fault detection is performed, and then the amplifier enters the play mode, AC load diagnostic can begin to be performed.

The amplifier is turned off with IB1[D0]=0, soft mute is enabled, then output falls and SVR is discharged.

If the battery voltage drops below the minimum operating voltage of 6V the amplifier is muted, the capacitor on SVR is discharged and the amplifier restarts when the battery voltage returns to the correct voltage.

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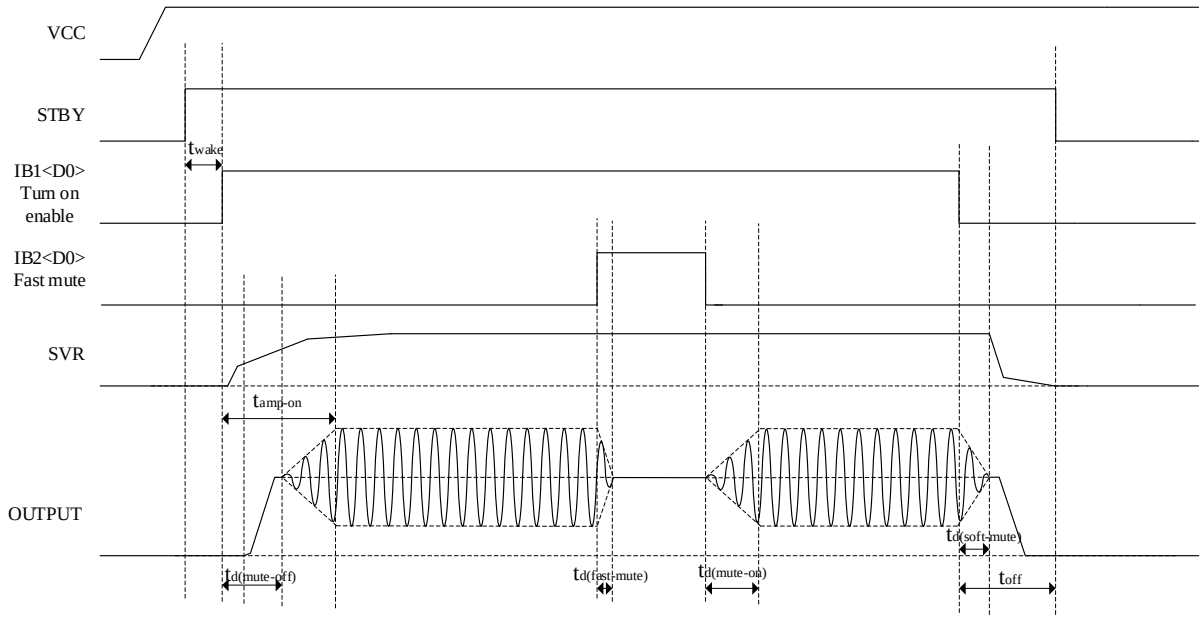

Figure 9-1 Turn on and turn off sequence

9.2 Start stop function and low voltage operation

In automobiles, a start-stop system or stop-start system automatically shuts down and restarts the internal combustion engine to reduce the amount of time the engine spends idling, thereby reducing fuel consumption and emissions. The typical start stop battery curves is shown below in Figure 9-2.

AC7325 allows to go on playing when battery falls down to 6V during such conditions. If the battery falls below 6V, the amplifier can mute without producing pop noise and play automatically when the battery voltage back to 6V or above.

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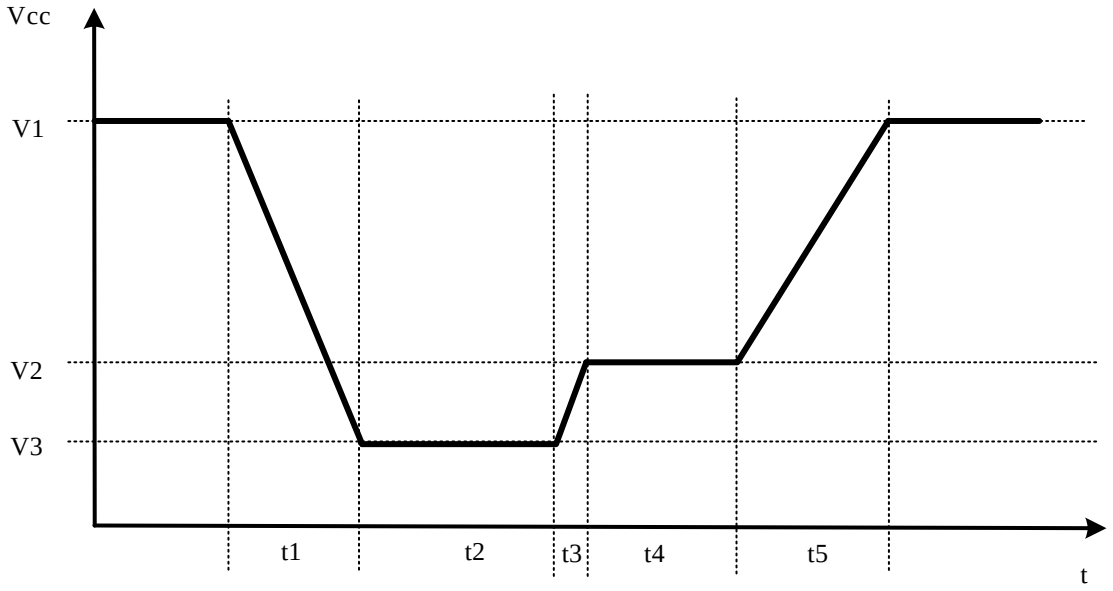

V1=12V/16V V2=6V V3=7V
t1=2ms t2=15ms t3=50ms t4=1s t5=100ms

Figure 9-2 Start stop curve

9.3 Protection

9.3.1 Output protection and short-circuit protection

When the amplifier output shorts to power supply, ground, or across the load, the amplifier will close the shorted channel to avoid audible distortion. The short to power supply and the short to ground protection window prevents the channel a restart. When the output exits the protection window or short across load, the channel will turn on after 15ms to check if the short is still be present. If yes, the channel turns off again. The channel repeats the above process again and again until it exists short circuit, then returns to normal state. The 15ms interval period reduces the power consumption of the amplifier.

Short circuit and short circuit type information can be read via the I^2C-bus. The short circuit information can also be indicated on the DIAG pin. If the DIAG pin is enabled to indicate the fault information, set with IB2[D4] = 0, the DIAG pin will be pulled low once a short circuit occurs.

9.3.2 Miss connect of Ground or Vcc

Miss connect of Ground or Vcc is a complex fault: the ground (or Vcc) is not connected and the ground (or Vcc) correctly but is connected to one of the amplifier outputs. In this short condition, the amplifier is not connected correctly so the protection circuit cannot work and protect the amplifier from this fault. It must resist this short current by the output stage itself.

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The output PDMOS and NDMOS transistors of AC7325 have been optimized for this fault and can avoid amplifier damage from this kind of fault.

9.3.3 Thermal protection

Thermal protection function is achieved by attenuating the output signal swing (Figure 9-3).

Thermal attenuation starts to work when the junction temperatures rises above the normal operating range. This behavior can significantly limit the output power and protect the chip from being too hot with a method that does not interrupt the chip normal operation.

If the chip temperature rises too high to trigger the thermal protection, the output power shrinks which will cool the chip. When the chip temperature drops to a fixed point, the thermal attenuation stops. It's called thermal equilibrium and this point is called thermal equilibrium point.

As the chip temperature rises from a relatively lower level to high enough to trigger the thermal protection, it will first trigger the thermal warning before the output power is attenuated. As shown in Figure 9-3 two thermal warning thresholds can be programmed by I^2C setting.

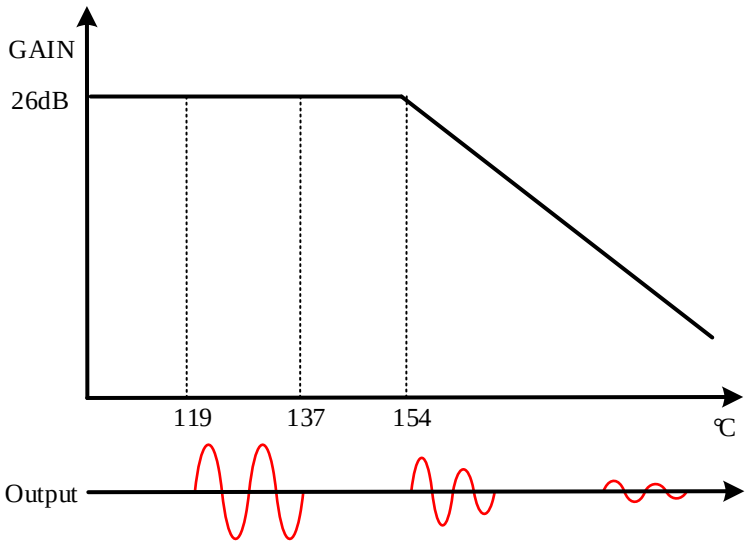

Figure 9-3 Thermal mute

9.3.4 Overvoltage warning and load dump protection

When the battery power rises beyond the allowed maximum voltage, the chip normal operation will be interrupted to protect the chip internal devices from damage. This is called load dump protection. The maximum voltage is Vth(ovp) which is determined by the chip design and fabrication process.

When the battery power starts to rise from the typical value to Vovp, it will first trigger the overvoltage warning before load dump protection occurs and the threshold voltage is defined as Vcc_warn.

The overvoltage warning flag can also be sent out at the diagnostic output (DIAG pin) since the diagnostic output functionality is chosen through I^2C setting.

Even though the normal operation of the chip has been disabled during load dump conditions. The master can still communicate with the chip slave and all the digital is alive, which help users to read

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the status of chip channel output and overvoltage warning.

9.4 Diagnostics

9.4.1 DIAG pin

Diagnostic information can be read via the I²C-bus, but many diagnostics messages can also be available at pin DIAG. These diagnostics information could be seen at pin DIAG as a logical NOR and pin DIAG is an OD(Open Drain) pin. If there is a failure, DIAG remains low and microcontroller can read the failure information via the I²C bus. Pin DIAG could also minimize the I²C bus traffic by being used as a microcontroller interrupt. Pin DIAG will be released when the failure is removed. The detailed trigger sources of pin DIAG can be seen from Table 9-1.

Table 9-1 Diagnostic information on pin DIAG

Diagnostic information	DIAG pin
Power-On Reset(POR)	After POR, pin DIAG remains LOW until amplifier starts (inverse of start-up bit)
Low battery	Yes
Clip detection	Can be enabled per channel (can be enabled below Vcc = 10 V, by IB1[D7]); default is 'blocked'
Temperature pre-warning	Can be enabled; default: $T_{j(AV)(pwarn)}$ = 160°C
Short	Can be enabled; default is enabled
Speaker fault detection	No
Offset detection	No
Load detection	No
Overvoltage protection(20 V)	Yes
Overvoltage pre-warning (16 V)	Can be enabled; default is disabled
Maximum temperature protection (active)	Yes
Start-up diagnostics indication	No

9.4.2 DC load detection during turn on

If IB1D1 is set to 1, the turn on diagnostics is enabled. AC7325 will report the load condition of all four channels while the diagnostics stage is ended. The load information can be known by reading I²C register. The load information is shown in Table 9-2**.**

Table 9-2 Short circuit detection thresholds

Short load		Normal load		Open load
0Ω —— 1.5Ω		**3.2Ω —— 20Ω**		**80Ω —— ∞**

There is a spike filter to remove any spike or glitch caused by switching relays in the wiring harness or EMC. Only the load information sustaining more than 10ms will be acknowledged and sent to I²C register.

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During turn on diagnostics stage, the invalid bits(see Table 9-3) are set, and “the start-up diag busy bit” (DB5[D5]) is set to 1 to show that turn on diagnostics stage is in progress. When turn on diagnostics stage is ended, the “start-up diag busy bit” is reset to 0.

Several abnormal statuses can make the turn on diagnostics invalid. They are overvoltage, Vcc<10V, POR or OCP trigger. In these cases, load information is set to 11. For example, if a start stop is occurred during the turn on diagnostics stage, Vcc will drop below 10V, so the load information DBx[D4:D5] is set to 11. In such case, repeating the turn on diagnostics may get a new load information result and DBx[D4:D5] will be rewritten.

Turn on diagnostics (IB1[D1]) and amplifier on (IB1[D0]) command are independent.

If IB1[D1:D0]=10 is sent, turn on diagnostics will be executed and after this turn on diagnostics stage ends, amplifier will return to turn off state.

If IB1[D1:D0]=11 is sent, turn on diagnostics will be executed first and after this turn on diagnostics stage ends, amplifier on command will be executed.

Table 9-3 Load information I²C-bus bits

I²C bits		Description
DBx[D5]	DBx[D4]	
0	0	Normal load
0	1	Reserved
1	0	Open load
1	1	Invalid: overvoltage or V_{cc} < 10 V has occurred, or turn on diagnostics not completed, or OCP triggered.

9.4.3 Speaker fault detection

If one side of the speaker is connected to an output, the other side is grounded/powered when the other output of the channel is left open, speaker fault protection will be triggered to protect the speaker.

The speaker fault type can be read via I²C-bus. When the speaker fault protection is triggered, the amplifier channel does not turn off, just indicates in I²C. The amplifier will perform a speaker fault detection during amplifier start-up until mute is released. If the speaker fault current is 1A, the speaker fault will be identified.

9.4.4 DC offset detection

The offset detection can be performed with or without (e.g. AMP is muted after start up) an input signal. The I²C bus DBx[D2] will be set if the I²C bus read that the output offset detection occurs. If the amplifier BTL output voltage is within a window with a threshold of 1.3 V (typical), the DBx[D2] latches are reset and their setting is disabled. Another case is that I²C bus read is performed and the offset bits are set at the first read time and still set after 1 s (the second read time), it means that the output did not cross the offset threshold window during the last 1 second. It means either a frequency below

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1 Hz was applied (1 s I²C-bus read interval) or an output offset of more than 1.3 V is present. Detail information is presented in Figure 9-4.

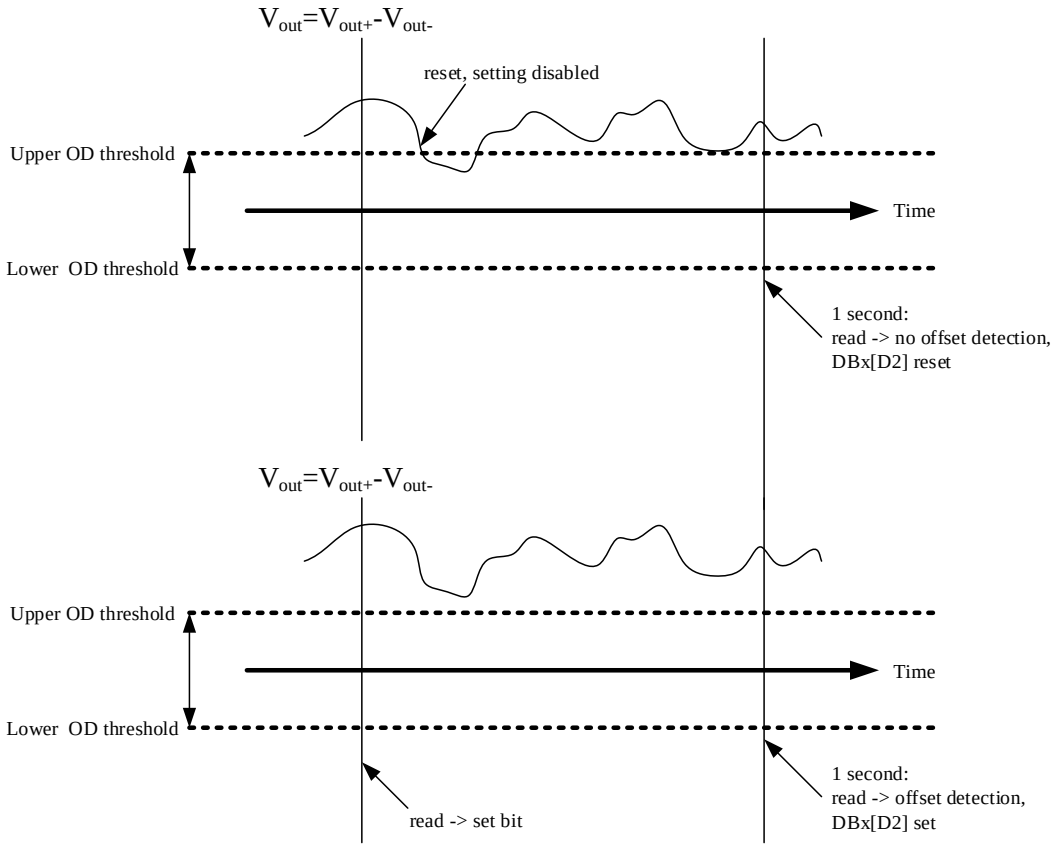

Figure 9-4 Offset detection

9.4.5 AC load diagnostic

AC load diagnostic, set with IB1[D2], is targeted at detecting disconnection of 2-way speaker with AC coupled section, such as speaker with tweeters, more generally, woofer with parallel tweeter. When performing the AC load diagnostic, the high efficiency mode must be disabled by setting IB5[D7] to 0.

The diagnostic principle is that a speaker with a tweeter, the part (woofer) other than the tweeter will become high impedance at high frequencies because this frequency band is out of its operating range. So if the tweeter is not connected, the impedance of the entire speaker will increase at high frequencies. Apply a voltage across the speaker can make a diagnostic based on the peak output current. There are high and low current levels to select form. When the output peak current of the amplifier triggers 500mA (with IB4[D1]=1) 64 times, the AC load diagnostic bit is set. When set to the low current level (with IB4[D1]=0), the trigger threshold becomes 275mA. The purpose of the 64 trigger count is to prevent false AC load diagnostic results when the input signal is turned on and off.

- High current level IB4 [D1] = 1
  Output current > 500 mApk, AC load detected
  Output current < 250 mApk, AC load not detected

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- Low current level IB4[D1]=0
  Output current > 275 mApk, AC load detected
  Output current < 100 mApk, AC load not detected

The frequency and amplitude of the input signal depend on the impedance characteristic of specific speaker. To implement the above diagnostic function, a 19 kHz signal must be added to the input of the amplifier. AC load diagnostic is only performed after start-up mute is released and high efficiency mode is disabled during diagnostic. The AC load diagnostic information can be read by setting IB4[D4]=1. In the case IB4[D4]=0, the AC Load information cannot be read but preserved

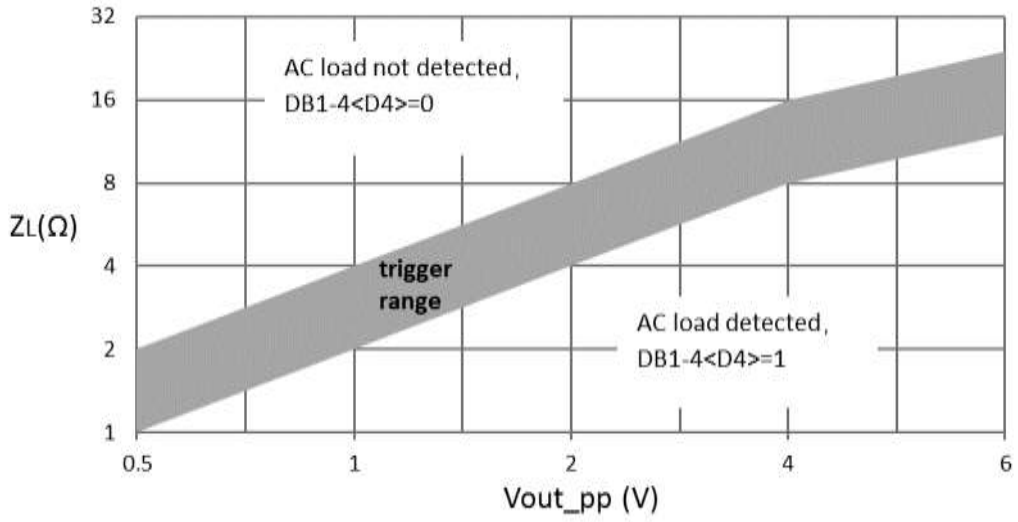

Figure 9-5 High current level, AC load impedance vs peak Vout_app

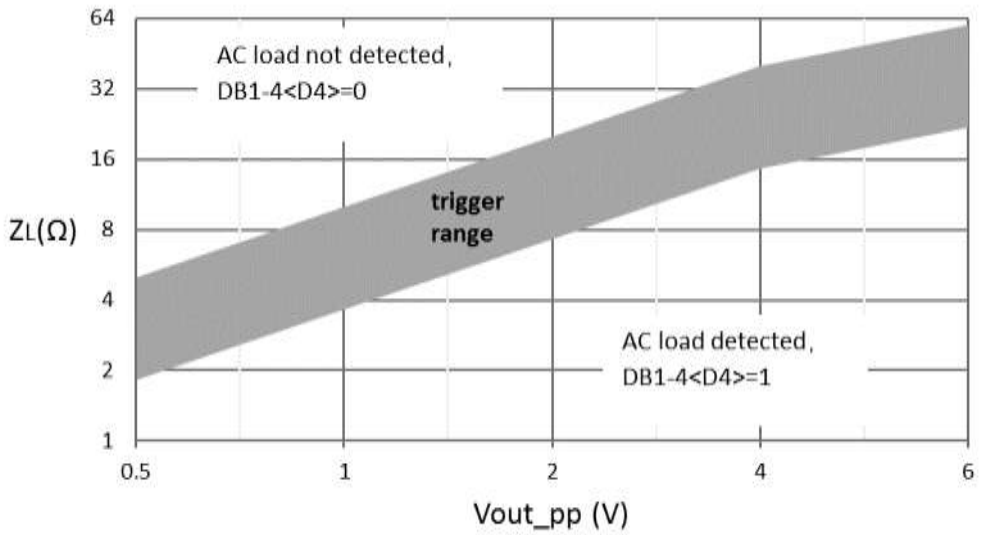

Figure 9-6 Low current level, AC load impedance vs peak Vout_pp

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9.4.6 Clip detection

When the input signal of the amplifier is large, the output of amplifier begins to distort near the power source or the ground, that is clipping distortion. The clipping information is sent directly to the DIAG pin, same as temperature and protection information. It can be programmed via the I^2C-bus by disabling the temperature and protection information on the DIAG pin to indicate clipping information only. When the clipping distortion reaches the preset value, the DIAG pin will be pulled low.

There are three detect thresholds for the clipping detection can be selected by setting IB2[D7:D6] (2%, 5% or 10%). Meanwhile, IB2[D7:D6] set to 11 can disable clipping detection.

The clipping information will be blocked below 10V of power supply voltage. However, it can operate at the voltage less than 10V through I^2C programming, but the accuracy of the clipping detection information is not guaranteed.

9.5 HE mode

HE mode is designed for a small signal whose amplitude less than several values avoiding output saturation. By closing the switch, two channels work in single ended mode, the output current flow from one end to the other through this switch.

In HE mode, lower current in connected channels will result in the less power dissipation. For this reason, one positive and one negative output are connected to the switch.

Therefore, to save power dissipation, the ideal condition is the two channels have the same signal. The current shared between different channels is maximum. Comparing with standard bridge connection, HE mode power dissipation will be saved up to 65%.

Now in many advanced audio systems, more intensive digital signal processor is used. This DSP processing bring the introduction of different equalization and delays among different channels, this makes the saved current not so valid. By using a new HE structure, there is more chance to have two or more channels in HE mode. The connected terminals also have more independent currents summing for saving current when input signals are uncorrelated.

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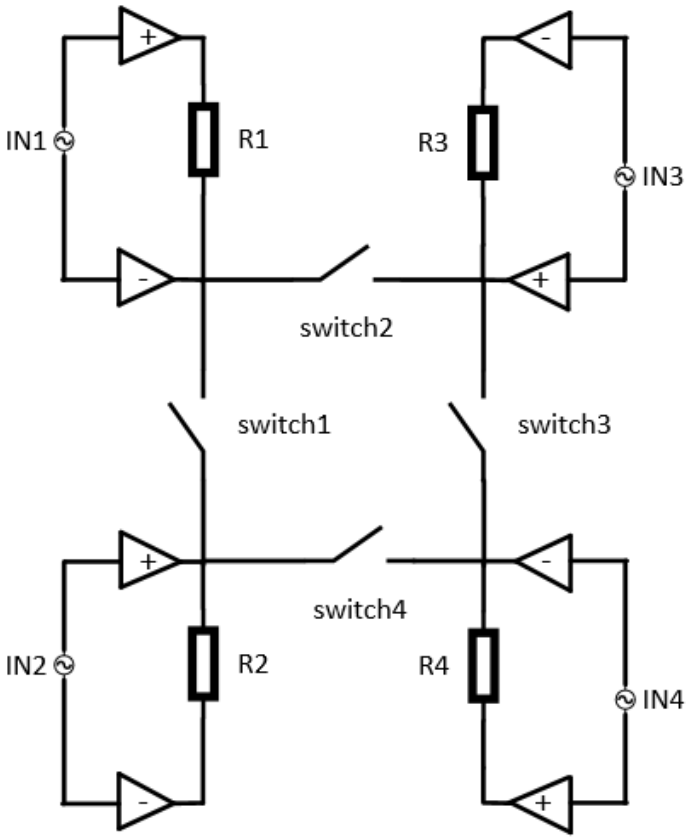

Figure 9-7 HE mode structure

9.6 Address select

With the help of pin ADSEL, the amplifier can support address selection. The value of resistor connected between ground and pin ADSEL determines the address as shown in Table 9-4**.** Only when the battery power is above 6V, this function can be guaranteed.

Table 9-4 AC7325 address select resistor

R ADSEL	D6	D5	D4	D3	D2	D1	D0	R/W	HEX
OPEN	1	1	0	1	1	0	1	0 = Write to AC7325 1 = Read from AC7325	DA
100 kΩ ± 1%	1	1	0	1	1	1	0		DC
30 kΩ ± 1%	1	1	0	1	1	1	1		DE
10 kΩ ± 1 %	1	1	0	1	0	1	0		D4

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10 Performance Diagrams

10.1 THD vs frequency in BTL mode

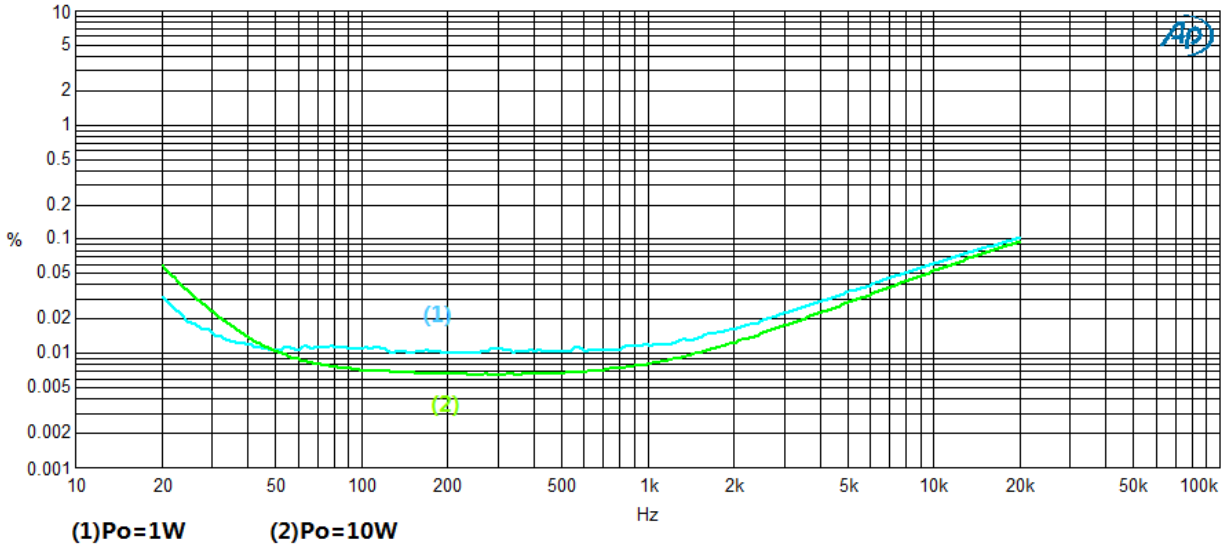

Figure 10-1 THD vs frequency in BTL mode

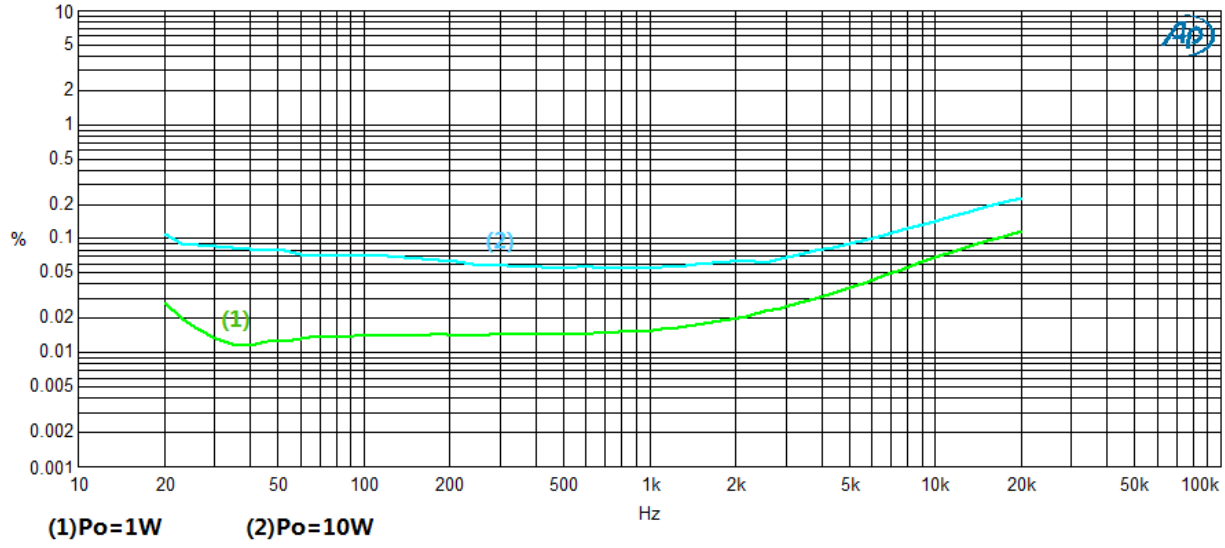

Figure 10-2 THD vs frequency in High efficiency mode

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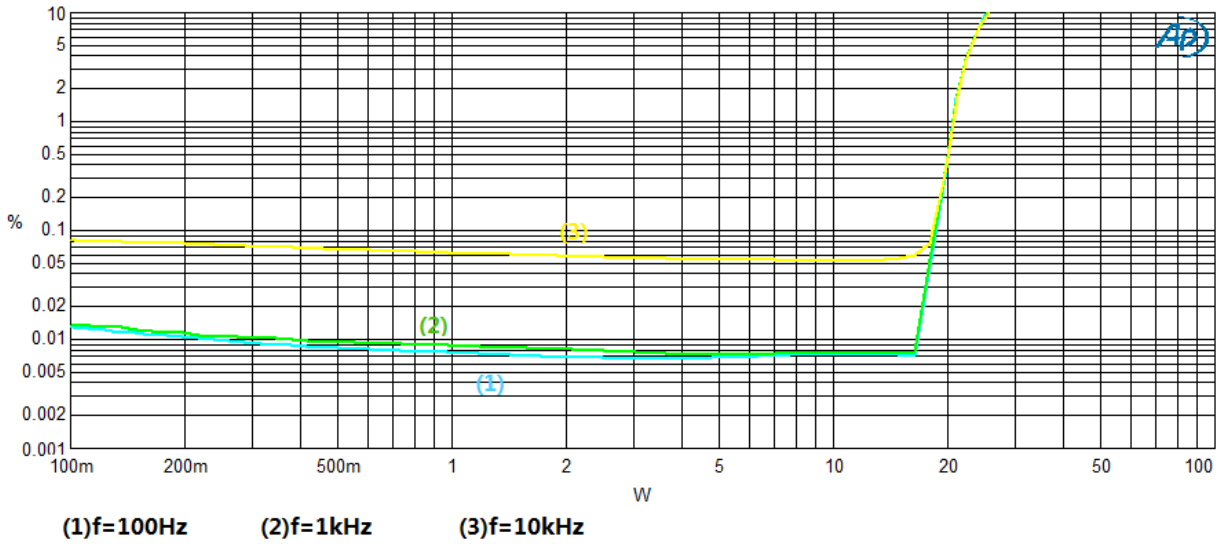

Figure 10-3 THD vs output power in BTL mode

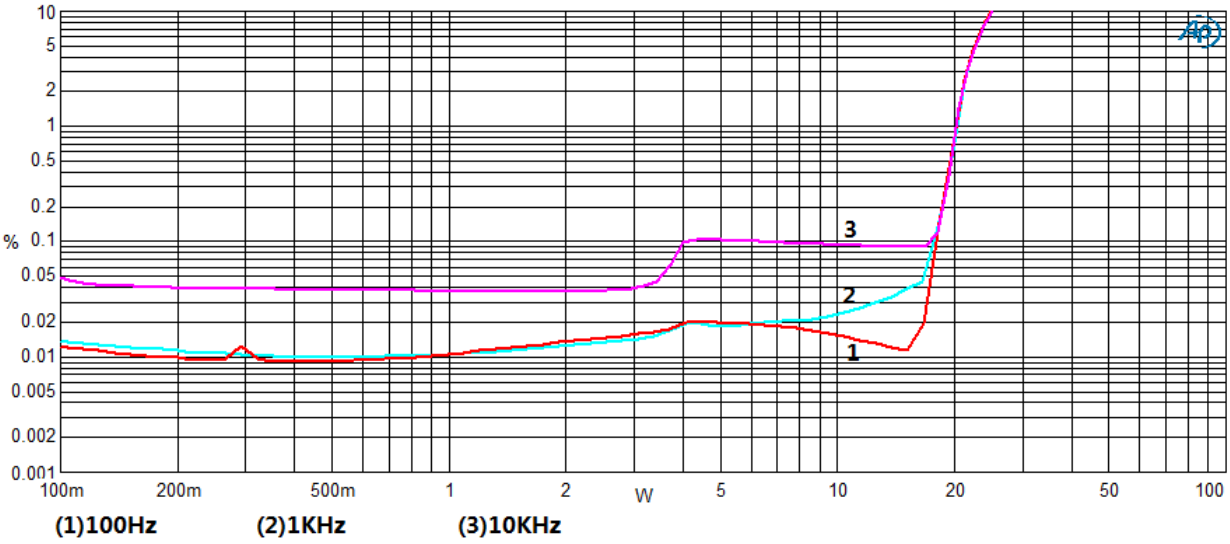

Figure 10-4 THD vs output power in High efficiency mode

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10.2 Crosstalk vs frequency

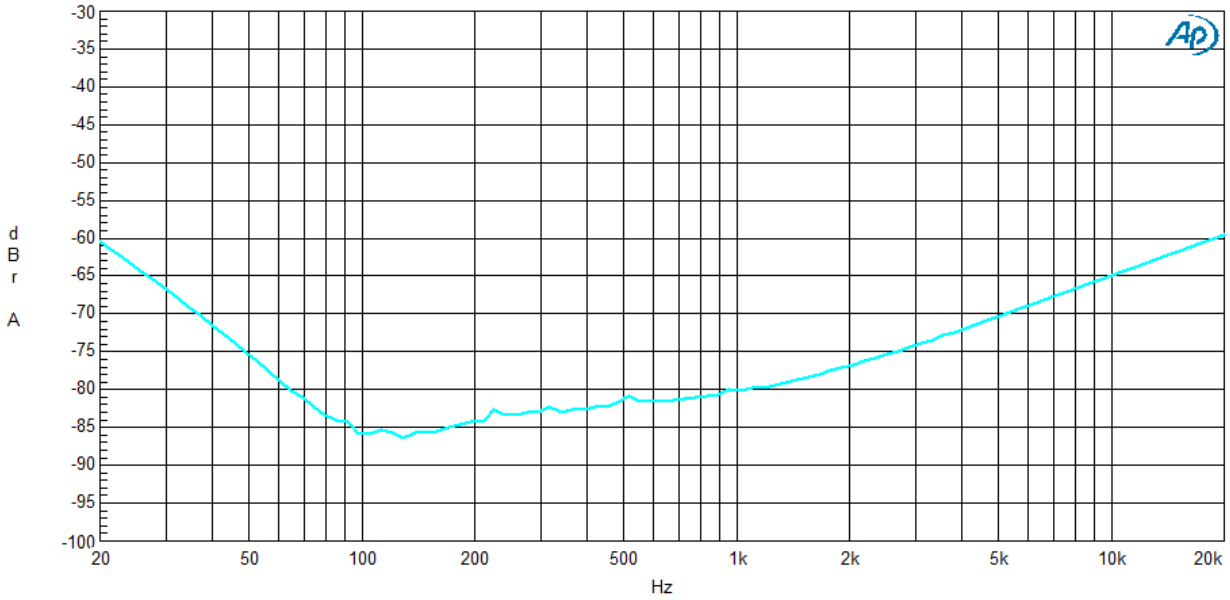

Figure 10-5 Crosstalk vs frequency

10.3 PSRR vs frequency

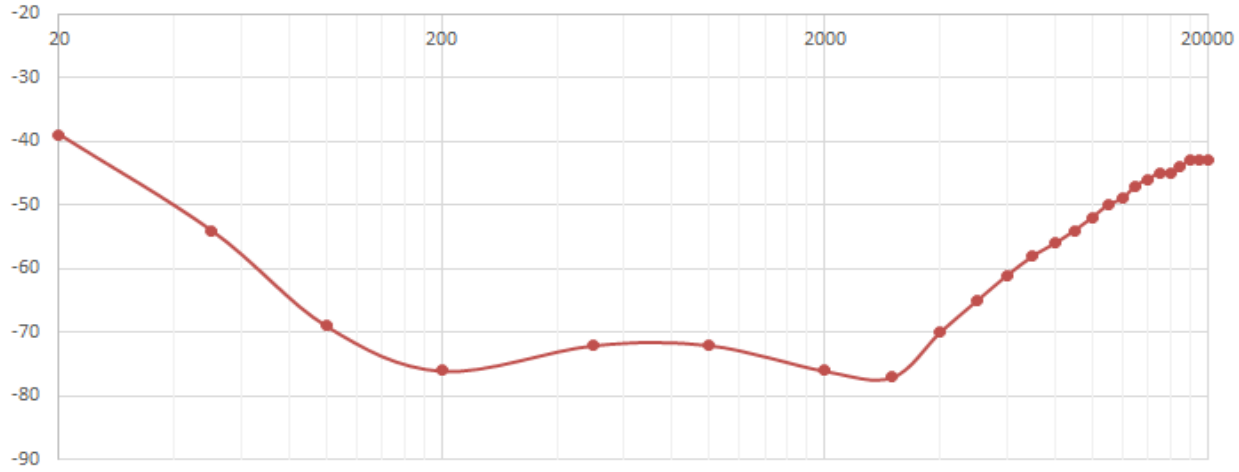

Figure 10-6 PSRR vs frequency

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10.4 Output power vs Vcc

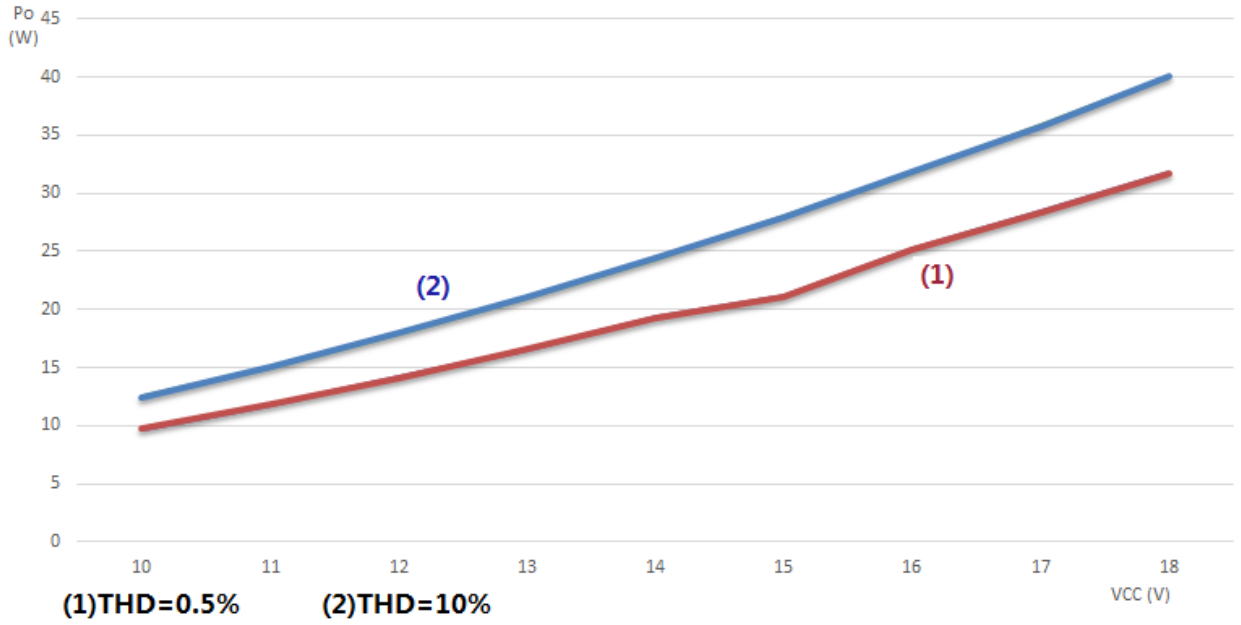

Figure 10-7 Output power vs Vcc

10.5 Power dissipation vs output power

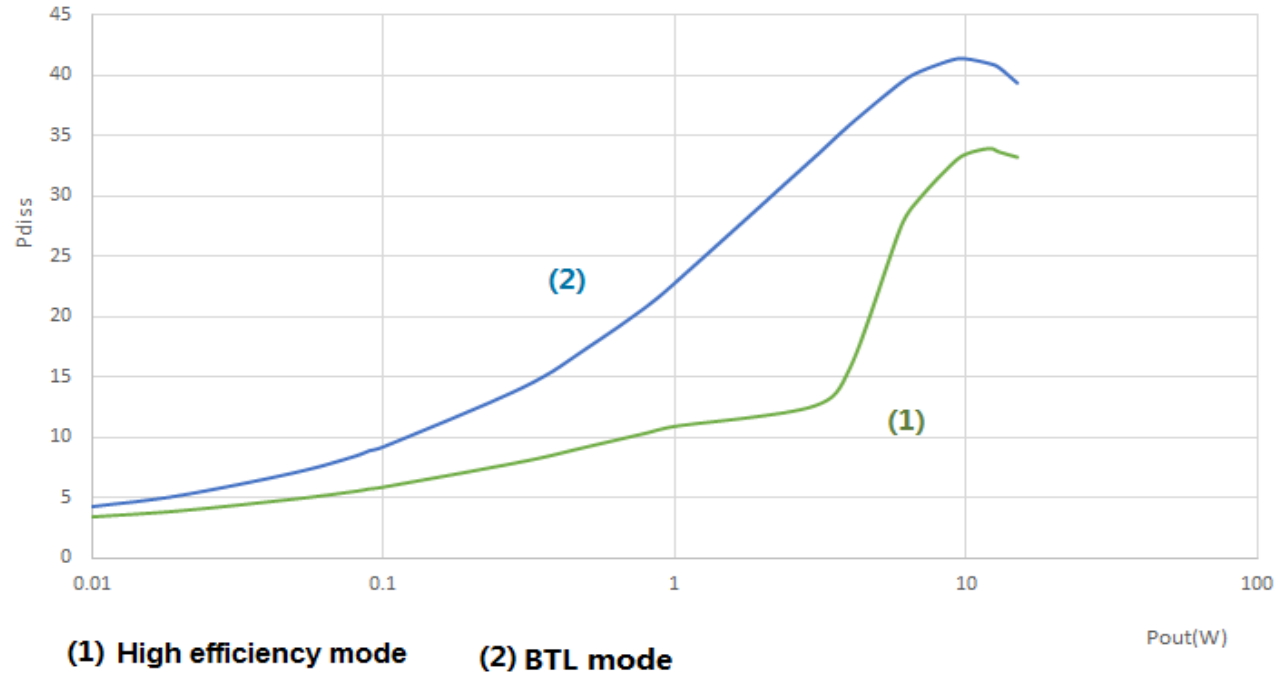

Figure 10-8 Power dissipation vs output power, correlation input signal

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10.6 Power dissipation vs output power

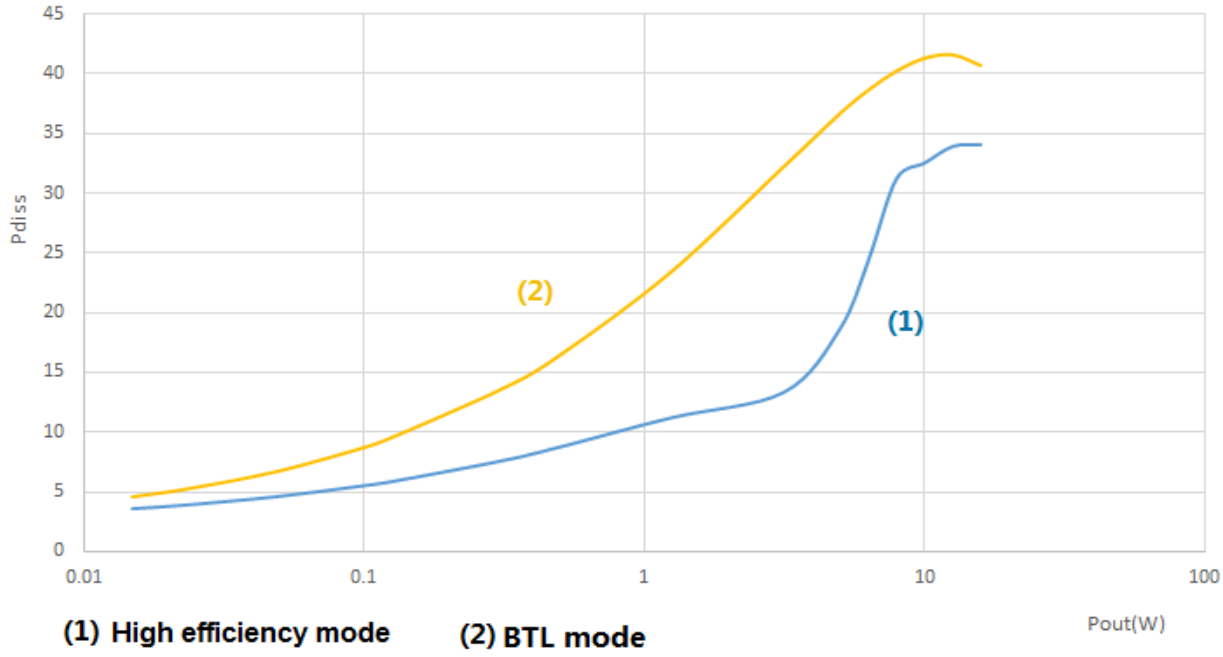

Figure 10-9 Power dissipation vs output power, no correlation input signal

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11 Application Information

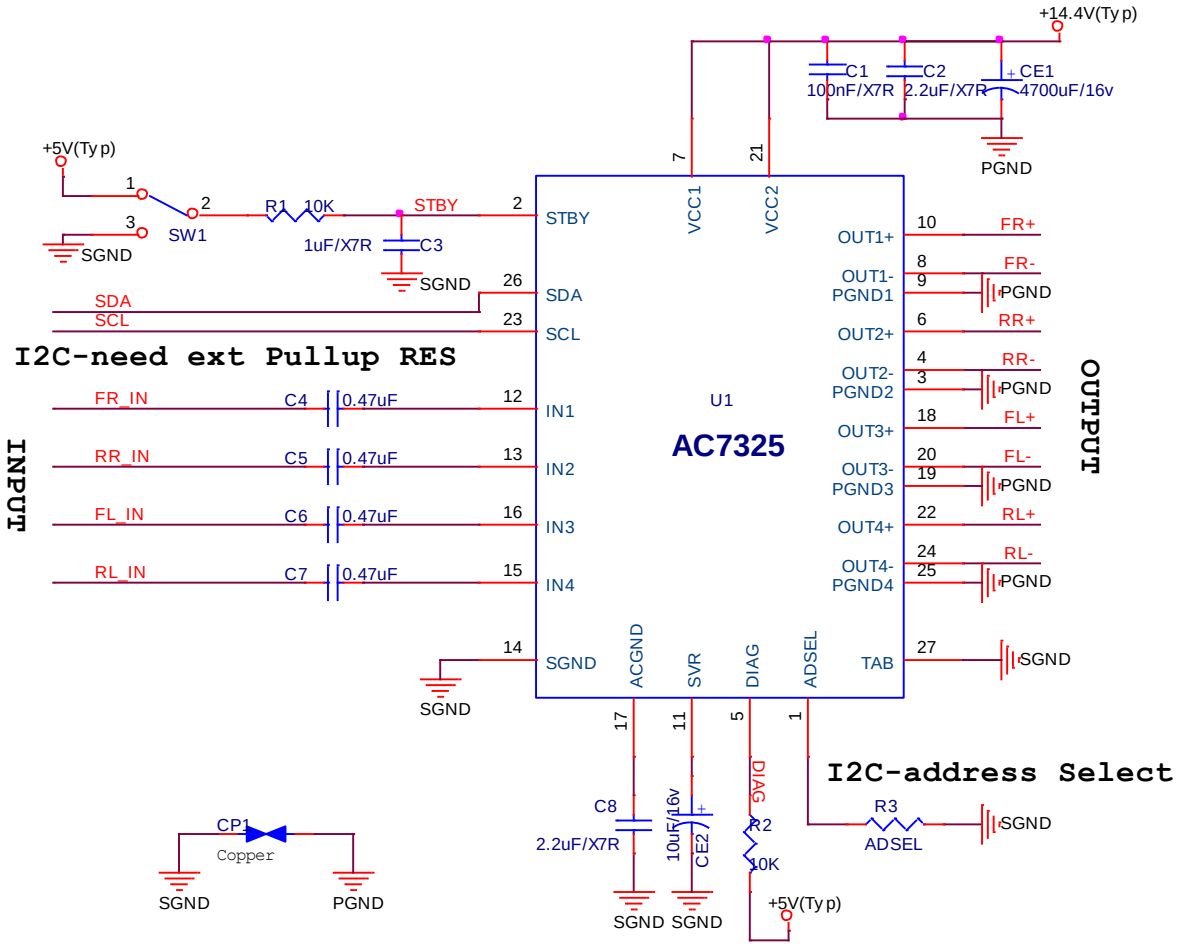

Figure 11-1 Application circuit

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12 Package Outline

12.1 Package outline

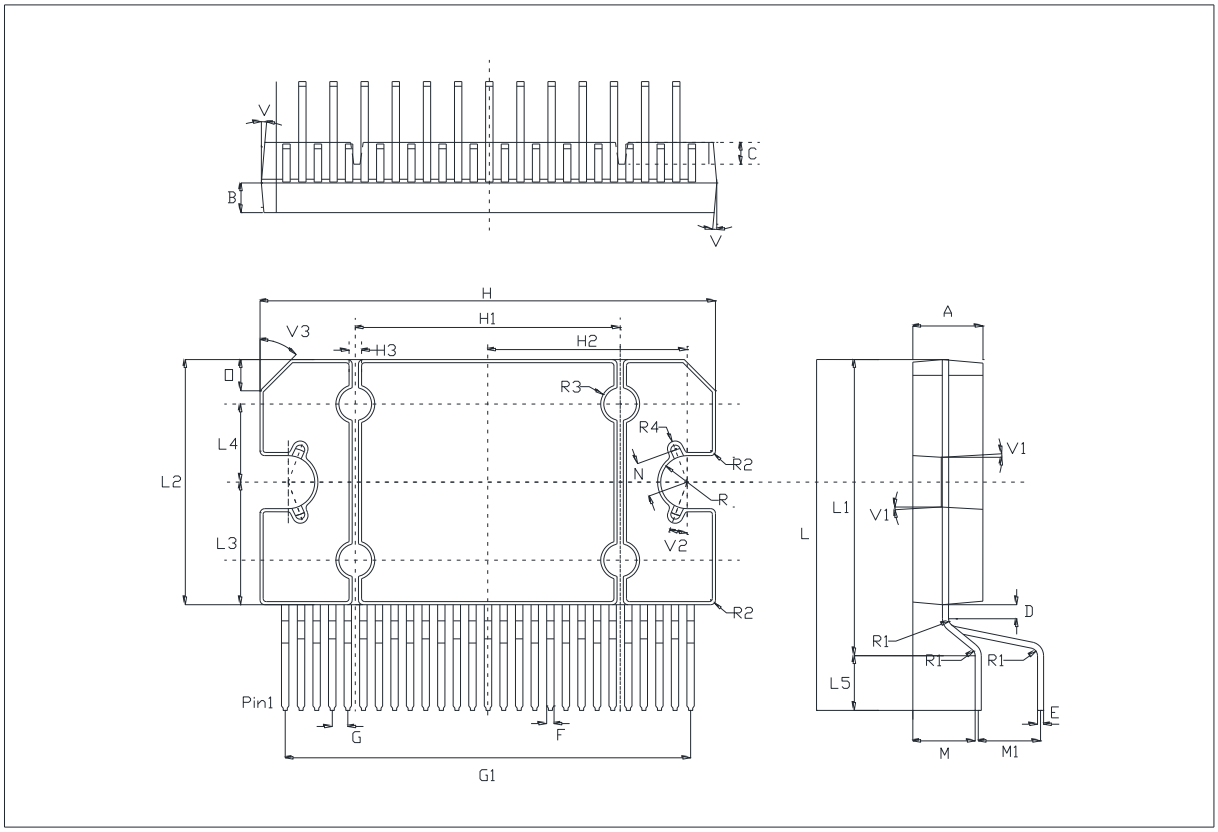

Figure 12-1 HZIP 27-pin Package Outline[1]

[1] Drawing is not to scale.

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12.2 Package dimensions

Table 12-1 HZIP 27-pin Mechanical Data and Package Dimensions[1]

SYMBOL	Min.	Typ.	Max.
A	4.45	4.50	4.65
B	1.80	1.90	2.00
C		1.40	
D	0.75	0.90	1.05
E	0.37	0.39	0.42
F			0.57
G	0.80	1.00	1.20
G1	25.75	26.00	26.25
H	28.90	29.23	29.30
H1		17.00	
H2		12.80	
H3		0.80	
L	22.07	22.47	22.87
L1	18.57	18.97	19.37
L2	15.50	15.70	15.90
L3	7.70	7.85	7.95
L4		5	
L5		3.5	
M	3.70	4.00	4.30
M1	3.60	4.00	4.40
N		2.20	
O		2	
R		1.70	
R1		0.5	
R2		0.3	
R3		1.25	
R4		0.50	
V		5°(Typ.)	
V1		3°(Typ.)	
V2		20°(Typ.)	
V3		45°(Typ.)	

[1] Dimensions are expressed in millimeters.

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