

### General Description

The SA24403 develops a high efficiency synchronous step-down DC/DC converter capable of delivering 3.5A load current. The SA24403 operates over a wide input voltage range from 4.2V to 40V and integrates main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

The SA24403 adopts peak current control scheme. The switching frequency is adjustable from 300kHz to 2.2MHz using an external resistor. The device also features ultra low quiescent operating to achieve high efficiency under light load. And the internal soft-start limits inrush current during power on.

### Ordering Information

SA24403 □(□□)□  
 └───┬───┬───  
 Temperature Code  
 Package Code  
 Optional Spec Code

Ordering Number	Package Type	Note
SA24403FCA	SO8E	

### Features

- Low  $R_{DS(ON)}$  for Internal Switches (Top/Bottom): 115/80mΩ
- 4.2-40V Input Voltage Range
- Internal Compensation
- Internal 1ms Soft-start Limits the Inrush Current
- Adjustable Switching Frequency Range: 300kHz to 2.2MHz
- 3.5A Output Current Capability
- ±2% 0.6V Reference Over -40 °C~125 °C
- Cycle-by-cycle Peak Current Limitation
- Short Circuit Protection
- Thermal Shutdown and Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package: SO8E
- Automotive AEC-Q100 Grade 1 certified

### Applications

- Automotive
- Industrial
- High-Voltage DC/DC Converters

### Typical Application

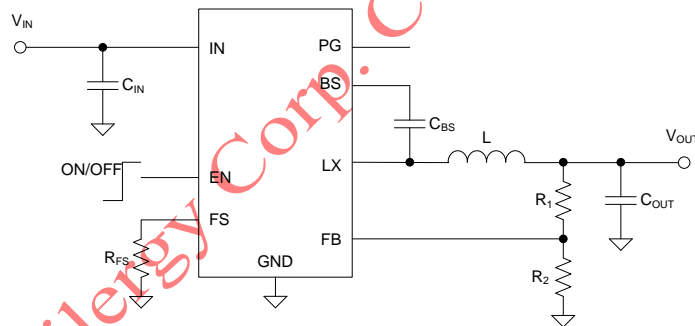


Figure1. Schematic Diagram

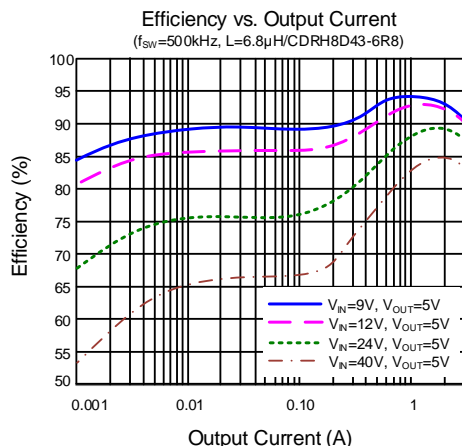
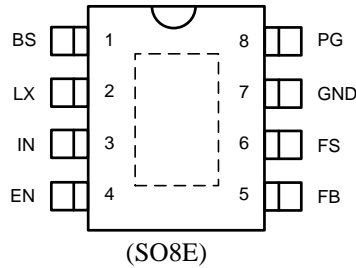


Figure2. Efficiency vs. Output Current

### Pinout (Top View)



**Top Mark: BTSxyz** (device code: BTS, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1 μF ceramic capacitor between the BS and the LX pin.
LX	2	Inductor pin. Connect this pin to the switching node of inductor.
IN	3	Input pin. Decouple this pin to GND pin with at least a 4.7μF ceramic capacitor.
EN	4	Enable control. Pull high to turn on. Do not leave it floating.
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_1/R_2)$
FS	6	Frequency setting pin. Connect a resistor from this pin to GND to program the switching frequency. The switching frequency equals to: $f_{sw}(kHz) = 10^6 / (9.3 \times R_{FS}(k\Omega) + 30)$
GND	7	Ground.
PG	8	Power good indicator. Open drain output. Externally pulled high when $V_{OUT}$ is within regulation range. Otherwise, internally pulled low.

### Block Diagram

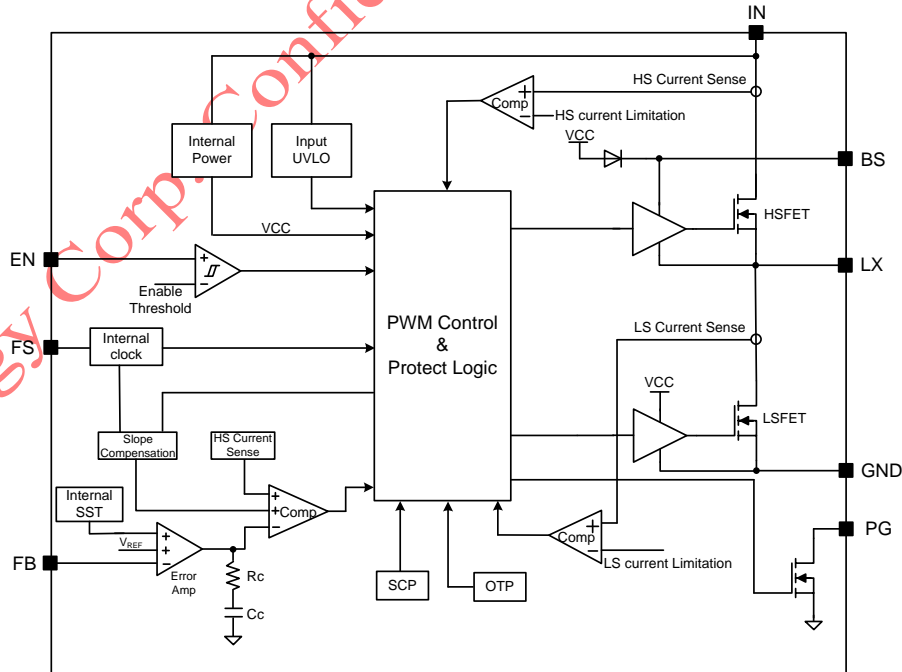


Figure3. Block diagram

**Absolute Maximum Ratings** (Note 1)

IN to GND	-----	-0.3V to 44V
LX, FB, EN, FS, PG to GND	-----	-0.3V to 44V
BS-LX	-----	4V
Power Dissipation, P <sub>D</sub> @ T <sub>A</sub> = 25 °C, SO8E	-----	2.5W
Package Thermal Resistance (Note 2)		
θ <sub>JA</sub>	-----	40 °C/W
θ <sub>JC</sub>	-----	12 °C/W
Junction Temperature Range	-----	-40 °C to 150 °C
Lead Temperature (Soldering, 10 sec.)	-----	260 °C
Storage Temperature Range	-----	-65 °C to 150 °C

**Recommended Operating Conditions** (Note 3)

Supply Input Voltage	-----	4.2V to 40V
Ambient Temperature Range	-----	-40 °C to 125 °C

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## Electrical Characteristics

( $V_{IN} = 12V$ ,  $T_J = -40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$ . Typical values are at  $T_J=25\text{ }^\circ\text{C}$ , unless otherwise specified. The values are guaranteed by test design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		4.2		40	V
Input UVLO Threshold	$V_{UVLO}$		3.6	3.9	4.2	V
UVLO Hysteresis	$V_{HYS}$			0.3		V
Quiescent Current	$I_Q$	$I_{OUT}=0, V_{FB}=V_{REF}\times 105\%, T_J=25\text{ }^\circ\text{C}$	10	18	25	$\mu\text{A}$
		$I_{OUT}=0, V_{FB}=V_{REF}\times 105\%, T_J=-40\text{ }^\circ\text{C}\sim 125\text{ }^\circ\text{C}$	5	18	33	
Shutdown Current	$I_{SHDN}$	$EN=0, T_J=25\text{ }^\circ\text{C}$			1	$\mu\text{A}$
		$EN=0, T_J=-40\text{ }^\circ\text{C}\sim 125\text{ }^\circ\text{C}$			5	
Feedback Reference Voltage	$V_{REF}$	$T_J=25\text{ }^\circ\text{C}$	0.594	0.6	0.606	V
		$T_J=-40\text{ }^\circ\text{C}\sim 125\text{ }^\circ\text{C}$	0.588	0.6	0.612	
FB Input Current	$I_{FB}$	$V_{FB}=0.65V$	-50		50	nA
Top FET RON	$R_{DS(ON)1}$		70	115	210	m $\Omega$
Bottom FET RON	$R_{DS(ON)2}$		45	80	135	m $\Omega$
Top FET Current Limit	$I_{LIM, TOP}$		4.4	5.5	6.6	A
EN High Threshold	$V_{ENH}$		1.08	1.2	1.32	V
EN Low Threshold	$V_{ENL}$		0.9	1.0	1.1	V
Hiccup Duty Cycle	$D_{HICcup}$			12.5		%
Output Discharge Current	$I_{DIS}$			45		mA
Oscillator Frequency Program Range	$f_{OSC, RNG}$	$R_{FS}=45.6k\sim 360k$	300		2200	kHz
Oscillator Frequency Accuracy	$f_{OSC, ACC}$	$f_{OSC}=2\text{MHz}$ , with $R_{FS}$ resistor of 1% accuracy	-12%		12%	$f_{OSC}$
Output Under Voltage Protection Threshold	$V_{UVP}$			33%		$V_{REF}$
Power Good Threshold	$V_{PG}$	$V_{FB}$ falling, PG from high to low		89%		$V_{REF}$
		$V_{FB}$ rising, PG from low to high		93%		$V_{REF}$
		$V_{FB}$ rising, PG from high to low		115%		$V_{REF}$
		$V_{FB}$ falling, PG from low to high		113%		$V_{REF}$
PG Delay	$t_{PG, F}$	PG falling edge		10		$\mu\text{s}$
	$t_{PG, R}$	PG rising edge		150		$\mu\text{s}$
Power Good Output Low Voltage	$V_{PG, LOW}$	$I_{PG, LOW}=10\text{mA}$			0.7	V
Soft-start Time	$t_{SS}$		0.5	1	2	ms
Min ON Time	$t_{ON, MIN}$			90		ns
Min OFF Time	$t_{OFF, MIN}$	$f_{OSC}=2\text{MHz}$		90		ns
Thermal Shutdown Temperature	$T_{SD}$			160		$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{SD, HYS}$			20		$^\circ\text{C}$

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25\text{ }^\circ\text{C}$  on a two-layer Silergy demo board.

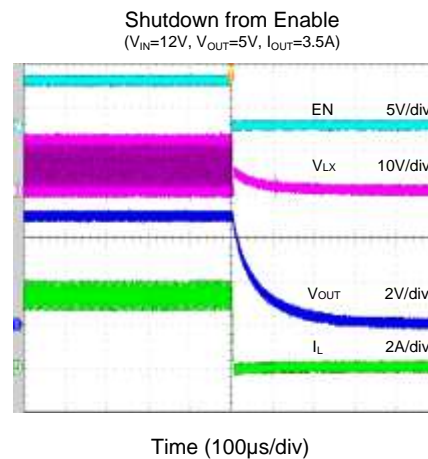
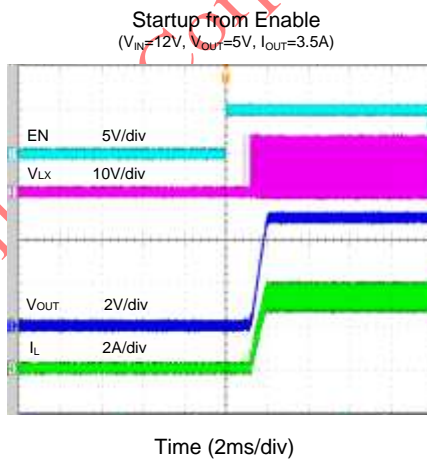
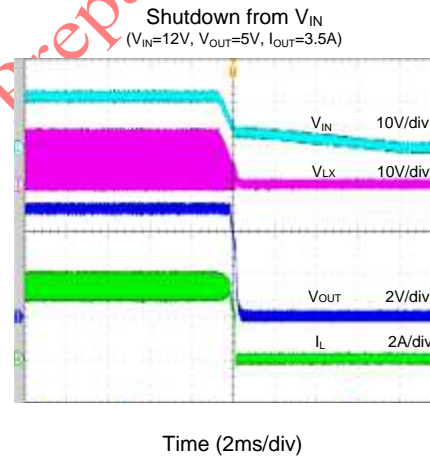
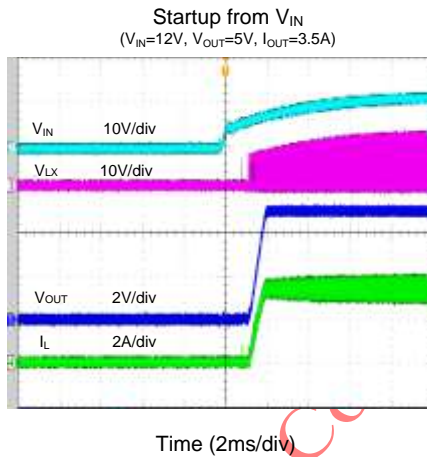
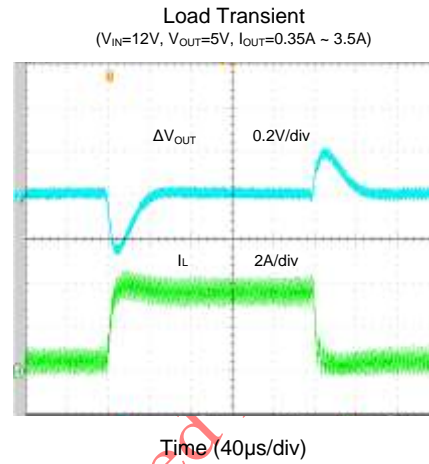
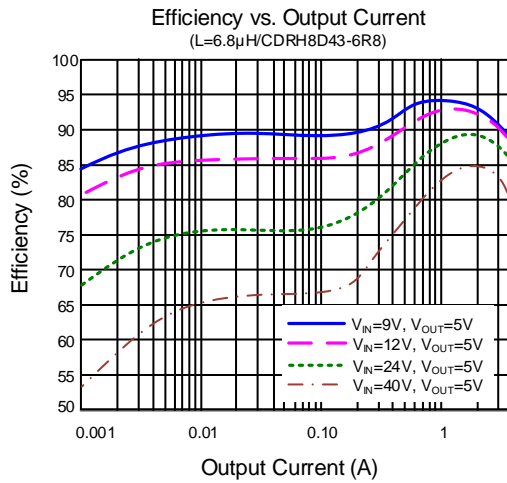
**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** High junction temperatures degrade operating lifetime. Operating lifetime is derated for junction temperatures greater than  $125\text{ }^\circ\text{C}$ .

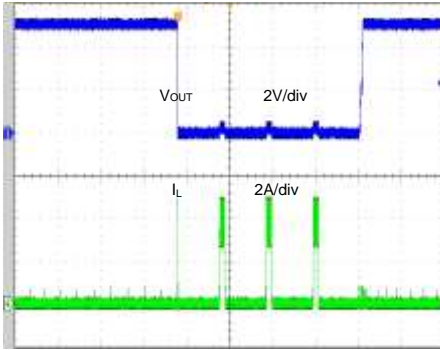
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## Typical Performance Characteristics

( $f_{sw}=500kHz$ ,  $T_A=25\text{ }^\circ C$ )

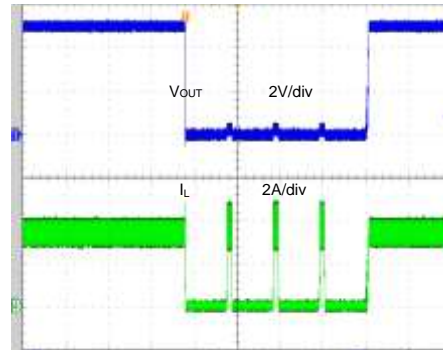


Short Circuit Protection  
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ , 0A to Short)



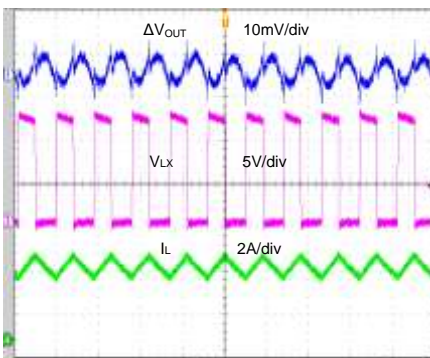
Time (20ms/div)

Short Circuit Protection  
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ , 3.5A to Short)



Time (20ms/div)

Output Ripple  
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=3.5A$ )



Time (2μs/div)

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## Operation

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The SA24403 adopts peak current control scheme. The switching frequency is adjustable from 300kHz to 2.2MHz using an external resistor. The device also features ultra low quiescent operating to achieve high efficiency under light load. And the internal soft-start limits inrush current during power on.

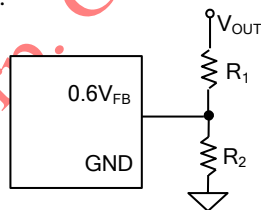
## Applications Information

Because of the high integration in the SA24403, the application circuit based on this regulator is rather simple. Only input capacitor  $C_{IN}$ , output capacitor  $C_{OUT}$ , output inductor L and feedback resistors ( $R_1$  and  $R_2$ ) need to be selected for the targeted applications specifications.

### Feedback Resistor Dividers $R_1$ and $R_2$ :

Choose  $R_1$  and  $R_2$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_1$  and  $R_2$ . A value of between 10k $\Omega$  and 1M $\Omega$  is highly recommended for both resistors. If  $V_{OUT}$  is 3.3V,  $R_1=100k$  is chosen, then using following equation,  $R_2$  can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} \times R_1$$



### Input Capacitor $C_{IN}$ :

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by  $C_{IN}$ , and IN/GND pins. In this case, a 4.7 $\mu$ F low ESR ceramic capacitor is recommended.

### Output Capacitor $C_{OUT}$ :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor greater than 22 $\mu$ F capacitance.

### Output Inductor L:

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

where  $f_{sw}$  is the switching frequency and  $I_{OUT,MAX}$  is the maximum load current.

The SA24403 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

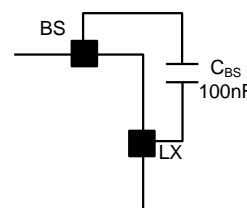
- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 50m\Omega$  to achieve a good overall efficiency.

### External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.





### Switching Frequency Setting:

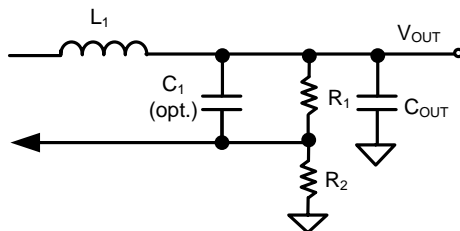
Connect a resistor from FS pin to GND to adjust the switching frequency. The switching frequency is adjustable from 300kHz to 2.2MHz. The switching frequency can be calculated by below equation:

$$f_{sw}(\text{kHz}) = \frac{10^6}{9.3 \times R_{FS}(\text{k}\Omega) + 30}$$

Where  $R_{FS}$  is in k $\Omega$ .

### Load Transient Considerations:

The SA24403 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic cap in parallel with  $R_1$  may further speed up the load transient response and it is recommended for applications with large load transient step requirements.



### Short-Circuit Protection:

The SA24403 integrates hic-cup mode short circuit protection function. If the device  $V_{OUT}$  drops below 33% of the set-point, the short-circuit protection mode will be initiated. The device will shut down for approximately 20ms, and then restart with a complete soft-start cycle that is approximately 2ms. If the short circuit condition remains another 'hiccup' cycle of shutdown and restart will continue indefinitely.

### Over-temperature Protection (OTP)

The SA24403 includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching

operation when the junction temperature exceeds 160 °C. Once the junction temperature cools down by approximately 20 °C the IC will resume normal operation with a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

### Layout Design:

The layout design of the SA24403 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC:  $C_{IN}$ , L,  $R_1$ , and  $R_2$ .

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2)  $C_{IN}$  must be close to the Pins IN and GND. The loop area formed by  $C_{IN}$  and GND must be minimized.
- 3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.
- 4) The components  $R_1$  and  $R_2$  and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1M $\Omega$  resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

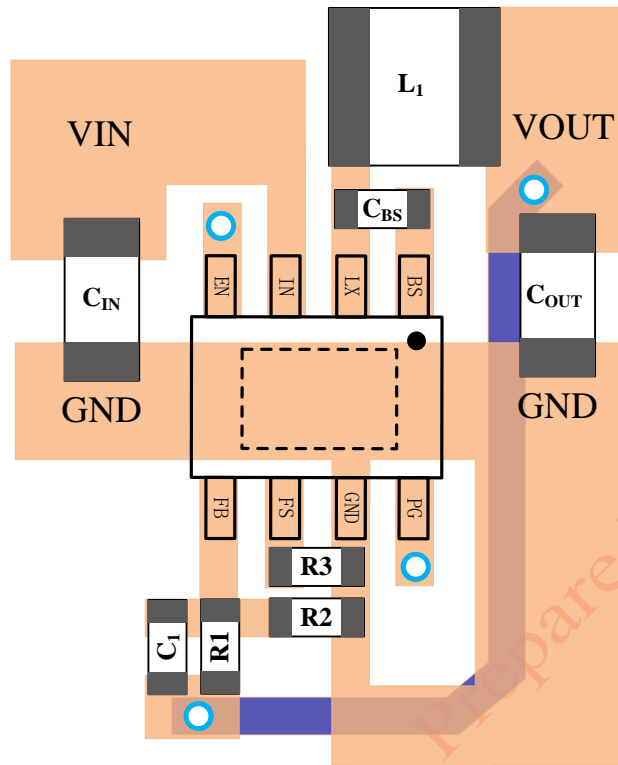
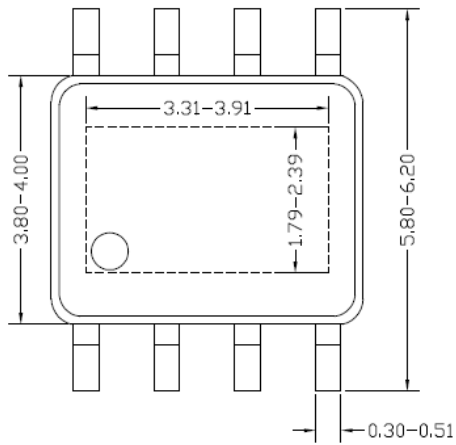
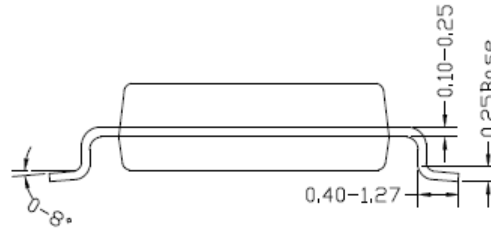


Figure4. PCB Layout Suggestion

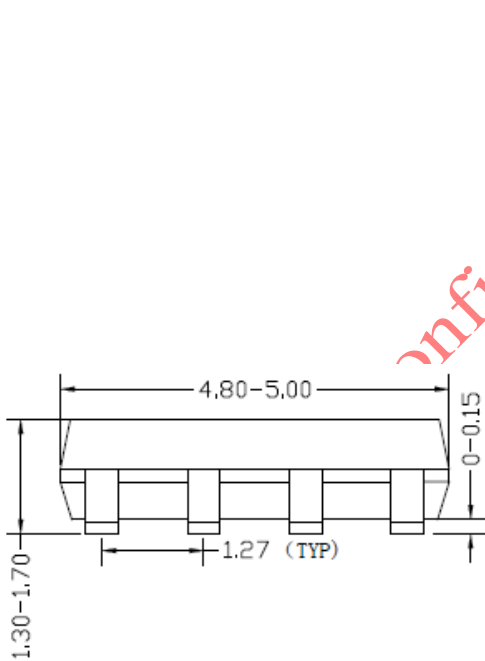
### SO8E Package Outline & PCB Layout



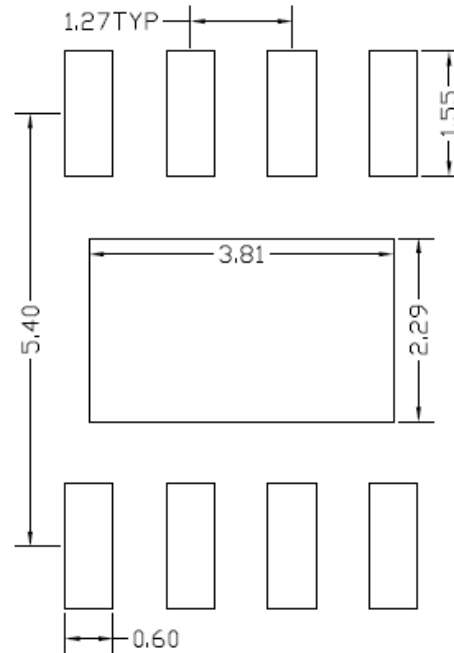
Top view



Side view



Front view

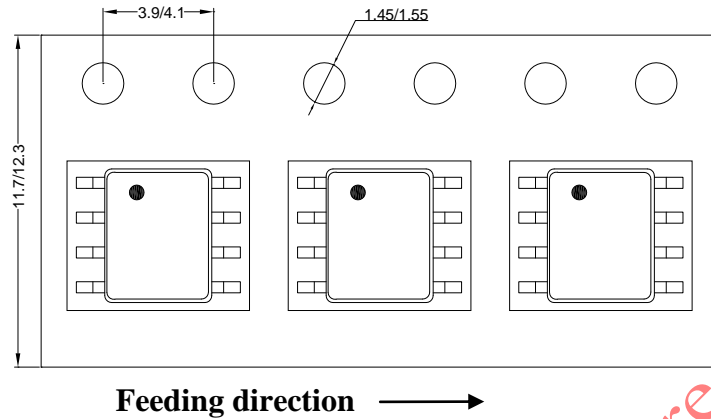


Recommended PCB Layout  
(Reference Only)

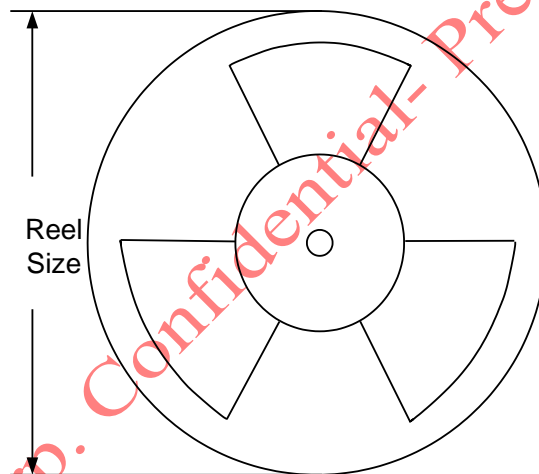
**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Taping & Reel Specification

### 1. Taping orientation SO8E



### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8E	12	8	13"	400	400	2500

### 3. Others: NA

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