M1220

16V Input, 20A Step-down DC-DC Power SoC with Integrated Inductor

FEATURES

- Wide Input Voltage from 2.4V to 16V
  - 2.4V to 16V with External 3.3V VCC Bias
  - 3.5V to 16V with Internal VCC Bias
- Adjustable Output Voltage from 0.6V to 5.5V
- Continuous Output Current
  - Output <1.5V, 20A Continuous
  - Otherwise, 15A Continuous, 20A Peak Output Current
- Constant On Time (COT) Control
- Stable with low ESR Ceramic Capacitors
- Selectable Switching Frequency from 600kHz, 800kHz and 1MHz
- Selectable Power Saving Mode (PSM) or Forced Continuous Conduction Mode (FCCM) for Light Load
- Pre-Biased Start-Up
- Differential Output Voltage Sense
- Output Voltage Discharge
- Power Good Indicator
- Junction Temperature Range from −40°C to 125°C
- Programable Soft-Start Time
- Programable Output Current Limit
- Cycle-by-Cycle Output Current Limit
- Hiccup Mode for Short Circuit and Over-Load Protection
- Thermal Shutdown Protection
- Over-Voltage Protection
- QFN-29 (7mm×7mm×3.95mm) Package
- Pb-Free RoHS Compliant

DESCRIPTION

The M1220 is a 15A Continuous, 20A Peak step-down switching mode Power SoC (System on Chip) with integrated controller, power MosFETs, inductor and input decoupling capacitor in QFN-29 package. The input voltage is from 2.4V to 16V and the output voltage is adjustable from 0.6V to 5.5V. The M1220 also has flexible programable functions such as the soft-start time and output current limit. And the switching frequency is selectable from 600kHz, 800kHz and 1MHz.

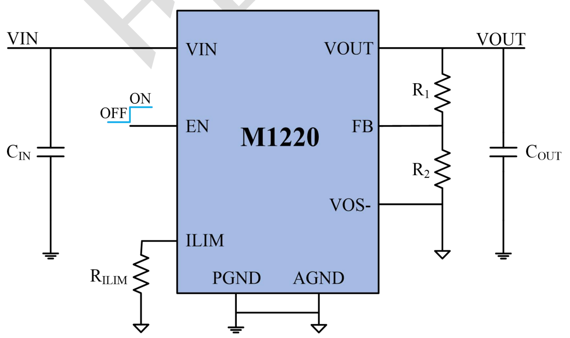
The M1220 provides high efficiency with Constant On Time (COT) control mode for fast transient response and good loop stability. It can work on selectable Power Saving Mode (PSM) or Forced Continuous Conduction Mode (FCCM) for light load with excellent load regulation and line regulation.

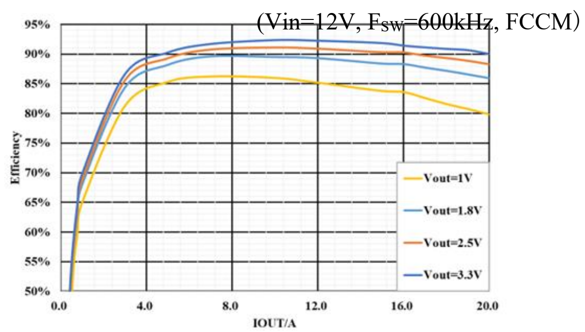
The M1220 can also indicate faults and provide over-load and short circuit hiccup protection, UVP, OVP and OTP protection.

APPLICATIONS

- Telecom Systems
- Servers & Data Centers
- FPGA & ASIC Cards
- Industrial Systems

TYPICAL APPLICATION&EFFICIENCY



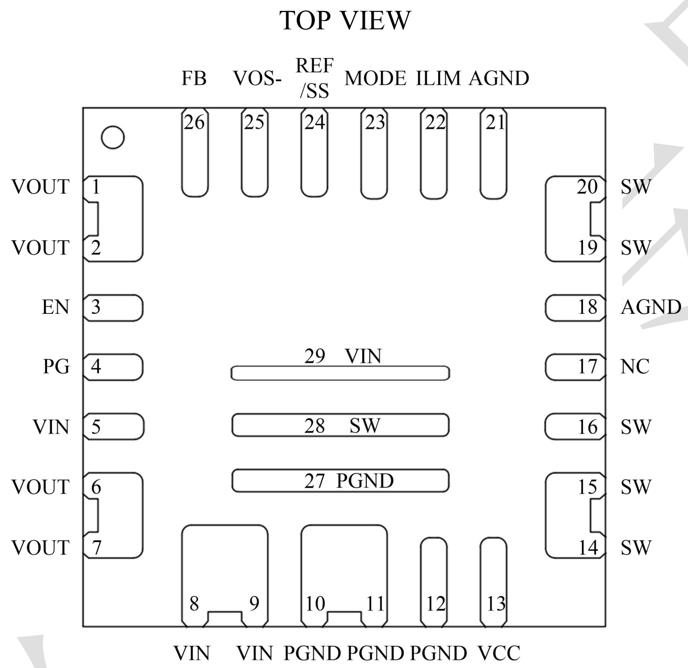


ORDERING INFORMATION

PART NUMBER	TOP MARKING	PACKAGE	MOQ	MSL
M1220DQEE	M1220 YWWLLL	QFN-29 (7mm×7mm×3.95mm)	1000/ Tape & Reel	3

NOTES: Y: Year, WW: Week, LLL: Lot Number.

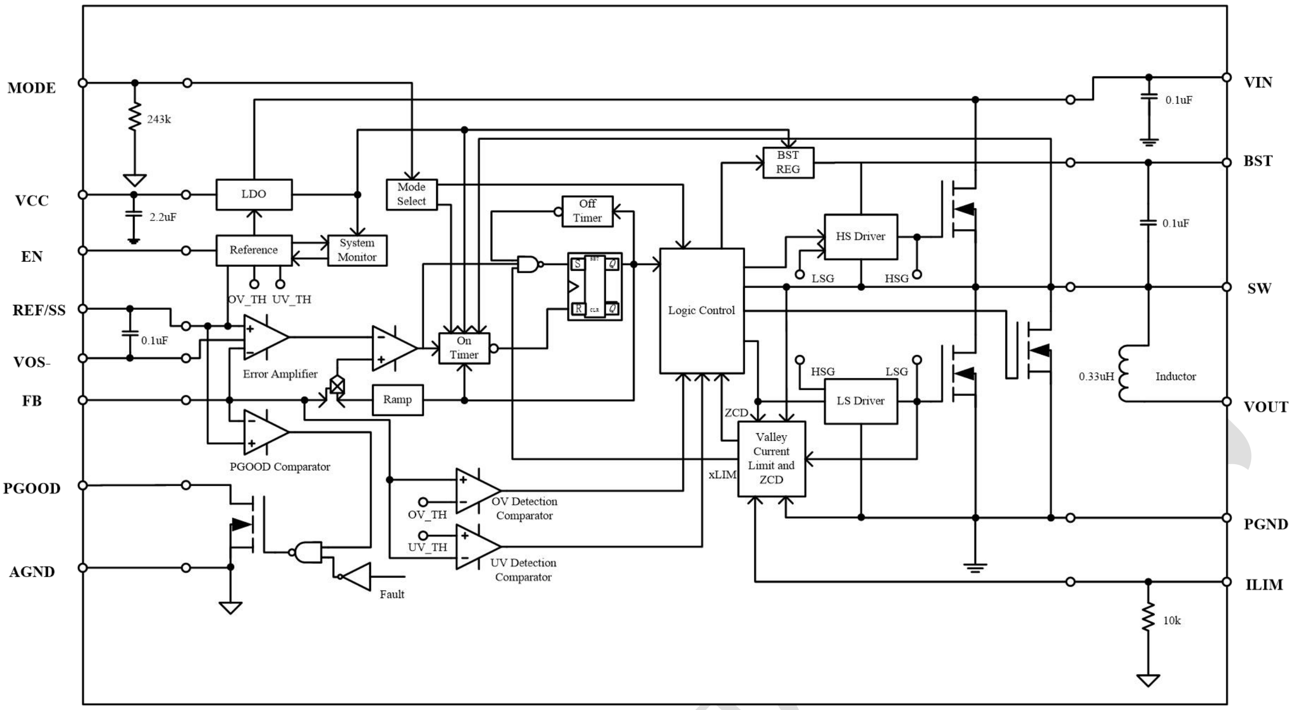
PACKAGE REFERENCE



PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1,2,6,7	VOUT	**Output Voltage.** Connect this pin with the load. Output capacitor is recommended to be placed between VOUT and PGND.
3	EN	**Enable Control.** Pulling this pin low can shut down the chip. Pulling it up can enable the chip.
4	PG	**Power Good.** The output of PG is an open drain, a pull-up resistor to power source is needed if used. If the chip works normally, PG is pulled high, else, PG is latched low.
5,8,9,29	VIN	**Input Voltage.**
10,11,12,27	PGND	**Power Ground.**
13	VCC	**Not Connected. Internal 4.8V LDO Output.** An output capacitor to AGND has been placed internally.
14,15,16,19,20,28	SW	**Not Connected. Internal SW Pad.**
17	NC	**Not Connected. Internal Bootstrap Pad.** A Bootstrap capacitor to SW has been placed internally.
18,21	AGND	**Analog Ground.**
22	ILIM	**Output Current Limit.** Connect a resistor to AGND to program the current limit.
23	MODE	**Operation Mode Selection.** Connect a resistor to AGND to program the operation mode and the switching frequency. This pin is floating for PSM and 600kHz as the default status.
24	REF/SS	**Output Voltage Tracking Reference/Soft Start.** The output voltage tracks this input signal. A decoupling ceramic capacitor is recommended to be placed close to this pin. The capacitance determines the soft-start time.
25	VOS−	**VOUT Sense−.** Connect to the negative side of the voltage sense point directly. Connect to AGND if not used.
26	FB	**Feedback (VOUT Sense+).** Connect this pin with an external resistor divider from the output to VOS- and keep them as close as possible to the pin.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	SYMBOL	MIN	MAX	UNIT
Voltage at V_{IN} Pins	V_{IN}	−0.3	20	V
Voltage at SW Pins	V_{SW}(DC)	−0.3	20	V
Voltage at SW Pins	V_{SW}(25ns)	−5	25	V
Voltage at VCC Pins	VCC	−0.3	5.5	V
Voltage at Other Pins		−0.3	5.5	V
Junction Temperature Range	T_J	−40	125	℃
Storage Temperature Range	T_S	−55	150	℃
Power Dissipation (T_A=+25℃)	P_D Notes 1)		5.9	W

ESD Ratings

ESD	STANDARD	VALUE
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	1500V
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101F	2000V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNIT
Input Voltage Range	V_{IN}	3.5	16	V
Output Voltage Range	V_{OUT}	0.6	5.5	V
Output Current Range	I_{OUT}		20	A
EN Voltage Range	V_{EN}		4.5	V
Junction Temperature Range	T_J	−40	125	℃

THERMAL RESISTANCE

	SYMBOL	MIN	MAX	UNIT
Junction to Ambient	θ_{JA} Notes 2)		17	℃/W
Junction to Case	θ_{JC} Notes 2)		1	℃/W

NOTES:

1) The maximum allowable continuous power dissipation at any ambient temperature (T_A) is calculated by $P_D(max)=(T_J(max)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the power module will go into thermal shutdown.
2) Measured on EVB, 6-layer PCB 2oZ.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_A=25°C, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	with Internal LDO	3.5		16	V
Input Voltage	V_{IN}	with External VCC Bias	2.4		16	V
VIN Hysteresis			500	600	700	mV
Shutdown Current	I_{SD}	V_{EN}=0V		7	10	µA
Quiescent Current (No Switching)	I_{Q1}	V_{EN}=2V, V_{FB}=1V		1950		µA
Quiescent Current (No Load)	I_{Q2}	V_{IN}=12V, V_{OUT}=1.2V, PSM			2	mA
EN On Threshold	V_{EN_R}	V_{EN} Rising	1.0	1.22	1.4	V
EN Hysteresis			150	200	250	mV
Soft Discharge FET Resistance	R_{ON_DIS}		150	180	200	Ω
VCC under Voltage Lockout rising Threshold	VCC_{UVLO_R}	V_{CC} Rising	2.5	3.0	3.5	V
VCC Hysteresis			0.2	0.3	0.5	V
VCC Regulator	VCC	5.3V<V_{IN}<16V	4.5	4.8	5.1	V
VCC Output Current Limit			25			mA
VCC Load Regulation		I_{VCC}=25mA			2.2	%
Feedback Voltage	V_{FB_REF}		594	600	606	mV
Current Limit	V_{ILIM}		0.9	1.2	1.5	V
I_{ILIM} to I_{OUT} Ratio	I_{ILIM}/I_{OUT}		9.5	10	11	µA/A
LS Negative Current Limit			−8	−10	−13	A
Switching Frequency	F_{SW}	MODE=AGND/VCC	500	600	700	kHz
		MODE=Float/34.8kΩ	700	800	900	kHz
		MODE=243kΩ/80.6kΩ	900	1000	1100	kHz
Soft-Start Time	T_{SS}	C_{REF}=1nF	1.2	1.5	1.8	ms
REF/SS sourcing current	I_{REF_SO}		32	36	52	µA
REF/SS sinking current	I_{REF_SI}		9	12	20	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25°C, unless otherwise noted.

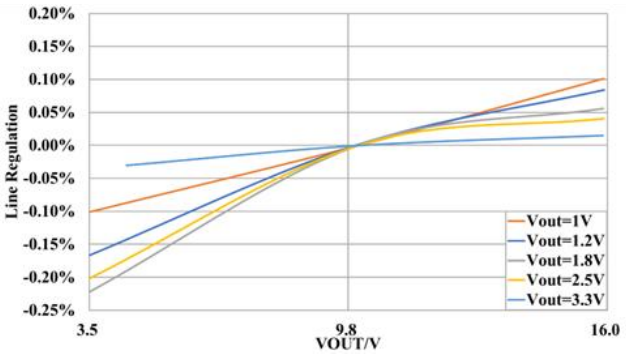
PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
PG High Threshold	V_{PGH_R}	V_{FB} Rising, V_{FB} in respect to V_{FB_REF}, VOUT < Target	85	92.5	95	%
PG Low Threshold	V_{PGL_F}	V_{FB} Falling, V_{FB} in respect to V_{FB_REF}, VOUT < Target	65	70	75	%
	V_{PGL_R}	V_{FB} Rising, V_{FB} in respect to V_{FB_REF}, VOUT > Target	112	116	120	%
PGOOD Leakage Current VPG=3.3V					2.66	uA
PGOOD Low-Level Output Voltage		VIN=0V, 10KΩ Pull up		0.8	1	V
Over-Voltage Protection	V_{OVP}	V_{FB} in respect to V_{FB_REF}	113	116	119	%
		LS OFF Threshold		50		%
Under Voltage Protection	V_{UVP}	V_{FB} in respect to V_{FB_REF}	77	80	83	%
Thermal Shutdown				160		°C
Thermal Shutdown Hysteresis				30		°C

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, T_A=25°C, FCCM, F_{SW}=600kHz, V_{OUT}=1.2V, unless otherwise noted.

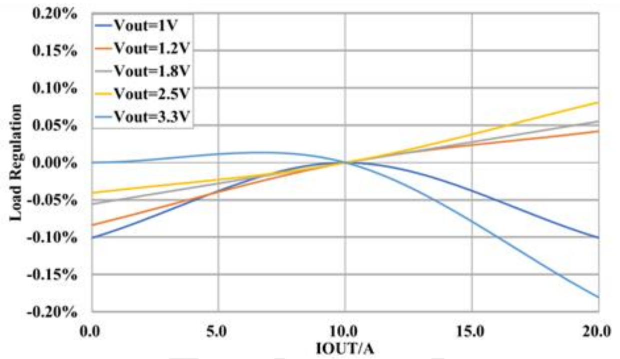
Line Regulation

V_{OUT}=1V/1.2V/1.8V/2.5V/3.3V, I_{OUT}=15A, V_{IN}=3.5~16V



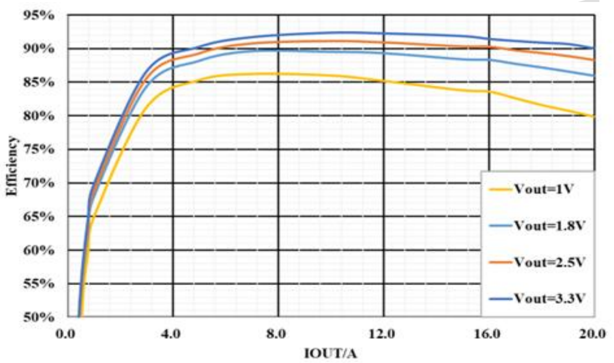
Load Regulation

V_{IN}=12V, V_{OUT}=1V/1.2V/1.8V/2.5V/3.3V, I_{OUT}=0~20A



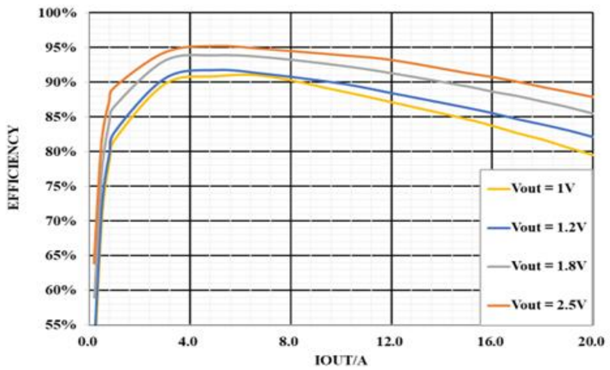
Efficiency

V_{IN}=12V, V_{OUT}=1V/1.8V/2.5V/3.3V, I_{OUT}=0~20A



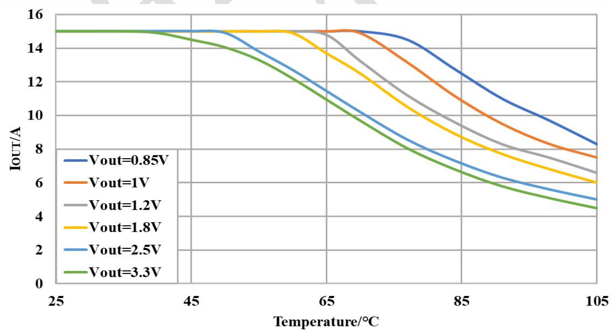
Efficiency

V_{IN}=5V, V_{OUT}=1V/1.2V/1.8V/2.5V, I_{OUT}=0~20A



Thermal Derating

V_{IN} = 12V, V_{OUT}=0.85V/1V/1.2V/1.8V/2.5V/3.3V

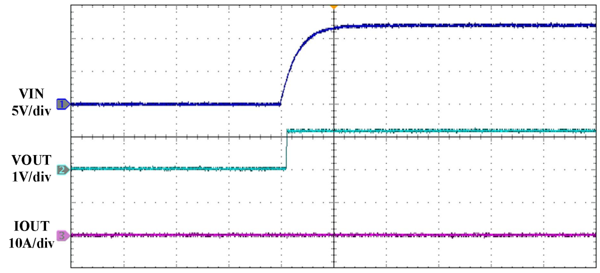


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25°C, FCCM, F_{SW}=600kHz, V_{OUT}=1.2V, unless otherwise noted.

VIN Start-up

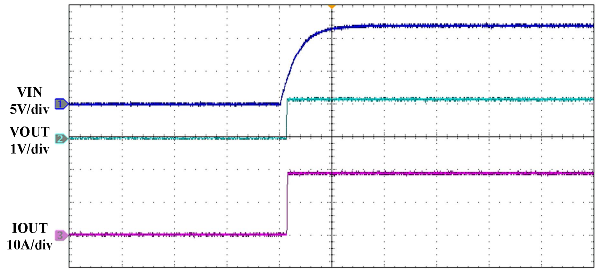
I_{OUT}=0A



100ms/div

VIN Start-up

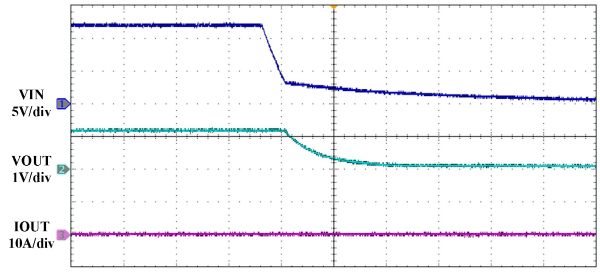
I_{OUT}=20A



100ms/div

VIN Shutdown

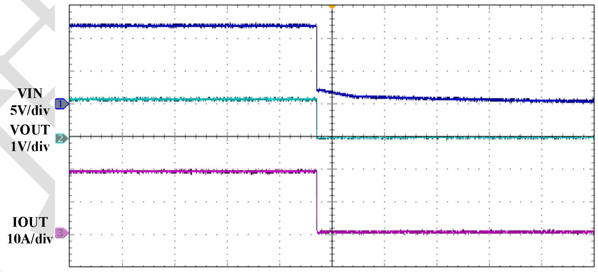
I_{OUT}=0A



100ms/div

VIN Shutdown

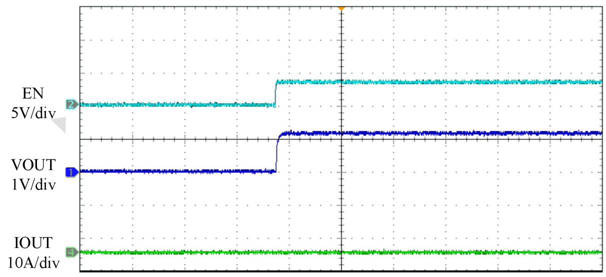
I_{OUT}=20A



100ms/div

EN Start-up

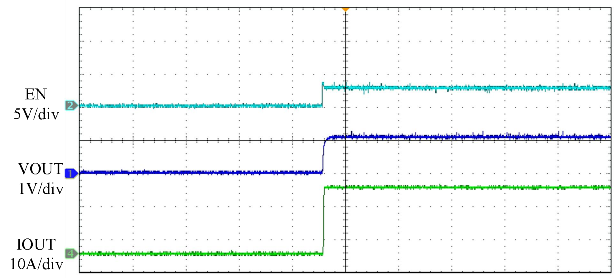
I_{OUT}=0A



100ms/div

EN Start-up

I_{OUT}=20A



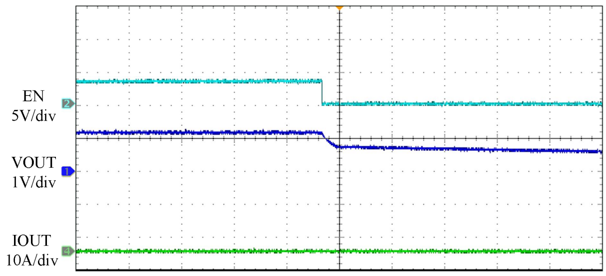
100ms/div

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25°C, FCCM, F_{SW}=600kHz, V_{OUT}=1.2V, unless otherwise noted.

EN Shutdown

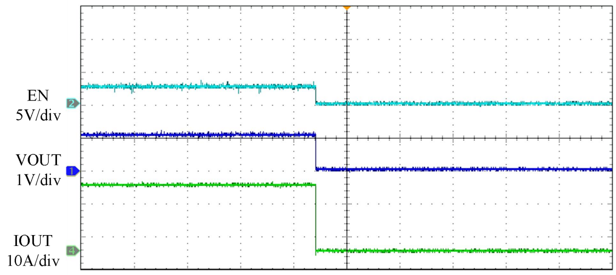
I_{OUT}=0A



100ms/div

EN Shutdown

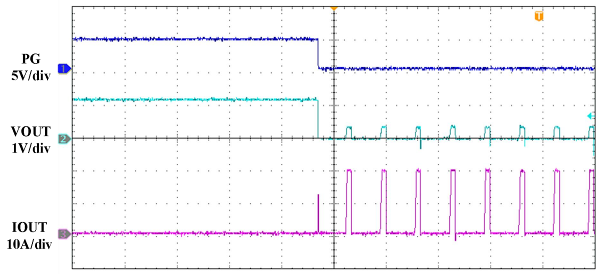
I_{OUT}=20A



100ms/div

SCP Entry

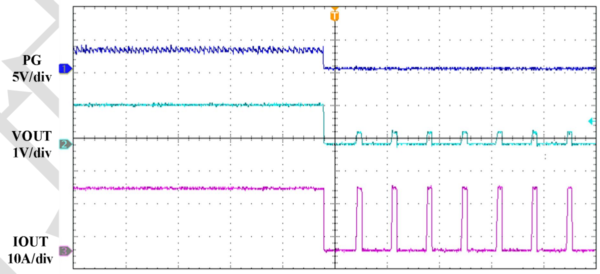
I_{OUT}=0A



20ms/div

SCP Entry

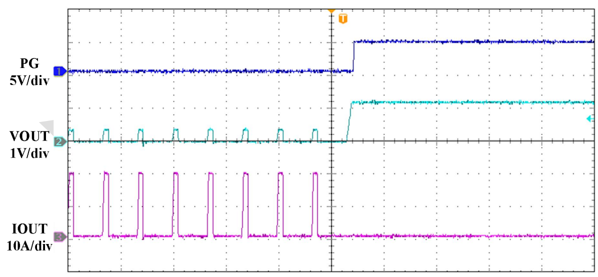
I_{OUT}=20A



20ms/div

SCP Recovery

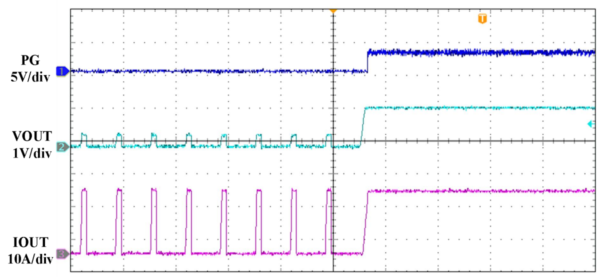
I_{OUT}=0A



20ms/div

SCP Recovery

I_{OUT}=20A



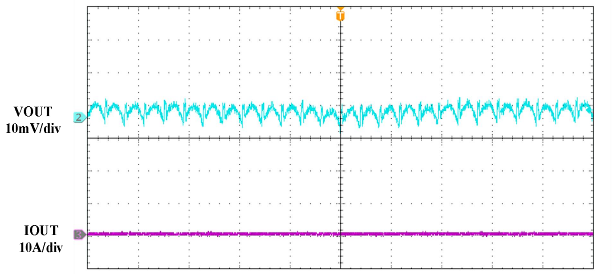
20ms/div

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25°C, FCCM, F_{SW}=600kHz, V_{OUT}=1.2V, unless otherwise noted.

VOUT Ripple

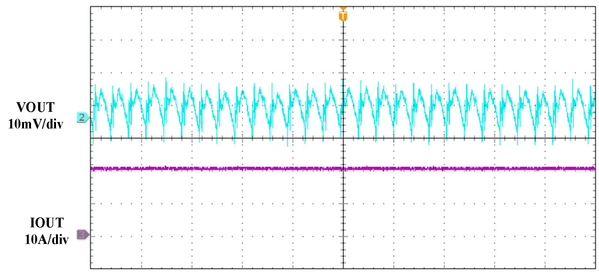
I_{OUT}=0A



4us/div

VOUT Ripple

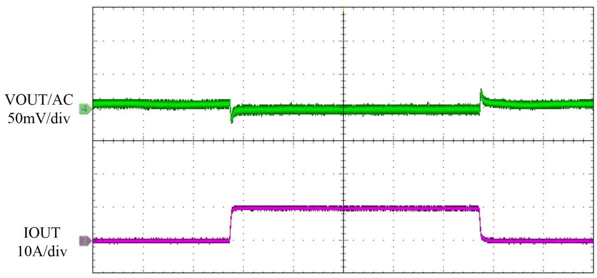
I_{OUT}=20A



4us/div

Load Transient

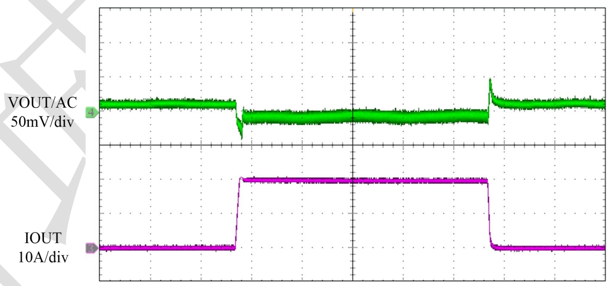
I_{OUT}=0A to 10A, 2.5A/µs



200µs/div

Load Transient

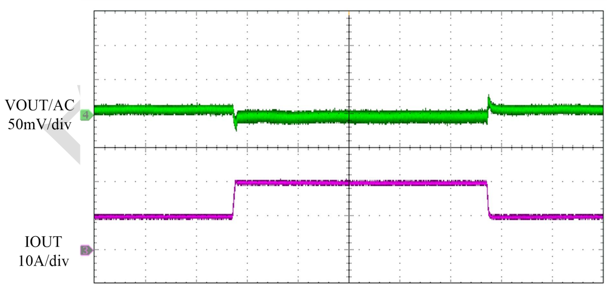
I_{OUT}=0A to 20A, 2.5A/µs



200µs/div

Load Transient

I_{OUT}=10A to 20A, 2.5A/µs



200µs/div

OPERATION

The M1220 is a 15A Continuous, 20A Peak synchronous step-down switching mode Power SOC with integrated high-side and low-side power MosFETs, inductor and input decoupling capacitor in QFN-29 package. And the integrated input decoupling capacitor can minimize the parasitic inductance of input circuit and reduce the voltage spike on switching pin which simplify the PCB layout.

M1220 works on COT control mode that offers excellent transient response over a wide input voltage range. M1220 can provide excellent load regulation both Power Saving Mode and Forced Continuous Conduction Mode for light load, which can be programmed by MODE pin. The switching frequency can also be programmed from 600kHz, 800kHz and 1MHz.

Fully integrated protection features include OCP, OVP, UVP and OTP and all these faults can be indicated by PG. The protection function details are shown below.

OVER CURRENT PROTECTION (OCP)

M1220 has a cycle-by-cycle Low-Side valley current limit protection to prevent inductor current from running away. This current limit value can be programmed as shown in the **USER GUIDE**. When the Low-Side switch reaches the current limit, M1220 will enter hiccup mode.

OCP hiccup mode is active 3ms after M1220 is enabled. If M1220 detects an over-current condition for 31 consecutive cycles, or if V_{FB} drops below the UVP threshold, the device enters hiccup mode. Both High-side and Low-side MosFETs latch off in hiccup mode. The REF/SS capacitor is also discharged. M1220 automatically tries to soft start after about 11ms.

If the over-current condition remains after 3ms of running, the M1220 repeats this operation cycle until the over-current condition disappears..

OVER VOLTAGE PROTECTION (OVP)

M1220 monitors the output voltage by connecting FB to the net between the output voltage feedback resistors to detect an over-voltage condition. If V_{FB} exceeds 116% of V_{FB_REF}, it triggers OVP. High-Side MosFET turns off and the Low-Side MosFET turns on until reaching a negative current limit during this period. The Low-Side MosFET is turned off for 200ns upon reaching the negative current limit. After 200ns the Low-Side MosFET turns on. The M1220 operates in this cycle until the output voltage is pulled down below 50% of the program point value.

The M1220 also employs output sinking mode (OSM) to regulate the output voltage to the targeted value when V_{FB} exceeds 104% of V_{FB_REF} but is below the OVP threshold. During OSM, the Low-Side MosFET remains on until it reaches the negative current limit. Upon reaching, the Low-Side MosFET turns off for 200ns and the High-Side MosFET turns on during this period. After 200ns, the Low-Side switch turns on. The M1220 maintains this operation until V_{FB} drops below 102% of V_{FB_REF}. Once it does, the M1220 exits OSM after 15 consecutive cycles of FCCM.

OVER TEMPERATURE PROTECTION (OTP)

M1220 will stop switching when the junction temperature exceeds typically 160 °C. The device will power up again when the junction temperature drops below typically 130°C.

USER GUIDE

Output Voltage

The output voltage is programmed by the external feedback resistors as the typical application circuit on Page 1. The top feedback resistor R_1 can impact the loop stability. The bottom feedback resistor R_2 can be calculated as:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

Table 1 lists the recommended feedback resistor values for common output voltages. The values of feedback resistors are recommended to be less than 20kΩ. And a feedforward resistor R_{FF} and capacitor C_{FF} are recommended for better load transient response.

Table 1: FB Resistor Value for Common Output Voltages.

V_{OUT}	R_1	R_2
5V	8.2kΩ	1.1kΩ
3.3V	8.2kΩ	1.8kΩ
1.8V	4.02kΩ	2kΩ
1.2V	4.02kΩ	4.02kΩ
1.0V	2kΩ	3kΩ

Input Capacitor Selection

The input current of the step-down converter is discontinuous with sharp edges; therefore, putting filter capacitors is necessary. For better performance, low ESR ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their lowest temperature variations. The RMS current of the input capacitors is calculated:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

in which D is the Duty Cycle and when the current is continuous, $D=V_{OUT}/V_{IN}$; I_{OUT} is the output load current. As the equation above, when D is 0.5, the highest RMS current is approximately:

$$I_{CIN\_RMS} = \frac{I_{OUT}}{2}$$

So, it is recommended to choose the capacitors with the RMS current rating higher than 1/2 I_{OUT}.

The power dissipation on the input capacitors can be estimated with the RMS current and the ESR resistance.

Electrolytic or tantalum capacitors can also be used. There has been a small size 0.1μF ceramic capacitor placed close to VIN and PGND in M1220 already. The input voltage ripple caused by the capacitors can be calculated as.:

$$\Delta V_{CIN} = \frac{I_{OUT}}{F_{SW} \cdot C_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

in which, FSW is switching frequency.

Output Capacitor Selection

Output capacitors are required to keep output voltage stable. To minimize the output voltage ripple, low ESR ceramic capacitors should be used. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \cdot F_{SW}{}^2 \cdot C_{OUT} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In which, L=0.33μH.

If electrolytic or tantalum capacitors are used, the ESR will dominate the output voltage ripple as:

$$\Delta V_{OUT} = R_{ESR} \cdot \frac{V_{OUT}}{F_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Enable Control

When input voltage is above the under-voltage-lock-out threshold, M1220 can be enabled by pulling the EN pin.

- EN can be driven by a logical signal to enable M1220. M1220 can be enabled by pulling the EN pin to above 1.22V, but under 4.5V.
- The EN is programmed by the external resistors R_{PULL_UP} and R_{PULL_DOWN} as the typical application circuit on figure 2. The V_{EN} is calculated:

$$V_{EN} = \frac{R_{PULL\_DOWN}}{R_{PULL\_UP} + R_{PULL\_DOWN}} \cdot VIN$$

For example, if VIN=12V, the R_{PULL_UP} is 499 kΩ, the R_{PULL_DOWN} is 200 kΩ, so the V_{EN} is 3.4V.

Power Good Indicator

M1220 has an open drain PG indicator. A pull-up resistor to VCC or any other power source less than

3.6V is needed if used and its recommended value is about 100kΩ. PG will be pulled down when the output voltage is out of regulation, otherwise PG is pulled up. PG goes high after a 0.9ms delay when the output voltage becomes within ±7.5% of the target value. The PG is latched low when VFB drops to 80% or exceeds 116% of the regulation and will be pulled high after a new soft start.

Mode Selection & Switching Frequency

M1220 can work on FCCM or PSM mode under the light load by selecting different resistors connected with MODE pin. PSM mode means **M1220 works at DCM under light load. FCCM mode means M1220 is forced to work at CCM under light load.** And the switching frequency is also programmed by this pin. Table 2 shows the values of the resistors for different operating modes and switching frequency.

Table 2: Mode & Switching Frequency Selection

Mode	Light-Load Mode	F_{SW}
VCC (Default)	PSM	600kHz
Float	PSM	800kHz
243kΩ (±10%) to AGND	PSM	1000kHz
AGND	FCCM	600kHz
34.8kΩ (±10%) to AGND	FCCM	800kHz
80.6kΩ (±10%) to AGND	FCCM	1000kHz

Current Limit

M1220 features a current sense and a configurable current limit threshold. By using a resistor (R_{ILIM}) from ILIM to AGND, the current limit is program as:

$$\frac{R_{ILIM}(M\Omega) \times 0.01}{R_{ILIM}(M\Omega) + 0.01} = \frac{V_{ILIM}}{G_{CS} \cdot (I_{ILIM} - \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \cdot \frac{1}{2F_{SW}(MHz) \cdot L(\mu H)})}$$

in which, V_{ILIM} =1.2V, G_{CS} =10μA/A, L=0.33μH.

Table 3 shows the recommended values of the resistor R_{ILIM} for different operating modes.

Table 3: R_{ILIM} & Operation

Operation	F_{SW}	I_{LIM}(TYP)	R_{ILIM}
V_{IN}=12V, V_{OUT}=5V	600kHz	18A	NC
V_{IN}=12V, V_{OUT}=3.3V	600kHz	19A	140kΩ
V_{IN}=12V, V_{OUT}=1.8V	600kHz	20A	28kΩ
V_{IN}=12V, V_{OUT}=1.2V	600kHz	20A	22kΩ
V_{IN}=12V, V_{OUT}=1V	600kHz	20A	21kΩ

Soft Start Time

M1220 has 1.5ms default soft-start time internally. The time can be increased by adding an external capacitor C_{SS} between REF/SS and AGND. C_{SS} can be calculated as:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \cdot 36(\mu A)}{0.6(V)} - 100(nF)$$

VIN Pin High Frequency Bypass and Snubber Circuit Recommendation

To operate the M1220 within absolutely maximum ratings without ringing issue, some reduction techniques may require external components to further ringing levels. A lossless way is using a high frequency bypass capacitor on the VIN pins by minimizing the power loop parasitic inductances. A 4.7nF capacitor still be recommended to be connected to 29 PIN. As the placement of this capacitor is critical to its effectiveness， the ideal placement is shown in PCB layout guidelines.

A R-C snubber circuit can also be recommended to achieve a lower ringing level. As a reference, two 2Ω resistors in parallel and 1nF capacitor between SW and PGND are recommended.

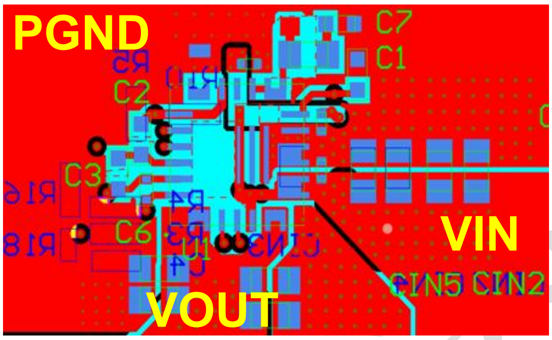
PCB Layout Guide

To optimize the electrical and thermal performance, some PCB layout guidelines should be considered as below:

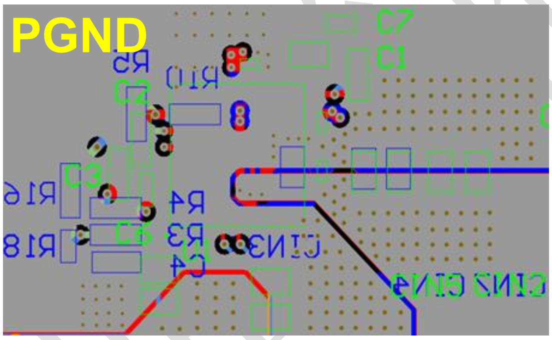
1. Use wide trace for the high current paths and keep it as short as possible. It helps to minimize the PCB conduction loss and thermal stress.

2. The M1220 has integrated the input decoupling capacitor, and **it is also recommended to place other input decoupling capacitors close to VIN and PGND to minimize the power loop as shown as (f)**.
3. Connect all feedback network to FB shortly.
4. Keep the sensitive components away from the SW.
5. The PGND should be connected to a strong ground plane for better heat dissipation and noise protection.
6. M1220 supports remote voltage sense to compensate any voltage drop in the leads/traces. Make Sure that differential lines are used to do Output Voltage Sense from capacitor terminals.

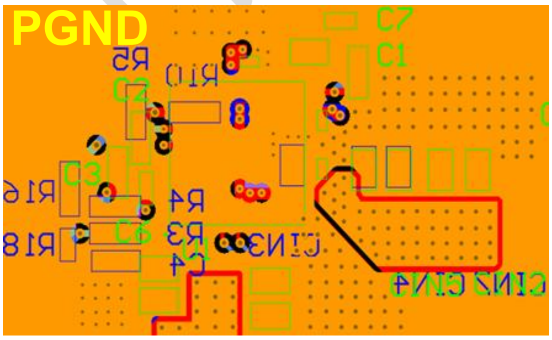
Figure 1 gives a good example of the recommended layout.



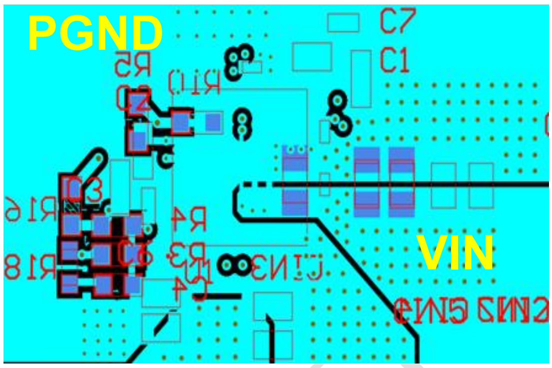
(a) Top Layer



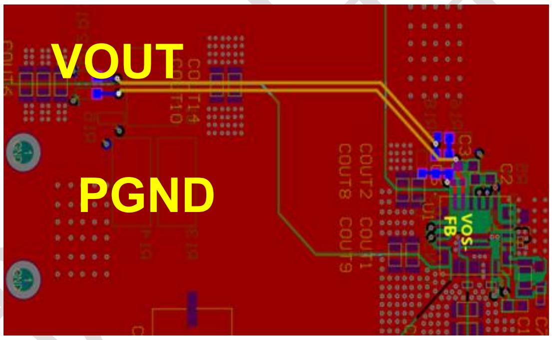
(b) Inner Layer 2



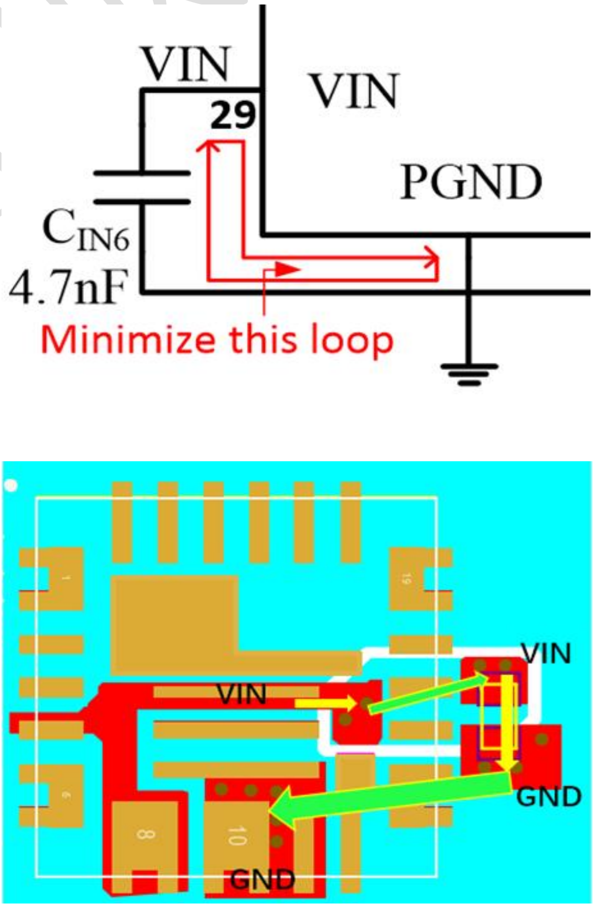
(c) Inner layer 1/3/4



(d) Bottom Layer



(e) Remote Sense Traces



(f) Input Decoupling Cap

Figure 1. Recommended Layout

TYPICAL APPLICATION

- **VIN=12V**

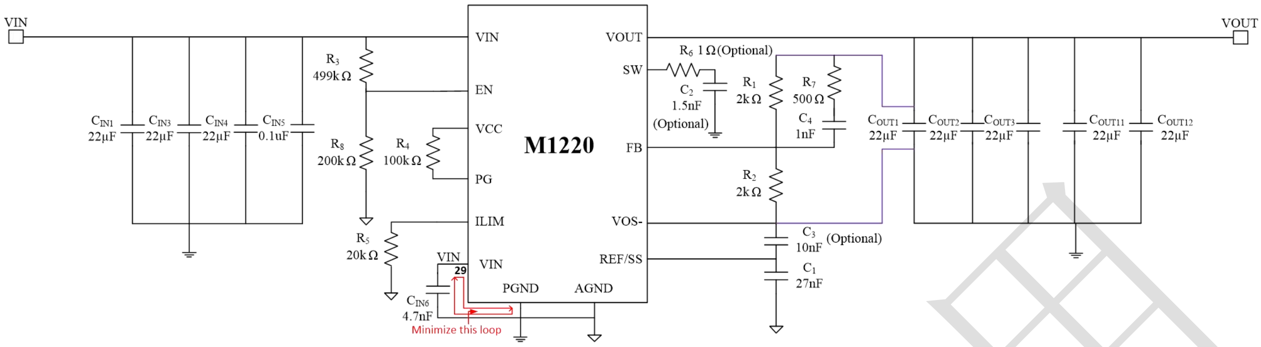


Figure 2. Typical Application Circuits of M1220 for 12V Input 1.2V@20A Output, Fsw=600kHz

NOTES:

1) R_6 and C_2 are Snubber circuit to minimize ringing level, which are not connected (**NC**) if not used.

2) R_7 and C_4 are forward network to improve transient response ability, which are optional.

Table 4: M1220 Reference Design for 12V Input

VOUT	CIN	COUT	Vout Ripple	R_1	R_2	R_5	I_{LIM} TYP (Fsw=600kHz)
5.0V	3×22uF	8×22uF	67mV(15A)	8.2kΩ	1.1kΩ	NC	18A
3.3V	3×22uF	8×22uF	50mV(15A)	8.2kΩ	1.8kΩ	140kΩ	19A
1.8V	3×22uF	8×22uF	30mV(20A)	4.02kΩ	2kΩ	28kΩ	20A
1.2V	3×22uF	8×22uF	22mV(20A)	4.02kΩ	4.02kΩ	22kΩ	20A
1.0V	3×22uF	8×22uF	20mV(20A)	2kΩ	3kΩ	21kΩ	20A

NOTES:

CIN is the sum of the input capacitors, COUT is the sum of the output capacitors, please refer to Figure 2 for parameters of other components.

TYPICAL APPLICATION (continued)

- **VIN=5V**

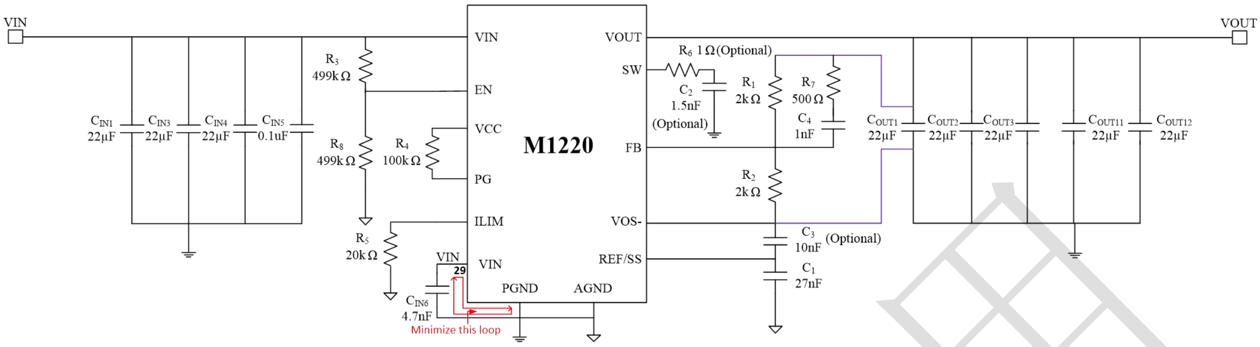


Figure 3. Typical Application Circuits of M1220 for 5V Input 1.2V@20A Output, Fsw=600kHz

NOTES:

1) R_6 and C_2 are Snubber circuit to minimize ringing level, which are not connected (**NC**) if not used.

2) R_7 and C_4 are forward network to improve transient response ability, which are optional.

Table 4: M1220 Reference Design for 5V Input

VOUT	CIN	COUT	Vout Ripple	R1	R2	R5	I_{LIM} TYP (Fsw=600kHz)
3.3V	3×22uF	8×22uF	23mV(15A)	8.2kΩ	1.8kΩ	140kΩ	19A
1.8V	3×22uF	8×22uF	20mV(20A)	4.02kΩ	2kΩ	28kΩ	20A
1.2V	3×22uF	8×22uF	16mV(20A)	4.02kΩ	4.02kΩ	22kΩ	20A
1.0V	3×22uF	8×22uF	14mV(20A)	2kΩ	3kΩ	21kΩ	20A

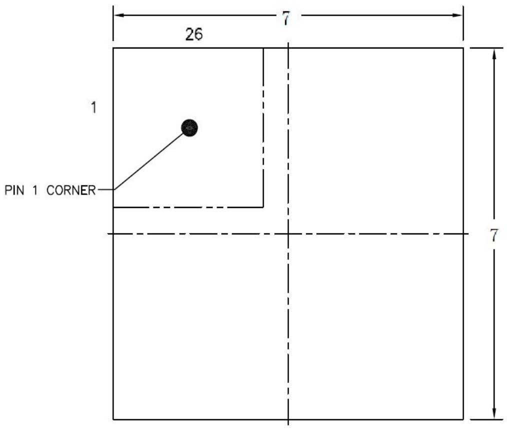
NOTES:

CIN is the sum of the input capacitors, COUT is the sum of the output capacitors, please refer to Figure 3 for parameters of other components.

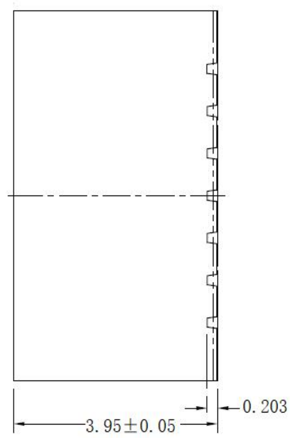
PACKAGE INFORMATION

QFN-29 (7mm×7mm×3.95mm) Package

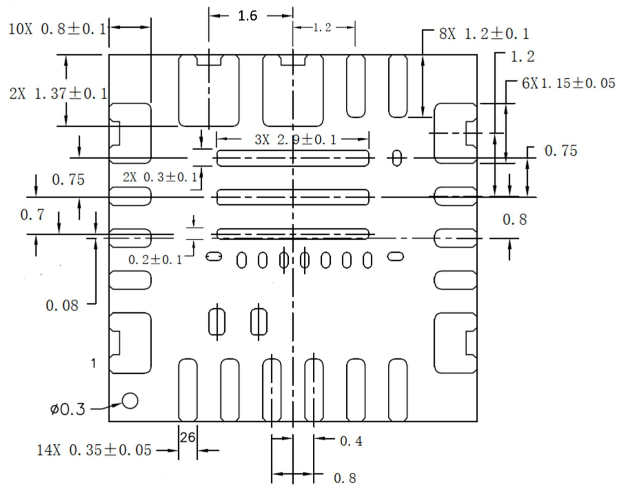
TOP VIEW



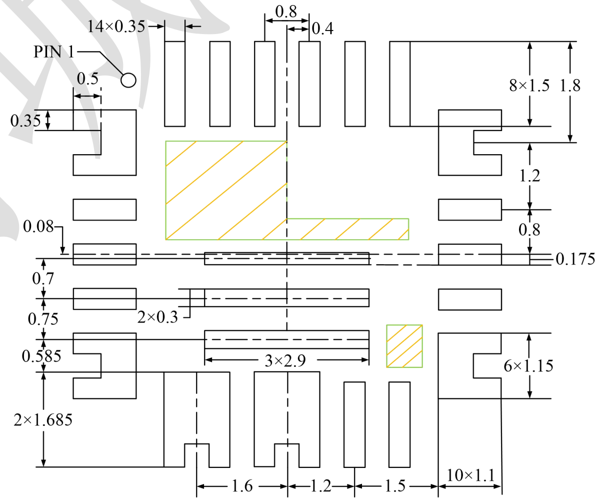
SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

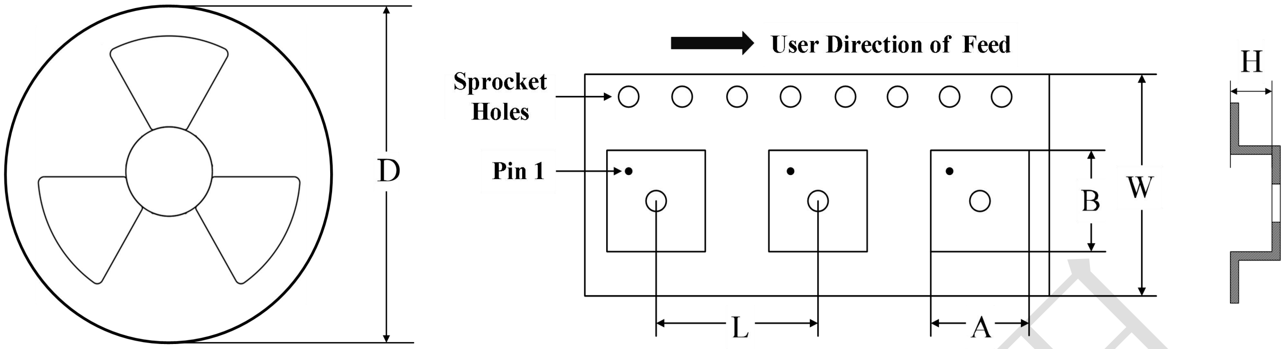


NOTES:

1) All dimensions are in MM.

2) The shaded area is the keep-out zone. Do not connect to any electrical or mechanical area.

CARRIER INFORMATION



PART NUMBER	PACKAGE	QUANTITY /REEL	D	A	B	L	W	H
M1220DQEE	QFN-29 (7mm×7mm×3.95mm)	1000	13 in	7.7mm	7.7mm	12mm	16mm	4.2mm

单击下面可查看定价，库存，交付和生命周期等信息

>>iModule(沃芯)