FEATURES

- Wide Input Voltage Range: 4.5V to 48V
  - Positive Output: Input Voltage Range from 4.5V to 48V
  - Negative Output: VIN ≥ 4.5V; VIN+|VOUT| ≤48V
- Output Voltage
  - Positive Output: Output Voltage Range from 1V to 25V
  - Negative Output: Output Voltage Range from −1V to −15V
- 0.7A Continuous, 1A Peak Output Current
  - Positive Output: 0.7A Continuous, 1A Peak Output Current
  - Negative Output: $\frac{0.7 \times VIN}{VIN+|VOUT|}A$
- Peak Current Control Mode
- 1.6MHz Switching Frequency
- Power Saving Mode (PSM) for Light Load
- High Duty Cycle Operation for Low Dropout
- Pre-Biased Start-Up
- Internal Soft-Start
- Junction Temperature Range: −40℃ to 125℃
- Cycle-by-Cycle Output Current Limit Protection
- Hiccup Mode for Short Circuit and Over-Load Protection
- Thermal Shutdown Protection
- LGA-8 (4mm×4.5mm×1.68mm) Package
- Pb-Free RoHS Compliant

DESCRIPTION

The M4001 is a 0.7A fully integrated power module in LGA-8 package with step-down switching mode Power SoC (System on Chip) with integrated power MOSFETs, inductor and input decoupling capacitor inside. The input voltage is from 4.5V to 48V and the switching frequency is fixed at 1.6MHz.

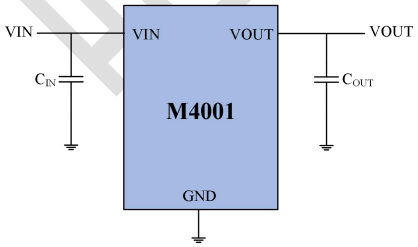
The M4001 provides high efficiency with Peak Current Control Mode. It works on PSM mode for light load and supports high duty cycle for low dropout. Also, M4001 is suitable for negative output.

The M4001 can indicate faults with complete protection features, including over-load hiccup protection and over temperature shutdown protection.

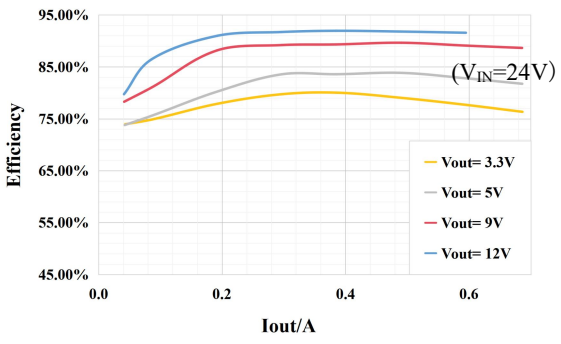
APPLICATIONS

- Power Meter
- Industrial & Medical Systems
- Electrical Tools

TYPICAL APPLICATION&EFFICIENCY



PART NUMBER	Default VOUT
M4001DLCC-5V	5V
M4001DLCC-3V3	3.3V



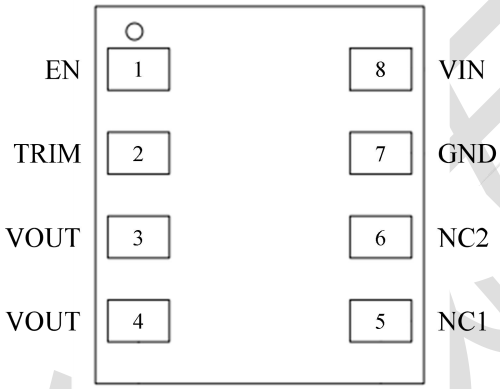
ORDERING INFORMATION

PART NUMBER	TOP MARKING	PACKAGE	MOQ	MSL LEVEL
M4001DLCC-5V	M4001-5V YWWLLL	LGA-8 (4mm×4.5mm×1.68mm)	3000/ Tape & Reel	3
M4001DLCC-3V3	M4001-3V3 YWWLLL	LGA-8 (4mm×4.5mm×1.68mm)	3000/ Tape & Reel	3

NOTES: Y: Year, WW: Week, LLL: Lot Number.

PACKAGE REFERENCE

TOP VIEW

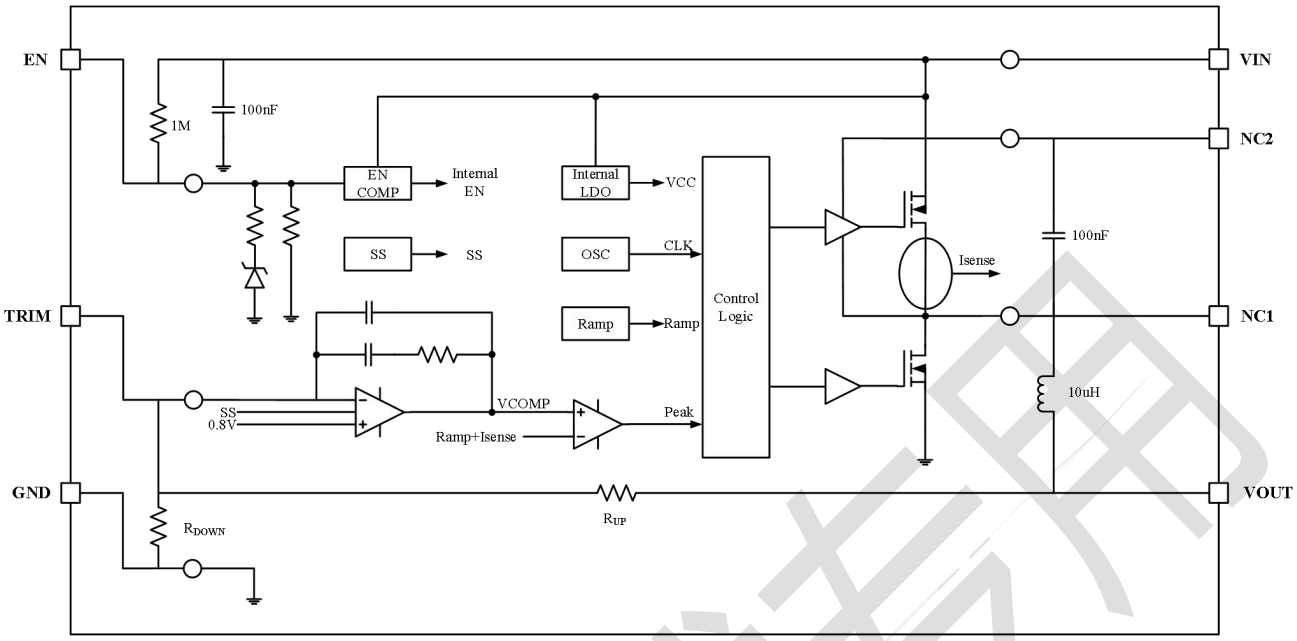


PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1	EN	**Enable Control.** Pull this pin low to shut down the chip. Otherwise, pull it high to enable the chip.
2	TRIM	**Trim.** The resistor divider from the VOUT to GND has been placed internally to set the output voltage. The default output voltage is 3.3V or 5V. An external resistor divider can also be placed to change the output voltage.
3,4	VOUT	**Output Voltage.** Connect this pin with the load. Output capacitor is recommended to be placed between VOUT and GND.
5	NC1	**Not Connected.**
6	NC2	**Not Connected.**
7	GND	**Power Ground.**
8	VIN	**Input Voltage.**

NOTES: All the NC pins should not connect to each other.

FUNCTIONAL BLOCK DIAGRAM



PART NUMBER	Default VOUT	R_{UP}	R_{DOWN}
M4001DLCC-5V	5V	604kΩ	115kΩ
M4001DLCC-3V3	3.3V	604kΩ	191kΩ

ABSOLUTE MAXIMUM RATINGS

	SYMBOL	MIN	MAX	UNIT
Voltage at V_{IN} Pins	V_{IN}	−0.3	50	V
Voltage at Other Pins		−0.3	6	V
Junction Temperature Range	T_J	−40	125	℃
Storage Temperature Range	T_S	−55	150	℃
Solder Reflow Body Temperature Range			245	℃
Power Dissipation (T_A=+25℃)	P_D Notes 1)		0.88	W

ESD Rating

ESD	STANDARD	VALUE
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	4000V
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101F	2000V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNIT
Input Voltage Range	V_{IN}	4.5	48	V
Output Voltage Range	V_{OUT}	1	25	V
Output Current Range	I_{OUT}		0.7	A
Junction Temperature Range	T_J	−40	125	℃

THERMAL RESISTANCE

	SYMBOL	MIN	MAX	UNIT
Junction to Ambient	θ_{JA} Notes 2)		114	℃/W
Junction to Case	θ_{JC} Notes 2)		37	℃/W

NOTES:

1) The maximum allowable continuous power dissipation at any ambient temperature (T_A) is calculated by $P_D(max)=(T_J(max)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the power module will go into thermal shutdown.

2) Measured on EVB, 2-layer PCB 1oZ.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_A=25℃, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		4.5		48	V
Input Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Increasing	4.15	4.3	4.45	V
Input Under Voltage Lockout Hysteresis				335		mV
Shutdown Current	I_{SD}	V_{EN}=0V, V_{IN}=15V		16	18	μA
Quiescent Current	I_Q	V_{Trim}=0.83V, no switching		166	180	μA
EN On Threshold		V_{EN} Increasing	1.5	1.55	1.6	V
EN Off Threshold		V_{EN} Decreasing	1.1	1.22	1.3	V
Trim Voltage	V_{Trim_REF}		785	797	809	mV
Trim Current	I_{Trim}	V_{EN}=1V, V_{Trim}= 2V		21	22	μA
LS Switch Current Limit			0.8	1	1.2	A
Switching Frequency	F_{SW}		1.4	1.6	1.9	MHz
Soft-Start Time	T_{SS}	V_{Trim} from 10% to 90%	0.35	0.6	0.85	ms
Maximum Duty cycle	D			98		%
Thermal Shutdown				151		℃
Thermal Shutdown Hysteresis				21		℃

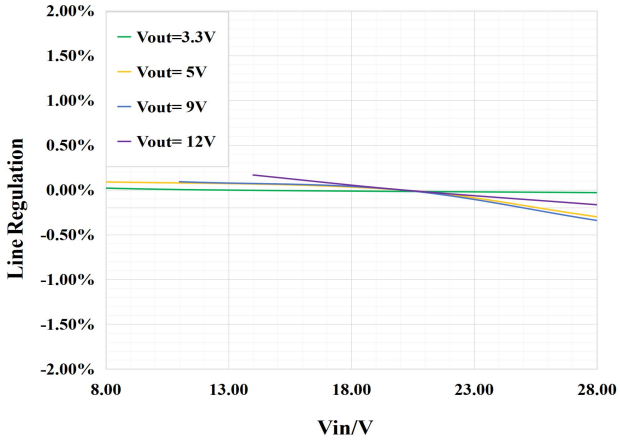
TYPICAL PERFORMANCE CHARACTERISTICS (POSITIVE OUTPUT)

V_{IN}=24V and T_A=25℃, unless otherwise noted.

Line Regulation

V_{OUT}=3.3V/5V/9V/12V, I_{OUT}=0.7A,

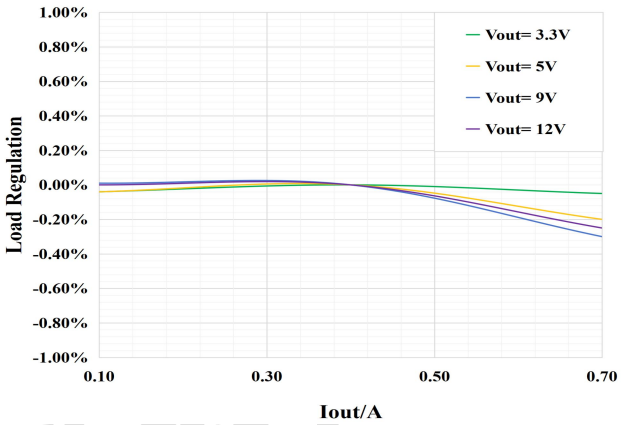
V_{IN}=8V ~ 28V



Load Regulation

V_{IN}=24V, V_{OUT}=3.3V/5V/9V/12V,

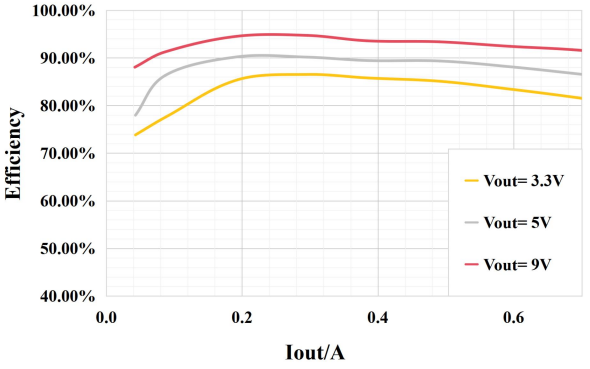
I_{OUT}=0.1A ~ 0.7A



Efficiency

V_{IN}=12V, V_{OUT}=3.3V/5V/9V,

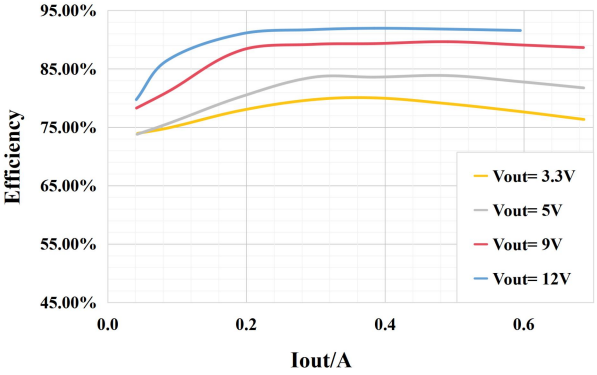
I_{OUT}=0A~0.7A



Efficiency

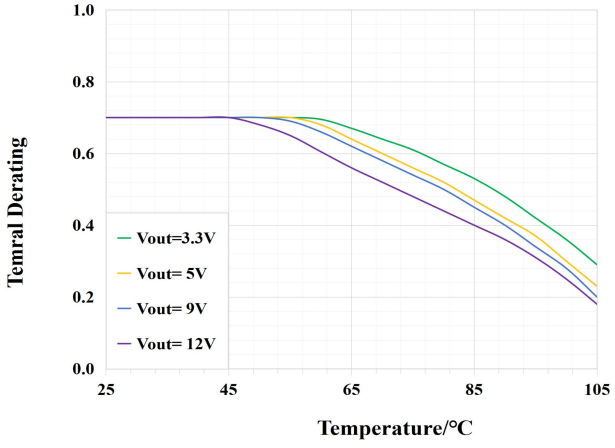
V_{IN}=24V, V_{OUT}=3.3V/5V/9V/12V,

I_{OUT}=0A~0.7A



Thermal Derating

V_{IN}=24V,V_{OUT}=3.3V/5V/9V/12V



TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=24V and T_A=25℃, unless otherwise noted.

Line Regulation

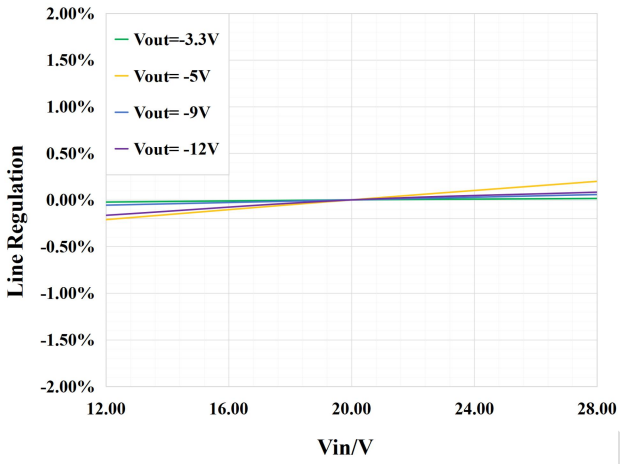
V_{OUT}=−3.3V, I_{OUT}= −0.6A;

V_{OUT}=−5V, I_{OUT}= −0.5A;

V_{OUT}=−9V, I_{OUT}= −0.4A;

V_{OUT}=−12V, I_{OUT}= −0.3A;

V_{IN}=12V~28V



Load Regulation

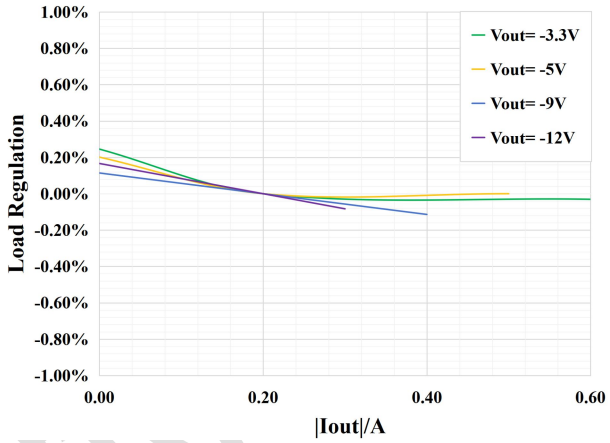
V_{OUT}=−3.3V, I_{OUT}=0A ~ −0.6A;

V_{OUT}=−5V, I_{OUT}=0A ~ −0.5A;

V_{OUT}=−9V, I_{OUT}=0A ~ −0.4A;

V_{OUT}=−12V, I_{OUT}=0A ~ −0.3A;

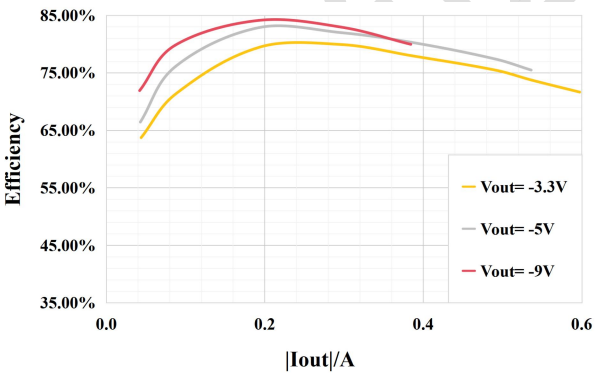
V_{IN}=24V



Efficiency

V_{IN}=12V, V_{OUT}=−3.3V/−5V/−9V,

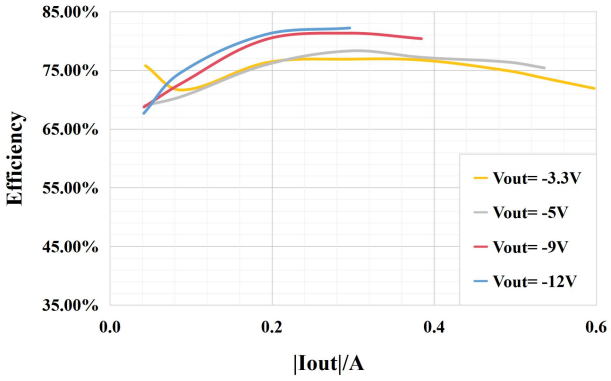
I_{OUT}=0A ~ −0.6A



Efficiency

V_{IN}=24V, V_{OUT}=−3.3V/−5V/−9V/−12V,

I_{OUT}=0A ~ −0.6A

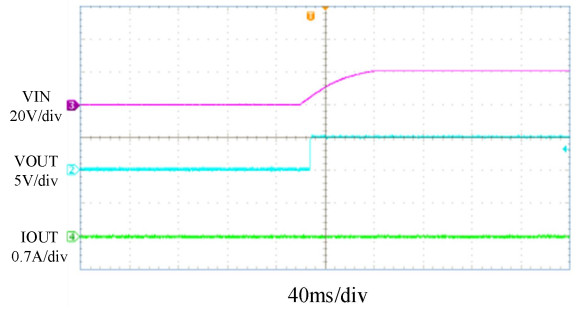


TYPICAL PERFORMANCE CHARACTERISTICS (POSITIVE OUTPUT)

V_{IN}=24V, V_{OUT}=5V, T_A=25℃, unless otherwise noted.

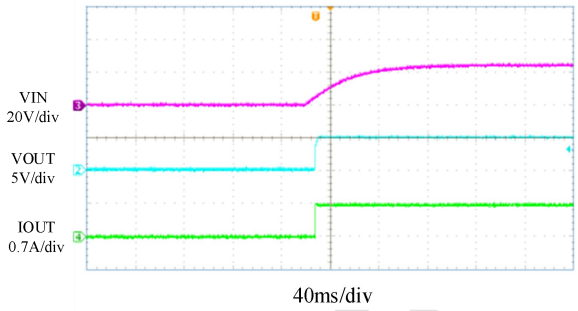
VIN Start-up

I_{OUT}=0A



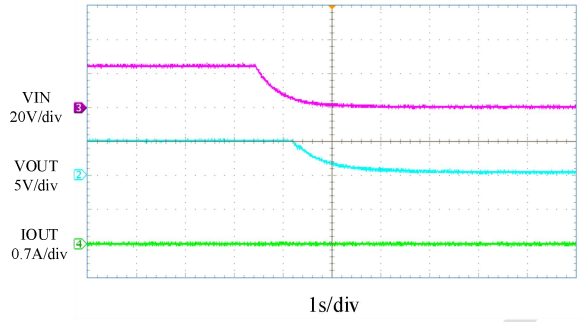
VIN Start-up

I_{OUT}=0.7A



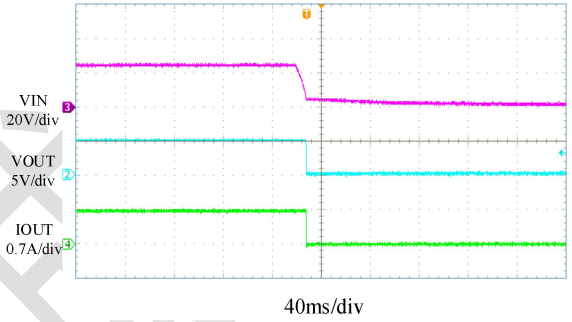
VIN Shutdown

I_{OUT}=0A



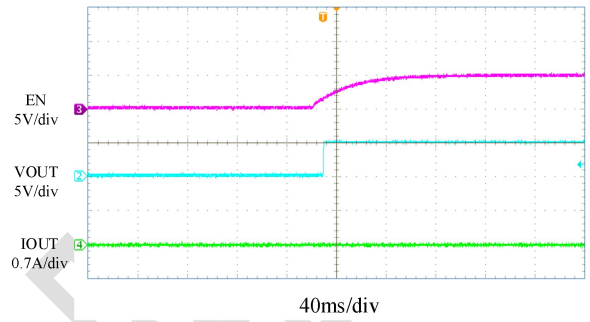
VIN Shutdown

I_{OUT}=0.7A



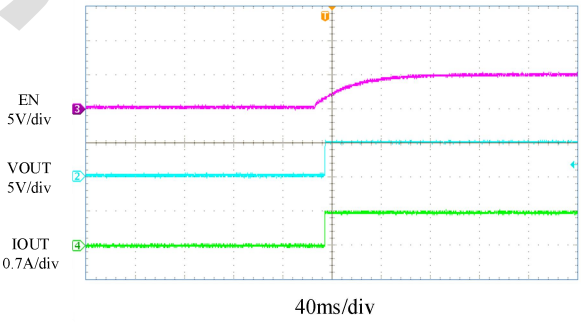
EN Start-up

I_{OUT}=0A



EN Start-up

I_{OUT}=0.7A

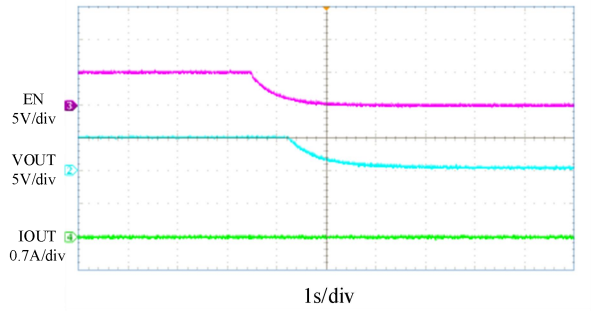


TYPICAL PERFORMANCE CHARACTERISTICS (POSITIVE OUTPUT)

V_{IN}=24V, V_{OUT}=5V, T_A=25°C, unless otherwise noted.

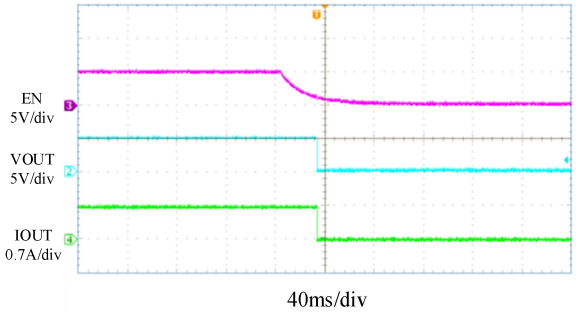
EN Shutdown

I_{OUT}=0A



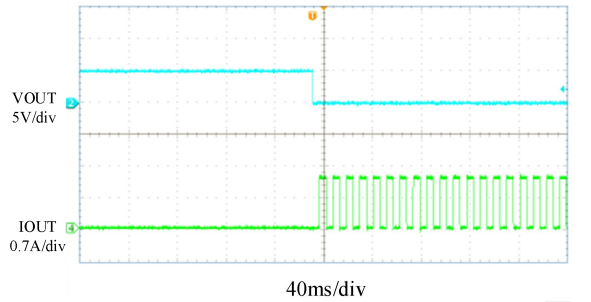
EN Shutdown

I_{OUT}=0.7A



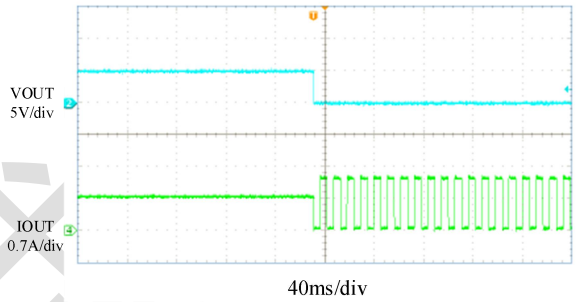
SCP Entry

I_{OUT}=0A



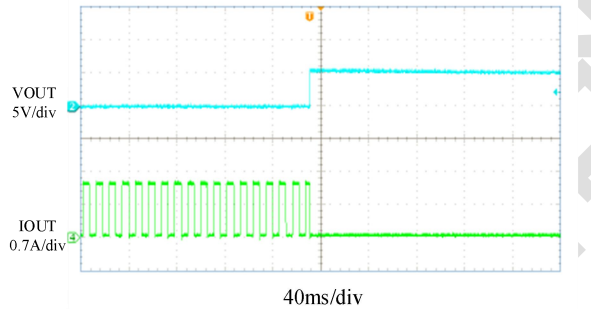
SCP Entry

I_{OUT}=0.7A



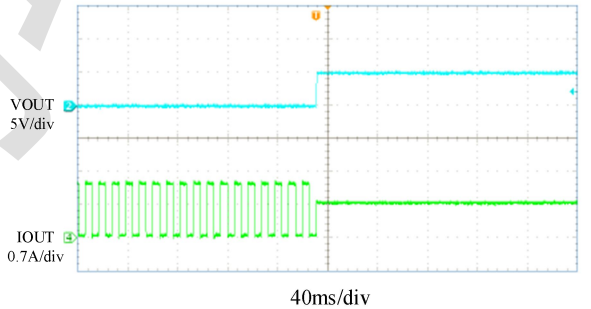
SCP Recovery

I_{OUT}=0A



SCP Recovery

I_{OUT}=0.7A

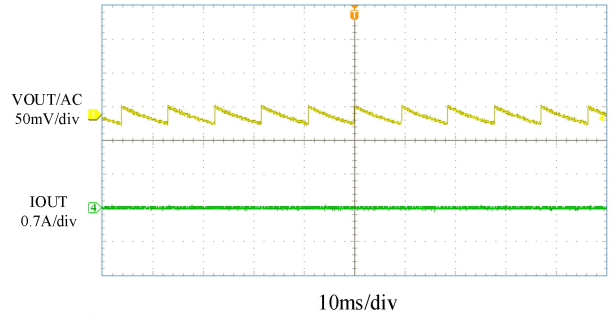


TYPICAL PERFORMANCE CHARACTERISTICS (POSITIVE OUTPUT)

V_{IN}=24V, V_{OUT}=5V, T_A=25°C, unless otherwise noted.

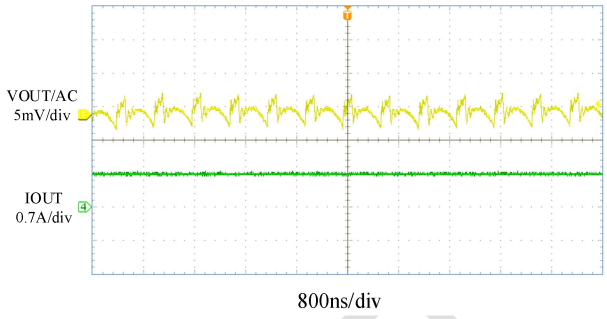
VOUT Ripple

IOUT=0A



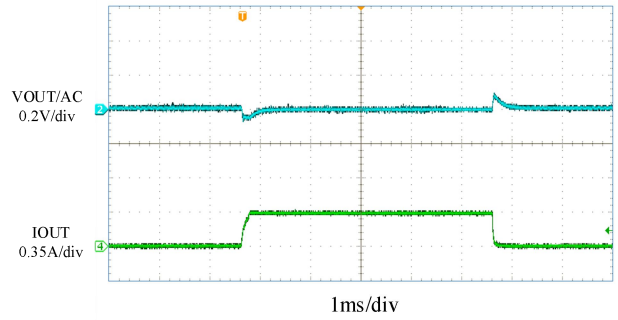
VOUT Ripple

IOUT=0.7A



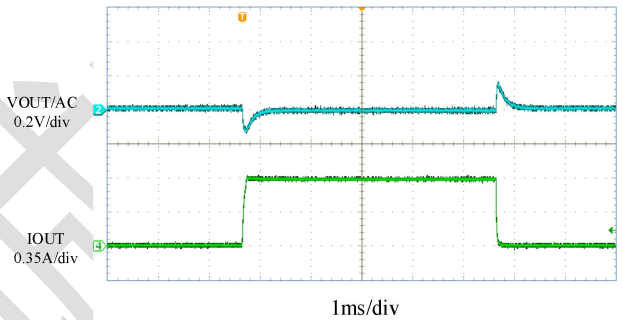
Load Transient

IOUT=0A to 0.35A, 1A/μs



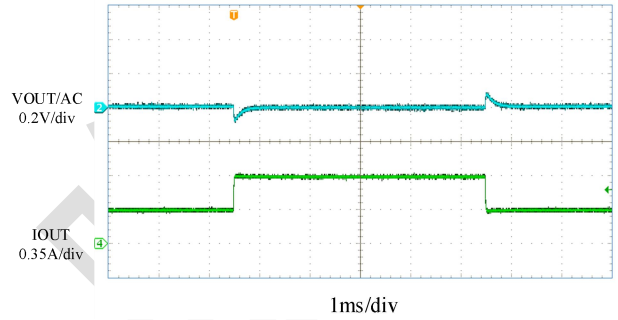
Load Transient

IOUT=0A to 0.7A, 1A/μs



Load Transient

IOUT=0.35A to 0.7A, 1A/μs

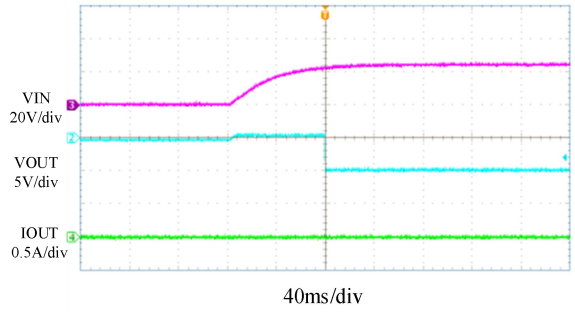


TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=24V, V_{OUT}=−5V, T_A=25℃, unless otherwise noted.

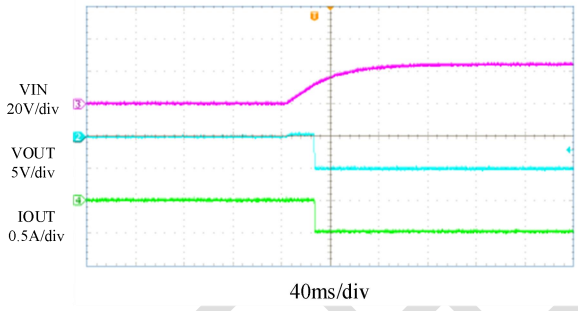
VIN Start-up

I_{OUT}=0A



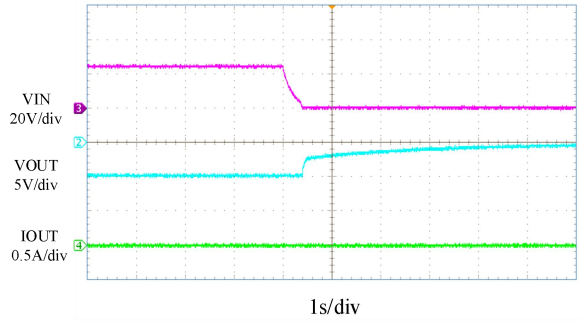
VIN Start-up

I_{OUT}=−0.5A



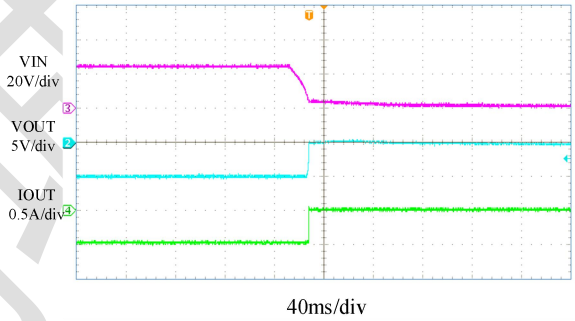
VIN Shutdown

I_{OUT}=0A



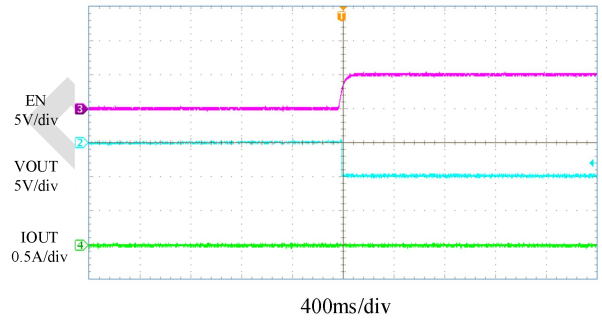
VIN Shutdown

I_{OUT}=−0.5A



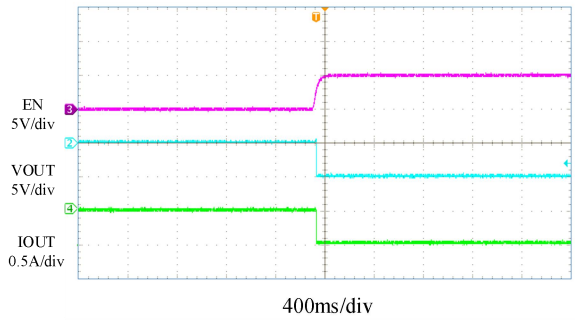
EN Start-up

I_{OUT}=0A



EN Start-up

I_{OUT}=−0.5A

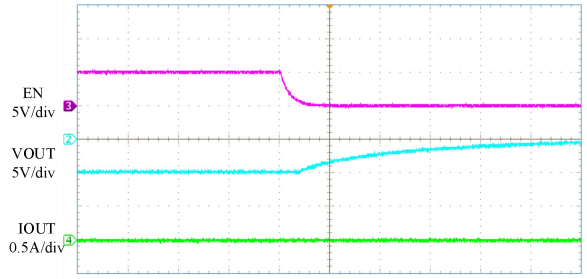


TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=24V, V_{OUT}=−5V, T_A=25℃, unless otherwise noted.

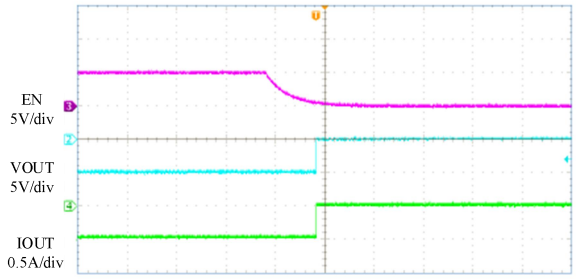
EN Shutdown

I_{OUT}=0A



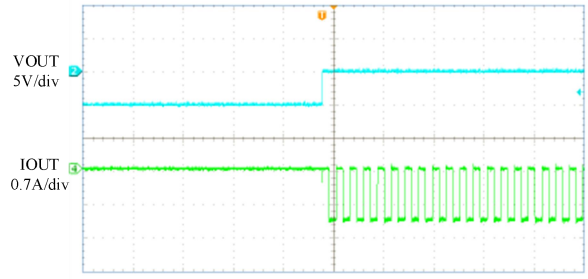
EN Shutdown

I_{OUT}=−0.5A



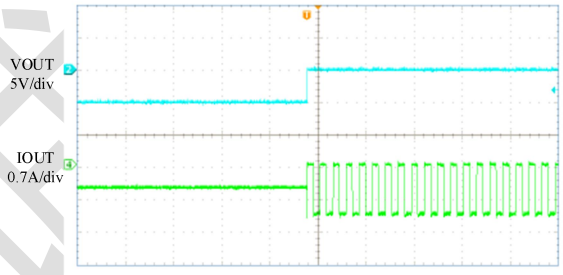
SCP Entry

I_{OUT}=0A



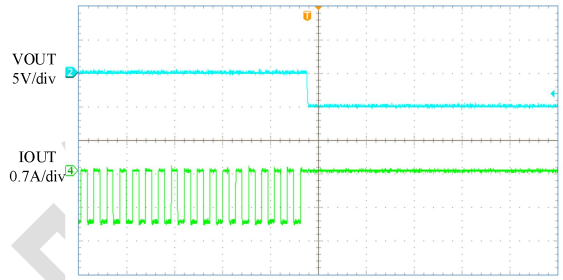
SCP Entry

I_{OUT}=−0.5A



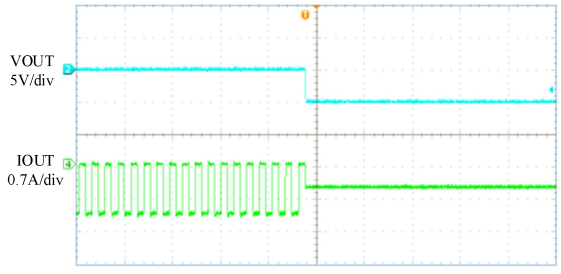
SCP Recovery

I_{OUT}=0A



SCP Recovery

I_{OUT}=−0.5A

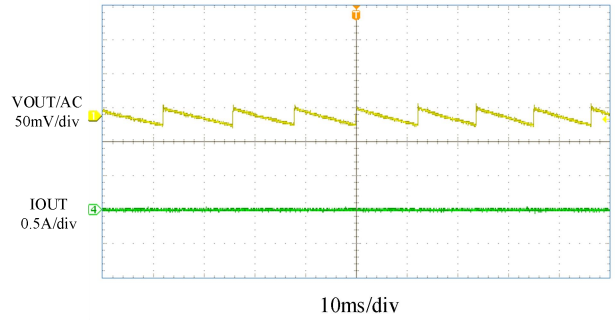


TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=24V, V_{OUT}=−5V, T_A=25℃, unless otherwise noted.

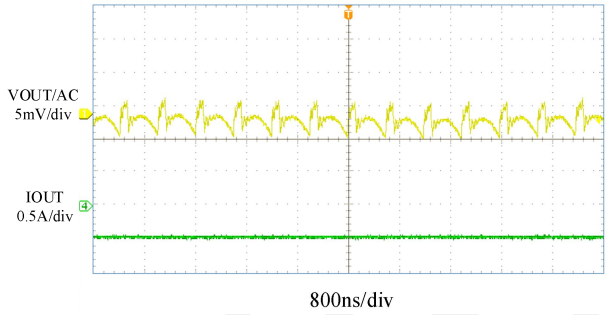
V_{OUT} Ripple

I_{OUT}=0A



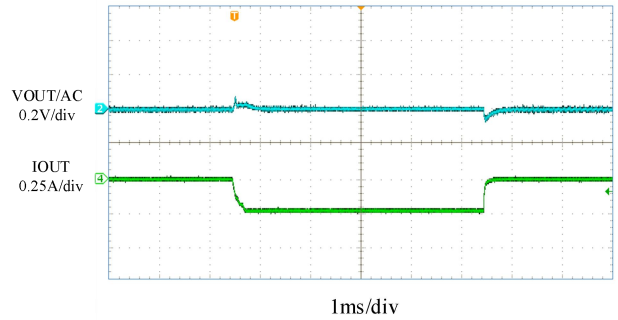
V_{OUT} Ripple

I_{OUT}=−0.5A



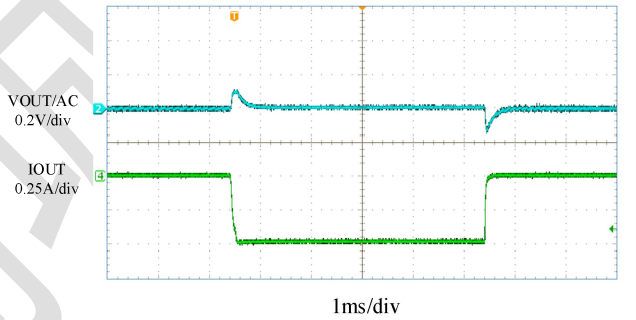
Load Transient

I_{OUT}=0A to −0.25A, 1A/μs



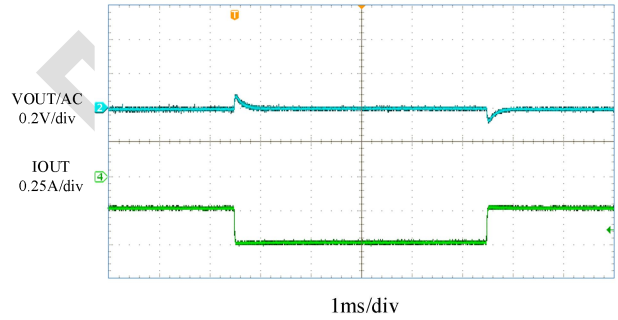
Load Transient

I_{OUT}=0A to −0.5A, 1A/μs



Load Transient

I_{OUT}=−0.25A to −0.5A, 1A/μs



OPERATION

The M4001 is a 0.7A synchronous step-down switching mode Power SoC with integrated High-Side and Low-Side power MOSFETs, inductor and other passives in LGA-8 package. M4001 works on peak current control mode to regulate the output voltage with the fixed switching frequency of 1.6MHz. M4001 operates in Power Saving Mode (PSM) at light load condition to achieve excellent efficiency. M4001 can support up to 98% maximum duty cycle and has 0.6ms soft-start timer internally.

Only input and output capacitors are needed to complete the design over 4.5V to 48V input voltage range with the default 3.3V or 5V output. External resistor divider can be used to change the output voltage. And the integrated input decoupling capacitor can minimize the parasitic inductance of input circuit and reduce the voltage spike on switching pin which simplifies the PCB layout.

Fully integrated protection features including OCP and OTP are shown below.

OVER CURRENT PROTECTION (OCP)

M4001 implements a cycle-by-cycle Low-Side valley current limit protection to prevent inductor from saturation, When the Low-Side switch reaches the current limit, M4001 will enter hiccup mode. It will stop switching for a pre-determined period of time and automatically start up again. It always starts up with soft-start to limit inrush current and avoid output overshoot.

OVER TEMPERATURE PROTECTION (OTP)

M4001 will stop switching when the junction temperature exceeds 151 ℃. The device will power up again when the junction temperature drops below 130℃.

APPLICATION INFORMATION (POSITIVE OUTPUT)

The Output Voltage

Apart from the default configuration, the output voltage of M4001 can be modified by trim connection as exhibited in Figure 1. For a desired output voltage, the following equation is applicable,

$$|V_{OUT}|=V_{trim}\frac{R_1//R_{UP}+R_2//R_{DOWN}}{R_2//R_{DOWN}}$$

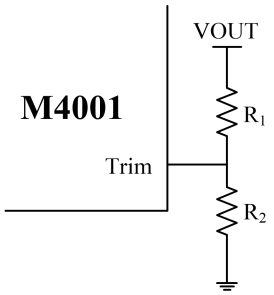


Figure 1: Typical Trim Connection of M4001

Table 1 lists a series of recommended resistor values for common output voltages.

Table 1：Resistor Values for Common Output Voltages

P/N	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	R_{UP} (kΩ)	R_{DOWN} (kΩ)
M4001-3V3	3.3	NC	NC	604	191
	5	NC	287		
	9	NC	84.5		
	12	324	16.2		
M4001-5V	3.3	100	36	604	115
	5	NC	NC		
	9	150	13		
	12	270	15		

Input Capacitor Selection

The input current of the step-down converter is discontinuous with sharp edges. Therefore, putting filter capacitors is necessary. For better performance, low ESR ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their lowest temperature variations. The RMS current of the input capacitors is calculated according to:

$$I_{CIN\_RMS}=I_{OUT}\sqrt{D(1-D)}$$

with the output load current I_{OUT} and the Duty Cycle D of D $=V_{OUT}/V_{IN}$. Mathematically, the RMS current reaches its highest value as D equal to 1/2:

$$I_{CIN\_RMS}=\frac{1}{2}\times I_{OUT}$$

Therefore, capacitors with their RMS current rating higher than half I_{OUT} are preferred. Respectively, the maximal power dissipation on these input capacitors can be estimated with their ESR and the actual RMS current. The resulted input voltage ripple can be calculated by

$$\Delta V_{CIN}=\frac{I_{OUT}}{F_{SW}\cdot C_{IN}}\cdot\frac{V_{OUT}}{V_{IN}}\cdot(1-\frac{V_{OUT}}{V_{IN}})$$

where F_{SW} is switching frequency of 1.6MHz and C_{IN} is the total input capacitance.

In addition, a small-size 0.1μF ceramic capacitor has been internally placed close to V_{IN} and GND in M4001 for noise reduction.

Output Capacitor Selection

Output capacitors are required to precisely stabilize output voltage. For the best output voltage ripple suppression, using low ESR ceramic capacitors are a prior; accordingly, the ripple ΔV_{OUT} can be estimated as

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\cdot F_{SW}{}^2\cdot C_{OUT}\cdot L}\cdot(1-\frac{V_{OUT}}{V_{IN}})$$

in which L is the inductance fixed at 10μH internally and C_{OUT} is the total output capacitance.

Nevertheless, if using electrolytic or tantalum capacitors is a must, their ESR becomes the dominant factor in determining the output voltage ripple, and thus,

$$\Delta V_{OUT}=R_{ESR}\cdot\frac{V_{OUT}}{F_{SW}L}\cdot(1-\frac{V_{OUT}}{V_{IN}})$$

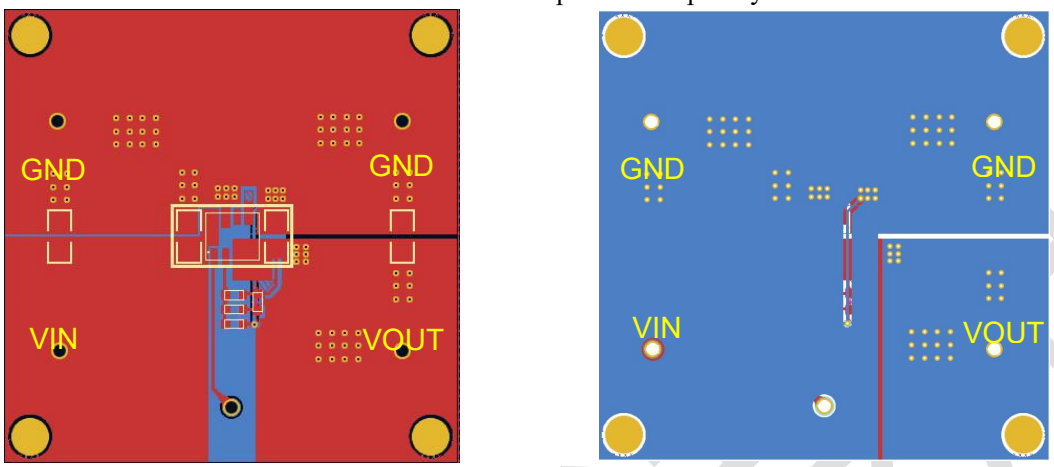
where R_{ESR} is the summed ESR of the used electrolytic or tantalum capacitors.

PCB Layout Guide

To optimize the electrical and thermal performance, useful PCB layout guidelines are recommended to consider as below:

1. Use wide traces for high current paths and keep them as short as possible for minimizing PCB conduction loss and thermal stress.
2. Place input decoupling capacitors close to V_{IN} and GND.
3. Keep the feedback network short and connect it as close to the TRIM of Power IC as possible.
4. Connect GND to a strong ground plane for enhancing heat dissipation and noise protection.

Figure 2 presents a recommended example of the positive output layout.



(a) Top Layer (b) Bottom Layer

Figure 2: Recommended Positive Output Layout

APPLICATION INFORMATION (NEGATIVE OUTPUT)

The Output Voltage

Apart from the default configuration, the output voltage of M4001 can be modified by trim connection as exhibited in Figure 3. For a desired output voltage, the following equation is applicable,

$$|V_{OUT}|=V_{trim}\frac{R_1//R_{UP}+R_2//R_{DOWN}}{R_2//R_{DOWN}}$$

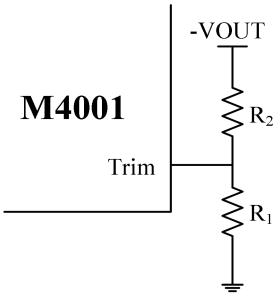


Figure 3: Typical Trim Connection of M4001

Table 2 lists a series of recommended resistor values for common output voltages.

Table 2：Resistor Values for Common Output Voltages

P/N	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	R_{UP} (kΩ)	R_{DOWN} (kΩ)
M4001-3V3	-3.3	NC	NC	604	191
	-5	NC	287		
	-9	NC	84.5		
	-12	324	16.2		
M4001-5V	-3.3	100	36	604	115
	-5	NC	NC		
	-9	150	13		
	-12	270	15		

Capacitor Selection for Negative Output Buck-Boost Converter

To realize stable negative output, extra capacitors between V_{IN} and V_{OUT} are recommended, which can be treat as the C_{IO} in general negative output buck-boost converters. Typically, this C_{IO} consists of one or two ceramic capacitors and a parallelly connected small-size high frequency by-pass capacitor. Increasing C_{IO} capacitance is an option if instable output observed.

Similar to positive output usage, input capacitors are required to connect V_{IN} and GND. However, to accordingly calculate the input voltage ripple ΔV_{CIN}, the following equation must be used instead,

$$\Delta V_{CIN}=\frac{I_{OUT}}{F_{SW}\cdot C_{IN}}\cdot\frac{|V_{OUT}|}{V_{IN}+|V_{OUT}|}\cdot\left(1-\frac{|V_{OUT}|}{V_{IN}+|V_{OUT}|}\right)$$

Regarding output capacitors, they are required to supply current when Low-Side switch off in negative output application. Thereby, a minimum capacitance is requisite to fulfill this job, which can be determined by the following equation,

$$C_{OUT}=\frac{I_{OUTMAX}}{F_{SW}\Delta V_{OUT}}\cdot\frac{|V_{OUT}|}{V_{INMIN}+|V_{OUT}|}$$

where V_{INMIN} and I_{OUTMAX} are the minimum input voltage and maximum output current of a desired scenario, respectively, as well as the pre-defined absolute value of output voltage $|V_{OUT}|$ and output voltage ripple threshold.

Once the output capacitance is determined, the actual output voltage ripple in a particular condition can be estimated by

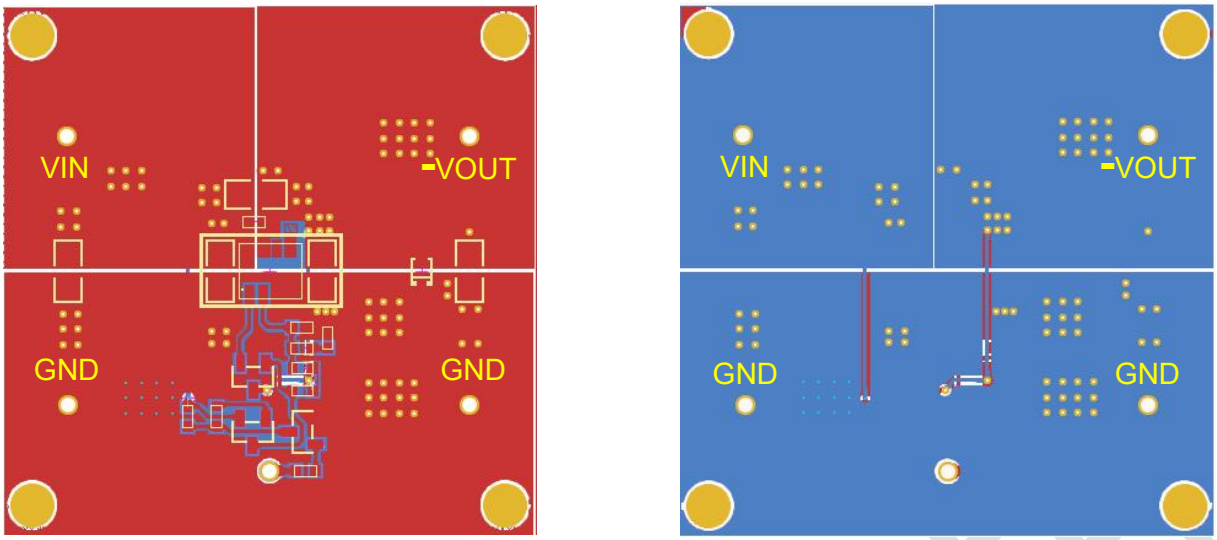
$$\Delta V_{OUT}=\frac{I_{OUT}}{F_{SW}C_{OUT}}\cdot\frac{|V_{OUT}|}{V_{IN}+|V_{OUT}|}$$

In addition, the output capacitors should be placed between V_{OUT} and GND directly.

PCB Layout Guide

Those PCB layout guidelines elaborated in the previous positive output session can be applied in negative output scenario. Figure 4 demonstrates a good example for negative output layout.

1. Use wide traces for high current paths and keep them as short as possible for minimizing PCB conduction loss and thermal stress.
2. Place input decoupling capacitors close to VIN and -VOUT.
3. Keep the feedback network short and connect it as close to the TRIM of Power IC as possible.
4. Connect GND to a strong ground plane for enhancing heat dissipation and noise protection.



(a) Top Layer (b) Bottom Layer

Figure 4: Recommended Negative Output Layout

TYPICAL APPLICATION

Positive Output

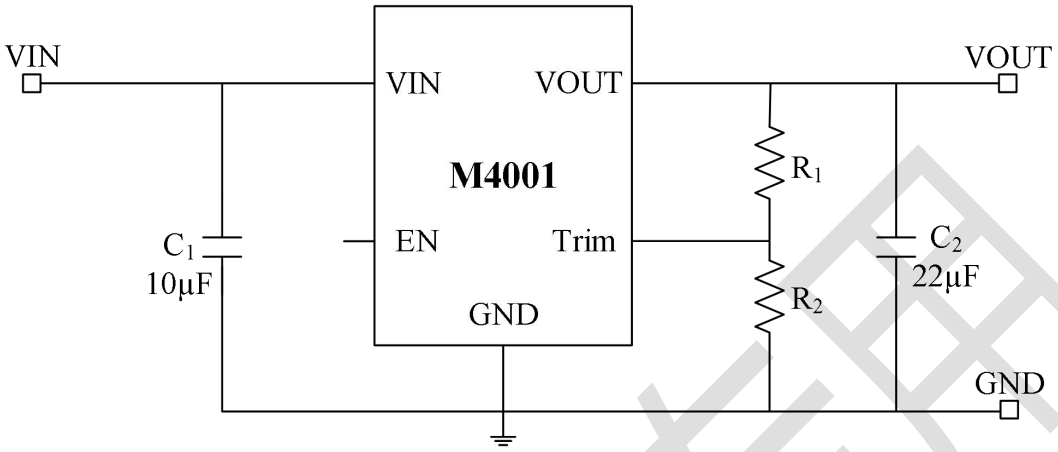


Figure 5: Typical Application Circuits of M4001 for Positive Output

Table 3：Reference Design for Positive Output

P/N	VOUT	CIN	COUT	R_1	R_2
M4001-3V3	3.3V	1×10μF	1×22μF	NC	NC
	5V	1×10μF	1×22μF	NC	287 kΩ
	9V	1×10μF	1×22μF	NC	84.5 kΩ
	12V	1×10μF	1×22μF	324 kΩ	16.2 kΩ
M4001-5V	3.3V	1×10μF	1×22μF	100 kΩ	36 kΩ
	5V	1×10μF	1×22μF	NC	NC
	9V	1×10μF	1×22μF	150 kΩ	13kΩ
	12V	1×10μF	1×22μF	270 kΩ	15 kΩ

NOTES:

CIN is the sum of the input capacitors, COUT is the sum of the output capacitors, please refer to Figure 5 for parameters of other components.

Negative Output

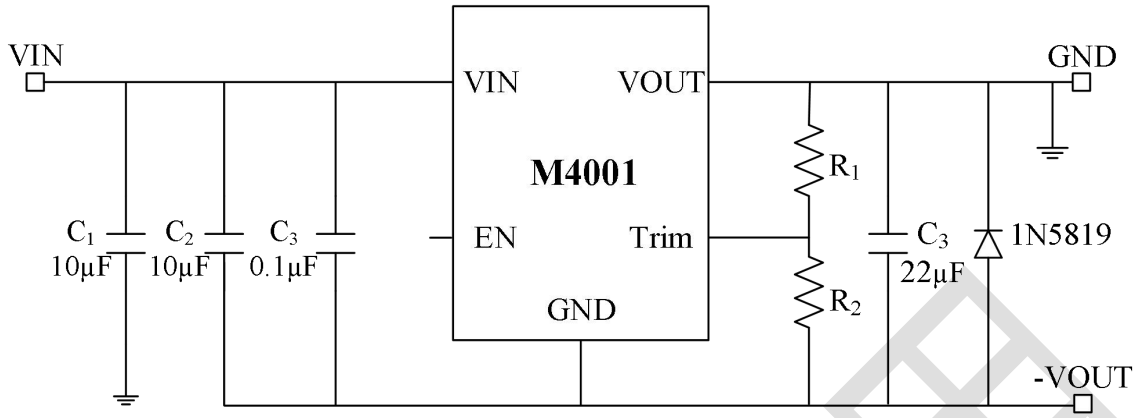


Figure 6: Typical Application Circuits of M4001 for Negative Output

Table 4：Reference Design for Negative Output

P/N	VOUT	CIN	COUT	CIO	R1	R2
M4001-3V3	−3.3V	1×10μF	1×22μF	1×10μF	NC	NC
	−5V	1×10μF	1×22μF	1×10μF	NC	287 kΩ
	−9V	1×10μF	1×22μF	1×10μF	NC	84.5 kΩ
	−12V	1×10μF	1×22μF	1×10μF	324 kΩ	16.2 kΩ
M4001-5V	−3.3V	1×10μF	1×22μF	1×10μF	100 kΩ	36 kΩ
	−5V	1×10μF	1×22μF	1×10μF	NC	NC
	−9V	1×10μF	1×22μF	1×10μF	150 kΩ	13kΩ
	−12V	1×10μF	1×22μF	1×10μF	270 kΩ	15 kΩ

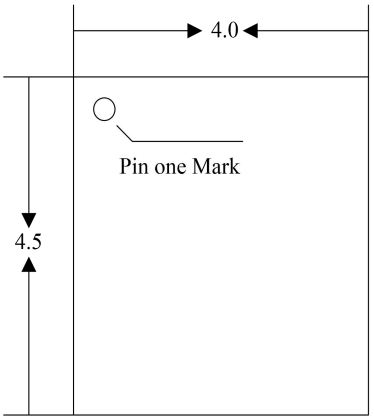
NOTES：

CIN is the sum of the input capacitors to GND, COUT is the sum of the output capacitors, CIO is the sum of input capacitor to output, please refer to Figure 6 for parameters of other components.

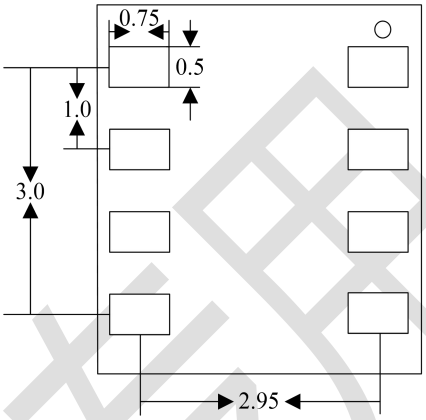
PACKAGE INFORMATION

LGA-8 (4mm×4.5mm×1.68mm) Package

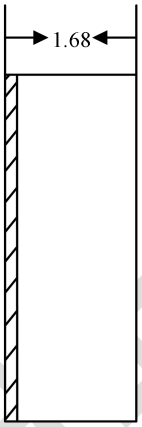
TOP VIEW



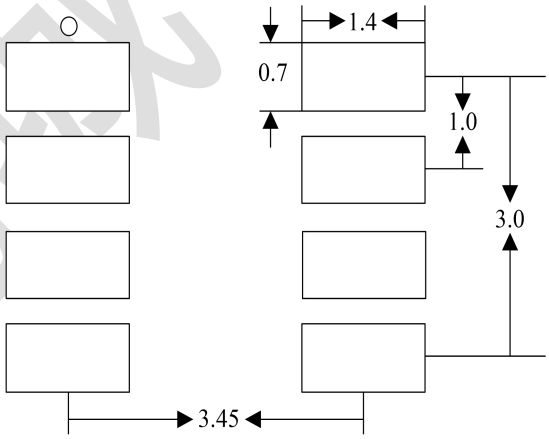
BOTTOM VIEW



SIDE VIEW



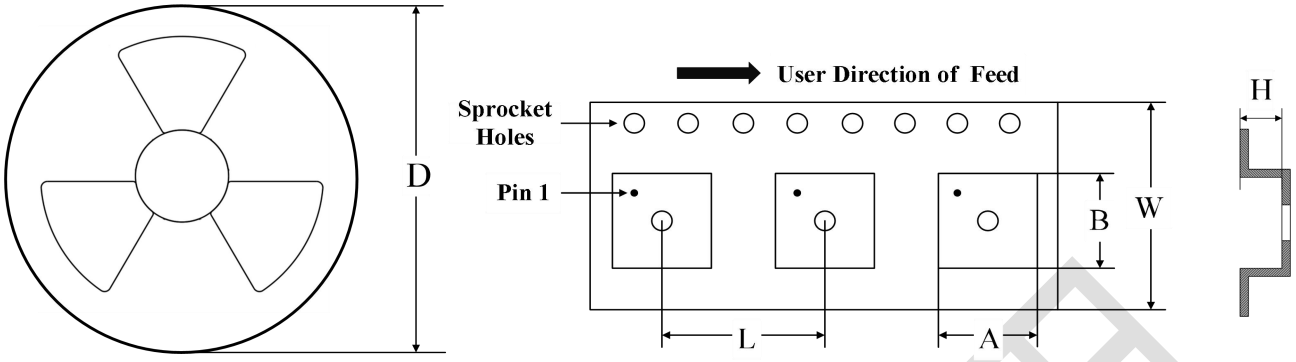
RECOMMENDED LAND PATTERN



NOTES:

All dimensions are in MM.

CARRIER INFORMATION



PART NUMBER	PACKAGE	QUANTITY /REEL	D	A	B	L	W	H
M4001DLCC-5V	LGA-8 (4mm×4.5mm×1.68mm)	3000	13 in	4.3mm	4.8mm	8mm	12mm	2mm
M4001DLCC-3V3	LGA-8 (4mm×4.5mm×1.68mm)	3000	13 in	4.3mm	4.8mm	8mm	12mm	2mm

单击下面可查看定价，库存，交付和生命周期等信息

>>iModule(沃芯)