FEATURES

- Wide Input Voltage Range: 6V to 80V
  - Negative Output: VIN ≥ 6V; VIN+|VOUT| ≤80V
- Up to 100V Input Rating Voltage
- Output Voltage
  - Default 5V Output Voltage
  - Positive Output: Range from 0.8V to 32V
  - Negative Output: Range from −0.8V to −32V
- Output Current
  - Positive Output: 5A Continuous
  - Negative Output: $5 \times \frac{VIN}{VIN+|VOUT|}A$
- Stable with low ESR Ceramic Capacitors
- Selectable light load mode
  - Diode Emulation Mode (DEM)
  - Forced Continuous Conduction Mode (FCCM)
- Ultra-short 40ns $t_{on(min)}$ for low duty ratio
- Short 190ns $t_{off(min)}$ for high duty ratio
- SYNCI and SYNCO Functions
- Pre-Biased Start-Up
- Power Good Indicator
- Junction Temperature Range: −40°C to 125°C
- Adjustable soft-start time
  - Default 3.8ms soft-start time
  - Compatible with external soft start regulation
- Cycle-by-cycle Output Current Limit
- Hiccup Mode for SCP and OCP
- Thermal Shutdown Protection
- Over Output Voltage Protection
- LGA-63 (9mm×12mm×4.4mm) Package
- Pb-Free RoHS Compliant

DESCRIPTION

The M8005 is a 5A step-down switching mode Power SoC (System on Chip) with integrated controller, power MosFETs, inductor, input decoupling capacitor and other passives. The input voltage ranges from 6V to 80V with wide output voltage range of 0.8V to 32V. The output voltage is 5V as default and can be programmed by adjusting a bottom feedback resistor accordingly. The M8005 has a soft-start time of 3.8ms which can be lengthened by adding external capacitors.

The M8005 provides high efficiency with voltage control mode for good loop stability. Either Diode Emulation Mode (DEM) or Forced Continuous Conduction Mode (FCCM) can be selected upon to application design for maintaining excellent load regulation and line regulation.

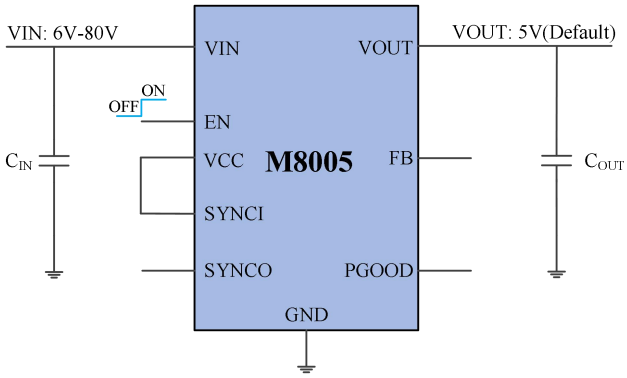
The M8005 can indicate faults with complete protection features, including under-voltage protection (UVP), overvoltage protection (OVP) and over-temperature protection (OTP). Particularly, over-load and short circuit are protected by hiccup mode.

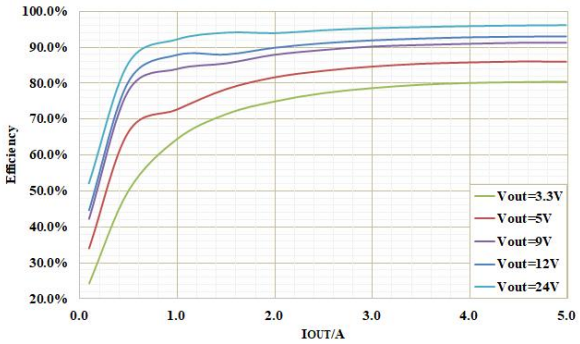
APPLICATIONS

- Telecom Systems
- Quick Charger
- PoE Power Supply
- Industrial Systems

TYPICAL APPLICATION&EFFICIENCY

(VIN=48V, FCCM)





ORDERING INFORMATION

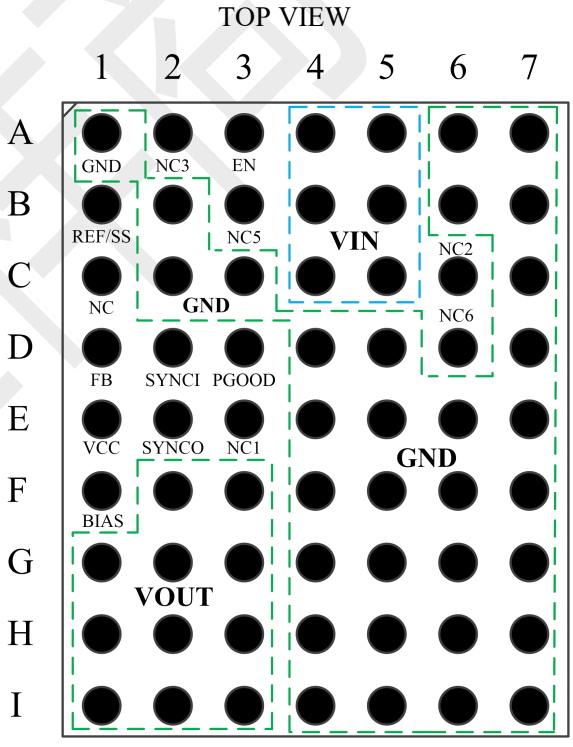
PART NUMBER	TOP MARKING	PACKAGE	MOQ	MSL LEVEL
M8005DLKK	M8005 YWWLLL	LGA-63 (9mm×12mm×4.4mm)	500/ Tape & Reel	3
M8005DLKK-T[Notes 1)]	M8005 YWWLLL	LGA-63 (9mm×12mm×4.4mm)	170/ Tray	3

NOTES:

1) Not recommended

2) Y: Year, WW: Week, LLL: Lot Number.

PACKAGE REFERENCE



PACKAGE REFERENCE (continued)

Table1: Pins A1–F7

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	GND	B1	REF/SS	C1	NC	D1	FB	E1	VCC	F1	BIAS
A2	NC3	B2	GND	C2	GND	D2	SYNCI	E2	SYNCO	F2	VOUT
A3	EN	B3	NC5	C3	GND	D3	PGOOD	E3	NC1	F3	VOUT
A4	VIN	B4	VIN	C4	VIN	D4	GND	E4	GND	F4	GND
A5	VIN	B5	VIN	C5	VIN	D5	GND	E5	GND	F5	GND
A6	GND	B6	GND	C6	NC2	D6	NC6	E6	GND	F6	GND
A7	GND	B7	GND	C7	GND	D7	GND	E7	GND	F7	GND

Table2: Pins G1–I7

PIN	NAME	PIN	NAME	PIN	NAME
G1	VOUT	H1	VOUT	I1	VOUT
G2	VOUT	H2	VOUT	I2	VOUT
G3	VOUT	H3	VOUT	I3	VOUT
G4	GND	H4	GND	I4	GND
G5	GND	H5	GND	I5	GND
G6	GND	H6	GND	I6	GND
G7	GND	H7	GND	I7	GND

PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
F2, F3, G1-G3, H1-H3, I1-I3	VOUT	**Output Voltage.** Connect this pin to the load. Output capacitors are recommended to be placed between VOUT and GND.
A3	EN	**Enable Control.** Pull this pin low to shut down the chip. Otherwise, pull it high to enable the chip.
D3	PGOOD	**Power Good.** PGOOD is an open drain output pin. Connect a resistor from PG to a pull-up power source if used.
A4, A5, B4, B5, C4, C5	VIN	**Input Voltage.**
A1, A6, A7, B2, B6, B7, C2, C3, C7, D4, D5, D7, E4-E7, F4-F7, G4-G7, H4-H7, I4-I7	GND	**Ground.**
B1	REF/SS	**Reference/Soft Start.** 1. The default soft-start time is 3.8ms. 2. The soft-start time can be programmed by adding an external capacitor C_{SS} between REF/SS and GND accordingly. 3. Connect an external signal (between 0V and 0.8V) to regulate reference voltage if needed.
D1	FB	**Feedback.** Connect this pin with an external resistor divider from the output to GND and keep them as close to the pin as possible.
D2	SYNCI	**Synchronization Input.** Multiple functions: 1. Optional external clock input. 2. DEM when SYNCI is connecting to GND or floating. 3. FCCM when SYNCI is connected to a voltage rail between 7.5V to 14V or VCC.
F1	BIAS	**External Biasing Power.** Connect this pin to a voltage source between 8.5V to 14V. Float it if not used
E2	SYNCO	**Synchronization Output.** Logical output provides a clock signal that is nearly 180° out-of-phase against the High-Side MOSFET drive signal.
E1	VCC	**VCC.** Output of the internal LDO.
C1	NC	**Not Connected.**
E3	NC1	**Not Connected.**
C6	NC2	**Not Connected.**
A2	NC3	**Not Connected.**
B3	NC5	**Not Connected.**
D6	NC6	**Not Connected.**

NOTES: All the NC pins should not connect to each other.

ABSOLUTE MAXIMUM RATINGS

	SYMBOL	MIN	MAX	UNIT
Voltage at V_{IN} Pins	V_{IN}	−0.3	100	V
Voltage at SW Pins	V_{SW}	−0.3	100	V
Voltage at SW Pins	V_{SW} (20ns)	−5	100	V
Voltage at EN Pins	V_{EN}	−0.3	100	V
Voltage at Pins	BIAS/SYNCI/SYNCO/PGOOD	−0.3	14	V
Voltage at Other Pins		−0.3	6.6	V
Junction Temperature Range	T_J	−40	125	℃
Storage Temperature Range	T_S	−55	150	℃

ESD Ratings

ESD	STANDARD	VALUE
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	1000V
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101F	2000V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNIT
Input Voltage Range	V_{IN}	6	80	V
Output Voltage Range	V_{OUT}	0.8	32	V
Output Current Range	I_{OUT}		5	A
EN Voltage Range	V_{EN}	−0.3	80	V
Junction Temperature Range	T_J	−40	125	℃

ELECTRICAL CHARACTERISTICS

V_{IN}=48V， V_{OUT}=5V， T_A=25°C, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		6		100	V
Shutdown Current	I_{Q-SD}	V_{EN}=0V		7.7		uA
Standby Current	I_{Q-STBY}	V_{EN}= 1V, I_{OUT}=0A		1.5		mA
Operating Current (No Switching)	$I_{Q-OPERAT}$	V_{EN}=1.5V, $V_{REF/SS}$=0V		1.8		mA
Quiescent Current (No Load)	I_Q	DEM, VIN=24V~75V, V_{OUT}=3.3V~24V		2.1	24.33	mA
VCC Regulation Voltage	VCC	$V_{REF/SS}$=0V， 9V≤VIN≤ 100V，0mA ≤ I_{VCC} ≤20mA		7.5		V
VIN to VCC dropout	$V_{VCC-LDO}$	VIN=6V， $V_{REF/SS}$=0V， I_{VCC}=20mA		0.25		V
VCC max current	$I_{MAX-LDO}$	$V_{REF/SS}$=0V， VCC=0V		30		mA
VCC under Voltage Lockout Threshold	VCC_{UVLO}	VCC Increasing		4.9		V
VCC under Voltage Lockout Hysteresis	$V_{VCC-UVH}$			0.26		V
Minimum external Bias Supply Voltage	$V_{VCC-EXT}$	＞VCC	8			V
External VCC Input	I_{VCC}	$V_{REF/SS}$=0V，VCC=13V		10		uA
EN rising to Standby Threshold	$V_{EN-STBY}$	VIN=48V, I_{OUT}=0.1A		0.8		V
EN falling to Shutdown Threshold	V_{EN-SD}	VIN=48V, I_{OUT}=0.1A		0.65		V
EN rising to Operating Threshold	V_{EN-H}	VIN=48V, I_{OUT}=0.1A		1.2		V
Hysteresis Input Current	I_{EN-HYS}	V_{EN} =1.5V		10		uA
Feedback Voltage	V_{FB_REF}	V_{FB}=V_{COMP}		0.8		V
FB Input Bias Current	I_{FB}	V_{FB}= 700mV		10	100	nA
Switching Frequency	F_{SW}			500		kHz
REF/SS Charging Current	I_{SS}	$V_{REF/SS}$= 0 V		10		μA
Discharge FET Resistance	R_{SS}	V_{EN}=1V, $V_{REF/SS}$ =0.1V		10		Ω
REF/SS to FB Offset	V_{SS-FB}			0		mV
REF/SS to FB Clamp Voltage	$V_{SS-CLAMP}$	$V_{REF/SS}$-V_{FB} (0.8V)		115		mV

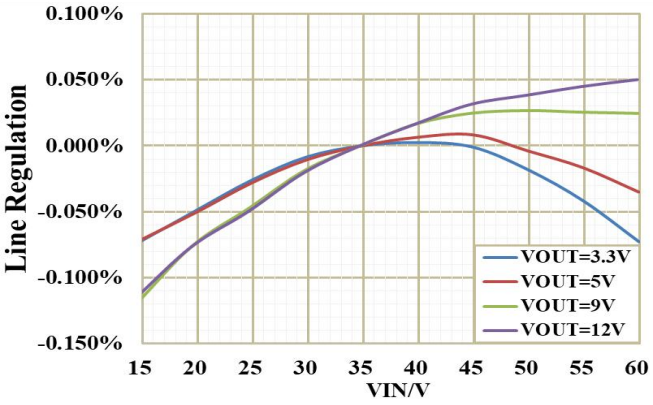
FB upper threshold for PGOOD high to low	$PGOOD_{UTH}$	% of V_{REF}, V_{FB} rising		108		%
FB lower threshold for PGOOD high to low	$PGOOD_{LTH}$	% of V_{REF}, V_{FB} falling		92		%
PGOOD upper threshold Hysteresis	$PGOOD_{HYS\_U}$	% of V_{REF}		3		%
PGOOD lower threshold Hysteresis	V_{PGOODL_F}	% of V_{REF}		2		%
PGOOD rising filter	$T_{PGOOD-RISE}$	FB to PGOOD rising edge		25		us
PGOOD falling filter	$T_{PGOOD-FALL}$	FB to PGOOD falling edge		25		us
PGOOD Low Threshold	$V_{PGOOD-L}$	V_{FB}=0.9V, I_{PGOOD}=2mA			150	mV
PGOOD High-state Leakage Current	$I_{PGOOD-H}$	V_{FB}=0.8V, V_{PGOOD}=13V			100	nA
SYNCI High Threshold	$V_{SYNC-IH}$		2			V
SYNCI Low Threshold	$V_{SYNC-IL}$				0.4	V
SYNCI Input Resistance	R_{SYNCI}	V_{SYNCI}=3V		20		kΩ
SYNCI Input Minimum Pulse Width	T_{SYNCI}	Minimum high/low state duration	50			ns
SYNCO High Threshold	$V_{SYNCO-OH}$	I_{SYNCO}= -1mA(sourcing)	3			V
SYNCO Low Threshold	$V_{SYNCO-OL}$	I_{SYNCO}= 1mA(sink)			0.4	V
Minimum on-time	$T_{ON(MIN)}$	HS Gate Signal Bootstrap voltage 7V		40		ns
Minimum off-time	$T_{OFF(MIN)}$	HS Gate Signal Bootstrap voltage 7V		190		ns
Hiccup mode activation delay	$C_{HICC-DEL}$	Clock cycle with current limiting before hiccup off-time activated		512		cycles
Hiccup mode off-time after activation	C_{HICCUP}	Clock cycle with no switching followed by REF/SS release		8192		cycles
Thermal Shutdown Threshold				175		℃
Thermal Shutdown Hysteresis				20		℃

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=48V, T_A=25°C, FCCM, F_{SW}=500kHz, V_{OUT}=5V, unless otherwise noted.

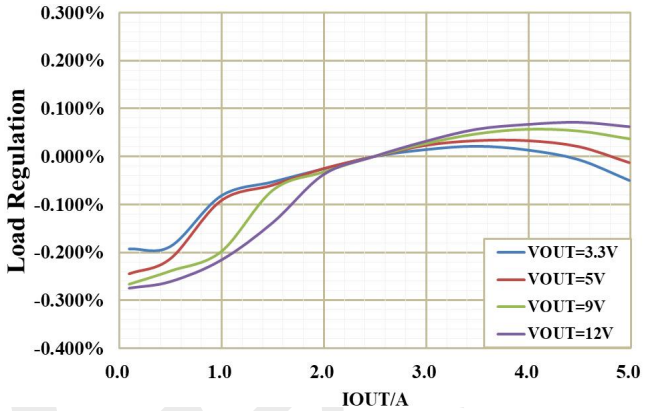
Line Regulation

V_{OUT}=3.3V/5V/9V/12V, I_{OUT}=5A,
V_{IN}=15V~60V



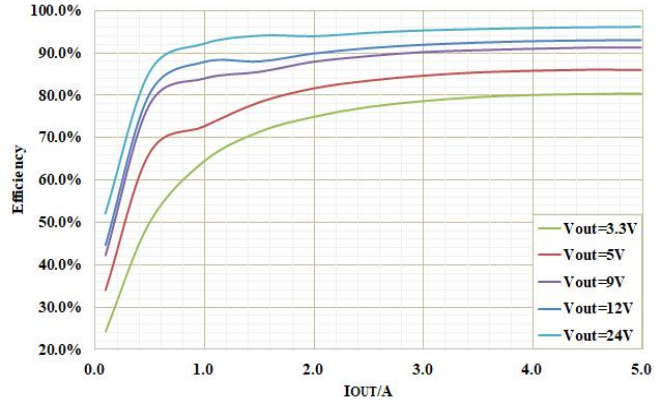
Load Regulation

V_{IN}=48V, V_{OUT}=3.3V/5V/9V/12V,
I_{OUT}=0~5A



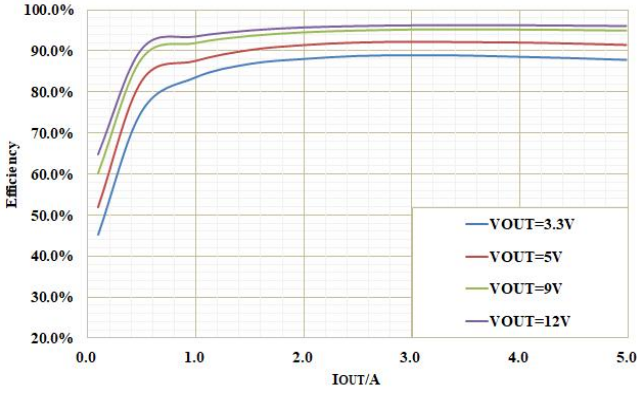
Efficiency

V_{IN}=48V, V_{OUT}=3.3V/5V/9V/12V/24V,
I_{OUT}=0A~5A



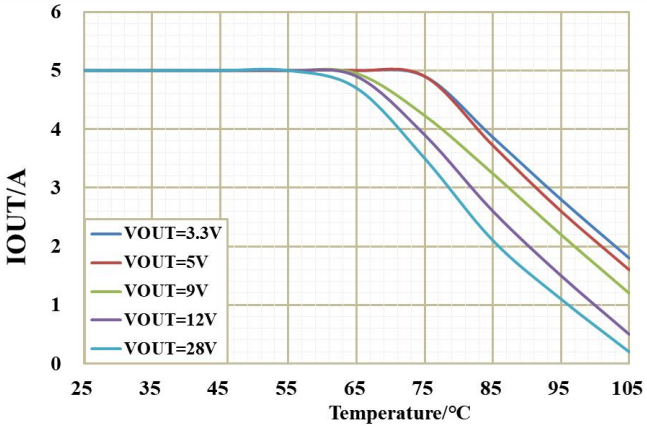
Efficiency

V_{IN}=24V, V_{OUT}=3.3V/5V/9V/12V,
I_{OUT}=0A~5A



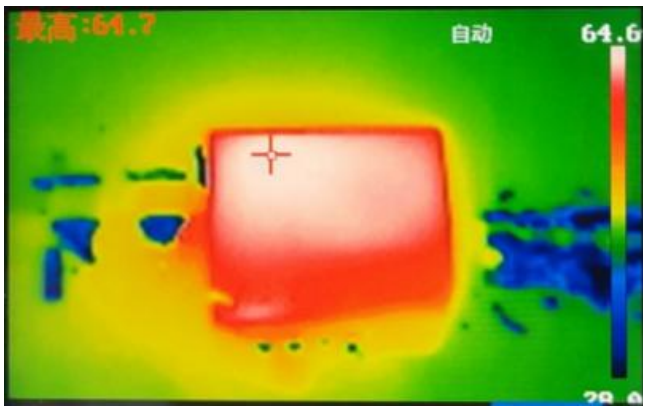
Thermal Derating

V_{IN}=48V, V_{OUT}=3.3V/5V/9V/12V/28V



Temperature

V_{IN}=48V, V_{OUT}=5V, IOUT=5A

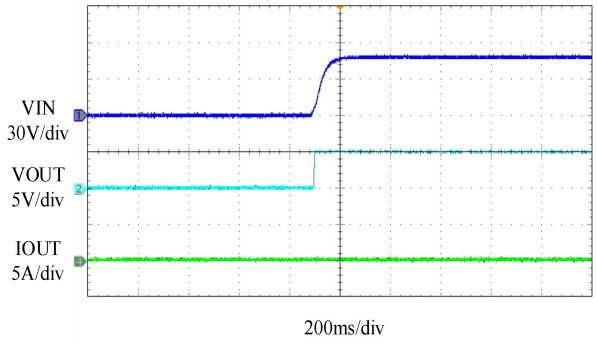


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=48V, T_A=25℃, FCCM, F_{SW}=500kHz, V_{OUT}=5V, unless otherwise noted.

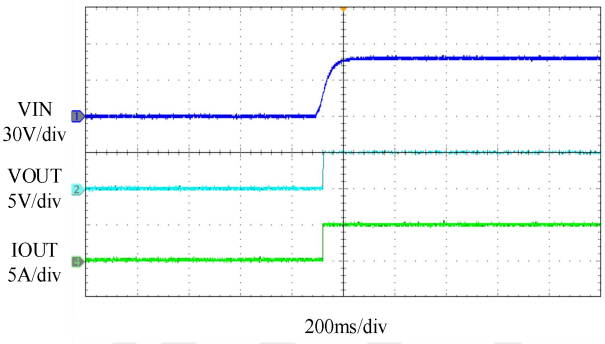
VIN Start-up

I_{OUT}=0A



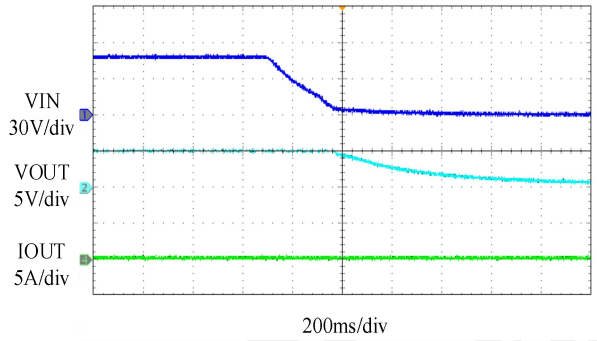
VIN Start-up

I_{OUT}=5A



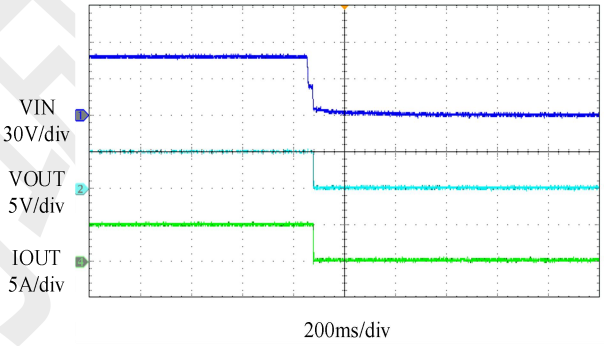
VIN Shutdown

I_{OUT}=0A



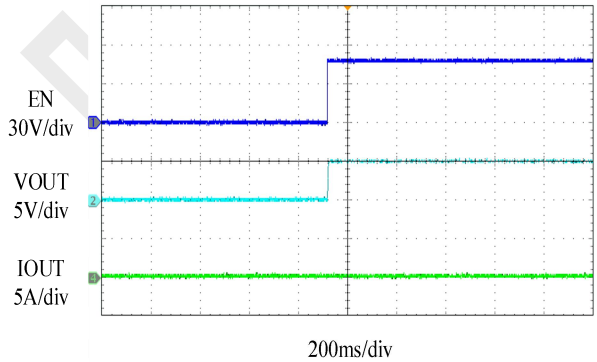
VIN Shutdown

I_{OUT}=5A



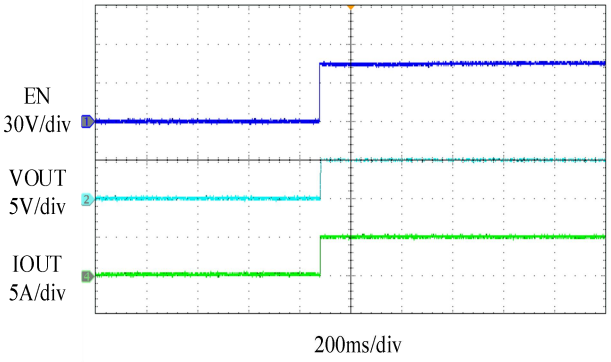
EN Start-up

I_{OUT}=0A



EN Start-up

I_{OUT}=5A

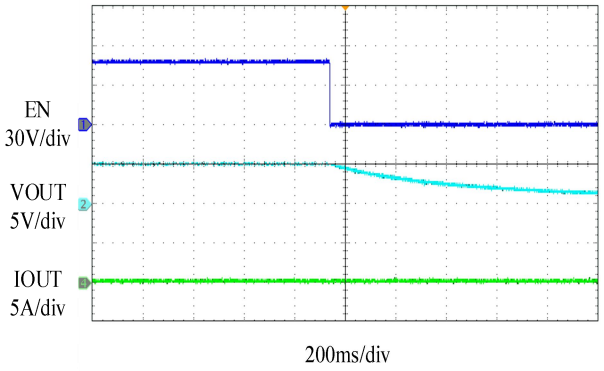


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=48V, T_A=25℃, FCCM, F_{SW}=500kHz, V_{OUT}=5V, unless otherwise noted.

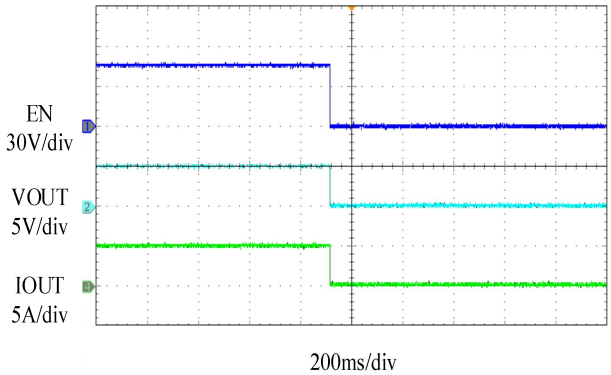
EN Shutdown

I_{OUT}=0A



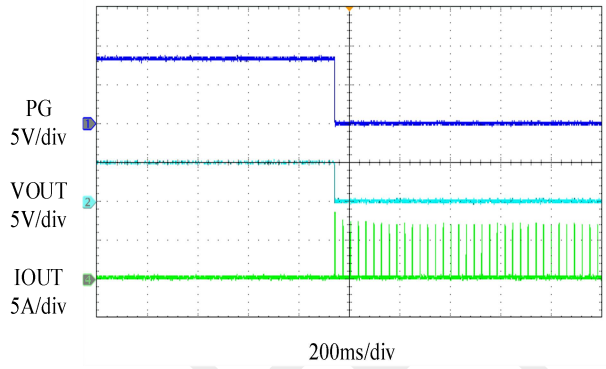
EN Shutdown

I_{OUT}=5A



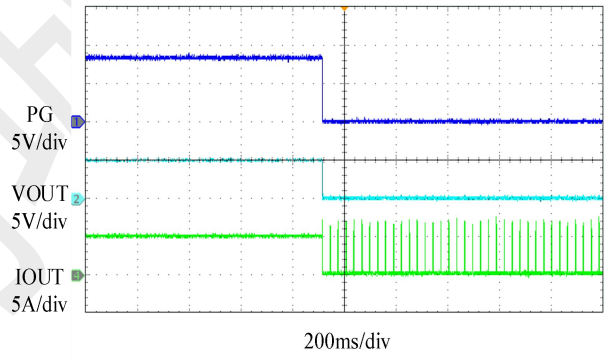
SCP Entry

I_{OUT}=0A



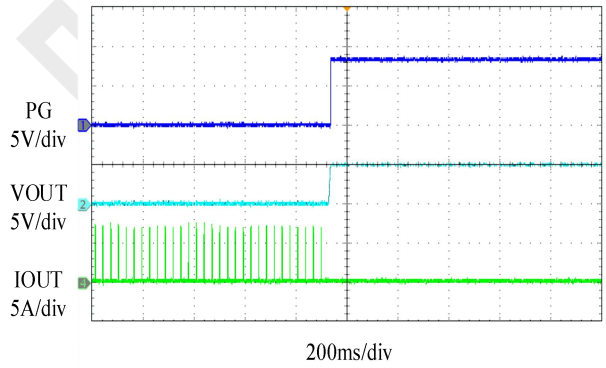
SCP Entry

I_{OUT}=5A



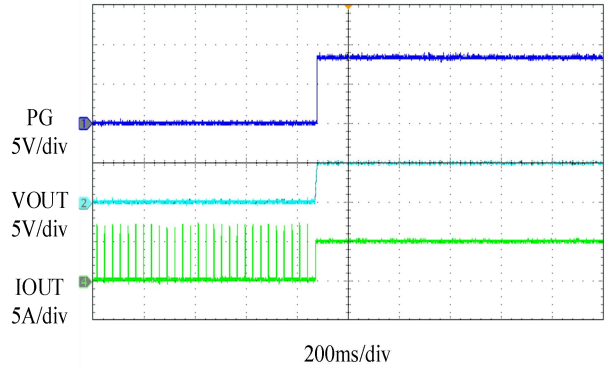
SCP Recovery

I_{OUT}=0A



SCP Recovery

I_{OUT}=5A

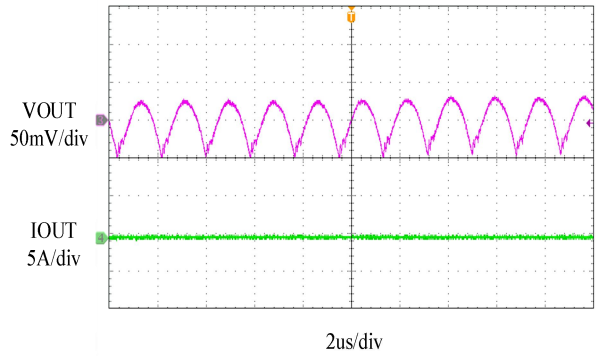


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=48V, T_A=25℃, FCCM, F_{SW}= 500kHz, V_{OUT}=5V, unless otherwise noted.

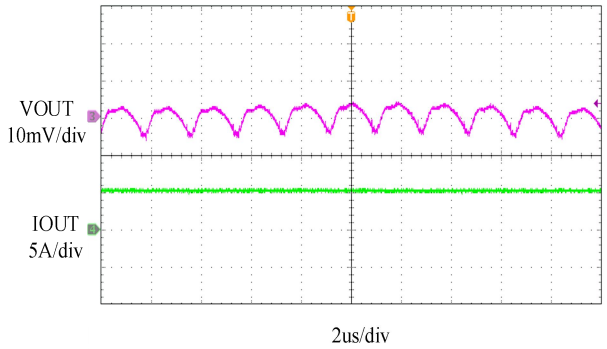
VOUT Ripple

I_{OUT}=0A



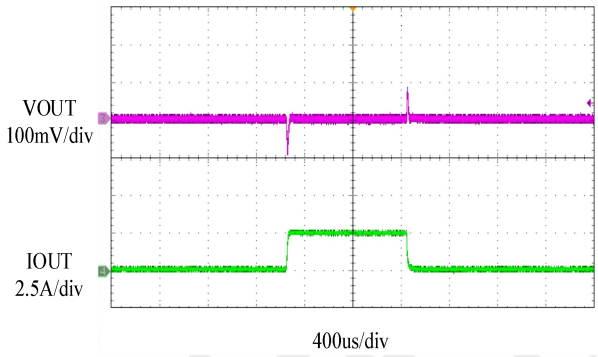
VOUT Ripple

I_{OUT}=5A



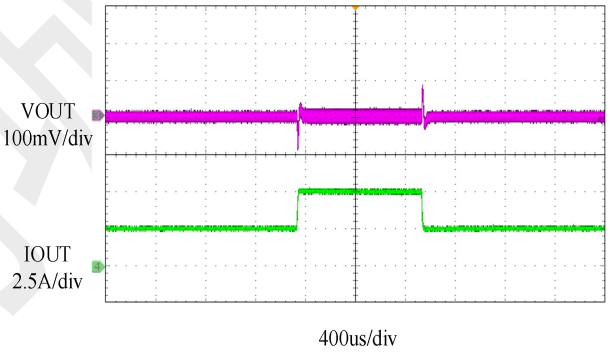
Load Transient

I_{OUT}=0A to 2.5A, 2.5A/μs



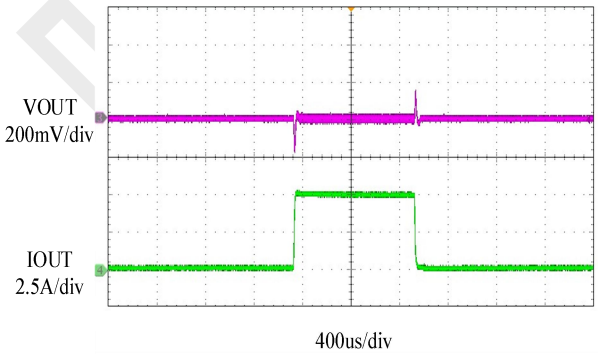
Load Transient

I_{OUT}=2.5A to 5A, 2.5A/μs



Load Transient

I_{OUT}=0A to 5A, 2.5A/μs

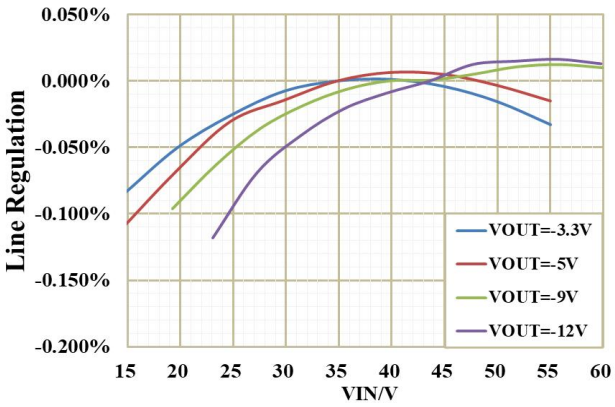


TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=48V, T_A=25℃, FCCM, F_{SW}=500kHz, V_{OUT}=−5V, unless otherwise noted.

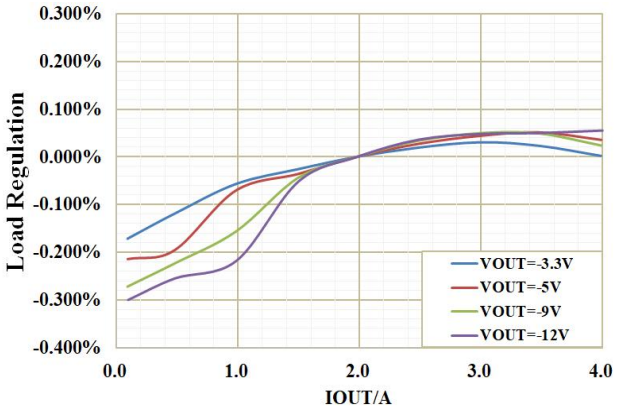
Line Regulation

V_{OUT}=−3.3V/−5V/−9V/−12V, I_{OUT}=4A,
V_{IN}=15V~60V



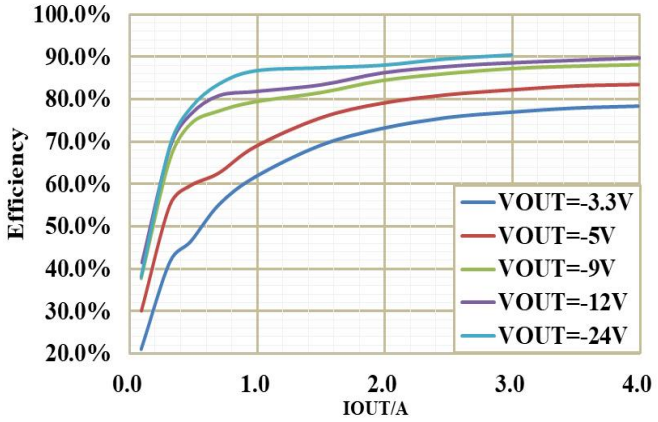
Load Regulation

V_{IN}=48V, V_{OUT}=−3.3V/−5V/−9V/−12V,
I_{OUT}=0~4A



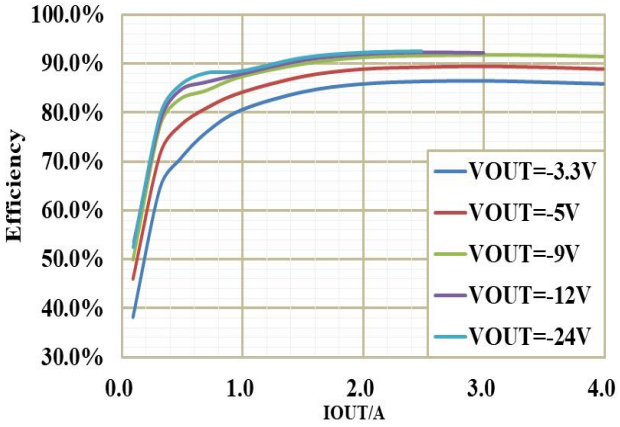
Efficiency

V_{IN}=48V, V_{OUT}=−3.3V/−5V/−9V/−12V/−24V,
I_{OUT}=0A~4A



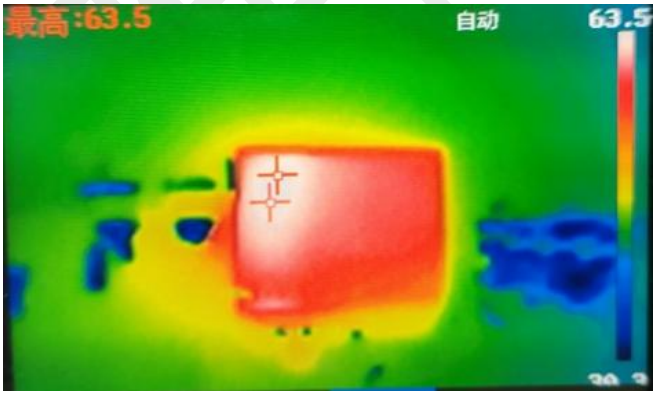
Efficiency

V_{IN}=24V, V_{OUT}=−3.3V/−5V/−9V/−12V/−24V,
I_{OUT}=0A~4A



Temperature

V_{IN}=48V, V_{OUT}=−5V, I_{OUT}=4A

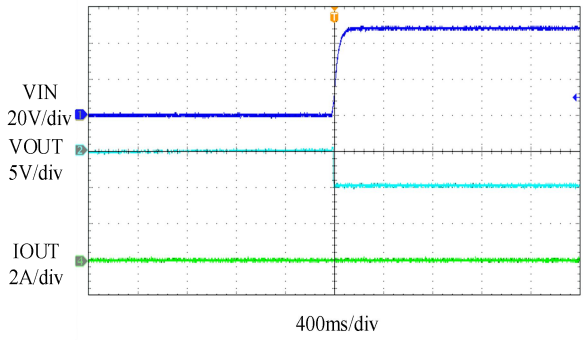


TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=48V, T_A=25°C, FCCM, F_{SW}=500kHz, V_{OUT}=−5V, unless otherwise noted.

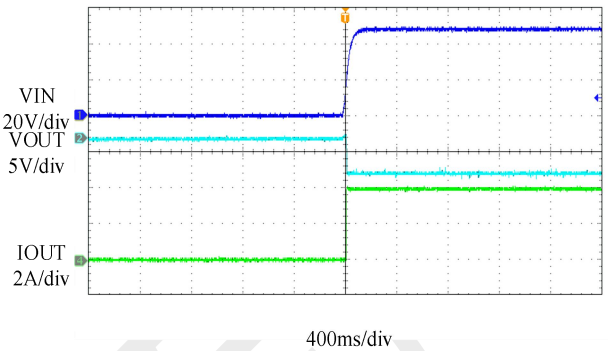
VIN Start-up

I_{OUT}=0A



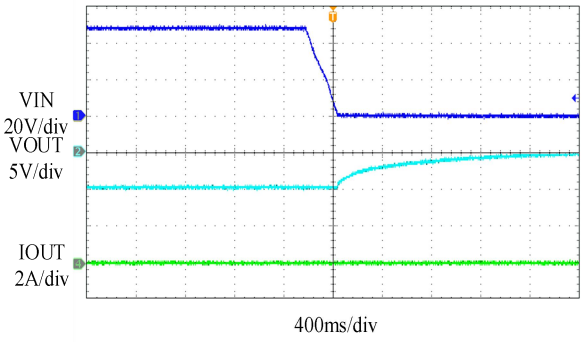
VIN Start-up

I_{OUT}=4A



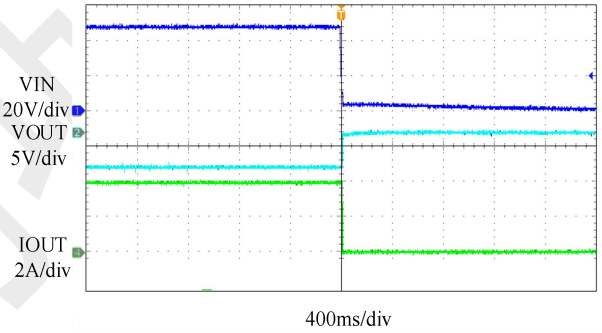
VIN Shutdown

I_{OUT}=0A



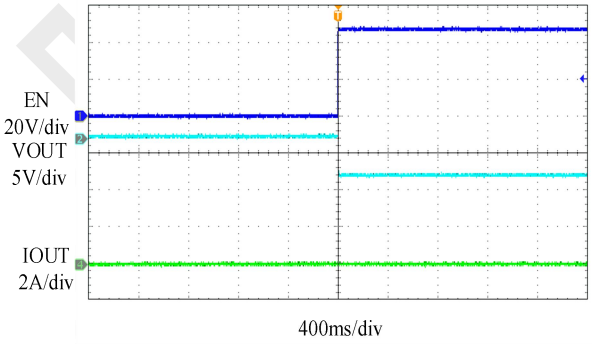
VIN Shutdown

I_{OUT}=4A



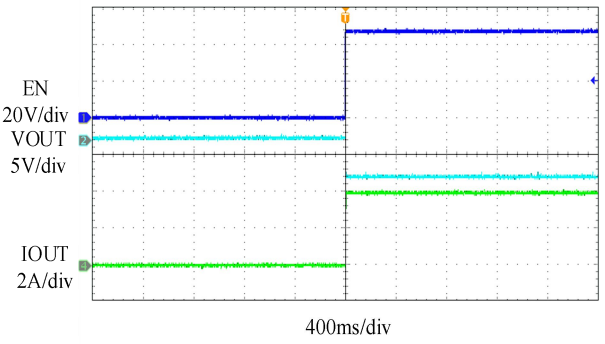
EN Start-up

I_{OUT}=0A



EN Start-up

I_{OUT}=4A

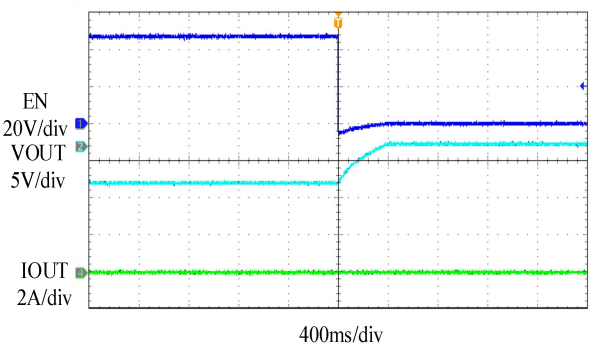


TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=48V, T_A=25℃, FCCM, F_{SW}=500kHz, V_{OUT}=−5V, unless otherwise noted.

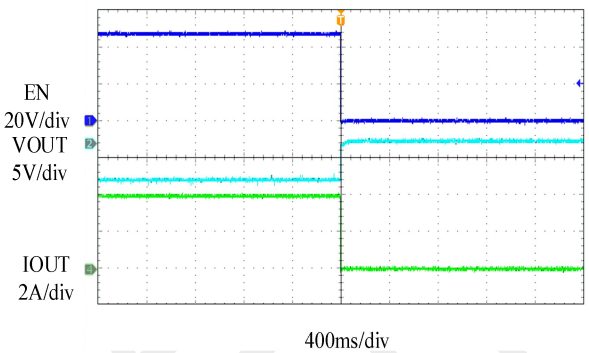
EN Shutdown

I_{OUT}=0A



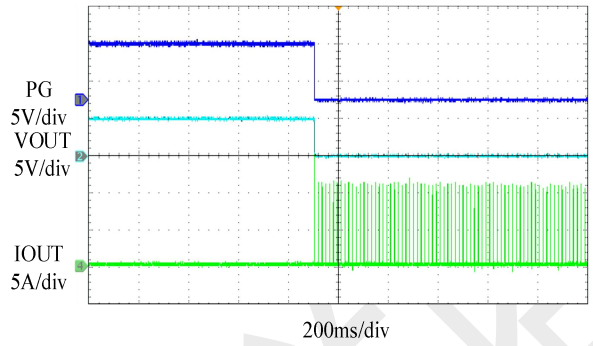
EN Shutdown

I_{OUT}=4A



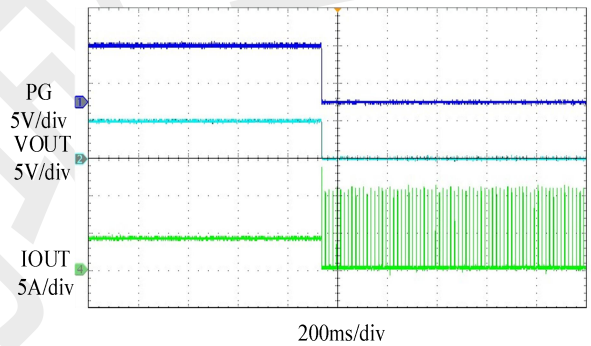
SCP Entry

I_{OUT}=0A



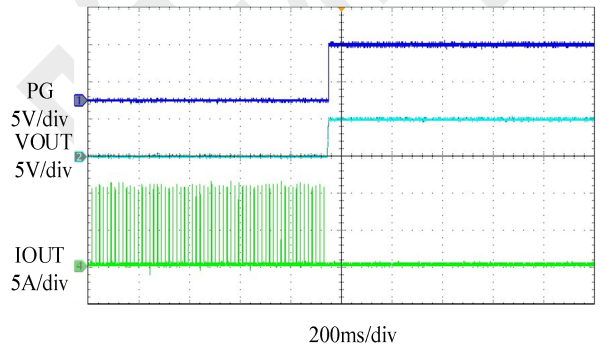
SCP Entry

I_{OUT}=4A



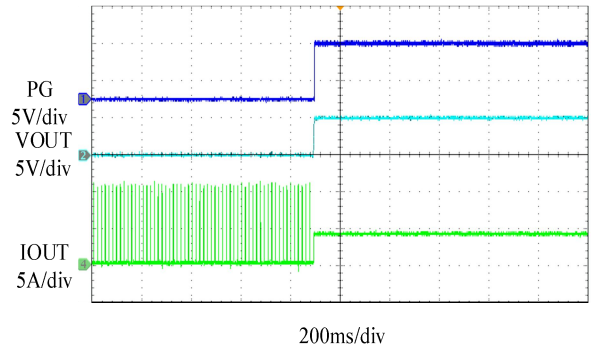
SCP Recovery

I_{OUT}=0A



SCP Recovery

I_{OUT}=4A

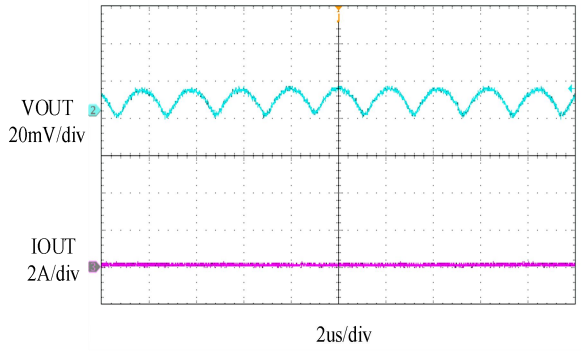


TYPICAL PERFORMANCE CHARACTERISTICS (NEGATIVE OUTPUT)

V_{IN}=48V, T_A=25℃, FCCM, F_{SW}= 500kHz, V_{OUT}=−5V, unless otherwise noted.

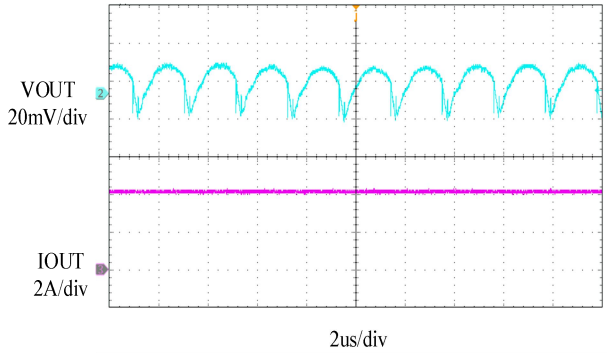
VOUT Ripple

I_{OUT}=0A



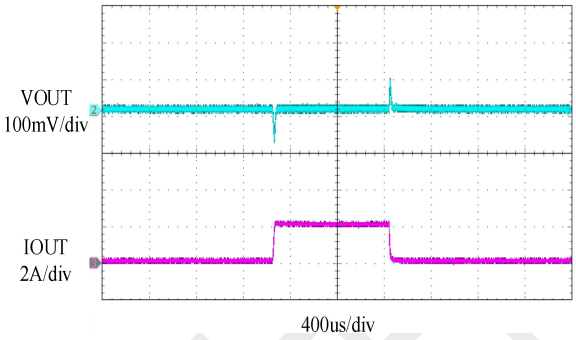
VOUT Ripple

I_{OUT}=4A



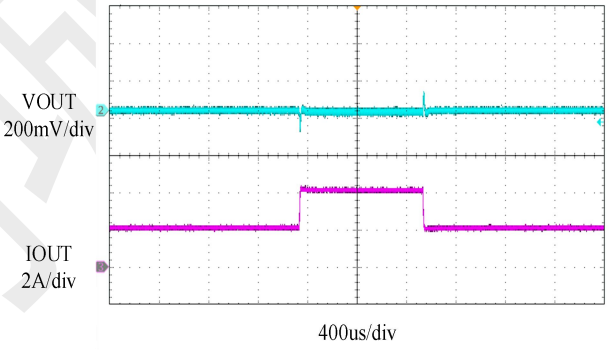
Load Transient

I_{OUT}=0A to 2A, 2.5A/μs



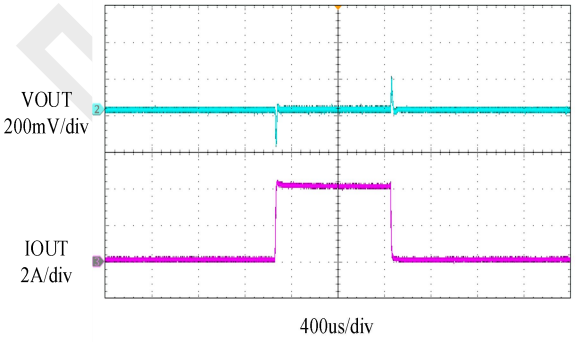
Load Transient

I_{OUT}=2A to 4A, 2.5A/μs



Load Transient

I_{OUT}=0A to 4A, 2.5A/μs



OPERATION

The M8005 is a 5A synchronous step-down switching mode Power SoC with integrated High-Side and Low-Side power MosFETs, inductor and passives in LGA-63 package. Particularly, the integrated input decoupling capacitor of M8005 effectively minimizes the parasitic inductance of input circuit and reduces the voltage spike on switching pin, thereby, simplifying the PCB layout.

M8005 employs the voltage mode control architecture to achieve accurate voltage output. M8005 provides excellent load regulation at both DEM and FCCM dependent upon selection. For optimal efficiency and performance in general application, the switching frequency of M8005 is fixed at 500kHz.

M8005 integrates full protection features including OCP, OVP, UVP and OTP, meanwhile, all these faults can be indicated by PGOOD. The protection functions are detailed below.

OVER CURRENT PROTECTION (OCP)

M8005 implements a cycle-by-cycle Low-Side valley current limit protection to prevent inductor from saturation. When the Low-Side switch reaches the current limit, M8005 will enter hiccup mode.

If M8005 detects an over-current condition for 512 consecutive cycles, or if V_{FB} drops below the UVP threshold, the device enters hiccup mode. In hiccup mode, the M8005 latches off the High-Side MOSFET immediately and latches off the Low-Side MOSFET after zero-current cross detection (ZCD). For every 8192-cycles period, M8005 automatically attempts to soft start. If the over-current state diminishes, the M8005 restores normal operation, otherwise, the hiccup mode remains.

OVER TEMPERATURE PROTECTION（OTP）

M8005 will stop switching when the junction temperature exceeds 175 ℃. The device will power up again as the junction temperature drops below 155℃.

APPLICATION INFORMATION (POSITIVE OUTPUT)

Output Voltage

The output voltage of M8005 can be set by an external feedback resistor divider as Figure 1. The output voltage can be set according to the following equation:

$$V_{OUT}=V_{FB}\frac{R_1//R_{UP}+R_2//R_{DOWN}}{R_2//R_{DOWN}}$$

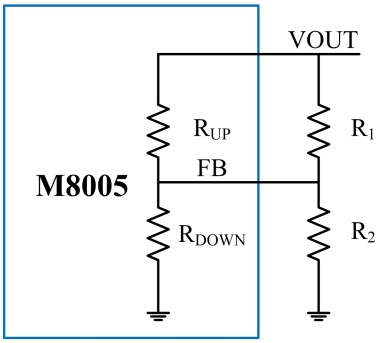


Figure 1: Typical FB Connection of M8005

Table 3 lists the recommended FB resistor values for common output voltages.

Table 3: FB Resistor Values for Common Output Voltages

P/N	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	R_{UP} (kΩ)	R_{DOWN} (kΩ)
M8005	3.3	16	NC	10.5	2
	5	NC	NC		
	9	NC	2.1		
	12	NC	1.2		

Input Capacitor Selection

The input current of the step-down converter is discontinuous with sharp edges; therefore, putting filter capacitors is necessary. For better performance, low ESR ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their lowest temperature variations. The RMS current of the input capacitors is calculated according to:

$$I_{CIN\_RMS}=I_{OUT}\cdot\sqrt{D(1-D)}$$

in which D is the Duty Cycle and I_{OUT} is the output load current, when the current is continuous, $D=V_{OUT}/V_{IN}$. Mathematically, when D is 0.5, the largest RMS current is:

$$I_{CIN\_RMS}=\frac{I_{OUT}}{2}$$

So, it is recommended to choose capacitors with their RMS current rating higher than 1/2 I_{OUT}.

Therefore, the maximal power dissipation on the input capacitors can be estimated with the RMS current and the ESR.

A small size 0.1μF ceramic capacitor has been internally placed close to VIN and GND in M8005 already. The input voltage ripple caused by the VIN capacitors can be calculated as:

$$\Delta V_{CIN}=\frac{I_{OUT}}{F_{SW}\cdot C_{IN}}\cdot\frac{V_{OUT}}{V_{IN}}\cdot(1-\frac{V_{OUT}}{V_{IN}})$$

in which, F_{SW} is switching frequency of 500kHz and C_{IN} is the sum of the input capacitance.

Output Capacitor Selection

Output capacitors are required to keep output voltage stable. To minimize the output voltage ripple, low ESR ceramic capacitors should be used. The output voltage ripple can be estimate as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\cdot F_{SW}{}^2\cdot C_{OUT}\cdot L}\cdot(1-\frac{V_{OUT}}{V_{IN}})$$

In which, L is the inductance fixed at 5.6μH internally and C_{OUT} is the total capacitance of the output capacitors.

If electrolytic or tantalum capacitors are used, the ESR will dominate the output voltage ripple as:

$$\Delta V_{OUT}=R_{ESR}\cdot\frac{V_{OUT}}{F_{SW}\cdot L}\cdot(1-\frac{V_{OUT}}{V_{IN}})$$

Where R_{ESR} is the ESR of the used electrolytic or tantalum capacitors.

Enable Control

The operation of M8005 can be tuned by pulling the EN pin:

(1) V_{EN} < 0.8V, shutdown mode, VIN-to-VCC LDO shutdowns;

(2) 0.8V≤V_{EN}<1.2V, standby mode, VIN-to-VCC LDO is regulated to 7.5V;

(3) V_{EN}>1.2V, operating mode, the chip starts to operate properly;

This tri-state control significantly reduces quiescent loss. EN pin can also be used to program the UVLO, a resistor divider can be used according to:

$$V_{IN\_UVLO} = V_{EN\_R} \cdot \frac{R_{EN\_UP} + R_{EN\_DOWN}}{R_{EN\_DOWN}}$$

where V_{EN_R} is 1.2V.

Mode Selection

M8005 is preferred to work on FCCM by connecting SYNCI to VCC for better VOUT ripple and load transient. M8005 can also work on DEM if SYNCI is floating or tied to GND.

Clock Synchronization (SYNCI)

There are three functions of SYNCI. When SYNCI is floating or tied to GND, M8005 operates in DEM. When SYNCI is connected to an external clock synchronization signal, the switching frequency is determined by this external clock signal and FCCM is activated instead. The switching frequency close to 500k is strongly recommended for best performance. When SYNCI is connected to a voltage rail between 7.5V to 14V or VCC, M8005 works in FCCM at default 500kHz.

Power Good Indicator

M8005 provides a PGOOD flag pin to indicate whether the output voltage is within the regulation tolerance. This PGOOD open-drain output requires a pull-up resistor to VCC or a stable DC source. The typical range of pull-up resistance is about 10kΩ to 100kΩ. If necessary, a resistor divider to a high voltage (>14V) rail is also applicable. When the FB voltage exceeds 95% of the reference, the internal switch will be turned off and PGOOD will be pulled high by the pull-up resistor. If the FB voltage falling below 92% of the reference or rising above 108% of the reference, that switch will be turned on and PGOOD is pulled low, indicating the output voltage out of regulation. Besides fault protection and output monitoring, the PGOOD can be applied in setting start-up sequencing of downstream converters, MCU and other devices.

Soft Start Time

The M8005 enters into soft-start immediately after EN exceeds its rising threshold of 1.2V. The default soft-start time is 3.8ms. The time can be increased by adding an external capacitor C_{SS} between SS and GND. The required C_{SS} for a targeted T_{SS} can be calculated as:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \cdot 10(\mu A)}{0.8(V)} - 47(nF)$$

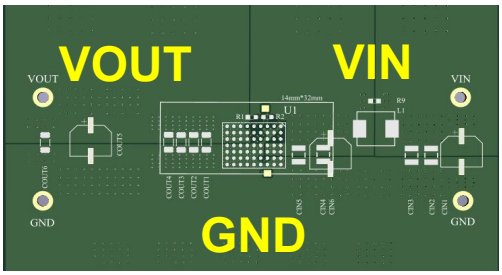
If an external voltage source is connected to the SS pin, the aforementioned internal soft-start capability of the M8005 is disabled. The regulated output voltage rising follows the rising function of external SS when the REF/SS pin is below 0.8V.

PCB Layout Guide

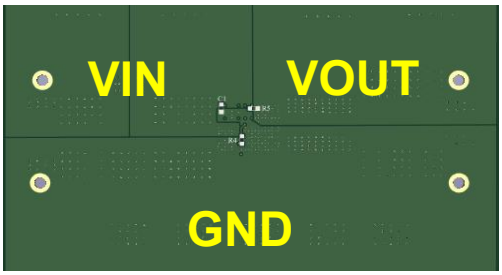
To optimize the electrical and thermal performance, some PCB layout guidelines should be considered as below:

1. Use wide trace for the high current paths and keep it as short as possible. It helps to minimize the PCB conduction loss and thermal stress.
2. Place the input decoupling capacitor close to VIN and GND.
3. Connect all feedback networks to FB shortly and directly and keep it as close to the Power IC as possible.
4. The GND should be connected to a strong ground plane for better heat dissipation and noise protection.

Figure 2 gives a good example of the recommended layout.



(a) Top Layer



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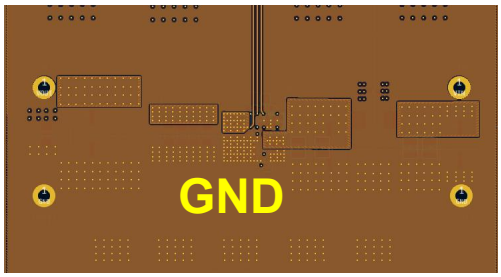
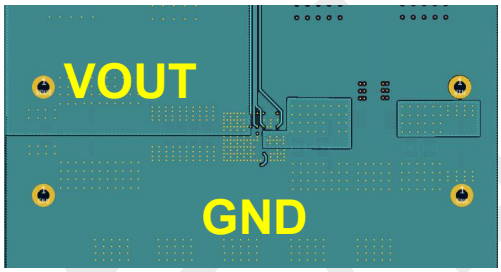


(c) Inner Layer 1



(d) Inner Layer 2

Figure 2.Recommended Positive Output Layout

APPLICATION INFORMATION (NEGATIVE OUTPUT)

Capacitor Selection for Negative Output Buck-Boost Converter

To realize stable negative output, extra capacitors between V_{IN} and V_{OUT} are recommended, which can be treat as the C_{IO} in general negative output buck-boost converters. Typically, this C_{IO} consists of one or two ceramic capacitors.

Similar to positive output usage, input capacitors are required to connect V_{IN} and GND. However, to accordingly calculate the input voltage ripple ΔV_{CIN}, the following equation must be used instead,

$$\Delta V_{CIN}=\frac{I_{OUT}}{F_{SW}\cdot C_{IN}}\cdot\frac{|V_{OUT}|}{V_{IN}+|V_{OUT}|}\cdot\left(1-\frac{|V_{OUT}|}{V_{IN}+|V_{OUT}|}\right),$$

Regarding output capacitors, they are required to supply current when Low-Side switch off in negative output application. Thereby, a minimum capacitance is requisite to fulfill this job, which can be determined by the following equation,

$$C_{OUT}=\frac{I_{OUTMAX}}{F_{SW}\Delta V_{OUT}}\cdot\frac{|V_{OUT}|}{V_{INMIN}+|V_{OUT}|},$$

where V_{INMIN} and I_{OUTMAX} are the minimum input voltage and maximum output current of a desired scenario, respectively, as well as the pre-defined absolute value of output voltage $|V_{OUT}|$ and output voltage ripple threshold.

Once the output capacitance is determined, the actual output voltage ripple in a particular condition can be estimated by

$$\Delta V_{OUT}=\frac{I_{OUT}}{F_{SW}C_{OUT}}\cdot\frac{|V_{OUT}|}{V_{IN}+|V_{OUT}|}.$$

In addition, the output capacitors should be placed between V_{OUT} and GND directly.

Enable Control for Negative Output

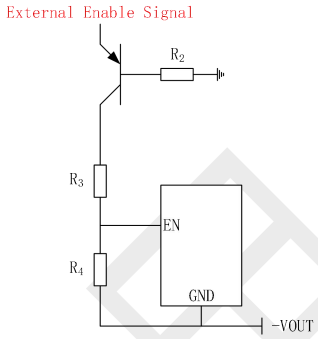


Figure 3. Enable Control Circuit for Negative Output

The circuit in Figure 3 is used to convert the external enable signal into appropriate EN control for negative output application. A negative EN signal is necessary to shut down the chip in negative output application, while a positive low signal is always applied in practice. Thus, this circuit ensures that pulling external enable signal generally low can shut the chip down.

Power Good Indicator for Negative Output

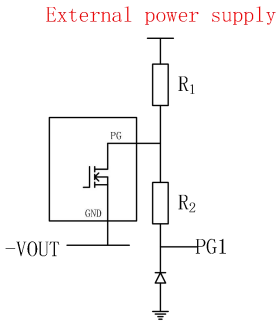


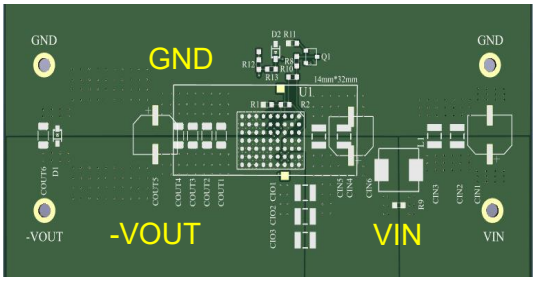
Figure 4. Power Good Indication circuit for Negative Output

The circuit in Figure 4 replaces the original PG pin with PG1 for correct Power Good indication. The PG is in fact floating at well-undefined value when the negative VOUT application works appropriately. To resolve this situation, the circuit above ensures PG1 still outputs in accordance with the External power supply but maintains low if the chip works abnormal.

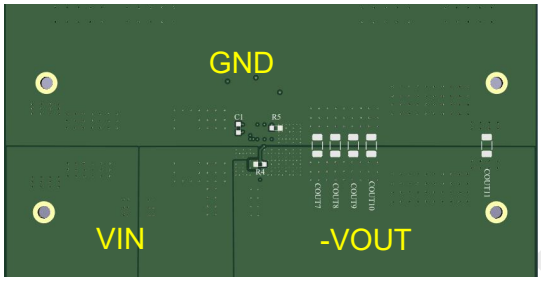
Be sure to check the Absolute Maximum Rating of PG.

PCB Layout Guide

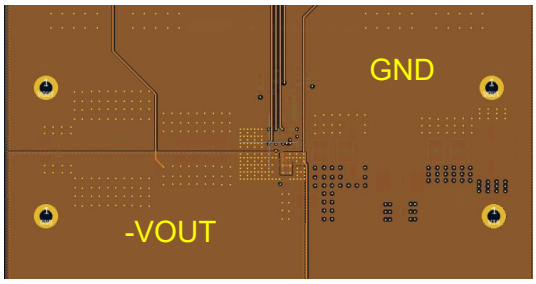
Those PCB layout guidelines elaborated in the previous positive output session can be applied in negative output scenario. Figure 5 demonstrates a good example for negative output layout.



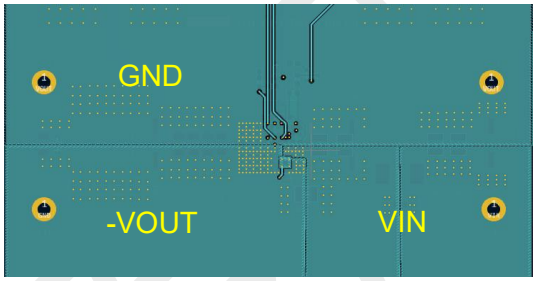
(a) Top Layer



(b) Bottom Layer



(c) Inner Layer2



(d) Inner Layer2

Figure 5.Recommended Negative Output Layout

TYPICAL APPLICATION

Positive Output

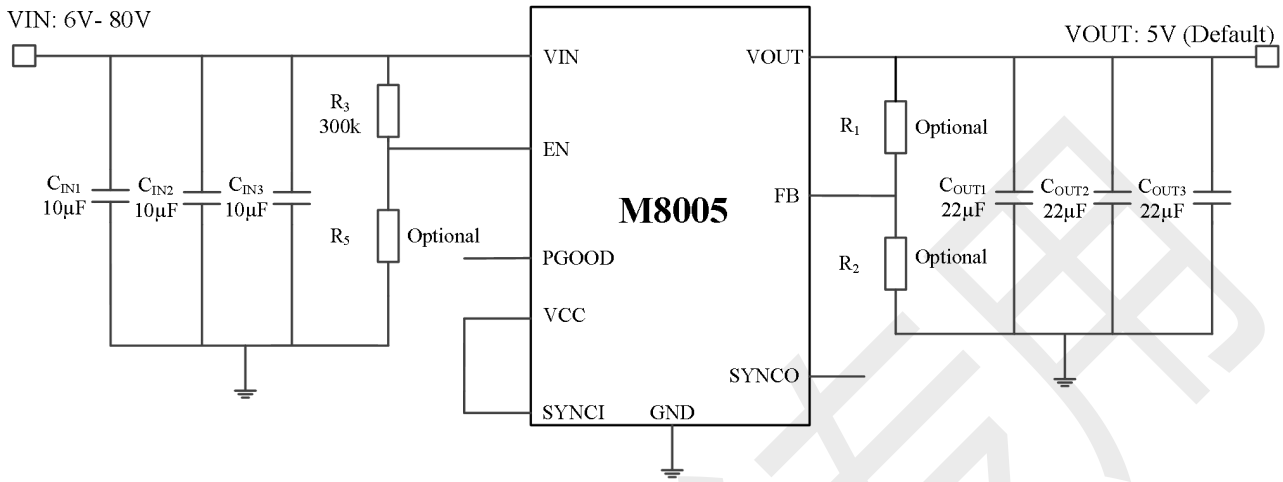


Figure 6.Typical Application Circuits of M8005 for positive output

Table 4: M8005 Reference Design for Typical Output

VOUT	CIN	COUT	R1	R2
3.3V	3×10uF	3×22uF	16kΩ	NC
5V	3×10uF	3×22uF	NC	NC
12V	3×10uF	6×22uF	NC	1.2kΩ
24V	3×10uF+47uF E-Cap	3×10uF+100uF E-Cap	NC	440Ω
28V	3×10uF+47uF E-Cap	3×10uF+100uF E-Cap	NC	365Ω

NOTES:

The output voltage can be programmed by the top feedback resistor R_1 and bottom feedback resistor R_2 from 0.8V to 32V.

TYPICAL APPLICATION (continued)

Negative Output

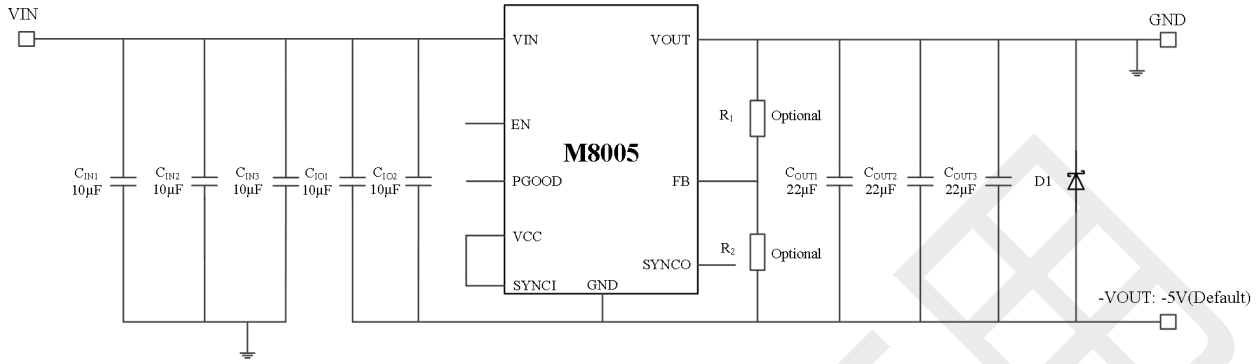


Figure 7.Typical Application Circuits of M8005 for Negative Output

Table 5: M8005 Reference Design for Negative Output

VOUT	CIN	COUT	CIO	R1	R2
−3.3V	3×10uF	3×22uF	2×10uF	16kΩ	NC
−5V	3×10uF	3×22uF	2×10uF	NC	NC
−12V	3×10uF	5×22uF	2×10uF	NC	1.2kΩ
−24V	3×10uF+47uF E-Cap	3×10uF+100uF E-Cap	2×10uF	NC	440Ω
−28V	3×10uF+47uF E-Cap	3×10uF+100uF E-Cap	2×10uF	NC	365Ω

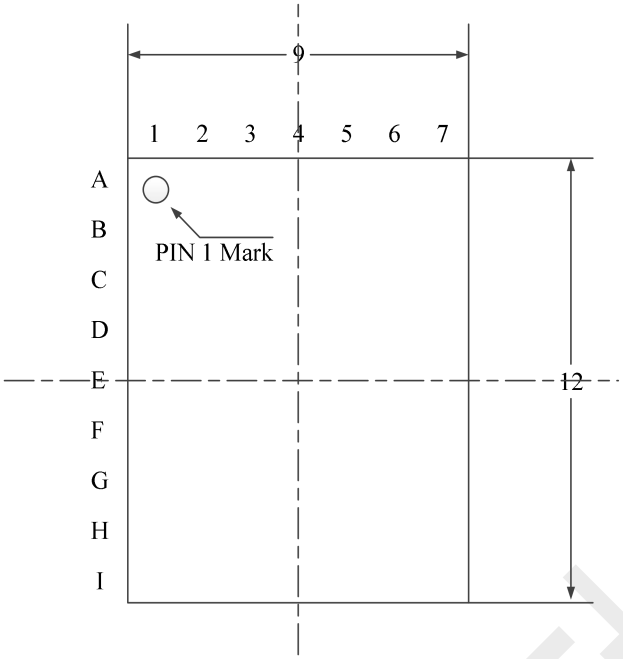
NOTES:

Please refer to the part of APPLICATION INFORMATION (NEGATIVE OUTPUT) for the design of EN control circuit and PG level shift circuit.

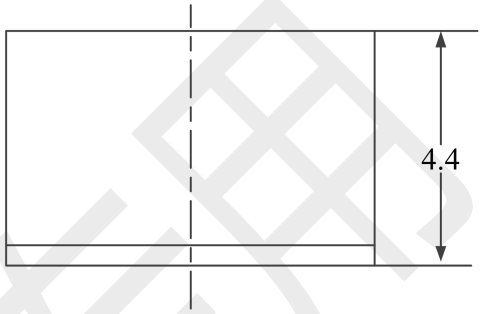
PACKAGE INFORMATION

LGA-63 (9mm×12mm×4.4mm) Package

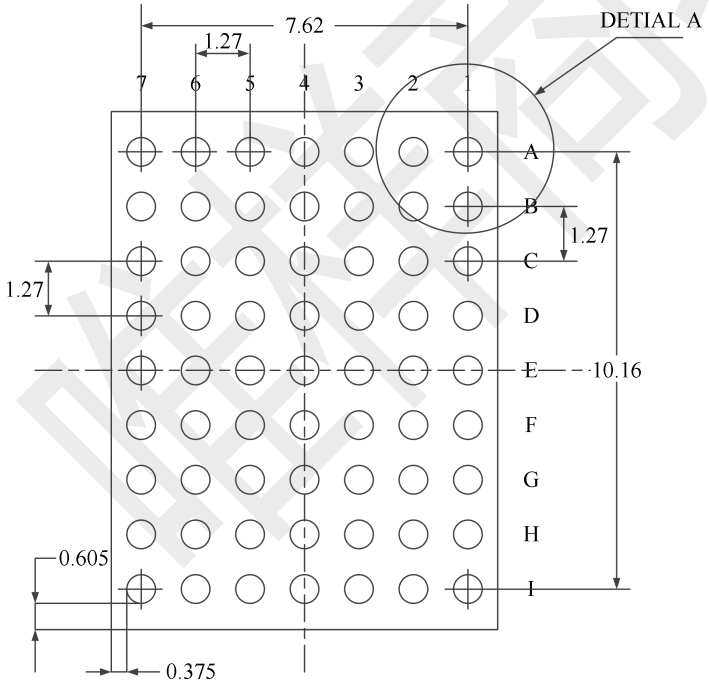
TOP VIEW



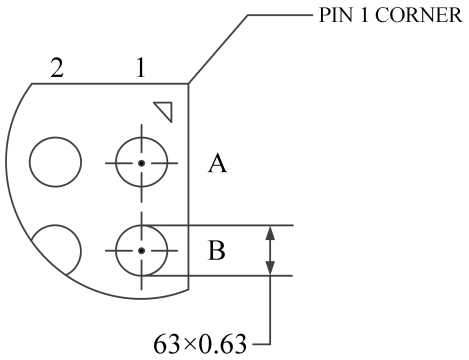
BOTTOM SIDE VIEW



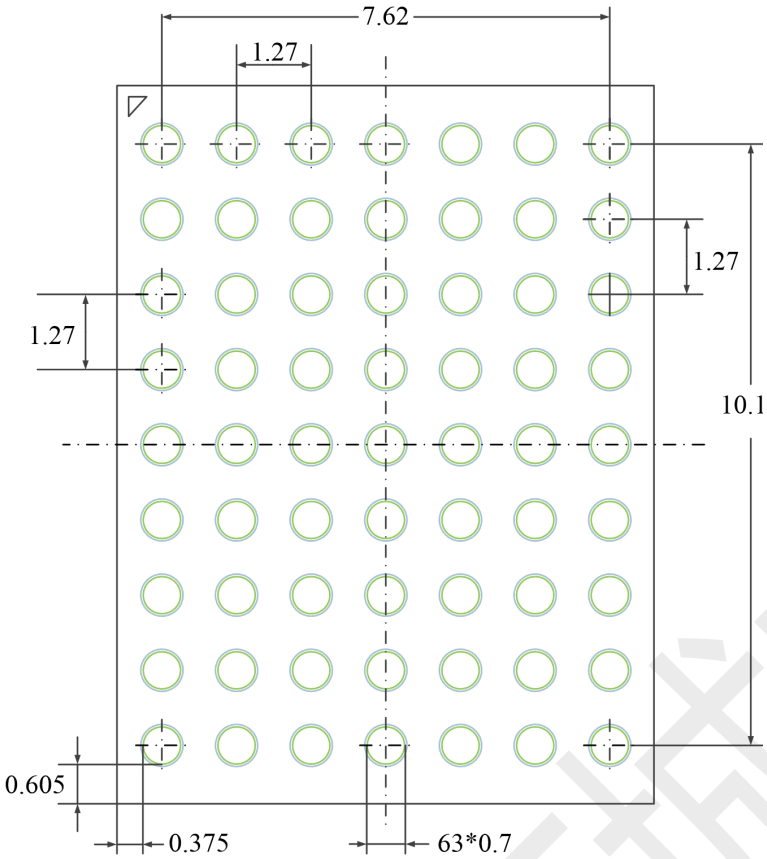
BOTTOM VIEW

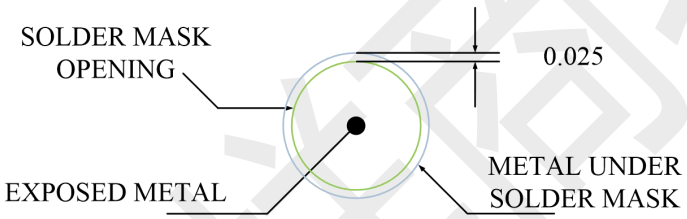


DETIAL A



RECOMMENDED LAND PATTERN





NOTES:

All dimensions are in MM.

单击下面可查看定价，库存，交付和生命周期等信息

>>iModule(沃芯)