GENERAL DESCRIPTION

The MXC3420AL is a small form factor, integrated digital output 3-axis accelerometer with a feature set optimized for industry applications, likes industry automatic control, device motion and tilt monitoring, remote controls, robot controls, etc.

The MXC3420AL features a dedicated motion block which implements algorithms to support “any motion” and shake detection, tilt/flip and tilt 35 position detection.

Low power consumption and small size are inherent in the monolithic fabrication approach, where the MEMS accelerometer is integrated in a single-chip with the electronics integrated circuit.

In the MXC3420AL the internal sample rate can be set from 128 to 1024 samples / second. The device supports the reading of sample and event status via polling or interrupts.

FEATURES

Range, Sampling & Power

- ±2, ±4, ±8, ±12, ±16g range
- 16-bit resolution
- 128 to 1024 Output Data Rate
- 4 μA typical Standby current
- Low typical active current

Simple System Integration

- I2C interface, up to 1 MHz
- 2×2×0.92 mm 12-pin LGA package
- High reliability thru single-chip 3D silicon MEMS technology
- Mechanical Shock 20000G
- RoHS compliant

Applications

- Industrial automatic control
- Smart robot controls
- Motion and tilt monitoring
- Remote controls
- Alarm module

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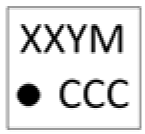
1 ORDER INFORMATION

Table 1. Order Information

Part Number	Resolution	Order Number	Package	Shipping
MXC3420AL	16-bit	MXC3420AL	VLGA-12	Tape & Reel, 10Ku



Row	Marking
XXYM	Device identifier and date code
CCC	Factory lot code
●	Pin 1 identifier

Table 2. Package Information

2 FUNCTIONAL BLOCK DIAGRAM

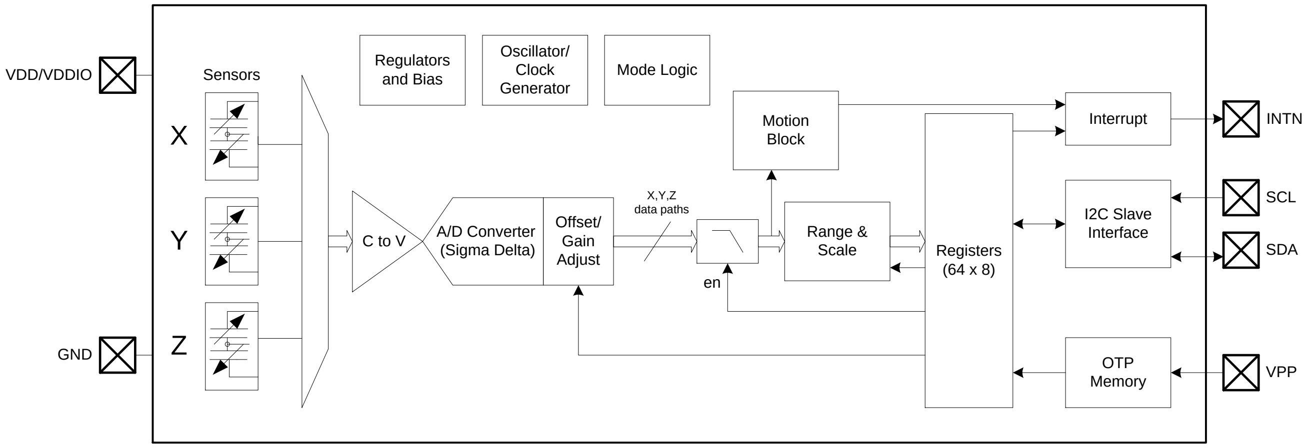
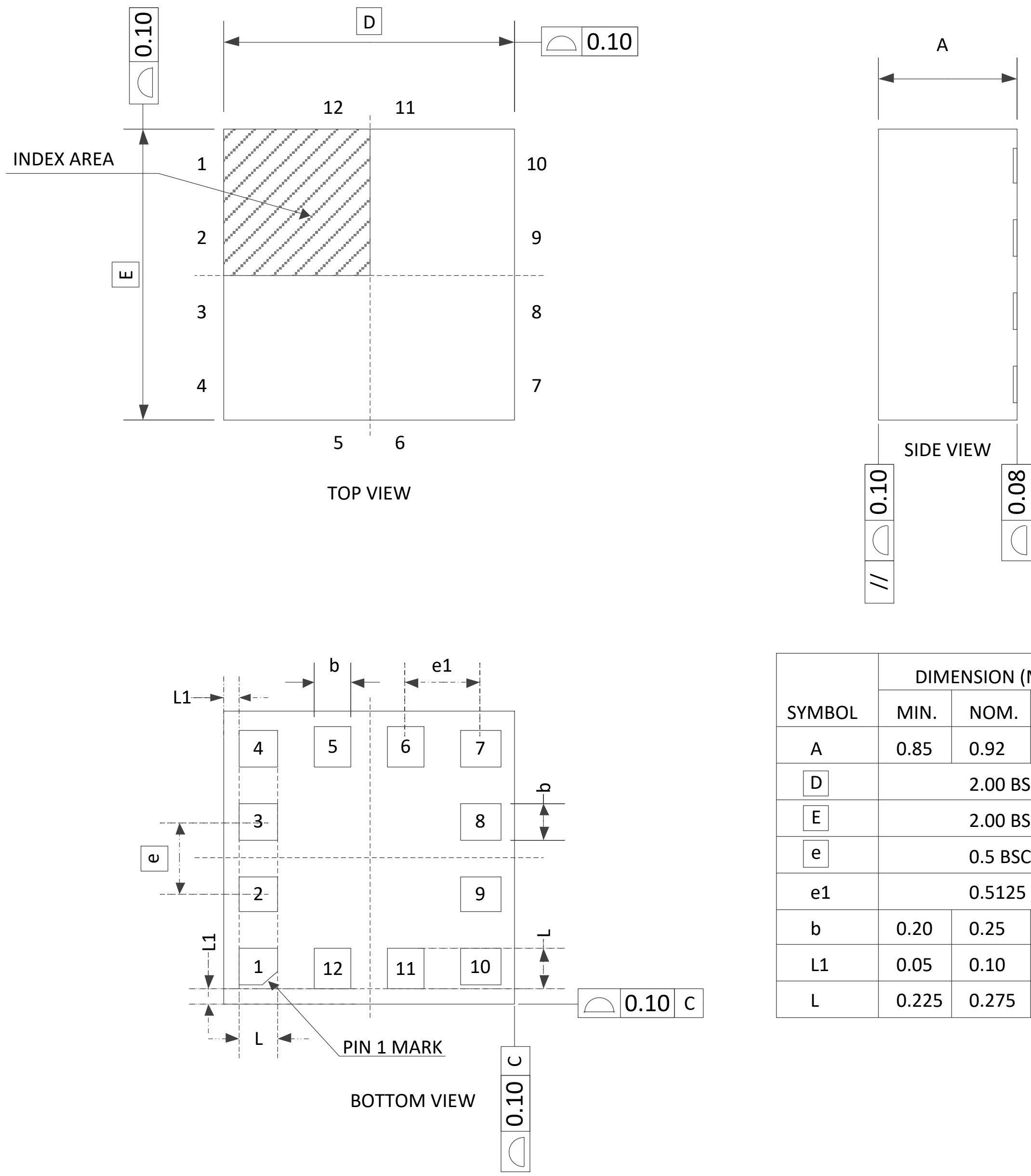


Figure 1. Block Diagram

3 PACKAGING AND PIN DESCRIPTION

3.1 PACKAGE OUTLINE



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.85	0.92	1.00
D	2.00 BSC		
E	2.00 BSC		
e	0.5 BSC		
e1	0.5125 REF		
b	0.20	0.25	0.30
L1	0.05	0.10	0.15
L	0.225	0.275	0.325

Figure 2. Package Outline and Mechanical Dimensions

3.2 PACKAGE ORIENTATION

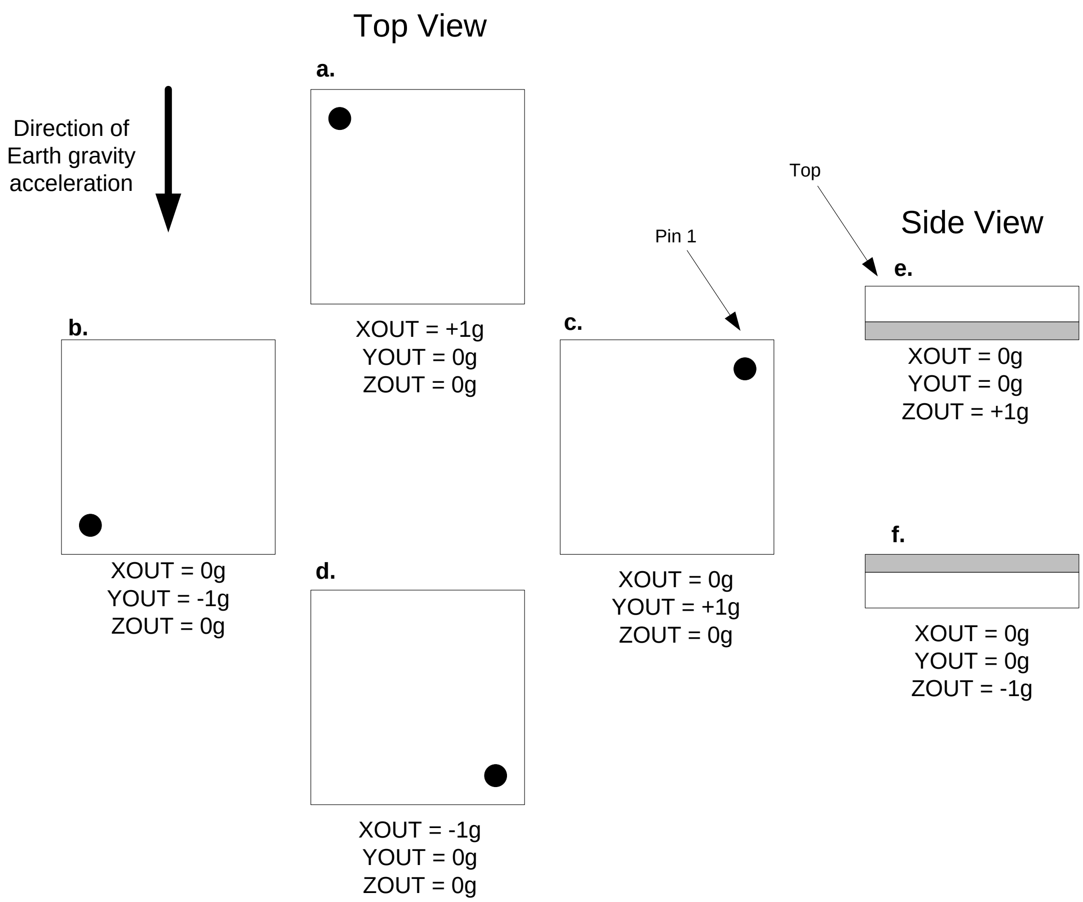


Figure 3. Package Orientation

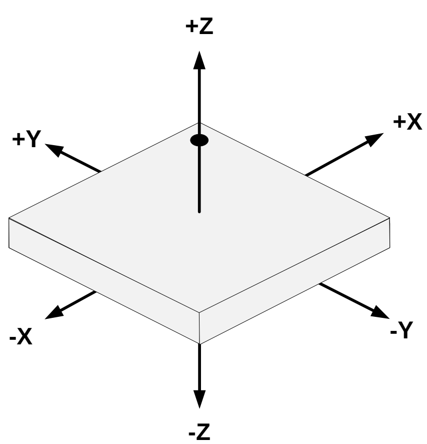


Figure 4. Package Axis Reference

3.3 PIN DESCRIPTION

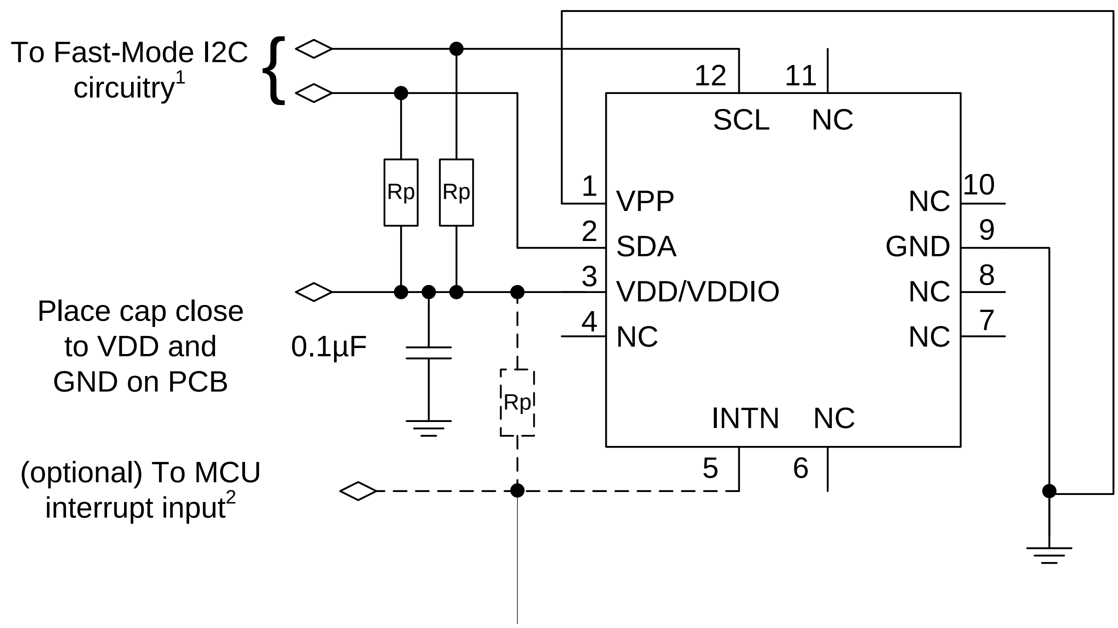
Pin	Name	Function
1	VPP	Connect to GND
2	SDA [1]	I2C serial data input/output
3	VDD/VDDIO	Power supply
4	NC	No connect
5	INTN [2]	Interrupt active LOW [3]
6	NC	No Connect
7	NC	No Connect
8	NC	No Connect
9	GND	Ground
10	NC	No Connect
11	NC	No connect
12	SCL [1]	I2C serial clock input

Table 3. Pin Description

Notes:

1) This pin requires a pull-up resistor, typically 4.7kΩ to pin VDD/VDDIO. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.
2) This pin can be configured by software to operate either as an open-drain output or push-pull output (**mode register**). If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to VDD/VDDIO.
3) INTN pin polarity is programmable in the **mode register**.

3.4 TYPICAL APPLICATION CIRCUITS



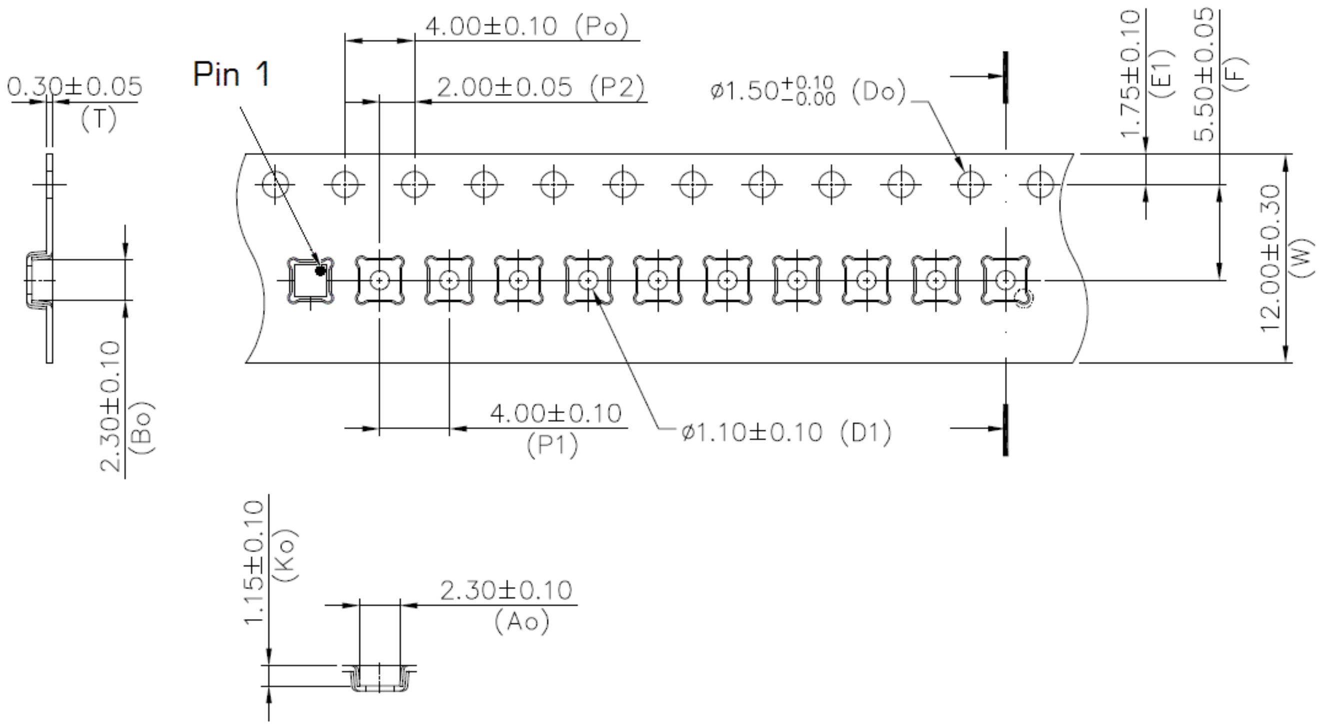
NOTE[1]: Rp are typically 4.7kΩ pullup resistors to VDD/VDDIO, per I2C specification. When pin VDD/VDDIO is powered down, SDA and SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 5. Typical Application Circuit for 3DOF Solution

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the sensor. Therefore, for some applications a lower-noise power supply might be desirable to power the VDD/VDDIO pin.

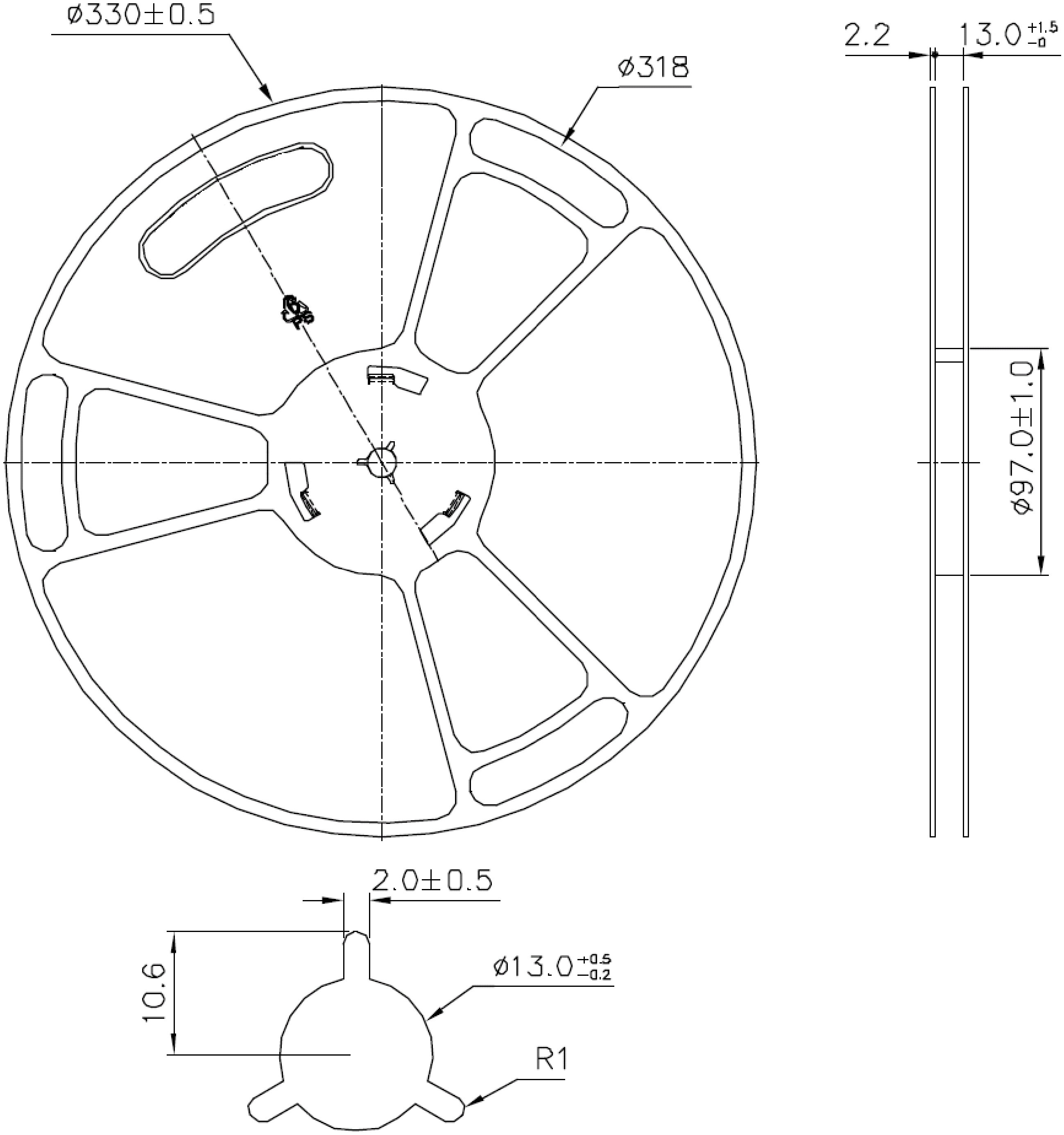
3.5 TAPE AND REEL

Devices are shipped in reels, in standard cardboard box packaging. See **Figure 6. MXC3420AL Tape Dimensions** and **Figure 7. MXC3420AL Reel Dimensions**.



- Dimensions in mm.
- 10 sprocket hole pitch cumulative tolerance ±0.2
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 6. MXC3420AL Tape Dimensions



- Dimensions in mm.

Figure 7. MXC3420AL Reel Dimensions

3.6 SOLDERING PROFILE

The LGA package follows the reflow soldering classification profiles described in *Joint Industry Standard, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices*, document number J-STD-020E. Reflow soldering has a peak temperature (T_p) of 260^{o}C

3.7 SHIPPING AND HANDLING GUIDELINES

Shipping and handling follow the standards described in *Joint Industry Standard, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*, document number J-STD-033C.

The following are additional handling guidelines (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- While the mechanical sensor is designed to handle high-g shock events, direct mechanical shock to the package should be avoided.
- SMT assembly houses should use automated assembly equipment with either plastic nozzles or nozzles with compliant tips (for example, soft rubber or silicone).
- Avoid g-forces beyond the specified limits during transportation.
- Handling and mounting of sensors should be done in a defined and qualified installation.

3.8 MOISTURE SENSITIVITY LEVEL CONTROL

The following are storage recommendations (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- Store the tape and reel in the *unopened* dry pack, until required on the assembly floor.
- If the dry pack has been opened or the reel has been removed from the dry pack, reseal the reel inside of the dry pack with a black protective belt. Avoid crushing the tape and reel.
- Store the cardboard box in a vertical position.

4 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Rating	Symbol	Minimum / Maximum Value	Unit
Supply Voltages	Pin VDD/VDDIO	-0.3 / +3.6	V
Acceleration, any axis, 200 µs	g_{MAX}	20000	g
Ambient operating temperature	T_{OP}	-40 / +105	^{0}C
Storage temperature	T_{STG}	-40 / +150	^{0}C
ESD human body model	HBM	± 4000	V
Latch-up current at T_{op} = 25 ^{0}C	I_{LU}	200	mA
Input voltage to non-power pin	Pins INTN, SCL and SDA	-0.3 / (VDD + 0.3) or 3.6 whichever is lower	V

Table 4. Absolute Maximum Ratings

4.2 SENSOR CHARACTERISTICS

VDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Acceleration range			±2.0 ±4.0 ±8.0 ±12.0 ±16.0		g
Sensitivity	Acceleration range = ±2.0g		16384		LSB/g
	Acceleration range = ±4.0g		8192		
	Acceleration range = ±8.0g		4096		
	Acceleration range = ±12.0g		2730		
	Acceleration range = ±16.0g		2048		
Sensitivity Temperature Coefficient [1]	-40 ≤ T_{op} ≤ +85 ^{0}C		±0.015		%/^{0}C
Zero-g Offset	Chip Level Board Level		±20 ±50		mg
Zero-g Offset Temperature Coefficient [1]	-40 ≤ T_{op} ≤ +85 ^{0}C		±0.5		mg/^{0}C
RMS Noise	ODR = 1024		0.8 (X,Y) 1.5 (Z)		mg RMS
Nonlinearity [1]	Acceleration range = ±2.0g		0.4		% FS
Cross-axis Sensitivity [1]	Between any two axes		±1		%
ODR, Output Data Rate		128		1024	Hz
[1] Values are based on device characterization, not tested in production.					

Table 5. Sensor Characteristics

4.3 ELECTRICAL AND TIMING CHARACTERISTICS

4.3.1 ELECTRICAL POWER AND INTERNAL CHARACTERISTICS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Supply voltage [1]	Pin VDD/VDDIO	VDD	1.7		3.6	V
Sample Rate Tolerance [2]		Tclock	-2		2	%

[1] Min and Max limits are hard limits without additional tolerance.

[2] Values are based on device characterization, not tested in production.

Test condition: VDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Standby current			4		µA
WAKE state current	ODR = 128 Hz		73		µA
Pad Leakage	Per I/O pad	-1	0.01	1	µA
Wake-Up time			3		ms
Start-Up time			1/ODR+1mS		ms

Table 6. Electrical Characteristics

4.3.2 I2C ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	VIL	-0.5	0.3*VDD	V
HIGH level input voltage	VIH	0.7*VDD	-	V
Hysteresis of Schmitt trigger inputs	Vhys	0.05*VDD	-	V
Output voltage, pin INTN, Iol ≤ 2 mA	Vol Voh	0 0	0.4 0.9*VDD	V V
Output voltage, pin SDA (open drain), Iol ≤ 1 mA	Vols	-	0.1*VDD	V
Input current, pins SDA and SCL (input voltage between 0.1*VDD and 0.9*VDD max)	Ii	-10	10	µA
Capacitance, pins SDA and SCL [1]	Ci	-	10	pF
[1] Values are based on device characterization, not tested in production.				

Table 7. I2C Electrical and Timing Characteristics

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL should exist. Also, care must be taken to not violate the I2C specification for capacitive loading.
- When pin VDD/VDDIO is not powered and set to 0V, INTN, SDA and SCL will be held to VDD plus the forward voltage of the internal static protection diodes, typically about 0.6V.
- When pin VDD/VDDIO is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.

4.3.3 I2C TIMING CHARACTERISTICS

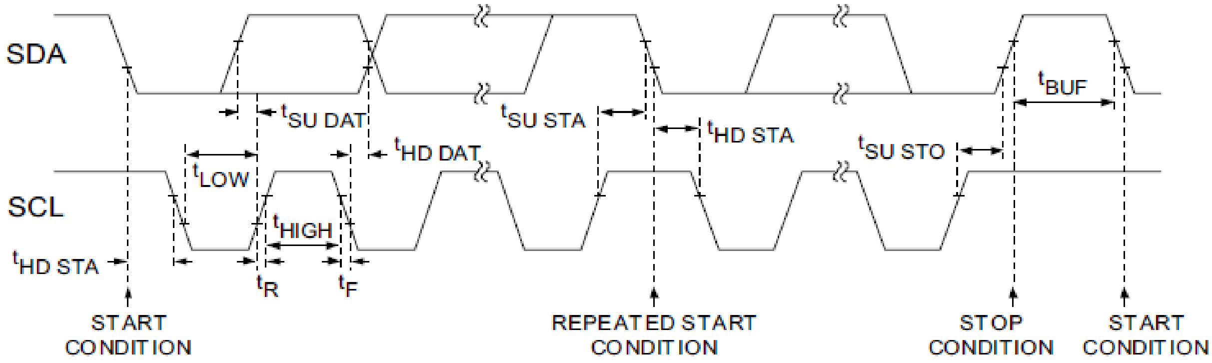


Figure 8. I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD; STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	Data hold time	5.0	-	-	-	-	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	50	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	0.5	-	µs

Table 8. I2C Timing Characteristics

NOTE: Values are based on I2C Specification requirements, not tested in production.

See also Section 10.3 **I2C Message Format**.

5 GENERAL OPERATION

The device supports the reading of samples and device status upon interrupt or by polling.

5.1 SENSOR SAMPLING

In the WAKE state, acceleration data for X, Y, and Z axes is sampled at a rate between 31 and 998 samples/second. See the **Sample Rate Register** section.

The detectable acceleration range is variable and is set in the RANGE bits of the **range and scale control register**.

Resolution	Acceleration Range	Value per bit (mg/LSB)	Full Scale Negative Reading	Full Scale Positive Reading	Comments
16-bit	± 2g	~.061	0x8000 (-32768)	0x7FFF (+32767)	Signed 2's complement number, results in XOUT, YOUT, ZOUT. The MSB is the sign bit. (Integer interpretation also shown)
	± 4g	~.122			
	± 8g	~.244			
	± 12g	~.366			
	± 16g	~.488			

Table 9. Summary of Resolution, Range, and Scaling

5.2 OFFSET AND GAIN CALIBRATION

Digital offset and gain calibration can be performed on the sensor, if necessary, in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values.

6 OPERATIONAL STATES

The device has two states of operation: STANDBY and WAKE. All states are controlled by the software, there is no automatic power control.

The device defaults to the STANDBY state following a power-up and must be in the WAKE state before executing a reset.

The time to change from the STANDBY to WAKE state takes one sample period (takes less than 10 µs).

State	I2C Bus	Description
STANDBY	R/W	• Lowest power consumption • Internal clocking is halted • No motion detection, sampling, or calibration • The I2C bus can read and write to registers (resolution, range, thresholds and other settings can be changed) • Reset not allowed • Default state after a power-up
WAKE	R[1]	• Highest power consumption • Internal clocking is enabled • Continuous motion detection and sampling; automatic calibration is available • The I2C bus can only write to the mode register[1] and read all other registers • Reset allowed
[1] If the unlock bit in the **mode register** is enabled, the I2C bus can write to all registers in the WAKE state.		

Table 10. Operational States

7 OPERATIONAL STATE FLOW

Figure 9. Operational State Flow shows the operational state flow for the device. The device defaults to STANDBY following power-on.

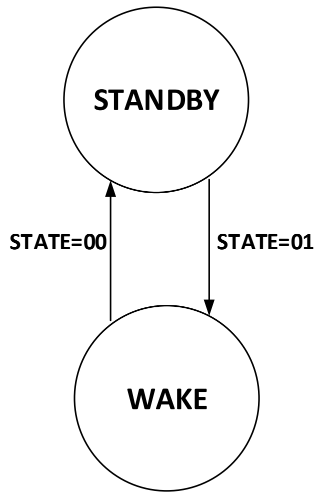


Figure 9. Operational State Flow

The operation state may be read from the STATE bits of the **device status register**. The operational state may be forced to a specific state by writing into the STATE bits of the **mode register**, as shown below. Two bits are specified in order to promote software compatibility with other MEMSIC devices. The operational state will stay in the mode specified until changed.

Action	Setting	Effect
Force STANDBY State	STATE[1:0] = 00	• Switch to the STANDBY state and stay there • Disable sensor and event sampling
Force WAKE State	STATE[1:0] = 01	• Switch to WAKE state and stay there • Continuous sampling

Table 11. Forcing Operational States

8 INTERRUPTS

The sensor device utilizes output pin INT*n* to signal to an external microprocessor that an event has been detected. The microprocessor should contain an interrupt service routine which would perform certain tasks after receiving this interrupt and reading the associated status bits, perhaps after a sample was made ready. If interrupts are to be used, the microprocessor must set up the registers in the sensor so that when a specific event is detected, the microprocessor would receive the interrupt and the interrupt service routine would be executed. If polling is used, there is no need for the interrupt registers to be set up.

For products that use polling, the microprocessor must periodically poll the sensor and read the status data (the INT*n* pin is not used). For most applications, this is likely best done at the sensor sampling rate or faster.

NOTE: At least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

8.1 ENABLING AND CLEARING INTERRUPTS

The **interrupt status register** contains the flag bits for the sample acquisition interrupt ACQ_INT. The **interrupt enable register** determines if a flag event generates interrupts.

The flags (and interrupts) are cleared and rearmed every time an interrupt status register is read.

When an event is detected, it is masked with a flag bit in the interrupt enable register, and then the corresponding status bit is set in the status registers.

The polarity and driving mode of the external interrupt signal may be chosen by setting the IPP and IAH bits in the **mode register**.

8.2 ACQ_INT INTERRUPT

The ACQ_INT flag bit in the status registers is always active. This bit is cleared when it is read. When a sample has been produced, an interrupt will be generated only if the ACQ_INT_EN bit in the interrupt enable register is active. The frequency of the ACQ_INT bit being set active is always the same as the sample rate.

9 SAMPLING

9.1 CONTINUOUS SAMPLING

The device has the ability to read all sampled readings in a continuous sampling fashion. The device always updates the XOUT, YOUT, and ZOUT registers at the chosen ODR.

An optional interrupt can be generated each time the sample registers have been updated (using the ACQ_INT bit in the **interrupt enable register**). See the **ACQ_INT Interrupt** section or **status register** for more information about ACQ_INT.

10 I2C INTERFACE

10.1 PHYSICAL INTERFACE

The I2C slave interface operates at a maximum speed of 1 MHz. The SDA (data) is an open-drain, bi-directional pin and the SCL (clock) is an input pin.

Note: The device always operates as an I2C slave.

An I2C master initiates all communication and data transfers and generates the SCL clock that synchronizes the data transfer. The I2C device address depends upon the state of the VPP pin during power-up as shown in the table below. After the I2C address is selected, it won't changed unless excuting one power on reset.

An optional I2C watchdog timer can be enabled to prevent bus stall conditions. See the **Watchdog Timer** section for more information.

7-bit Device ID	8-bit Address – Write	8-bit Address – Read	VPP level upon power-up
0x4C (0b1001100)	0x98	0x99	GND
0x6C (0b1101100)	0xD8	0xD9	VDD

Table 12. I2C Address Selection

The I2C interface remains active as long as power is applied to the VDD/VDDIO pin. In the STANDBY state, the device responds to I2C read and write cycles, but interrupts cannot be serviced or cleared. All registers can be written in the STANDBY state, but in the WAKE state, only the **mode register** can be modified (see the **Operational States** section for more information).

Internally, the registers which are used to store samples are clocked by the sample clock gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers, at least one I2C STOP condition must be present between samples.

Refer to the I2C specification for a detailed discussion of the protocol. Per I2C requirements, SDA is an open drain, bi-directional pin. SCL and SDA each require an external pull-up resistor, typically 4.7kΩ.

10.2 TIMING

See the **I2C Timing Characteristics** section for I2C timing requirements.

10.3 I2C MESSAGE FORMAT

Note: At least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

The device uses the following general format for writing to the internal registers: The I2C master generates a START condition and then supplies the 7-bit device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls SDA low during the 9th clock cycle indicating a positive ACK.

The second byte is the 8-bit register address of the device to access. The last byte is the data to write.

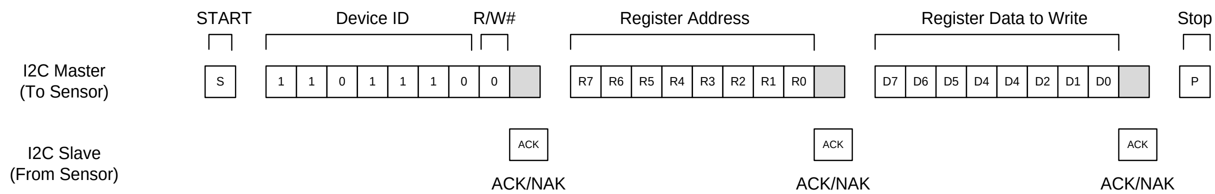


Figure 10. I2C Message Format, Write Cycle, Single Register Write

In a read cycle, the I2C master generates a START condition and then writes the device ID, R/W# flag (write cycle = 0), and register address. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to ‘1’. The device shifts out the contents of the register address.

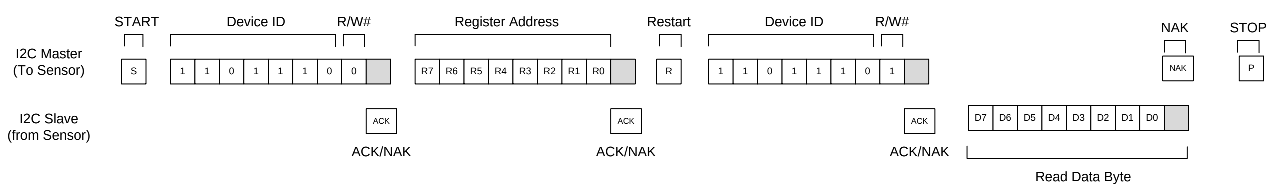


Figure 11. I2C Message Format, Read Cycle, Single Register Read

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

10.4 WATCHDOG TIMER

The I2C watchdog timer, when enabled (see the **mode register**), prevents bus stall conditions when the master does not provide enough clocks to the slave to complete a read cycle. The I2C watchdog timer does not resolve why the master did not provide enough clocks to complete a read cycle, but it does prevent a slave from holding the bus indefinitely.

During a read cycle, the slave that is actively driving the bus (SDA pin) does not release the bus until nine SCL clock edges are detected. While the SDA pin is held low by a slave open-drain output, any other I2C devices attached to the bus will not be able to communicate. If the slave does not see nine SCL clocks from the master within the timeout period (about 200 ms), the slave assumes a system problem has occurred and resets the I2C circuitry, releases the SDA pin, and readies the sensor for additional I2C commands.

When an I2C watchdog timer event is triggered, the I2C_WDT bit in the **device status register** is activated by the Watchdog timer hardware. No other registers are changed. External software can detect this activation by reading the I2C_WDT bit. Reading the interrupt status register (**0x14**) clears the I2C_WDT bit.

11 REGISTER INTERFACE

The device has a register interface which allows an MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, bit 0 is the least significant bit (LSB) of a byte register.

11.1 REGISTER SUMMARY

NOTE: Registers are not updated with new event status or samples while an I2C cycle is in process.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[1]
0x00 – 0x04		RESERVED[2]										
0x05	DEV_STAT	**Device Status**	OTP_BUSY	SEC_ENA (TMODE)	Resv	I2C_WDT	Resv	RES_MODE	STATE[1]	STATE[0]	0x00	R
0x06	INTR_CTRL	**Interrupt Enable**	ACQ_INT_EN	AUTO_CLR_EN	Resv	TILT_35_INT_EN	SHAKE_INT_EN	ANYM_INT_EN	FLIP_INT_EN	TILT_INT_EN	0x00	W
0x07	MODE	**Mode**	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0[3]	STATE1	STATE0	0x00	W
0x08	SR	**Sample Rate**	Resv	Resv	Resv	Resv	Resv	RATE[2]	RATE[1]	RATE[0]	0x00	W
0x09	MOTION_CTRL	**Motion Control**	MOTION_RESET	RAW_PROC_STAT	Z_AXIS_ORT	TILT_35_EN	SHAKE_EN	ANYM_EN	MOTION_LATCH	TF_ENABLE	0x00	W
0x0A – 0x0C		RESERVED[2]										
0x0D	XOUT_EX_L	**XOUT Accelerometer Data LSB**	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	**XOUT Accelerometer Data MSB**	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	**YOUT Accelerometer Data LSB**	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_L	**YOUT Accelerometer Data MSB**	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	**ZOUT Accelerometer Data LSB**	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	**ZOUT Accelerometer Data MSB**	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R
0x13	STATUS_2	**Status Register**	NEW_DATA	Resv	Resv	TILT_35_FLAG	SHAKE_FLAG	ANYM_FLAG	FLIP_FLAG	TILT_FLAG	0x00	R
0x14	INTR_STAT_2	**Interrupt Status Register**	ACQ_INT	Resv	Resv	TILT_35_INT	SHAKE_INT	ANYM_INT	FLIP_INT	TILT_INT	0x00	R
0x15 – 0x1F		RESERVED[2]										
0x18	Chip ID	**Chip Identification Register**	1	0	1	0	0	0	0	0	0xA0	R
0x20	RANGE	**Range Select Control**	Resv	RANGE[2]	RANGE[1]	RANGE[0]	1[4]	0[3]	0[3]	1[4]	0x00	W
0x21	XOFFL	**X-Offset LSB**	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	**X-Offset MSB**	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[1]
0x23	YOFFL	Y-Offset LSB	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x24	YOFFH	Y-Offset MSB	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x25	ZOFFL	Z-Offset LSB	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x27	XGAIN	X Gain	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W
0x28	YGAIN	Y Gain	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W
0x29	ZGAIN	Z Gain	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W
0x2A -0x3F		RESERVED[2]										
0x40	TF_THRESH_LSB	Tilt/Flip Threshold LSB	TF_THR[7]	TF_THR[6]	TF_THR[5]	TF_THR[4]	TF_THR[3]	TF_THR[2]	TF_THR[1]	TF_THR[0]	0x00	W
0x41	TF_THRESH_MSB	Tilt/Flip Threshold MSB	Resv	TF_THR[14]	TF_THR[13]	TF_THR[12]	TF_THR[11]	TF_THR[10]	TF_THR[9]	TF_THR[8]	0x00	W
0x42	TF_DB	Tilt/Flip Debounce	TF_DB[7]	TF_DB[6]	TF_DB[5]	TF_DB[4]	TF_DB[3]	TF_DB[2]	TF_DB[1]	TF_DB[0]	0x00	W
0x43	AM_THRESH_LSB	AnyMotion Threshold LSB	ANYM_THR[7]	ANYM_THR[6]	ANYM_THR[5]	ANYM_THR[4]	ANYM_THR[3]	ANYM_THR[2]	ANYM_THR[1]	ANYM_THR[0]	0x00	W
0x44	AM_THRESH_MSB	AnyMotion Threshold MSB	Resv	ANYM_THR[14]	ANYM_THR[13]	ANYM_THR[12]	ANYM_THR[11]	ANYM_THR[10]	ANYM_THR[9]	ANYM_THR[8]	0x00	W
0x45	AM_DB	AnyMotion Debounce	ANYM_DB[7]	ANYM_DB[6]	ANYM_DB[5]	ANYM_DB[4]	ANYM_DB[3]	ANYM_DB[2]	ANYM_DB[1]	ANYM_DB[0]	0x00	W
0x46	SHK_THRESH_LSB	Shake Threshold LSB	SH _THR[7]	SH _THR[6]	SH _THR[5]	SH _THR[4]	SH _THR[3]	SH _THR[2]	SH _THR[1]	SH _THR[0]	0x00	W
0x47	SHK_THRESH_MSB	Shake Threshold MSB	SH_THR[15]	SH _THR[14]	SH _THR[13]	SH _THR[12]	SH _THR[11]	SH _THR[10]	SH _THR[9]	SH _THR[8]	0x00	W
0x48	PK_P2P_DUR_THRESH_LSB	Peak-to-Peak Duration LSB	PK_P2P_DUR[7]	PK_P2P_DUR[6]	PK_P2P_DUR[5]	PK_P2P_DUR[4]	PK_P2P_DUR[3]	PK_P2P_DUR[2]	PK_P2P_DUR[1]	PK_P2P_DUR[0]	0x00	W
0x49	PK_P2P_DUR_THRESH_MSB	Shake Duration and Peak-to-Peak Duration MSB	Resv	SHK_CNT_DUR[2]	SHK_CNT_DUR[1]	SHK_CNT_DUR[0]	PK_P2P_DUR[11]	PK_P2P_DUR[10]	PK_P2P_DUR[9]	PK_P2P_DUR[8]	0x00	W
0x4A	TIMER_CTRL	Timer Control	TEMP_PER_INT_EN	TEMP_PERIOD[2]	TEMP_PERIOD[1]	TEMP_PERIOD[0]	Resv	TILT_35[2]	TILT_35[1]	TILT_35[0]	0x00	W

[1] 'R' registers are read-only, via external I2C access. 'W' registers are read-write, via external I2C access.
[2] Registers designated as 'RESERVED' should not be accessed by software.
[3] Software must write a zero (0) to this bit.
[4] Software must write a one (1) to this bit.

Table 13. Register Summary

11.2 DEVICE STATUS REGISTER

The device status register reports various conditions of the sensor circuitry.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x05	DEV_ STAT	Device Status	OTP_ BUSY	Resv	Resv	I2C_WDT	Resv	RES_ MODE	STATE[1]	STATE[0]	0x00	R

Name	Description
STATE[1:0]	Operating mode of the current device. **00**: STANDBY. Clocks are not running and X, Y, and Z-axis data are not sampled. **01**: WAKE. Clocks are running and X, Y, and Z-axis data are acquired at the sample rate. **10**: Reserved. **11**: Reserved.
RES_MODE	Resolution mode of the current device. **0**: 16-bit (high) resolution is enabled. **1**: Reserved.
I2C_WDT	I2C watchdog timeout. This bit is cleared when register 0x14 is read. **0**: A watchdog event is not detected. **1**: A watchdog event has been detected by the hardware and the I2C slave state machine is reset to idle.
OTP_BUSY	One-Time programming (OTP) activity status. **0**: Internal memory is idle and the device is ready to use. **1**: Internal memory is active and the device cannot be used.

Table 14. Device Status Register

11.3 INTERRUPT ENABLE REGISTER

The interrupt enable register enables or disables the reporting of interrupt status for each interrupt source.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x06	INTR_CTRL	Interrupt Enable	ACQ_INT_EN	AUTO_CLR_EN	Resv	TILT_35_INT_EN	SHAKE_INT_EN	ANYM_INT_EN	FLIP_INT_EN	TILT_INT_EN	0x00	W

Name	Description
TILT_INT_EN	Use with the tilt/flip feature in the motion control register (register 0x09, bit 0) to activate the reporting status of the tilt interrupt. **0**: Tilt interrupt is disabled. **1**: Tilt interrupt is enabled.
FLIP_INT_EN	Use with the tilt/flip feature in the motion control register (register 0x09, bit 0) to activate the reporting status of the flip interrupt. **0**: Flip interrupt is disabled. **1**: Flip interrupt is enabled.
ANYM_INT_EN	Use with the AnyMotion feature in the motion control register (register 0x09, bit 2) to activate the reporting status of the AnyMotion interrupt. **0**: AnyMotion interrupt is disabled. **1**: AnyMotion interrupt is enabled.
SHAKE_INT_EN	Use with the shake feature in the motion control register (register 0x09, bit 3) and the AnyMotion feature in the motion control register (register 0x09, bit 2) to activate the reporting status of the shake interrupt. **0**: Shake interrupt is disabled. **1**: Shake interrupt is enabled.
TILT_35_INT_EN	Use with the tilt-35 feature in the motion control register (register 0x09, bit 4) and the AnyMotion feature in the motion control register (register 0x09, bit 2) to activate the reporting status of the tilt-35 interrupt. **0**: Tilt-35 interrupt is disabled. **1**: Tilt-35 interrupt is enabled.
AUTO_CLR_EN	Clear pending interrupts automatically or by reading a register. Enabling more than one interrupt timeout or service feature may produce unexpected results. **0**: Clear pending interrupts by reading register 0x14. **1**: Automatically clear pending interrupts if the interrupt condition is no longer valid. Refer to **Interrupts** for more information about interrupts.
ACQ_INT_EN	Generate interrupts. **0**: Disable automatic interrupt after each sample (default). **1**: Enable automatic interrupt after each sample (activates the ACQ_INT flag, bit 7, in register 0x14).

Table 15. Interrupt Enable Register

11.4 MODE REGISTER

The mode register controls the active operating state of the accelerometer. This register can be written from all operational states (WAKE, or STANDBY).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x07	MODE	Mode	IAH	IPP	I2C_ WDT_POS	I2C_ WDT_NEG	Resv	0[1]	STATE[1]	STATE[0]	0x00	W
[1]Software must write a zero (0) to bit 2.												

Name	Description
STATE[1:0]	Accelerometer operational state. **00**: STANDBY. Clocks are not running and X, Y, and Z-axis data are not sampled. **01**: WAKE. Clocks are running and X, Y, and Z-axis data are acquired at the sample rate. **10**: Reserved. **11**: Reserved.
I2C_WDT_NEG	Watchdog timer for negative SCL stalls. **0**: The I2C watchdog timer for negative SCL stalls is disabled (default). **1**: The I2C watchdog timer for negative SCL stalls is enabled.
I2C_WDT_POS	Watchdog timer for positive SCL stalls. **0**: The I2C watchdog timer for positive SCL stalls is disabled (default). **1**: The I2C watchdog timer for positive SCL stalls is enabled.
IPP	Interrupt Push Pull. **0**: Interrupt pin INT*n* is open drain (default) and requires an external pull-up to pin VDD/VDDIO. **1**: Interrupt pin INT*n* is push-pull. No external pull-up resistor should be installed.
IAH	Interrupt Active High. **0**: Interrupt pin INT*n* is active low (default). **1**: Interrupt pin INT*n* is active high.

Table 16. Mode Register States

11.5 SAMPLE RATE REGISTER

The sample rate register sets the sampling output data rate (ODR) for the sensor, the clock frequency of the main oscillator, and the oversampling ratio (OSR).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x08	SR	Sample Rate	Resv	Resv	Resv	Resv	Resv	RATE[2]	RATE[1]	RATE[0]	0x00	W

Name	Description
RATE[2:0]	Output data rate, determined by the frequency of the main oscillator and the OSR. **000**: 128 (default, slowest) **001**: 256 **010**: 512 **011**: Reserved. **100**: Reserved. **101**: 1024 (fastest) **110**: Reserved. **111**: Reserved.

Table 17. Sample Rate Register

11.6 MOTION CONTROL REGISTER

The motion control register enables the flags and interrupts for motion detection features.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x09	MOTION_ CTRL	Motion Control	MOTION_ RESET	RAW_ PROC_ STAT	Z_AXIS_ ORT	TILT_35_ EN	SHAKE_ EN	ANYM_EN	MOTION_ LATCH	TF_ ENABLE	0x00	W

Name	Description
TF_ENABLE	Enable or disable the tilt/flip feature. Used with the tilt/flip features in registers 0x13, 0x14, and 0x06. **0**: Tilt/Flip feature is disabled (default). **1**: Tilt/Flip feature is enabled.
MOTION_LATCH	If motion interrupts are used, this bit is generally not used. **0**: Motion block does not latch outputs. **1**: Motion block latches outputs.
ANYM_EN	Enable or disable the AnyMotion feature. Used with the AnyMotion feature in registers 0x13, 0x14, and 0x06 and the shake and tilt-35 features in registers 0x14 and 0x06. **0**: AnyMotion feature is disabled (default). **1**: AnyMotion feature is enabled.
SHAKE _EN	Enable or disable the shake feature. Used with the shake feature in registers 0x13, 0x14, and 0x06. **0**: Shake feature is disabled (default). **1**: Shake feature is enabled. ANYM_EN must also be enabled.
TILT_35 _EN	Enable or disable the tilt-35 feature. Used with tilt-35 feature in registers 0x13, 0x14, and 0x06. **0**: Tilt-35 feature is disabled (default). **1**: Tilt-35 feature is enabled. ANYM_EN must also be enabled.
Z_AXIS_ORT	Z-axis orientation. **0**: Z-axis orientation is positive through the top of the package (default). **1**: Z-axis orientation is positive through the bottom of the package.
RAW_PROC_STAT	Enable or disable filtering of motion data. **0**: Motion flag bits are filtered by debounce and other settings (default). **1**: Motion flag bits are real-time, raw data.
MOTION_RESET	Motion block reset. This bit is not automatically cleared. **0**: The motion block is not in reset (default). **1**: The motion block is held in reset. The software must set this bit for the reset to be cleared.

Table 18. Motion Control Register

11.7 XOUT, YOUT AND ZOUT DATA ACCELEROMETER REGISTERS

X, Y, and Z-axis accelerometer measurements in 14-bit and 16-bit resolutions and are in a signed 2's complement format. In raw bypass mode (RBM), the 14-bit value is used.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0D	XOUT_EX_L	XOUT Accelerometer Data LSB	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Accelerometer Data MSB	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Accelerometer Data LSB	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_L	YOUT Accelerometer Data MSB	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Accelerometer Data LSB	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Accelerometer Data MSB	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R

Table 19. Accelerometer LSB and MSB Registers

11.8 STATUS REGISTER

The status register contains the flag and status bits for sample acquisition and motion detection.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x13	STATUS_2	Status Register	NEW_ DATA	Resv	Resv	TILT_35_ FLAG	SHAKE_ FLAG	ANYM_ FLAG	FLIP_FLAG	TILT_ FLAG	0x00	R

Name	Description
TILT_FLAG	This bit is active when the tilt feature in the motion control register (register 0x09, bit 0) is enabled. If polling is used, use the tilt interrupt in the interrupt status register (register 0x14, bit 0) instead because this bit can transition quickly. **0**: Tilt condition is not detected. **1**: Tilt condition is detected.
FLIP_FLAG	This bit is active when the flip feature in the motion control register (register 0x09, bit 0) is enabled. If polling is used, use the flip interrupt in the interrupt status register (register 0x14, bit 1) instead because this bit can transition quickly. **0**: Flip condition is not detected. **1**: Flip condition is detected.
ANYM_FLAG	This bit is active when the AnyMotion feature in the motion control register (register 0x09, bit 2) is enabled. If polling is used, use the AnyMotion interrupt in the interrupt status register (register 0x14, bit 2) instead because this bit can transition quickly. **0**: AnyMotion condition is not detected. **1**: AnyMotion condition is detected.
SHAKE_FLAG	This bit is active when the shake feature in the motion control register (register 0x09, bit 3) is enabled. If polling is used, use the shake interrupt in the interrupt status register (register 0x14, bit 3) instead because this bit can transition quickly. **0**: Shake condition is not detected. **1**: Shake condition is detected.
TILT_35_FLAG	This bit is active when the tilt-35 feature in the motion control register (register 0x09, bit 4) is enabled. If polling is used, use the tilt-35 interrupt in the interrupt status register (register 0x14, bit 4) instead because this bit can transition quickly. **0**: Tilt-35 condition is not detected. **1**: Tilt-35 condition is detected.
NEW_DATA	This bit is always active, only operates in WAKE mode, and is cleared and rearmed each time this register is read. This flag is set when XYZ data is written to registers 0x0D - 0x12. The host must poll this bit at the sample rate or faster to see this bit transition. **0**: No data has been generated by the sensor since the last read. **1**: Data has been acquired and written to the output registers (0x0D - 0x12).

Table 20. Status Register

11.9 INTERRUPT STATUS REGISTER

The interrupt status register reports the status of any pending interrupt sources. Each interrupt source must be enabled by the corresponding interrupt enable bit in register 0x06. All interrupts are cleared each time this register is read.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x14	INTR_ STAT_2	Interrupt Status Register	ACQ_INT	Resv	Resv	TILT_35_ INT	SHAKE_ INT	ANYM_ INT	FLIP_INT	TILT_INT	0x00	R

Name	Description
TILT_INT	This bit is active when the tilt feature in the interrupt enable register (register 0x06, bit 0) is enabled and the tilt/flip feature in the motion control register (register 0x09, bit 0) is enabled. **0**: Tilt interrupt is not pending. **1**: Tilt interrupt is pending.
FLIP_INT	This bit is active when the flip feature in the interrupt enable register (register 0x06, bit 1) is enabled and the tilt/flip feature in the motion control register (register 0x09, bit 0) is enabled. **0**: Flip interrupt is not pending. **1**: Flip interrupt is pending.
ANYM_INT	This bit is active when the AnyMotion feature in the interrupt enable register (register 0x06, bit 2) is enabled and the AnyMotion feature in the motion control register (register 0x09, bit 2) is enabled. **0**: AnyMotion interrupt is not pending. **1**: AnyMotion interrupt is pending.
SHAKE_INT	This bit is active when the shake feature in the interrupt enable register (register 0x06, bit 3) is enabled, the shake feature in the motion control register (register 0x09, bit 3) is enabled, and the AnyMotion feature in the motion control register (register 0x09, bit 2) is enabled. **0**: Shake interrupt is not pending. **1**: Shake interrupt is pending.
TILT_35_INT	This bit is active when the tilt-35 feature in the interrupt enable register (register 0x06, bit 4) is enabled, the tilt-35 feature in the motion control register (register 0x09, bit 4) is enabled, and the AnyMotion feature in the motion control register (register 0x09, bit 2) is enabled. **0**: Tilt-35 interrupt is not pending. **1**: Tilt-35 interrupt is pending.
ACQ_INT	This bit only operates in WAKE mode. This bit is active when the interrupt feature in the interrupt enable register (register 0x06, bit 7) is enabled. **0**: Sample interrupt is not pending. **1**: Sample interrupt is pending.

Table 21. Interrupt Status Register

11.10 RANGE AND SCALE CONTROL REGISTER

The range and scale control register sets the resolution, range, and filtering options for the accelerometer. All values are in sign-extended 2's complement format. Values are reported in registers 0x0D – 0x12 (the hardware formats the output).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x20	RANGE	Range Select Control	Resv	RANGE[2]	RANGE[1]	RANGE[0]	1[2]	0[1]	0[1]	1[2]	0x00	W

[1]Software must write a zero (0) to bits 1 and 2.
[2]Software must write a one (1) to bit 0.

Name	Description
RANGE[2:0]	Resolution range of the accelerometer, based on the current resolution. **000**: ± 2g **001**: ± 4g **010**: ± 8g **011**: ± 16g **100**: ± 12g **101**: Reserved. **110**: Reserved. **111**: Reserved.

Table 22. Range and Scale Control Register

11.11 X-AXIS DIGITAL OFFSET REGISTERS

The X-axis digital offset registers contains a signed 2's complement 14-bit value used to offset the output of the X-axis filter. These registers are loaded from the OTP at device initialization and POR. If necessary, these values can be overwritten by software.

Register 0x22 bit 7 is the ninth bit of X-axis gain (XGAIN). See **X-Axis Digital Gain Registers** for more information about XGAIN.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x21	XOFFL	X-Offset LSB	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	X-Offset MSB	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W

Table 23. X-Axis Digital Offset Registers

11.12 Y-AXIS DIGITAL OFFSET REGISTERS

The Y-axis digital offset registers contains a signed 2's complement 14-bit value used to offset the output of the Y-axis filter. These registers are loaded from the OTP at device initialization and POR. If necessary, these values can be overwritten by software.

Register 0x24 bit 7 is the ninth bit of Y-axis gain (YGAIN). See **Y-Axis Digital Gain Registers** for more information about YGAIN.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x23	YOFFL	Y-Offset LSB	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x24	YOFFH	Y-Offset MSB	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W

Table 24. Y-Axis Digital Offset Registers

11.13 Z-AXIS DIGITAL OFFSET REGISTERS

The Z-axis digital offset registers contains a signed 2's complement 14-bit value used to offset the output of the Z-axis filter. These registers are loaded from the OTP at device initialization and POR. If necessary, these values can be overwritten by software.

Register 0x26 bit 7 is the ninth bit of Z-axis gain (ZGAIN). See **Z-Axis Digital Gain Registers** for more information about ZGAIN.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x25	ZOFFL	Z-Offset LSB	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W

Table 25. Z-Axis Digital Offset Registers

11.14 X-AXIS DIGITAL GAIN REGISTERS

The X-axis digital gain registers contains an unsigned 9-bit value. These registers are loaded from the OTP at device initialization and POR. If necessary, these values can be overwritten by software.

Register 0x22 bit 7 is the ninth bit of XGAIN.

NOTE: When modifying these registers with new gain values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x22	XOFFH	X-Offset MSB	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x27	XGAIN	X Gain	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W

Table 26. X-Axis Digital Gain Registers

11.15 Y-AXIS DIGITAL GAIN REGISTERS

The Y-axis digital gain registers contains an unsigned 9-bit value. These registers are loaded from the OTP at device initialization and POR. If necessary, these values can be overwritten by software.

Register 0x24 bit 7 is the ninth bit of YGAIN.

NOTE: When modifying these registers with new gain values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x24	YOFFH	Y-Offset MSB	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x28	YGAIN	Y Gain	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W

Table 27. Y-Axis Digital Offset Registers

11.16 Z-AXIS DIGITAL GAIN REGISTERS

The Z-axis digital gain registers contains an unsigned 9-bit value. These registers are loaded from the OTP at device initialization and POR. If necessary, these values can be overwritten by software.

Register 0x26 bit 7 is the ninth bit of ZGAIN.

NOTE: When modifying these registers with new gain values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x26	ZOFFH	Z-Offset MSB	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x29	ZGAIN	Z Gain	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W

Table 28. Z-Axis Digital Offset Registers

11.17 TILT/FLIP THRESHOLD REGISTERS

The tilt/flip threshold registers are used for both the flat/tilt/flip and tilt-35 algorithms.

For the flat/tilt/flip algorithm, these registers hold the programmed 15-bit threshold value to detect the flat/tilt/flip position of the device. If the sample value is greater than the programmed value of these registers, a tilt condition is detected. If the sample value is less than the programmed value of these registers, a flat/flip condition is detected. A flat/flip condition is dependent on the Z-axis value and the Z-axis orientation bit (register 0x09, bit 5).

For the tilt-35 algorithm, these registers hold the programmed 15-bit threshold value that defines the amount of tilt to detect. When the programmed tilt is detected, the tilt-35 interrupt is set in the interrupt status registers (register 0x14, bit 4).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x40	TF_ THRESH_ LSB	Tilt/Flip Threshold LSB	TF_THR[7]	TF_THR[6]	TF_THR[5]	TF_THR[4]	TF_THR[3]	TF_THR[2]	TF_THR[1]	TF_ THR[0]	0x00	W
0x41	TF_ THRESH_ MSB	Tilt/Flip Threshold MSB	Resv	TF_ THR[14]	TF_ THR[13]	TF_ THR[12]	TF_ THR[11]	TF_ THR[10]	TF_THR[9]	TF_ THR[8]	0x00	W

Table 29. Tilt/Flip Threshold Registers

11.18 TILT/FLIP DEBOUNCE REGISTER

The tilt/flip debounce register holds the programmed 8-bit duration of a tilt/flip. When a tilt/flip condition is detected and the duration of the condition is greater than the programmed value of this register, the tilt/flip interrupt is set in the interrupt status registers (register 0x14, bits 0 and 1).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x42	TF_DB	Tilt/Flip Debounce	TF_DB[7]	TF_DB[6]	TF_DB[5]	TF_DB[4]	TF_DB[3]	TF_DB[2]	TF_DB[1]	TF_DB[0]	0x00	W

Table 30. Tilt/Flip Debounce Register

11.19 ANYMOTION THRESHOLD REGISTERS

The Anymotion threshold registers hold the programmed 15-bit threshold value to detect a change in the position of the device. If the change in position between the current sample value and previous sample value on any axis is greater than the programmed value of this register, an AnyMotion condition is detected. When the change in position exceeds the programmed AnyMotion threshold, the AnyMotion interrupt is set in the interrupt status registers (register 0x14, bit 2).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x43	AM_ THRESH_ LSB	AnyMotion Threshold LSB	ANYM_ THR[7]	ANYM_ THR[6]	ANYM_ THR[5]	ANYM_ THR[4]	ANYM_ THR[3]	ANYM_ THR[2]	ANYM_ THR[1]	ANYM_ THR[0]	0x00	W
0x44	AM_ THRESH_ MSB	AnyMotion Threshold MSB	Resv	ANYM_ THR[14]	ANYM_ THR[13]	ANYM_ THR[12]	ANYM_ THR[11]	ANYM_ THR[10]	ANYM_ THR[9]	ANYM_ THR[8]	0x00	W

Table 31. AnyMotion Threshold Registers

11.20 ANYMOTION DEBOUNCE REGISTER

The AnyMotion debounce register holds the programmed 8-bit duration of any motion. After an AnyMotion condition is detected, if another AnyMotion condition is not detected for the programmed duration, the AnyMotion interrupt is cleared in the interrupt status registers (register 0x14, bits 0 and 1).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x45	AM_DB	AnyMotion Debounce	ANYM_DB[7]	ANYM_DB[6]	ANYM_DB[5]	ANYM_DB[4]	ANYM_DB[3]	ANYM_DB[2]	ANYM_DB[1]	ANYM_DB[0]	0x00	W

Table 32. AnyMotion Debounce Register

11.21 SHAKE THRESHOLD REGISTERS

The shake threshold registers hold the programmed 15-bit threshold value to detect a shake. If the change in position between the current sample value and previous sample value on any axis is greater than the programmed value of this register, a shake condition is detected.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x46	SHK_ THRESH_ LSB	Shake Threshold LSB	SH _ THR[7]	SH _ THR[6]	SH _ THR[5]	SH _ THR[4]	SH _ THR[3]	SH _ THR[2]	SH _ THR[1]	SH _ THR[0]	0x00	W
0x47	SHK_ THRESH_ MSB	Shake Threshold MSB	SH_ THR[15]	SH _ THR[14]	SH _ THR[13]	SH _ THR[12]	SH _ THR[11]	SH _ THR[10]	SH _ THR[9]	SH _ THR[8]	0x00	W

Table 33. Shake Threshold Registers

11.22 SHAKE DURATION, PEAK-TO-PEAK REGISTERS

The shake duration and peak-to-peak registers hold the programmed 12-bit threshold value of a peak and the peak-to-peak width of a shake and the programmed 3-bit threshold value of the shake counter.

The data in these registers and the shake threshold registers is used to determine if the shake interrupt should be set.

If a shake condition is detected, the shake counter is incremented and the shake's peak is detected and measured. If the peak's width is greater than the peak threshold set in this register, the shake counter continues to increment (measuring the duration of the peak event). When a shake condition is no longer detected, the peak-to-peak event is measured and the shake counter continues to increment (measuring the duration of the peak-to-peak event). When the peak-to-peak threshold is surpassed, the shake counter continues to increment, measuring the duration of the peak event. The shake counter continues to increment each time a peak or peak-to-peak threshold is surpassed. When the shake counter threshold is surpassed, the shake interrupt is set in the interrupt status registers (register 0x14, bit 3).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x48	PK_P2P_ DUR_ THRESH_ LSB	Peak-to-Peak Duration LSB	PK_P2P_ DUR[7]	PK_P2P_ DUR[6]	PK_P2P_ DUR[5]	PK_P2P_ DUR[4]	PK_P2P_ DUR[3]	PK_P2P_ DUR[2]	PK_P2P_ DUR[1]	PK_P2P_ DUR[0]	0x00	W
0x49	PK_P2P_ DUR_ THRESH_ MSB	Shake Duration and Peak-to-Peak Duration MSB	Resv	SHK_CNT_ DUR[2]	SHK_CNT_ DUR[1]	SHK_CNT_ DUR[0]	PK_P2P_ DUR[11]	PK_P2P_ DUR[10]	PK_P2P_ DUR[9]	PK_P2P_ DUR[8]	0x00	W

Table 34. Shake Duration and Peak-to-Peak Registers

11.23 TIMER CONTROL REGISTER

The timer control register sets the period or duration of two features driven by the 10 Hz low speed clock.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x4A	TIMER_ CTRL	Timer Control	TEMP_ PER_INT_ EN	TEMP_ PERIOD[2]	TEMP_ PERIOD[1]	TEMP_ PERIOD[0]	Resv	TILT_ 35[2]	TILT_35[1]	TILT_ 35[0]	0x00	W

Name	Description
TILT_35[2:0]	Duration of a valid tilt-35 angle detection. **000**: 1.6 s (default) **001**: 1.8 s **010**: 2.0 s **011**: 2.2 s **100**: 2.4 s **101**: 2.6 s **110**: 2.8 s **111**: 3.0 s
TEMP_PERIOD[2:0]	Timeout or re-arm time for the temporary latch on the TEST_INT pin. **000**: 200 ms (default) **001**: 400 ms **010**: 800 ms **011**: 1600 ms **100**: 3200 ms **101**: 6400 ms **110**: Reserved **111**: Reserved
TEMP_PER_INT_EN	Temporary latch. **0**: The temporary latch feature is disabled (default). **1**: The temporary latch feature is enabled.

Table 35. Timer Control Register

12 INDEX OF TABLES

13 REVISION HISTORY

Date	Revision	Description
2020-08	V1.0	Initial release