GigaDevice Semiconductor Inc.

GD30LD1002x
1.2A, 6.5V, Low Input Volatge, LDO

Datasheet

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- Output Voltage Range, 0.5 V to 5.2 V, Set by a Resistor Divider
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- Ultra Low Dropout Voltage: Maximum 200 mV at 1.2A
- Load and Temperature
- Current Limit Function
- Short Circuit Protection
- Enable Function

2 Applications

- Wireless Infrastructure
- Telecom/Networking Cards
- Industrial Application
- Set Top Box
- Medical Equipment
- Notebook Computers
- Battery Powered Systems

3 General description

The GD30LD1002x is a high-current, high accuracy, low-dropout linear regulator (LDO) capable of sourcing 1.2A with extreme low dropout (max, 200mV).

The device output voltage is adjustable from 0.5 V to 5.2 V using the external resistor divider. The device supports input supply voltage as low to 1.4 V. Additionally, the GD30LD1002x has an enable pin to further reduce power dissipation while shutdown.

The GD30LD1002x provides excellent regulation over variations in line, load and temperature. The output voltage can be set by an external divider depending on how the FB pin is configured.

The device is fully specified over the temperature range of T_J = −40°C to 125°C and is offered in a DFN8(Exposed Pad) package.

4 Device overview

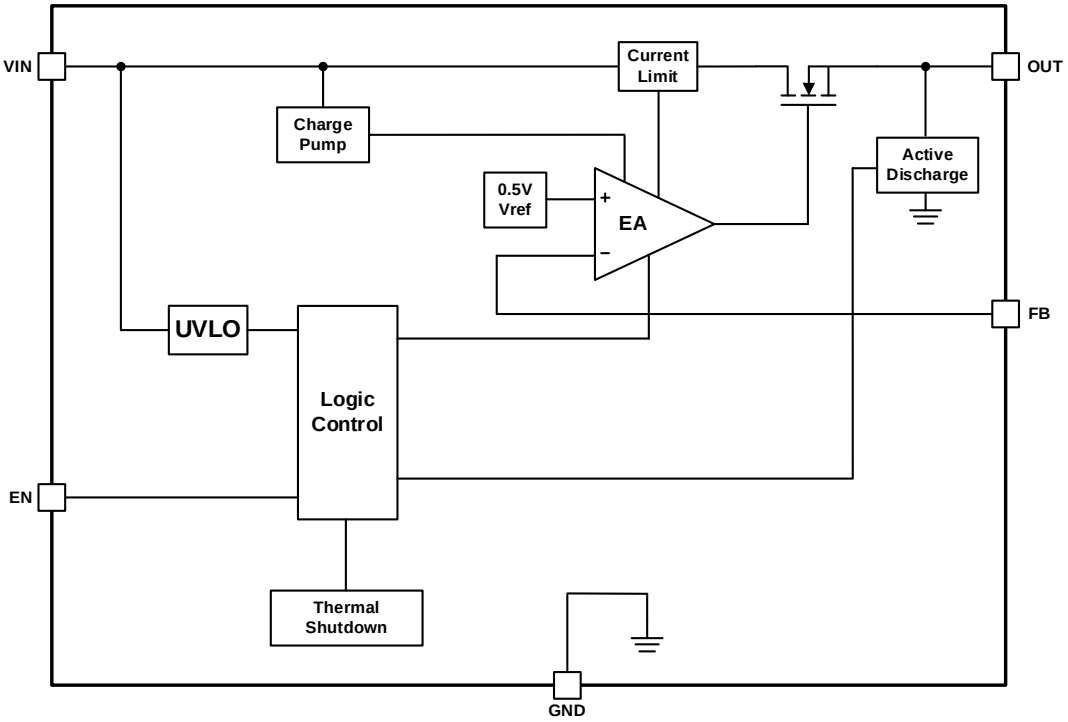
4.1 Device information

Table 4-1 Device information for GD30LD1002x

Part Number	Package	Function	Description
GD30LD1002x	DFN8	With enable pin(EN)	1.2A Low input voltage, low dropout LDO regulator

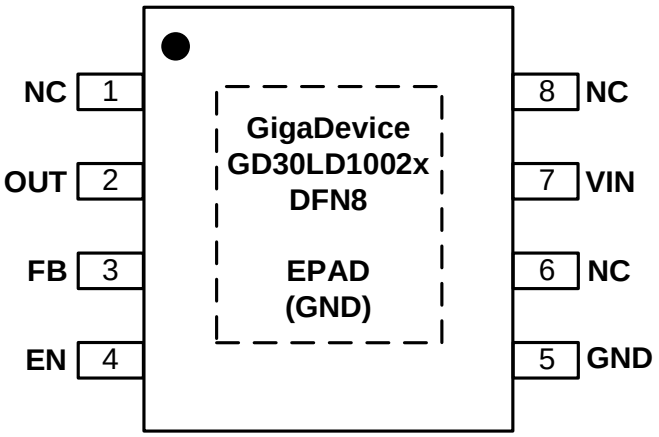
4.2 Block diagram

Figure 4-1 Block diagram for GD30LD1002x



4.3 Pinout and pin assignment

Figure 4-2 GD30LD1002x DFN8 pinouts



4.4 Pin definitions

Table 4-2 GD30LD1002x DFN8 pin definitions

Pin Name	Pins	Pin Type	Functions description
NC	1,6,8	—	These pins are not connected to silicon.
OUT	2	O	**Output of the Regulator**. A minimum of 10μF ceramic capacitor should be placed at this pin. The larger ceramic capacitor (10μF or greater) is stable.
FB	3	I	**Feedback Voltage Input**. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.5V typically.
EN	4	I	**Enable Control Input**. Connecting this pin to logic high enables the regulator, and driving this pin low puts it into shutdown mode.
GND	5	G	**Ground**. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
VIN	7	I	**Supply Input**. A minimum of 10μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.
GND	9(EPAD)	G	Device power ground.

Notes:

1. Type: I = input, O = output, G = Ground.

5 Functional description

5.1 Output Voltage Setting

The output voltage of the GD30LD1002x can be set by external resistors to achieve different output targets.

By using external resistors, the output voltage is determined by the values of R1 and R2 as shown in Figure 7-1. The values of R1 and R2 can be calculated for any voltage value using the following formula:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

5.2 Chip Enable Operation

The GD30LD1002x goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to only 25uA(max). The EN pin can be directly tied to keep the part on.

5.3 Recommended device selection

5.3.1 C_{IN} and C_{OUT} Selection

The GD30LD1002x is designed to support low-series resistance (ESR) ceramic capacitors. It is recommended to use ceramic capacitors with X7R, X5R, and C0G-rated ceramic capacitors to get good capacitive stability across different temperatures.

However, the capacitance of ceramic capacitors varies with operating voltage and temperature, and the design engineer must be aware of these characteristics. Ceramic capacitors are usually recommended to be derated by 50%. A 10μF or greater output ceramic capacitor is suggested to ensure stability. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of at least 10μF is highly recommended for minimal input impedance. If the trace inductance between the GD30LD1002x input pin and power supply is high, a fast load transient can cause V_{IN} voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors is available to restrict the ringing and keep it below the device absolute maximum ratings.

Generally, a 10μF 0805-sized ceramic capacitor in parallel with two 10μF 0805-sized ceramic capacitor ensures the minimum effective capacitance at high input voltage and high output voltage requirement. Place these capacitors as close to the pins as possible for

optimum performance and to ensure stability.

5.3.2 Feed-Forward Capacitor(C_{FF}) Selection

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

5.4 Undervoltage Lockout (UVLO)

The UVLO circuits ensure that the device stays disabled before its input reach the minimum operational voltage range, and ensures that the device properly shuts down when either the input collapses. Figure 5-1 and Table 5-1 explain one of the UVLO circuits being triggered to various input voltage events, assuming $V_{EN} \geq V_{IH(EN)}$.

Figure 5-1 Typical UVLO Operation

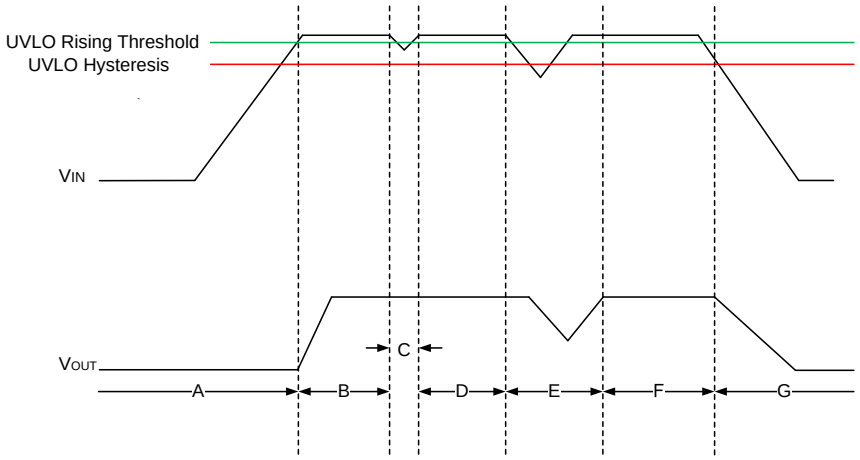


Table 5-1 Typical UVLO Operation Description

Region	EVENT	VOUT STATUS	COMMENT
A	Turn on, $V_{IN} \geq V_{UVLO\_1,2(IN)}$ and	Off	Startup
B	Regulation	On	Regulates to target V_{OUT}
C	Brown out, $V_{IN} \geq V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$	On	The output can fall out of regulation but the device is still enabled
D	Regulation	On	Regulates to target V_{OUT}
E	Brown out $V_{IN} < V_{UVLO(IN)} - V_{HYS(IN)}$	Off	The device is disabled and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO fault is

			removed when either the IN rising threshold is reached by the input a normal start-up then follows
F	Regulation	On	Regulates to target V_{OUT}
G	Turn off, $V_{IN} < V_{UVLO(IN)} - V_{HYS(IN)}$	Off	The output falls because of the load and active discharge circuit.

Similar to many other LDOs with this feature, the UVLO circuits take a few microseconds to fully assert. During this time, a downward line transient below approximately 0.8V causes the UVLO to assert for a short time; however, the UVLO circuits do not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLO circuits are not given enough time to fully discharge the internal nodes, the outputs are not fully disabled.

The effect of the downward line transient can be mitigated by using a larger input capacitor to increase the fall time of the input supply when operating near the minimum V_{IN}.

5.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

$V_{IN} \times I_{GND}$ represents the static power consumption of the LDO, the value is relatively small and can be ignored. An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB, device package, and the temperature of the ambient air (T_A).

$$T_J = T_A + \theta_{JA} \times P_D$$

$$I_{OUT} = (T_J - T_A) / [\theta_{JA} \times (V_{IN} - V_{OUT})]$$

6 Electrical characteristics

6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Voltage	IN, EN, OUT	-0.3	7.0	V
	FB	-0.3	3.6	V
Current	OUT	Internally limited		A
Thermal characteristics				
T_{stg}	Storage temperature	-65	150	°C

6.2 Recommended Operating Conditions

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	1.4	—	6.5	V
V_{OUT}	Output voltage range	0.5	—	5.2	V
V_{EN}	Enable Voltage range	0	—	6.5	V
I_{OUT}	Output current	0	—	1.2	A
C_{IN}	Input capacitor	—	10	—	uF
C_{OUT}	Output capacitor	—	10	—	uF
T_J	Operating junction temperature	-40	—	125	℃

6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample.

Table 6-3 Electrostatic Discharge characteristics

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2017	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2018	±500	V

6.4 Electrical Specifications

Over operating temperature range (T_J = −40°C to 125°C), Typical values are at T_J = 25°C. V_{IN} = 1.4 V or V_{IN} = $V_{OUT\ (TARGET)}$ + 0.4 V, $V_{OUT\ (TARGET)}$ = 0.5 V, V_{OUT} connected to 50 Ω to GND, V_{EN} = 1.4 V, C_{IN} = 10 μF, C_{OUT} = 10 μF, unless otherwise noted.

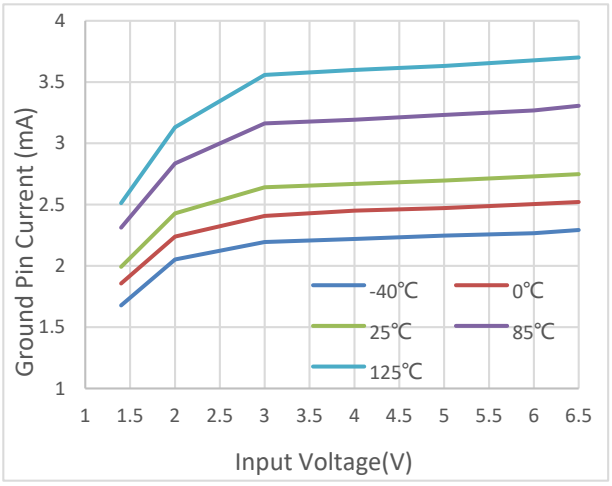
Table 6-4 Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Range	—	1.4	—	6.5	V
V_{FB}	Feedback Voltage	—	—	0.5	—	V
$V_{UVLO(IN)}$	UVLO	V_{IN} rising	—	1.33	1.39	V
$V_{HYS(IN)}$	UVLO hysteresis	—	—	230	—	mV
V_{OUT}	Output Voltage Range	Using external resistors	0.5 -1%	—	5.2 +1%	V
	Output Accuracy	V_{IN} = V_{OUT} + 0.3 V, 0.5 V ≤ V_{OUT}≤ 5.2 V	-1	—	1	%
$\triangle V_{OUT}$/ $\triangle V_{IN}$	Line Regulation	I_{OUT} = 5 mA, 1.4 V ≤ V_{IN}≤ 6.5 V	—	0.1	—	mV/V
$\triangle V_{OUT}$/ $\triangle I_{OUT}$	Load Regulation	5 mA ≤ I_{OUT}≤ 1.2A	—	0.3	—	mV/A
V_{DROP}	Dropout Voltage	V_{IN} = 1.4 V, I_{OUT} =1.2A, V_{FB} = 0.5 V – 3%	—	90	150	mV
		V_{IN} = 5.6V, I_{OUT} = 1.2A, V_{FB} = 0.5 V – 3%	—	100	200	mV
I_{LIM}	Output Current Limit	V_{OUT} = 90% * $V_{OUT(TARGET)}$ V_{IN} = $V_{OUT(TARGET)}$ + 400 mV	—	2.0	—	A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Short-Circuit Current Limit	I_{SC}	R_{LOAD} =20mΩ	—	1.0	—	A
I_{GND}	Ground Pin Current	Vin = 6.5 V, I_{OUT} = 5 mA	—	3.0	4.2	mA
		Vin = 1.4 V, I_{OUT} = 1.2A	—	4.2	5.5	mA
		Shutdown V_{IN} = 6.5 V, V_{EN} = 0.5 V	—	—	25	uA
I_{EN}	EN Pin Current	V_{IN} = 6.5 V, V_{EN} = 0 V and 6.5 V	-0.1	—	0.1	uA
V_{EN_H}	EN Pin High-Level	—	1.1	—	6.5	V
V_{EN_L}	EN Pin Low-Level	—	0	—	0.5	V
I_{FB}	FB Pin leakage Current	V_{IN} = 6.5 V	-100	—	100	nA
T_{SD}	Thermal Shutdown Threshold	Shut down, temperature increasing	—	160	—	°C
		Reset, temperature increasing	—	140	—	°C

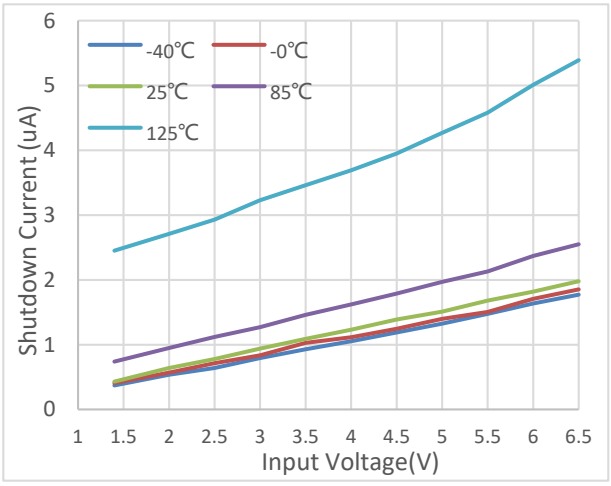
6.5 Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(TARGET)}$ + 0.4 V (whichever is greater), $V_{OUT(TARGET)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT}= 10 µF, unless otherwise noted.



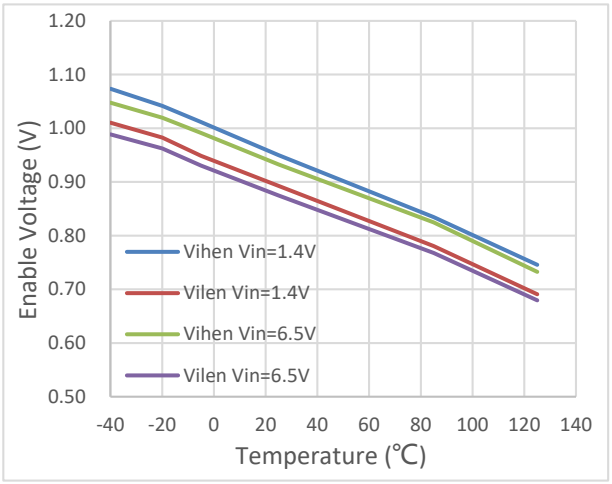
I_{OUT}=5mA

Ground Pin Current vs Input Voltage



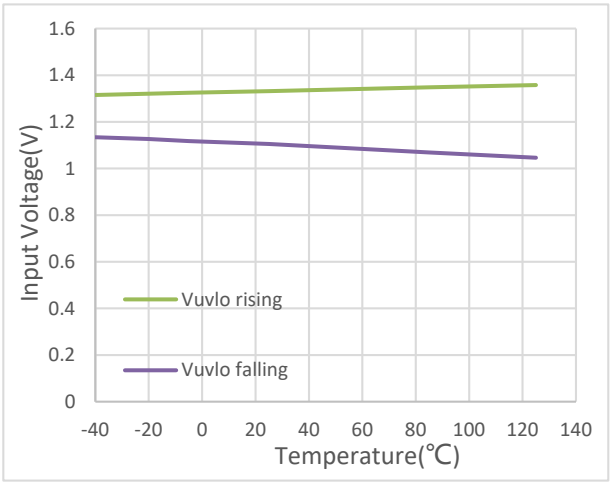
V_{EN}=0.5V

Shutdown Current vs Input Voltage



VIN=1.4V and VIN=6.5V

EN Threshold vs Temperature

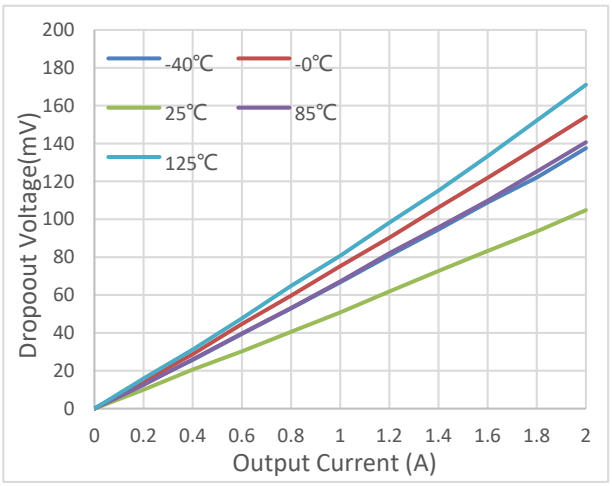


IOUT=5mA

VIN UVLO vs Temperature

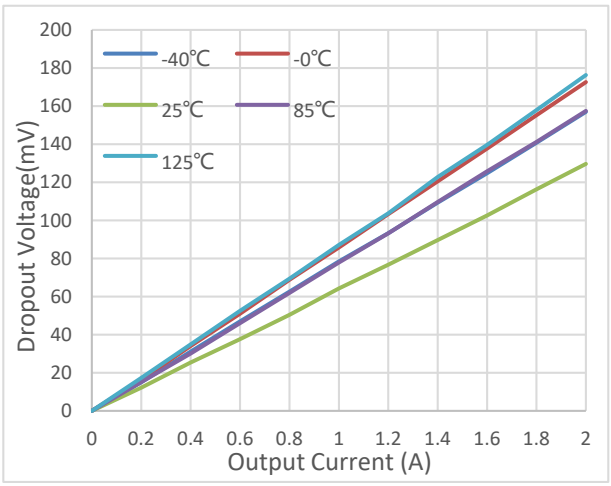
Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(TARGET)}$ + 0.4 V (whichever is greater), $V_{OUT(TARGET)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT}= 10 µF, unless otherwise noted.



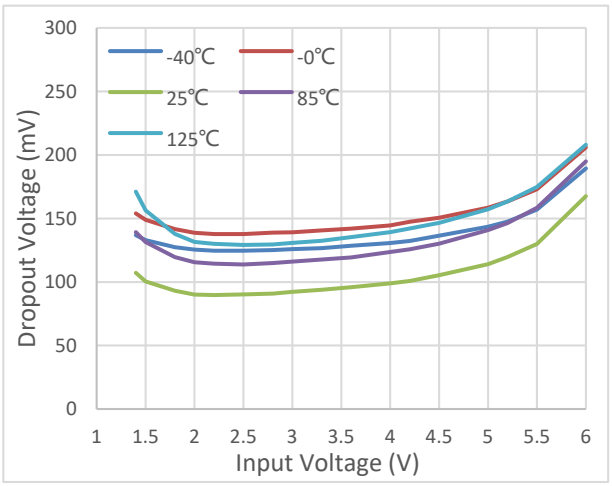
V_{IN}=1.4V

Dropout Voltage vs Output Current



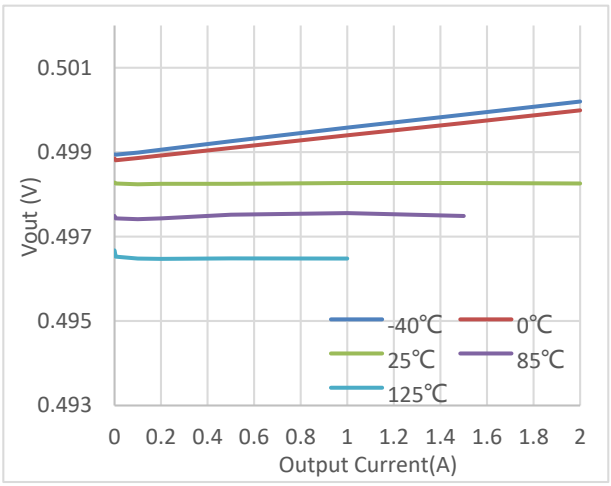
V_{IN}=5.5V

Dropout Voltage vs Output Current



IOUT=1.2A

Dropout Voltage vs Input Voltage

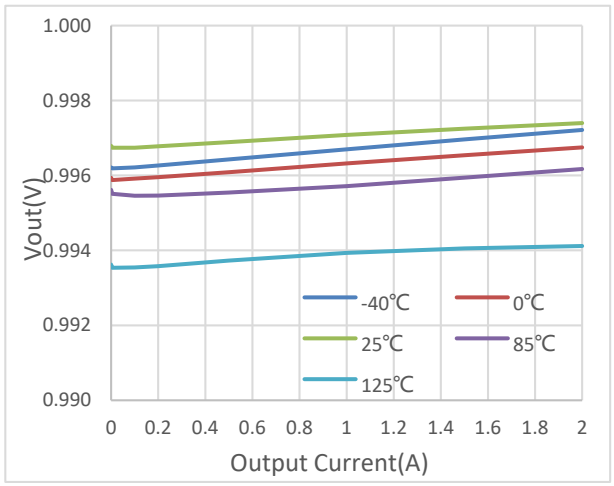


VIN=1.4V, VOUT=0.5V, OUT=FB

Output Voltage vs Output Current

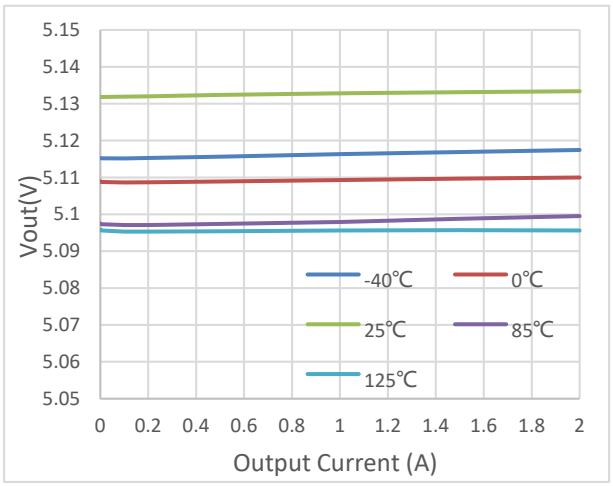
Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(TARGET)}$ + 0.4 V (whichever is greater), $V_{OUT(TARGET)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT}= 10 µF, unless otherwise noted.



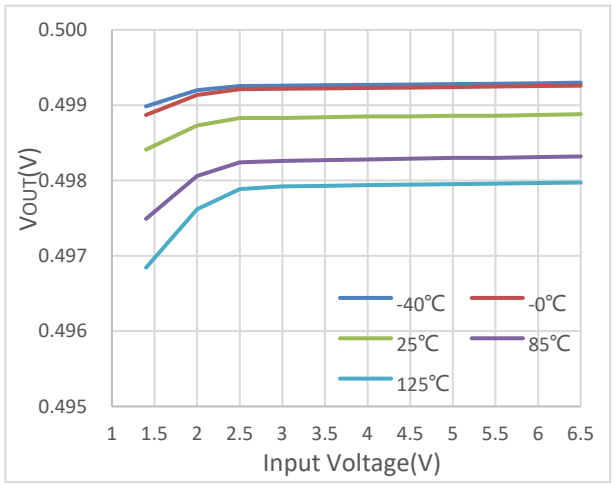
V_{IN}=1.4V, V_{OUT}=1.0V

Output Voltage vs Output Current



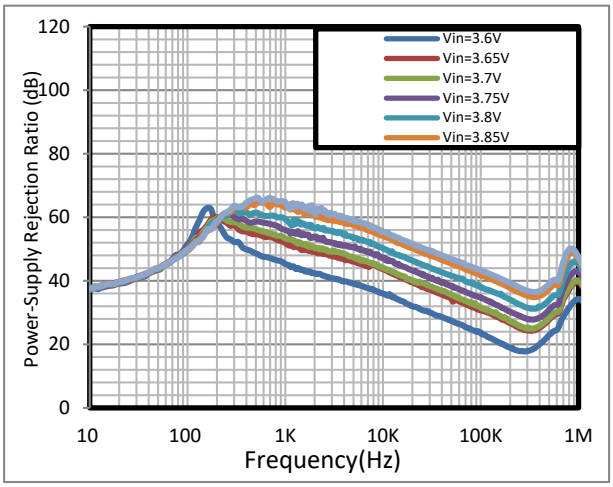
V_{OUT}=5.1V

Output Voltage vs Output Current



V_{IN}=1.4V, V_{OUT}=0.5V, OUT=FB

Output Voltage vs Input Voltage



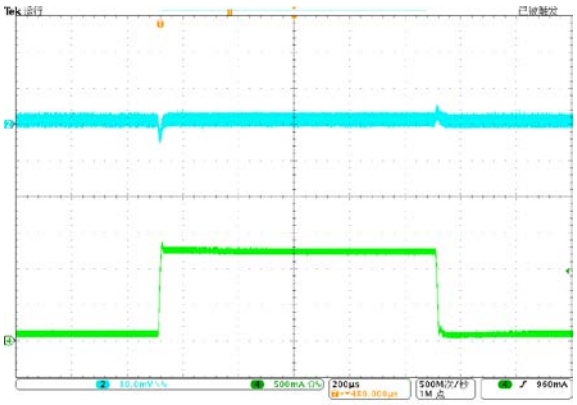
V_{OUT} = 3.3V, I_{OUT} = 1.2A

C_{OUT} = 10 µF || 10 µF, C_{FF} = 10 nF

PSRR vs Frequency and Vin for Vout = 3.3V

Typical Operating Characteristics

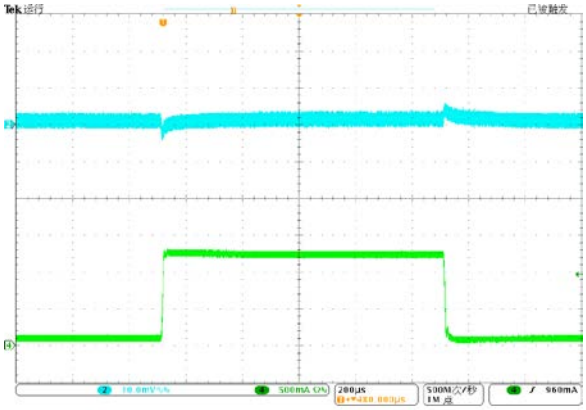
T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(TARGET)}$ + 0.4 V (whichever is greater), $V_{OUT(TARGET)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT}= 10 µF, unless otherwise noted.



CH2=V_{OUT}，CH4=I_{OUT}

V_{IN}=1.4V, V_{OUT}=0.5V, I_{OUT}=100mA – 1.2A

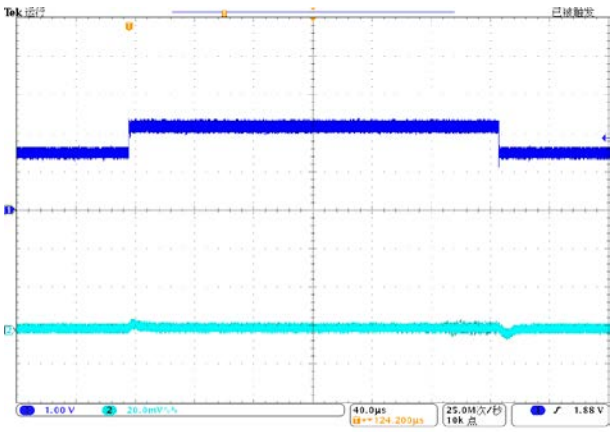
Load Transient V_{OUT} = 0.5V



CH2=V_{OUT}，CH4=I_{OUT}

V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=100mA – 1.2A

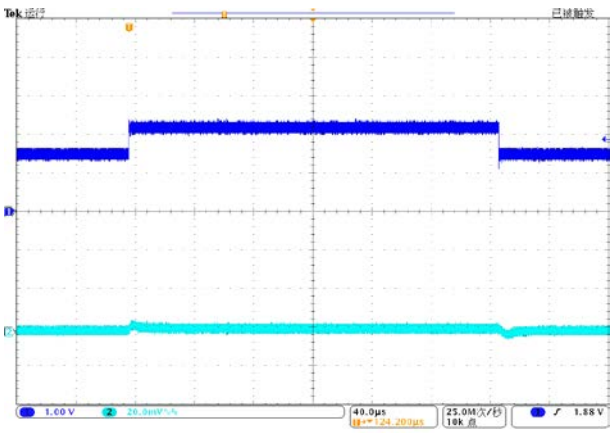
Load Transient VOUT = 3.3V



CH1=V_{IN}, CH2=V_{OUT}

V_{IN}=1.4 - 2.0V, V_{OUT}=0.5V, I_{OUT}=5mA

Line Regulation @ V_{OUT}=0.5V



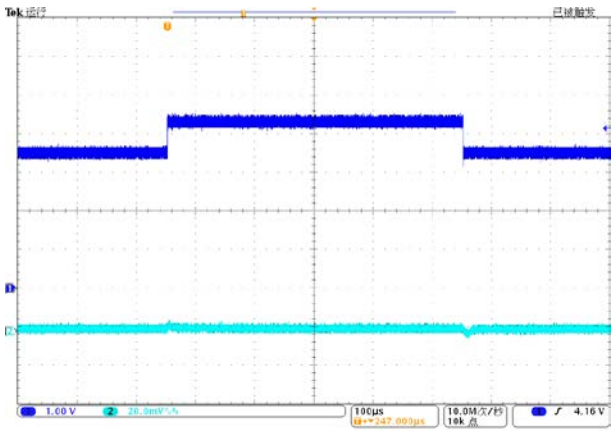
CH1=V_{IN}, CH2=V_{OUT}

V_{IN}=1.4 - 2.0V, V_{OUT}=1.2V, I_{OUT}=5mA

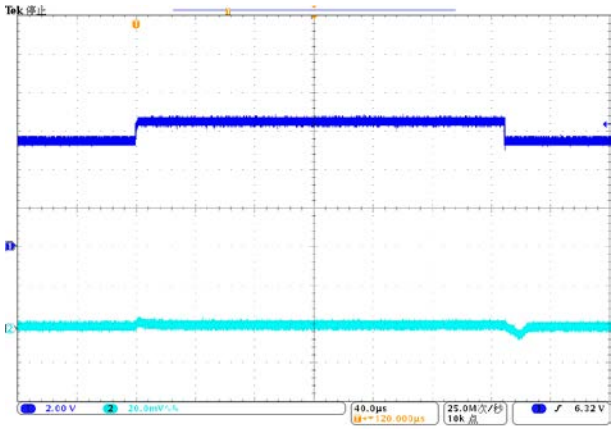
Line Regulation @ V_{OUT}=1.2V

Typical Operating Characteristics

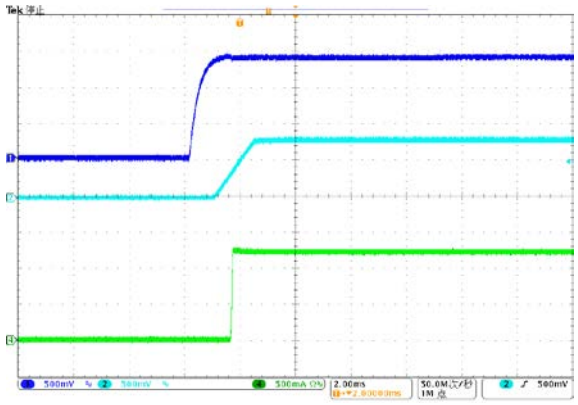
T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(TARGET)}$ + 0.4 V (whichever is greater), $V_{OUT(TARGET)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT}= 10 µF, unless otherwise noted.



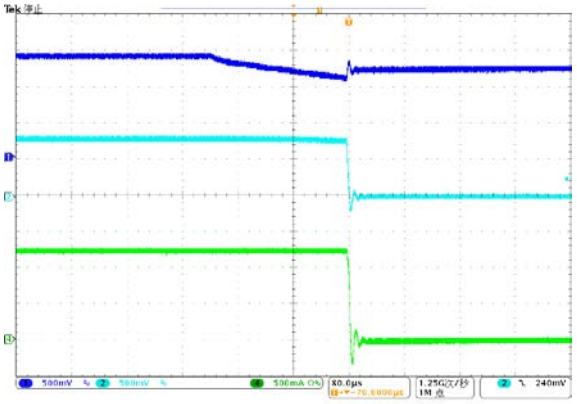
CH1=VIN, CH2=VOUT
VIN=2.0 – 3.5V, VOUT=3.3V, IOUT=5mA
Line Regulation @ VOUT=3.3V



CH1=VIN, CH2=VOUT
VIN=5.2 – 6.5V, VOUT=5.0V, IOUT=5mA
Line Regulation @ VOUT=5.0V



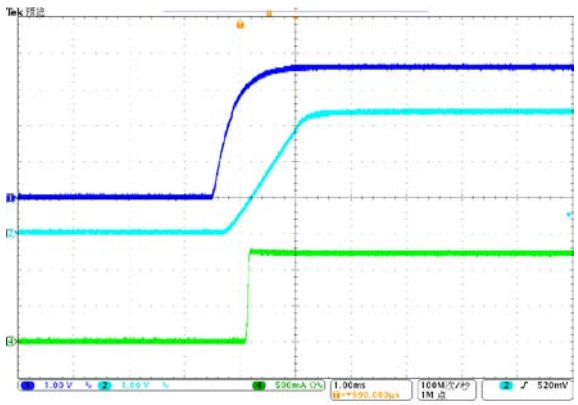
CH1=V_{IN}, CH2=V_{OUT}, CH4=I_{OUT}
V_{IN}=1.4V, V_{OUT}=0.5V, I_{OUT}=1.2A
Power On by VIN=VEN=1.4V @ V_{OUT}=0.5V



CH1=V_{IN}, CH2=V_{OUT}, CH4=I_{OUT}
V_{IN}=1.4V, V_{OUT}=0.5V, I_{OUT}=1.2A
Power Off by VIN=VEN=1.4V @ V_{OUT}=0.5V

Typical Operating Characteristics

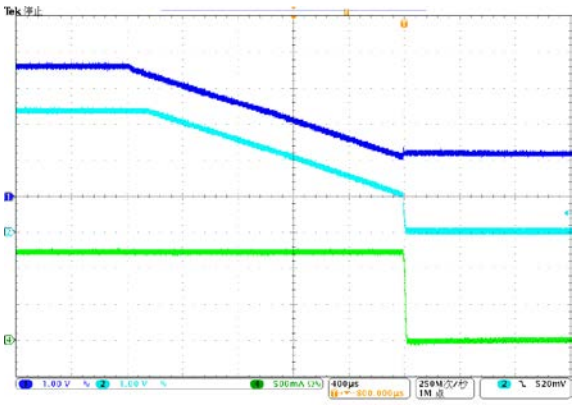
T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(TARGET)}$ + 0.4 V (whichever is greater), $V_{OUT(TARGET)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT}= 10 µF, unless otherwise noted.



CH1=V_{IN}, CH2=V_{OUT}, CH4=I_{OUT}

V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=1.2A

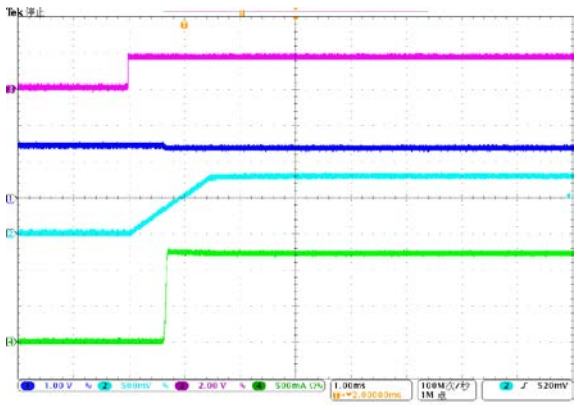
Power On by VIN=VEN=3.6V @ V_{OUT}=3.3V



CH1=V_{IN}, CH2=V_{OUT}, CH4=I_{OUT}

V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=1.2A

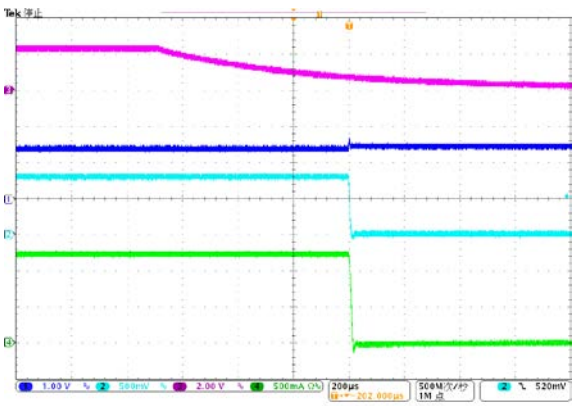
Power Off by VIN=VEN=3.6V @ V_{OUT}=3.3V



CH1=V_{IN}, CH2=V_{OUT}, CH3=EN, CH4=I_{OUT}

V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=1.2A

Power On by VEN @ V_{OUT}=3.3V



CH1=V_{IN}, CH2=V_{OUT}, CH3=EN, CH4=I_{OUT}

V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=1.2A

Power Off by VEN @ V_{OUT}=3.3V

7 Typical application circuit

Figure 7-1 Typical GD30LD1002x application circuit with adjustable resistance

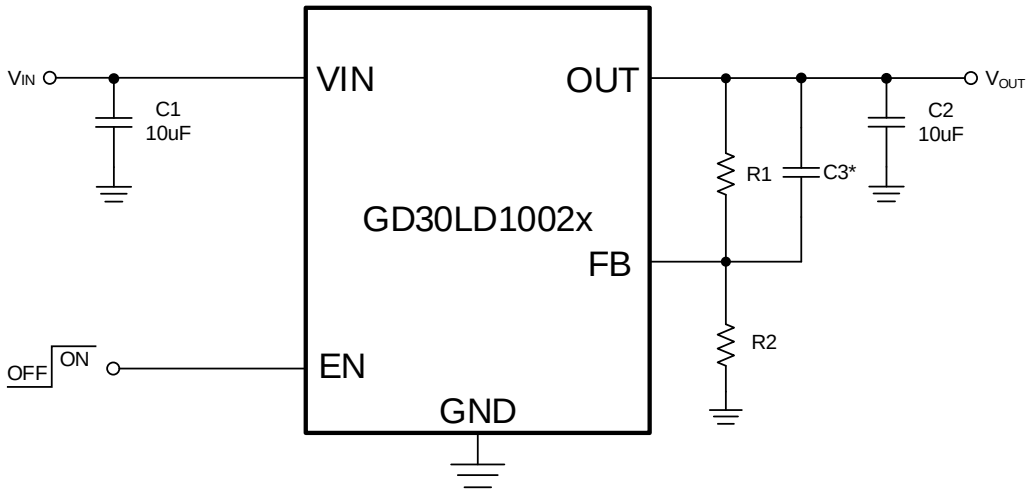
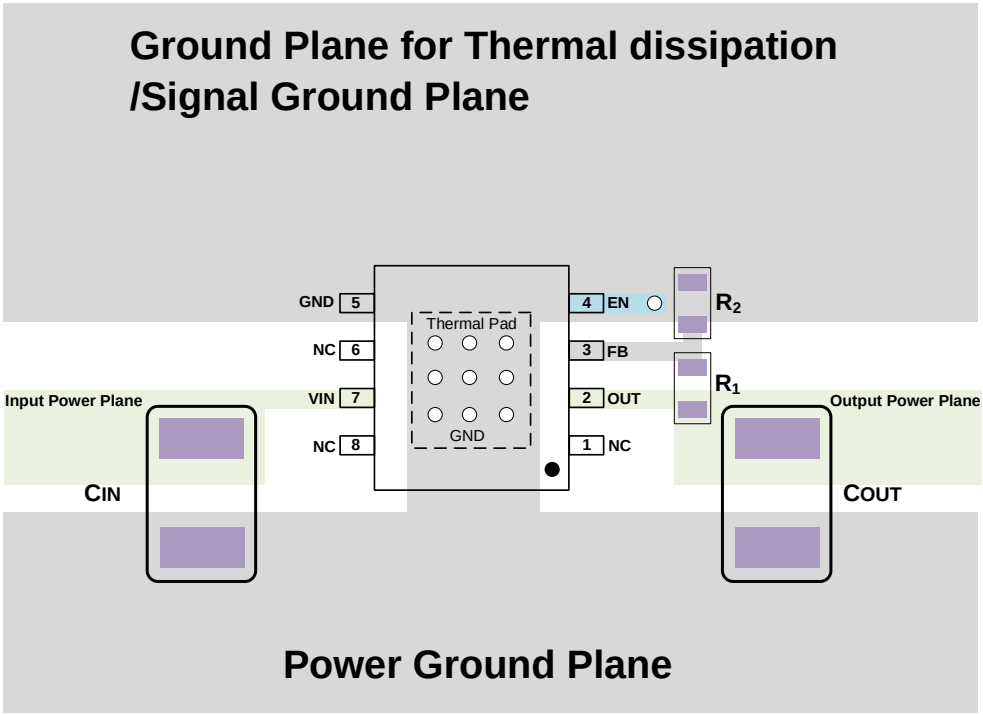


Table 7-1 Adjusted V_{OUT} by external feedback resistor

V_{OUT}(V)	External Feedback Resistor	
	R1 (kΩ)	R2(kΩ)
0.5	0	NC
0.6	11	54.9
0.7	10.2	25.5
0.8	10.7	17.8
0.9	11	13.7
1.0	11	11
1.2	9.31	6.65
1.8	10.2	3.92
2.5	10.8	2.7
3.0	11	2.2
3.3	11.2	2
5.0	10.8	1.2
5.2	12.22	1.3

8 Layout guideline

Figure 8-1 Typical GD30LD1002x layout guideline



Notes:

1. The capacitor C_{IN} and C_{OUT} should be placed on the top layer to reduce parasitic parameters.
2. All capacitors are as close as possible to the corresponding pins of the LDO regulator.

9 Package information

9.1 DFN8 package outline dimensions

Figure 9-1 DFN8 package outline

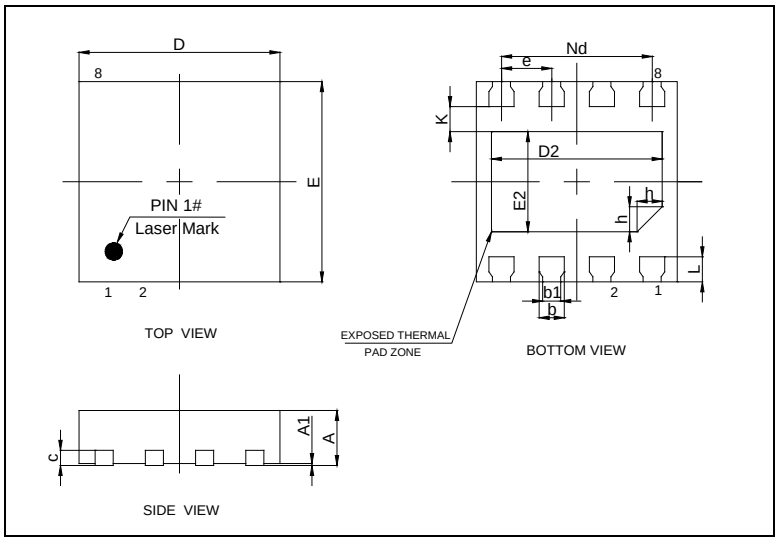
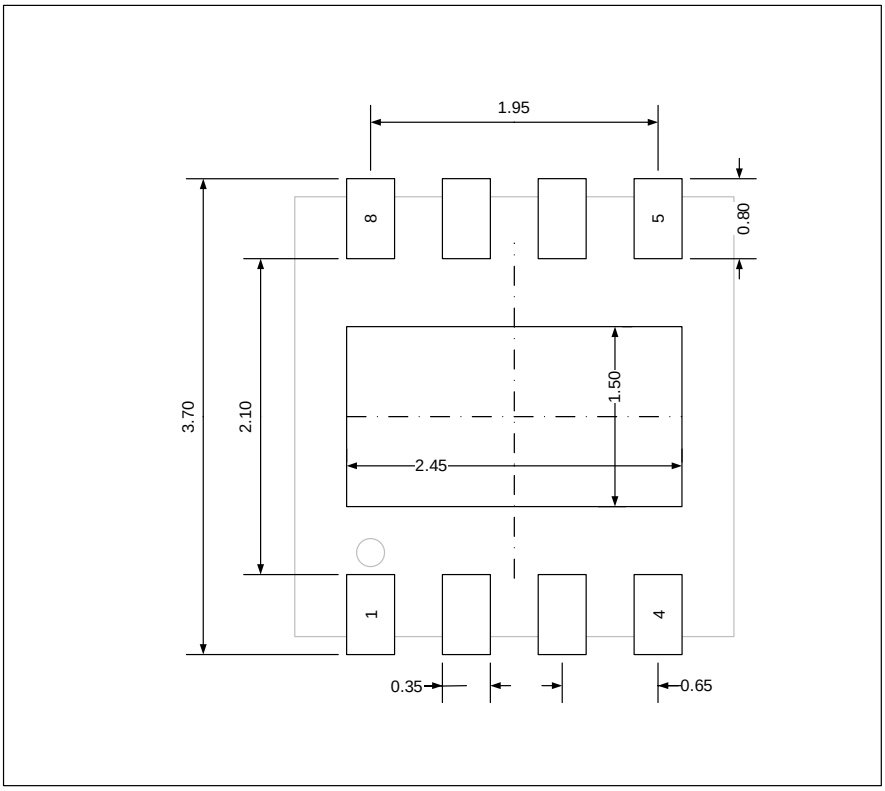


Table 9-1 DFN8 package dimensions(in mm)

Symbol	Min	Typ	Max
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1	—	0.20	—
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
e	—	0.65	—
h	0.20	0.25	0.30
K	—	0.325	—
L	0.30	0.40	0.50
Nd	—	1.50	—

(Original dimensions are in millimeters)

Figure 9-2 DFN8 recommend Footprint



9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J – T_B)/P_D$

$\Theta_{JC} = (T_J – T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 9-2 DFN8 Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	DFN8	74.9	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	DFN8	31.8	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	DFN8	36.7	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	DFN8	31.8	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	DFN8	2.60	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

10 Ordering information

Table 10-1 Part ordering code for GD30LD1002x devices

Ordering Code	Package	Package Type	Packing Type	MOQ	Temperature Junction Range
GD30LD1002WETR-I	DFN8	Green	Tape&Reel	3000	Industrial -40°C to +125°C

11 Revision history

Table 11-1 Revision history

Revision No.	Description	Date
1.0	Initial Release	May.29, 2023

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