5-Channel Capacitive Touch and Proximity Controller

Features

- 5-channel capacitive sensing
  - Self/Mutual capacitive sensing techniques
  - Capacitance resolution down to 1aF
  - Auto-Offset-Tuning (AOT)
  - Adaptive Temperature Compensation
  - Effective waterproof
  - Independent configurations per channel
- 400kHz I²C interface
  - Default address: 0x12
  - Address can be modified through CS2 pin
- External interrupt pin INTN, open-drain output
- Built-in brown-out reset(BOR)
- Embedded 8KB SRAM and 16KB FLASH
- Low power consumption
  - Active mode: 28μA
  - Doze mode: 7.7μA
  - Sleep mode: 6.3μA
  - Deep Sleep mode: 2.5μA
- 2.7V~3.6V power supply
- DFN 1.8mm×2.1mm×0.55mm -10L package

Applications

Mobile phones, Tablets, Notebooks

Wearable devices

General Description

AW96205DNR is a 5-channel low-power capacitive touch and proximity controller. Each channel can be independently configured as sensor input, shield output.

Advanced self-capacitance technology is adopted in AW96205DNR. For the device has a high-resolution ADC, the minimal capacitance that can be detected is as low as 1aF.

AW96205DNR integrates a ultra-low-power MCU, by executing the algorithm program in the FLASH, it implements diversified analog front end (AFE) sampling controlling and complicated data processing algorithms including signal filtering, RF noise suppression, baseline calculation, proximity detection, etc.

With the auxiliary of DSP algorithm, the device is able to track gradual environmental variations (such as temperature, humidity, etc.) and maintain high performance operation.

Typical Application Circuit

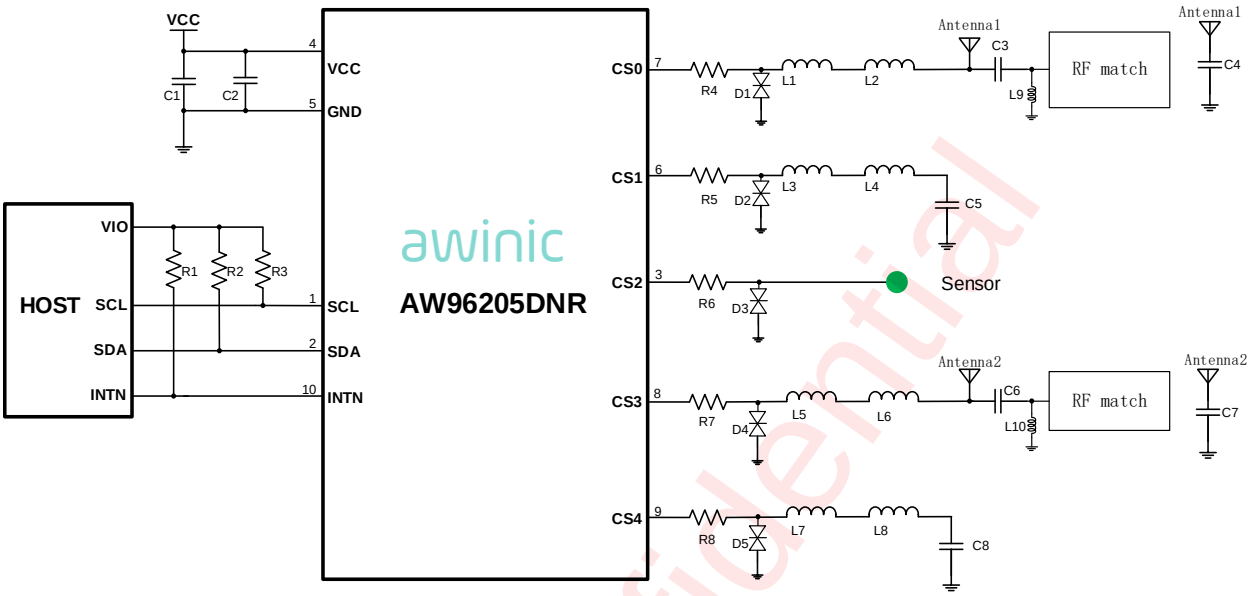
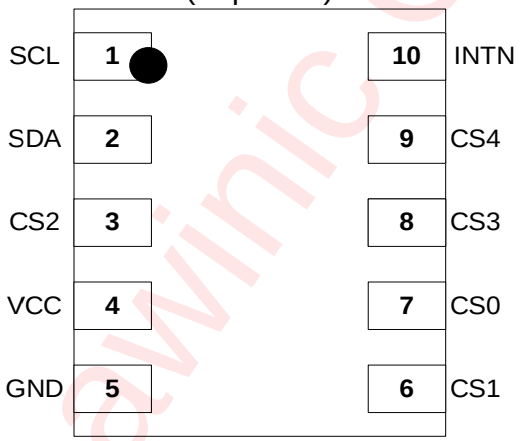


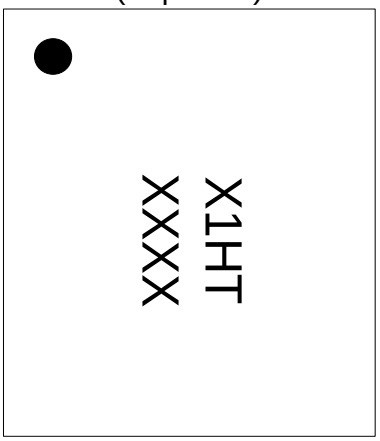
Figure 1 AW96205DNR Typical Application Circuit

Pin Configuration And Top Mark

AW96205DNR
(Top View)



AW96205DNR Marking
(Top View)

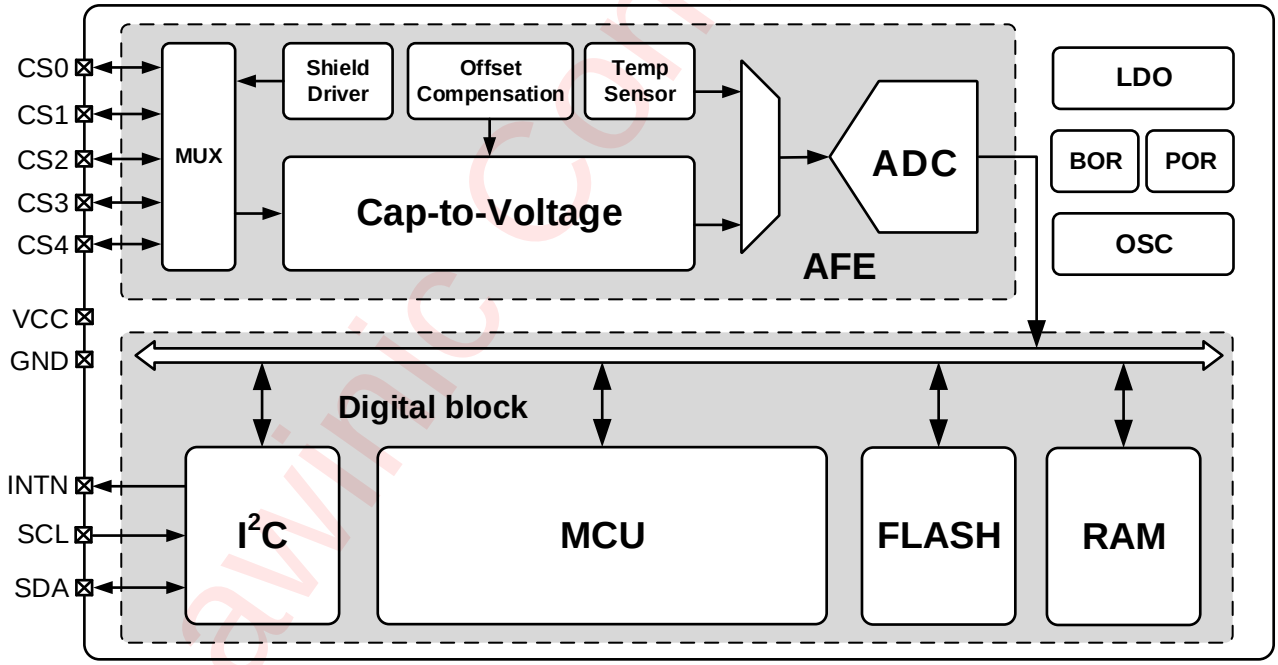


X1HT - AW96205DNR
XXXX - Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	SCL	Serial clock input for I²C interface
2	SDA	Serial data I/O for I²C interface
3	CS2	Sensor electrode or I²C address select input (Floating:0x12, GND:0x13, VCC:0x14)
4	VCC	Power supply(2.7V~3.6V)
5	GND	Ground
6	CS1	Sensor electrode
7	CS0	Sensor electrode
8	CS3	Sensor electrode
9	CS4	Sensor electrode
10	INTN	Interrupt output (open drain)

Functional Block Diagram



Notes: AFE means Analog Front-End.

Figure 2 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW96205DNR	-40°C~85°C	DFN 1.8mm×2.1mm ×0.55mm-10L	X1HT	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC		-0.5V to 3.9V
Input voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.9V
Output voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.9V
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including HBM CDM)(NOTE 2)		
HBM		±8kV
CDM		±1.5kV
Latch-Up		
Test condition: according to JESD78E		+IT：350mA -IT：-350mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method: ESDA/JEDEC JS-001-2017, the CDM test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

PARAMETERS	SYMBOL	MIN	MAX	UNIT
Supply voltage	VCC	2.7	3.6	V
Pull-up voltage	VIO	1.1	3.6	V
Ambient temperature	T_A	-40	85	°C

Electrical Characteristics

Note: Typical values are given for T_A = +25°C, VCC=2.8V unless otherwise specified.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
CHIP CURRENTS							
$I_{DEEPSLEEP}$	Deep Sleep Mode Current	LDO on, OSC off I²C listening			2.5		μA
I_{SLEEP}	Sleep Mode Current	LDO on, OSC on I²C listening			6.3		μA
I_{DOZE}	Doze Mode Current	SCANPERIOD = 400ms FREQ = 100kHz; CDCRES = 6 CHEN = b000001 Digital filter features OFF I²C listening. No load			7.7		μA
I_{ACTIVE}	Active Mode Current	SCANPERIOD = 30ms FREQ = 100kHz CDCRES = 6 CHEN = b000001 Digital filter features OFF I²C listening. No load			28		μA
CAPACITANCE SENSING							
C_{RANGE}	Measurement Range			±0.55	±2.2	±9.9	pF
N_{BIT}	Measurement Resolution				21		bits
C_{RES}				1			aF
F_{OSC}	Nominal OSC Frequency				4		MHz
F_{Trim}	OSC Trim Accuracy	Around Nominal Value, Ta=25°C, VCC=2.8V		-4		4	%
F_{Temp}	OSC Temp. Dependency	Around Nominal Value, Full Ta range, VCC=2.8V		-1		1	%
F_{VCC}	OSC VCC Dependency	Around Nominal Value, Ta=25°C, Full VCC range		-0.6		0.6	%
Fs	Nominal Sampling Freq	Programmable with FREQ				250	kHz
C_{DCEXT}	External DC Cap. to GND per Measurement Phase	One CSx as measured input	Normal Mode			220	pF
			Enhanced Mode			400	
R_{FILTIN}	Input driving Res			0		30	kΩ
R_{INT}	Compensation Res			125		1000	Ω
TEMPERATURE SENSING							
$T_{INRANGE}$	Input Range	Ambient Temperature(T_A)		-40		85	°C
$T_{OUTRANGE}$	Output Range			0		32767	LSB
I²C INTERFACE							
I_{OL} (SDA，INTN)	Output low current	V_{OL}≤0.4V		8			mA
V_{IH}	Input high level	SCL, SDA		0.84		3.6	V
V_{IL}	Input low level	SCL, SDA		-0.5		0.36	V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{DEG_SDA}	SDA deglitch time	SDA		88		ns
t_{DEG_SCL}	SCL deglitch time	SCL		77		ns

I²C Interface Timing

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency			400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
T_{LOW}	Low level width of SCL	1.3			μs
T_{HIGH}	High level width of SCL	0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6			μs
$T_{HD:DAT}$	Data hold time	0			μs
$T_{SU:DAT}$	Data setup time	0.1			μs
T_R	Rising time of SDA and SCL			0.3	μs
T_F	Falling time of SDA and SCL			0.3	μs
$T_{SU:STO}$	Stop condition setup time	0.6			μs
T_{BUF}	Time between start and stop condition	1.3			μs

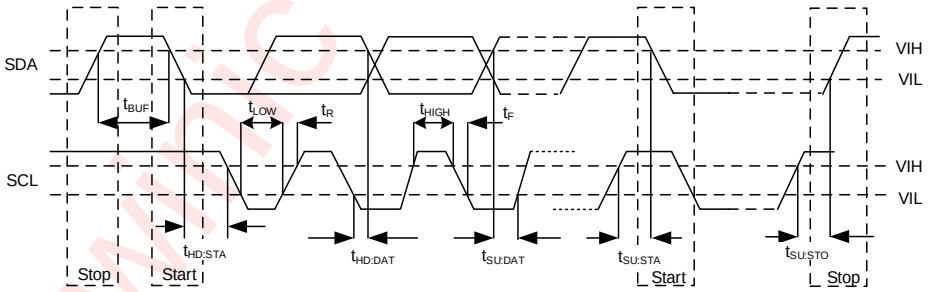


Figure 3 I²C Interface Timing

Detailed Functional Description

Overview

AW96205DNR is a capacitive proximity sensing controller with a built-in ultra-low-power MCU. It is comprised of high-performance self-capacitance detecting Analog-Front-End (AFE), imbedded 32bit MCU, FLASH, RAM, OSC and I^2C interface, etc. The AFE drive the sensor and shield electrode, and convert the capacitance of sensor to digital data. The MCU executes the algorithm program stored in the FLASH, and perform complicated data process such as signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency(RF) noise suppression, proximity decision, etc.

Capacitive Sensor Introduction

When a conductive object, such as a finger, comes in contact or close proximity with the sensing electrode, the capacitance of one or more sensors changes. The figure below shows the basic structure and equivalent model of a capacitive sensor. The top layer is the frontpanel, and the middle green area below is a copper sensor pad. The sensor is usually surrounded by ground, resulting in a parasitic capacitance(C_{PARA}).

There are two main operational modes in the capacitance sensing circuits: self-capacitance sensing and mutual capacitance sensing. An electric field is created around the sensor when system is working. In the self-capacitance sensing mode, with target object approaching, some of the electric field lines couple to the target object and add a small amount of finger capacitance (C_{PROX}) to the existing C_{PARA}. This feature can be used to detect proximity or touch action.

At least two electrodes are needed in the mutual capacitance sensing mode: one is a transmitter (Tx) and the other is a receiver (Rx). Tx and ground will form a capacitance (C_{Tx}); Rx and ground will form a capacitance (C_{Rx}); Tx and Rx will form a capacitance (C_M). When target object approaches, Tx and Rx will form a capacitance ($C_{M'}$) which is less than C_M.

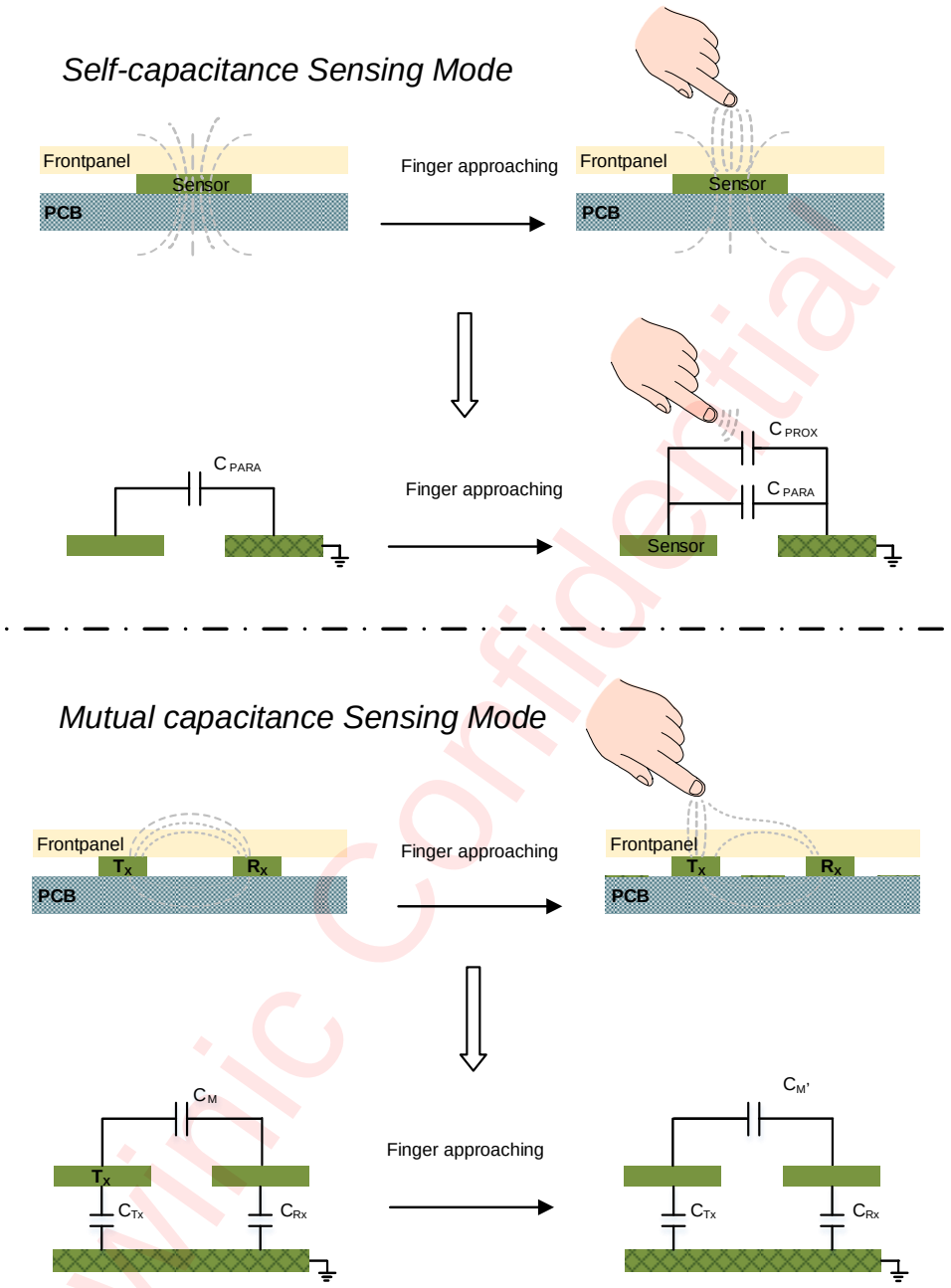


Figure 4 Capacitive Sensor Structure

Capacitive Sensing Techniques

The proximity sensing system consists of three parts: capacitive sensor, AFE and DSP. Among them, the function of AFE is to drive the capacitive sensor and the shield electrode, and convert the sensor capacitance into digital data. The function of DSP is to process the data from AFE and transmit the sensor capacitance value (CapDiff, CapValid) together with proximity status (status) to the host. When the target object is approaching or moving away, the proximity sensing system will transmit key information to the host after dedicated processing.

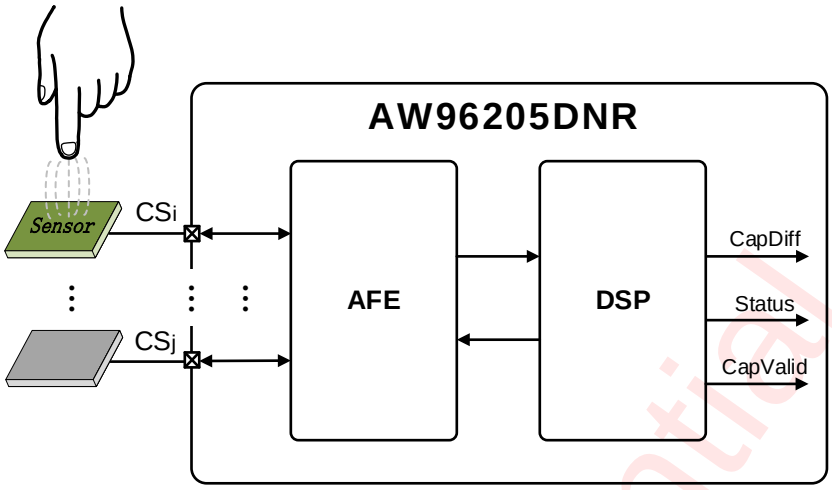


Figure 5 Proximity Sensor Operation Overview

AFE DESCRIPTION

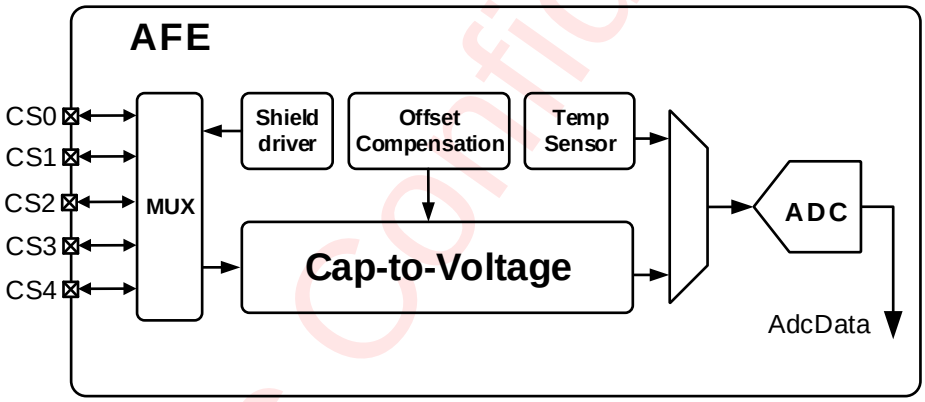


Figure 6 AFE Block Diagram

※ MUX selects CSx as capacitance measurement input or shield output

※ If CSx is used as shield electrode, it is excited by shield driver. The driven shield signal is a replica of the sensor signal. Shield electrode around can protect the sensor from environmental interference，and reduce the parasitic capacitance.

※ Cap-to-Voltage integrates a charge amplifier, it detects the sensor capacitance with a charge-transfer method. The capacitance is converted into a voltage signal, which is the input of ADC.

※ Offset Compensation measures parasitic capacitance(C_{PARA}), which is compensated during the process of charge transferring of Cap-to-Voltage. Thus, the input capacitance of Cap-to-Voltage is nearly C_{PROX} alone.

※ Temp Sensor measures the temperature of the chip, and the output is converted by ADC to digital data. The temperature data can be used as reference to correct the capacitance measurement result.

※ ADC converts voltage signals obtained by Cap-to-Voltage or Temp Sensor into AdcData.

DSP DESCRIPTION

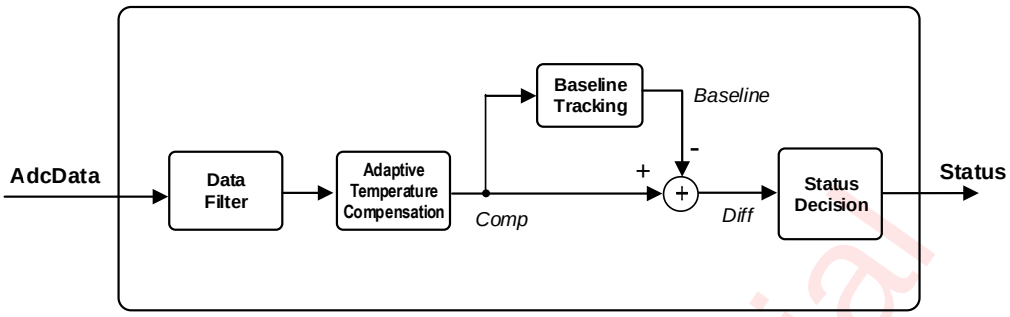


Figure 7 Digital Signal Processing Diagram

※ DSP processes the AdcData from the AFE, and finally outputs a series of reliable proximity status.

※ Data Filter effectively filters the high-frequency noise and interference, which greatly improves the signal-to-noise ratio(SNR).

※ The adaptive temperature compensation module can automatically compensate for environmental drift in real time, especially temperature drift. Thereby it can be ensured that the final proximity status will not be misjudged due to temperature drift.

※ The role of the Baseline is to further track the slowly varying data caused by the residual temperature compensation or other gradual environmental drift.

※ Finally, the Status Decision module outputs a certain and reliable proximity status based on the Diff data and the proximity threshold etc.

SCAN PERIOD

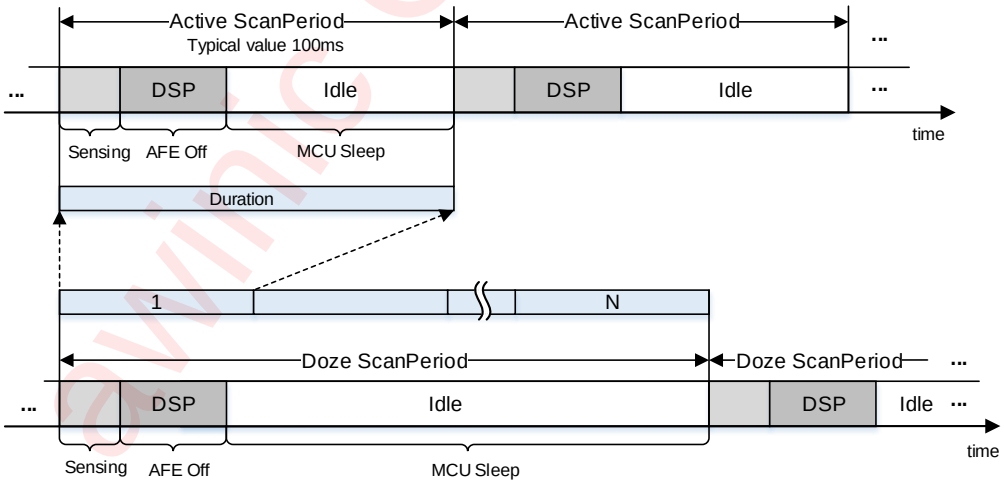


Figure 8 Active Mode and Doze Mode Scan Period

Each scan period can be divided into three stages. In the first stage, the selected sensor channel is scanned and AdcData is generated. In the second stage, the AFE is closed and the AdcData obtained by the DSP module is processed. In the last stage, all data processing has been completed and the chip enters idle status, in order to reduce power consumption, neither AFE nor MCU will work.

The figure above shows the composition and meaning of the active mode and doze mode scan periods. The scan period of active mode and doze mode can be configured by register SCANCTRL1(Address: 0x1A04)

and AFECFG3_CHx (x=0,…,4). Generally, doze mode consumes much lower power than active mode.

Clock

The chip uses a built-in 4MHz OSC clock.

Reset

POWER ON RESET (POR)

Reset operation is triggered during power up. When nRST released, the initialization process starts to perform and it will last for about 20ms. INTN will be set to low when the initialization process is completed, then I²C can communicate normally.

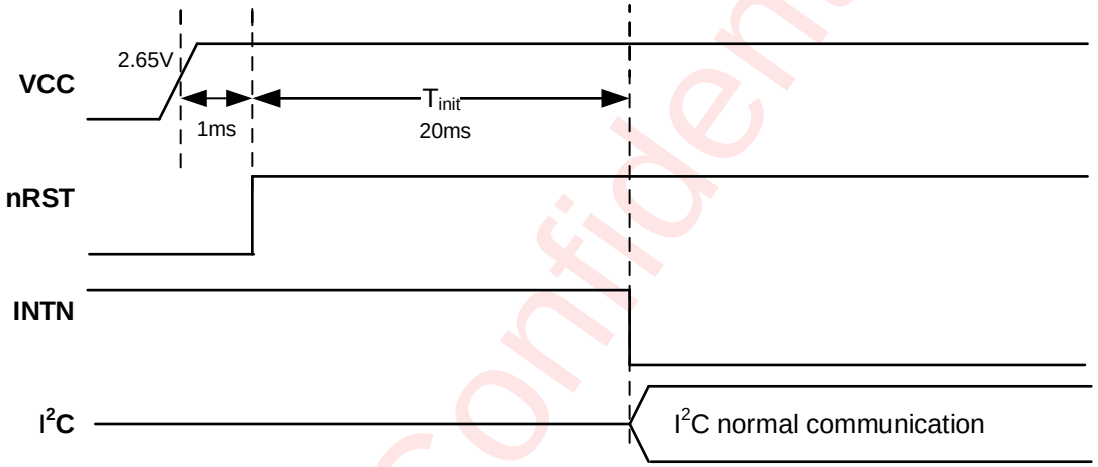


Figure 9 Power On Timing

BROWN OUT RESET (BOR)

Reset operation is triggered when VCC drop to the threshold of BOR. After the reset operation, all the registers will be reset to the default value. The chip returns to normal operation mode until the power supply rises to a normal value.

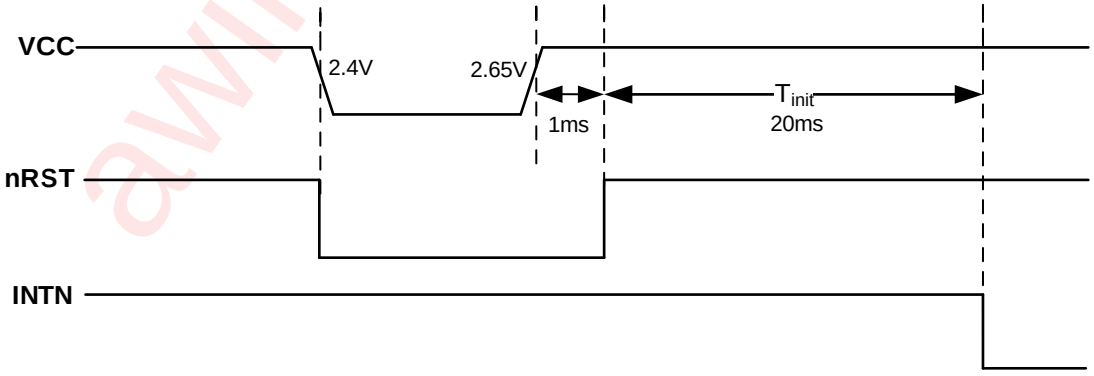


Figure 10 Brown Out Timing

SOFT RESET

The soft reset operation can be triggered by writing “0x3C” to the soft reset register (Address: 0xFF18). After

the reset operation is completed, all the registers will be reset to the default value.

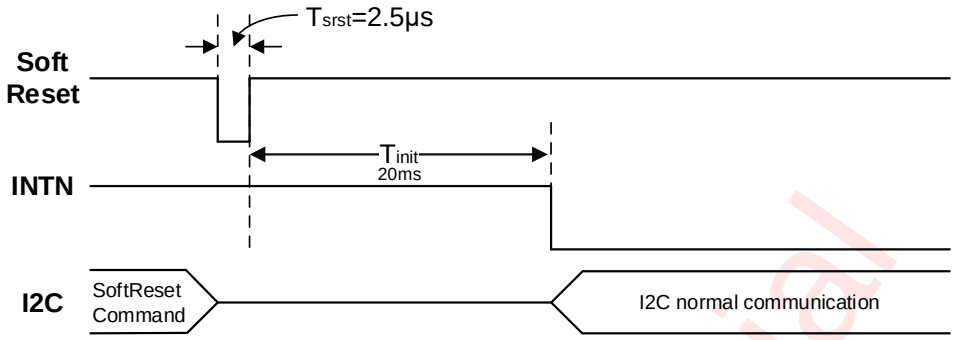


Figure 11 Soft Reset Timing

Initialization

After power on, OSC runs normally, and MCU starts to execute the initialization program in FLASH. It performs the following operations.

- Read information from NVM
- Set I²C device address according to CS2 pin status
- Issue an interrupt after initialization and then enters into sleep mode.

Operation Mode

There are four operation modes in the chip: DeepSleep, Sleep, Active and Doze.

DEEPSLEEP

The device power consumption is lowest in this mode. OSC and AFE are closed, CPU is sleeping, only I²C interface is active.

SLEEP

The device is in a low power state. OSC is on, AFE is off, and CPU is sleeping, waiting for interrupt to wake up.

ACTIVE

The device works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When no touch or proximity has been detected for some time, it will automatically switch to Doze mode. In this mode the external HOST can send SLEEP command to switch the device into sleep mode.

DOZE

Scan period is long, MCU and AFE work intermittently. During most of the period, quite a bit of modules are in idle state. So the average power consumption is lower.

Once a proximity is detected in doze mode, it will automatically return to active mode. The external HOST can also send SLEEP command to switch the device to sleep mode.

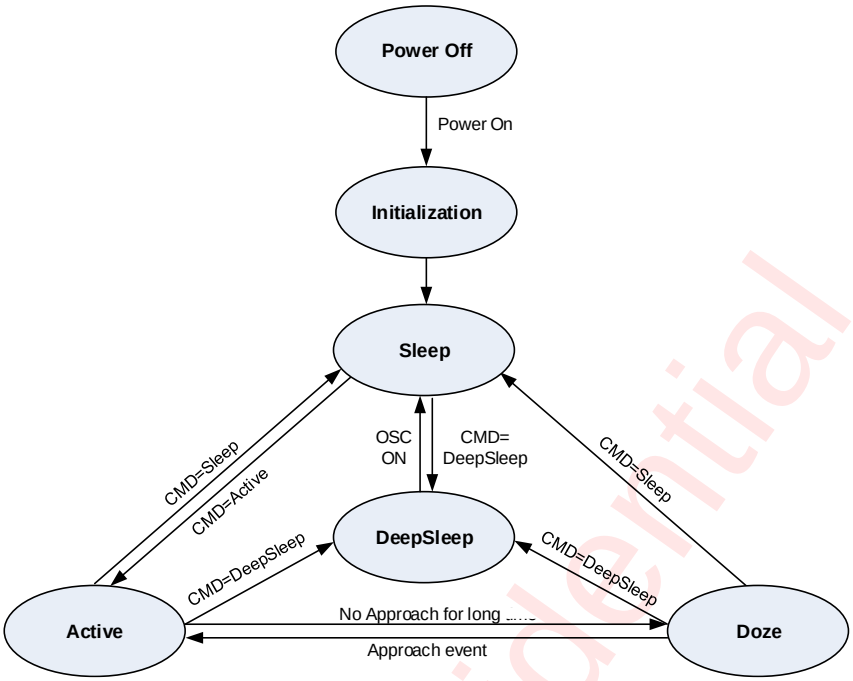


Figure 12 Operation Mode Switching

Interrupt

The chip reports the interrupt signal to the host through the INTN pin. Register IRQSRC (Address: 0x4410) stores interrupt information, including the completion of parasitic capacitance calibration, scan cycle completion, and so on. Register IRQSRC is cleared after host read. The specified interrupt signal can be shielded by configuring IRQEN (Address: 0x4414).

Power Consumption Description

When the program is executed in FLASH, the power consumption of the chip increases significantly due to the high power consumption of FLASH itself，but when the firmware program is moved to RAM for execution, FLASH can be turned off, so the power consumption of the chip is significantly reduced. The power consumption of the chip in the two cases is shown in the following table (Power supply: 2.8V):

OPERATING MODE	EXECUTE THE FIRMWARE IN FLASH	EXECUTE THE FIRMWARE IN RAM	UNIT
Active mode	55	28	μA
Doze mode	29.8	7.7	μA
Sleep mode	9.0	6.3	μA
Deep Sleep mode	2.5	2.5	μA

I²C Interface

AW96205DNR supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW96205DNR can

support different high level of the I²C interface. Additionally, the I²C device supports continuous read and write operations. The I²C register address is 16-bit and register data is 32-bit, and the data transmission is in big-endian mode.

DEVICE ADDRESS

I²C Device Address Configuration

CS2 Connection	Device Address
Floating	0x12
GND	0x13
VCC	0x14

The I²C device address (7-bit, followed by the R/W bit(Read=1/Write=0)) of AW96205DNR depends on the CS2 pin status. The default value of I²C device address is 0x12, connecting pad CS2 to GND or VCC will change the device address as showed in table above. Note that when pad CS2 is connected to GND or VCC, it can't be used as sensor pad.

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

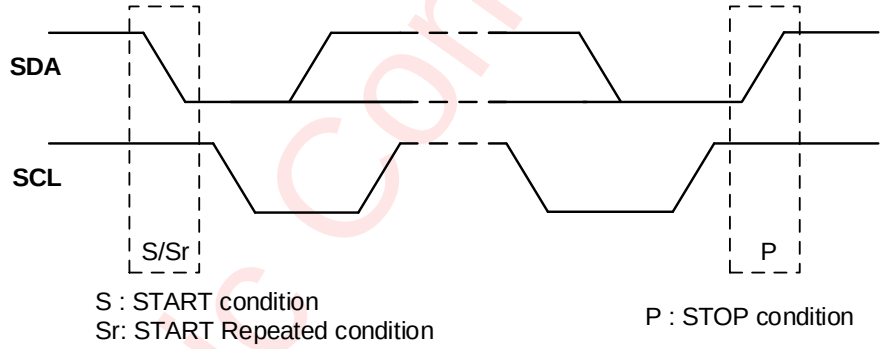


Figure 13 I²C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

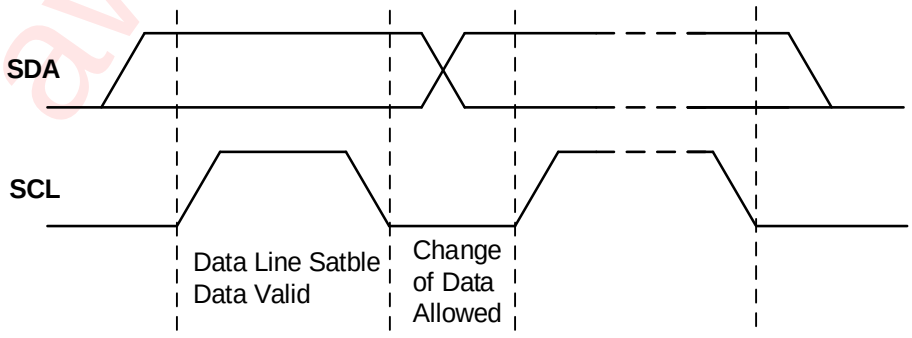


Figure 14 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

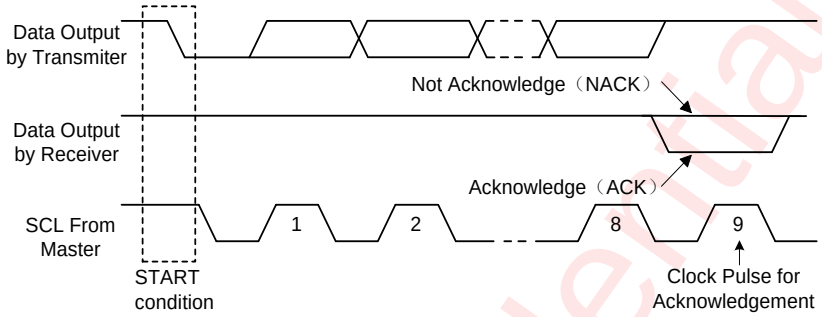


Figure 15 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 16-bit and register data is 32-bit. Note that I²C also support 8-bit data transfer. Writing process of I²C is showed as below picture.

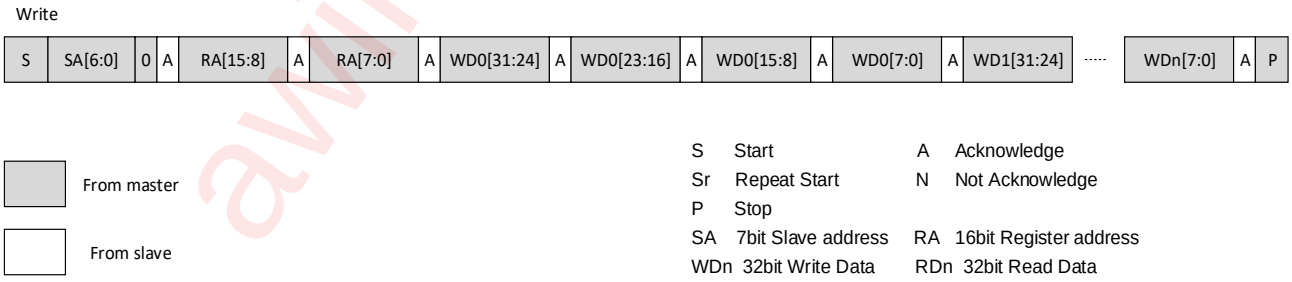


Figure 16 I²C Write Byte Cycle

READ CYCLE

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is showed as below picture.

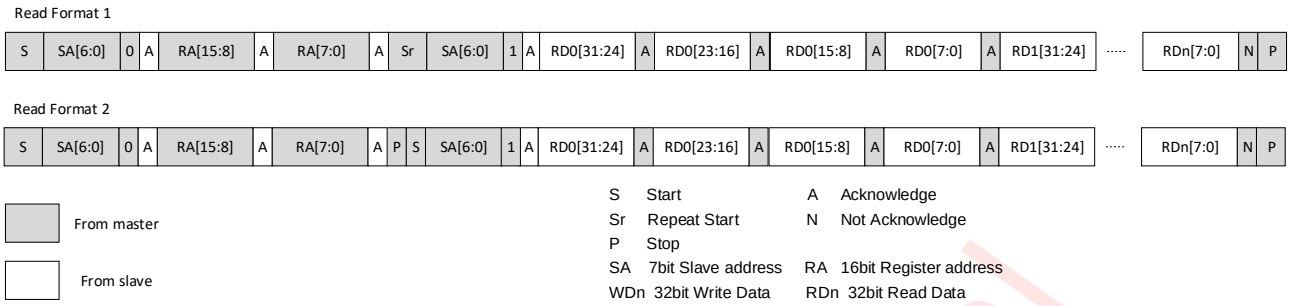


Figure 17 I²C Read Byte Cycle

Application Information

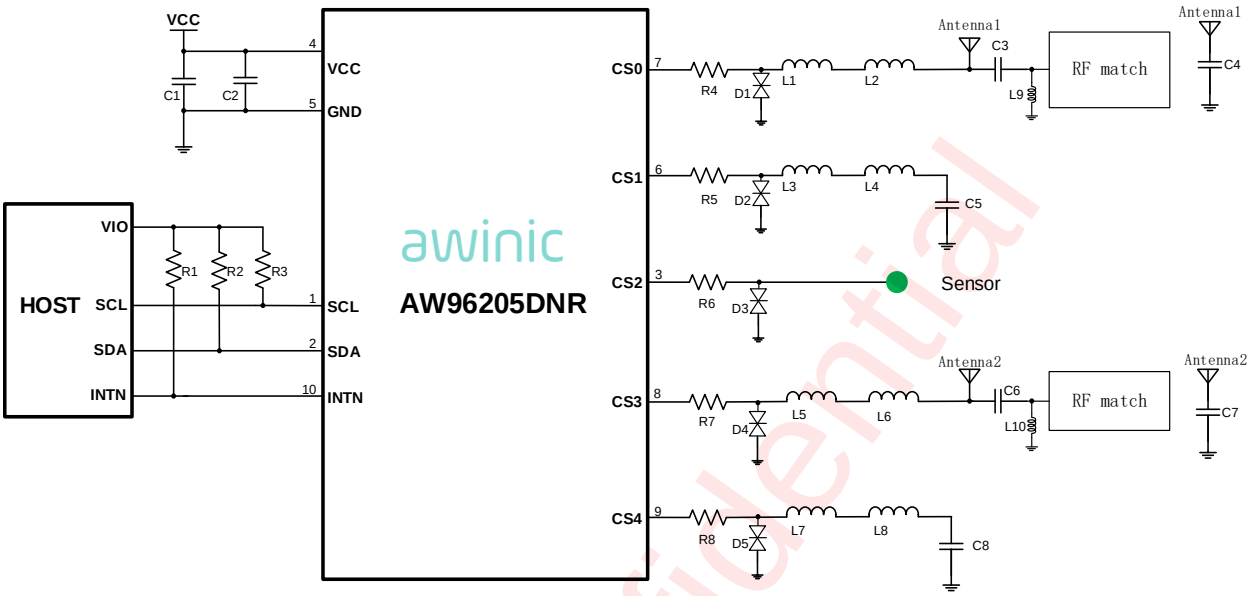


Figure 18 AW96205DNR Typical Application Circuit

Inductor Selection

The recommended values of the inductance L1~L8, which were applied in pins CS0, CS1, CS3, CS4, respectively, are all 100nH.

The recommended values of the inductance L9, L10, which were applied in CS0, CS3 pins, respectively, are all 68nH.

Transient Voltage Suppressor Selection

Transient voltage suppressor (TVS) with bipolar, low equivalent capacitance, operating voltage not less than 4.5V and equivalent capacitance not more than 0.5pF is recommended for CS0~CS4 pins (D1~D5).

Capacitor Selection

The recommended value of the capacitance C1 is 1μF and C2 is 0.1μF.

The recommended value of the capacitance C3~C8 are 22pF. It is suggested to use temperature insensitive capacitors to adjust the sensitivity, such as NP0 capacitors.

Resistor Selection

The recommended values of the resistor R1~R3, which were applied in pins SCL,SDA and INTN, are 4.7kΩ.

The recommended values of the resistor R4~R8, which were applied in pins CS0~CS4, are 1kΩ.

Recommended Components List

Component	Name	DESCRIPTION	TYP.	UNIT
L	L1~L8	-	100	nH
	L9, L10	-	68	nH
C	C1	-	1	μF
	C2	-	0.1	μF
	C3~C8	5% resolution Low temperature coefficient	22	pF
R	R1~R3	±5%	4.7	kΩ
	R4~R8	±5%	1	kΩ

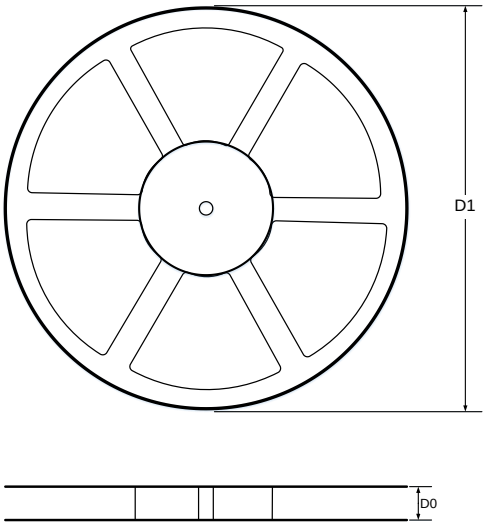
PCB Layout Consideration

AW96205DNR is a 5-channel capacitive touch and proximity controller, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

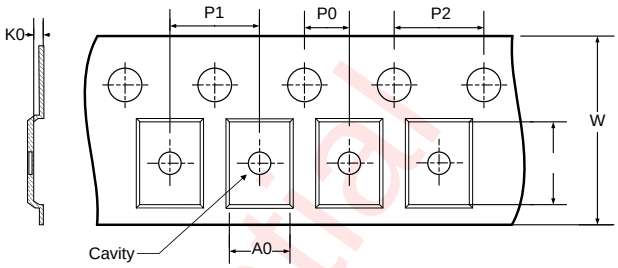
1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC.
2. Place the chip close to capacitive sensor and make trace as short as possible.
3. Make sure the sensor and traces be away from mic, earphone line in case of disturbing audio line.
4. Place reference channel along with sensor channel to get better performance.
5. Use low noise power supply for SAR sensor.

Tape And Reel Information

REEL DIMENSIONS

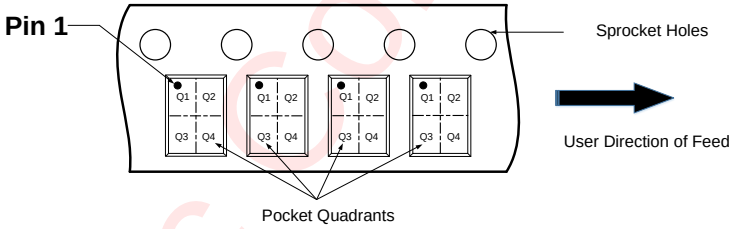


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

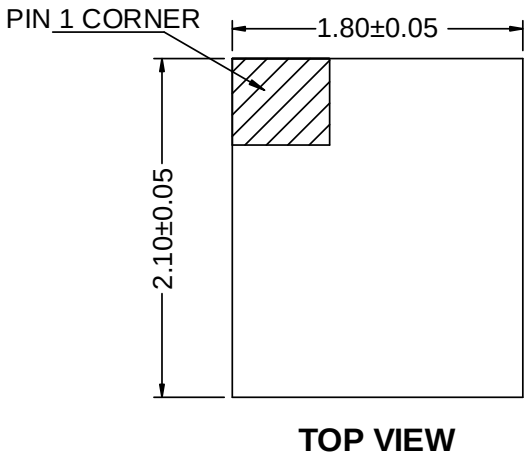


DIMENSIONS AND PIN1 ORIENTATION

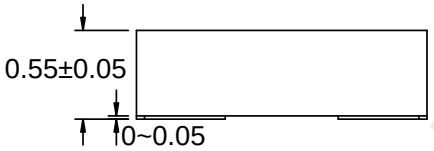
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2	2.3	0.75	2	4	4	8	Q1

All dimensions are nominal

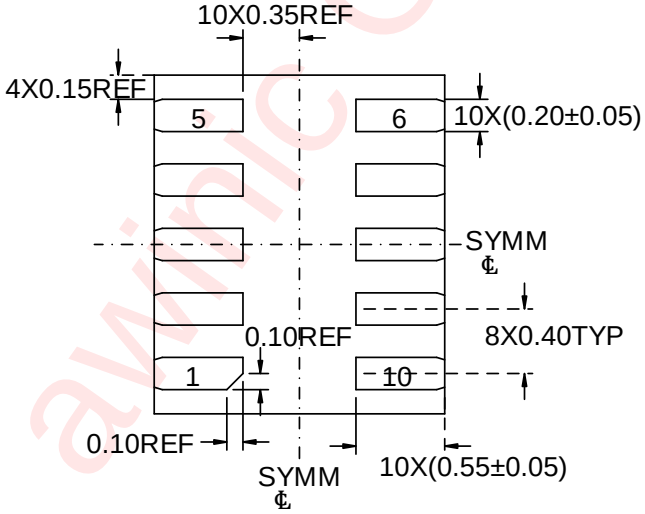
Package Description



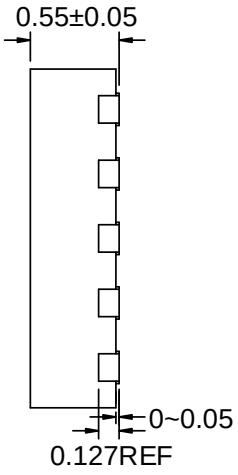
TOP VIEW



SIDE VIEW



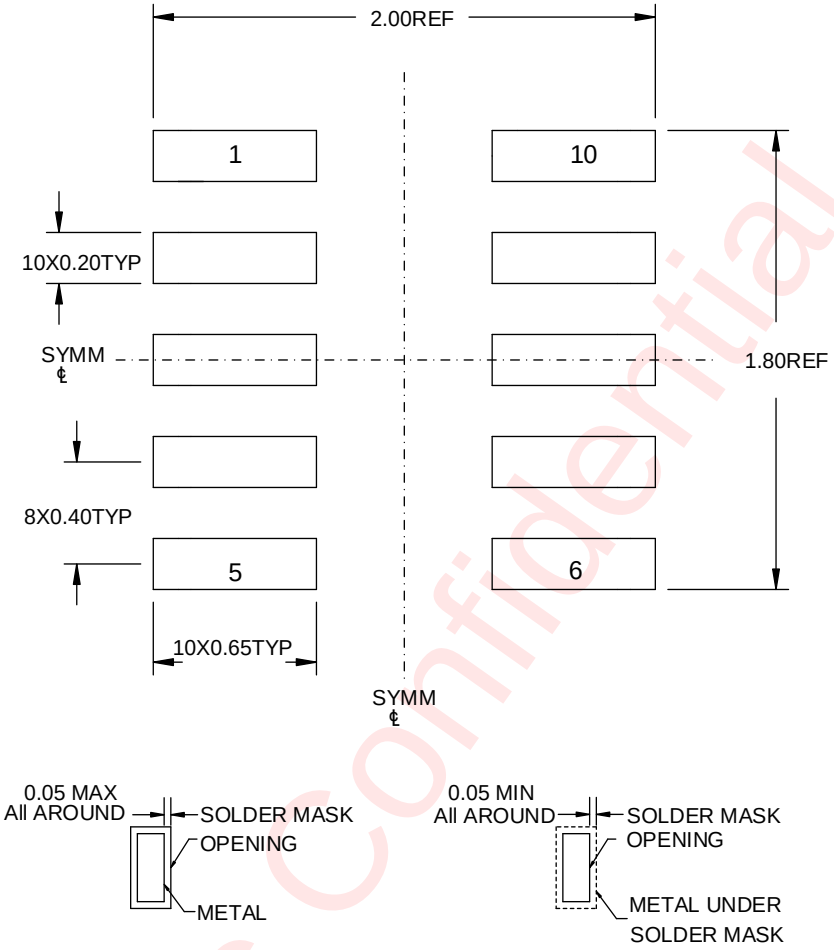
BOTTOM VIEW



SIDE VIEW

Unit: mm

Land Pattern Data



Unit：mm

Revision History

Version	Date	Change Record
V1.0	Jun. 2021	Officially released
V1.1	May. 2023	Changed the VCC, Input /Output voltage absolute maximum ratings from 3.6V to 3.9V (P4). Changed the VIO min from 1.2V to 1.1V (P4). Modified the equivalent capacitance of TVS from less than 1pF to not more than 0.5pF (P17). Changed the values of the resistors R4~R8 from 390Ω to 1kΩ (P18). Updated the description of PCB layout (P18).

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