

SLD90N10G

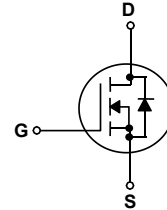
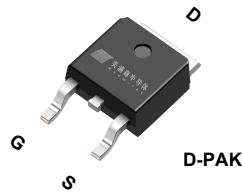
100V N -Channel MOSFET

General Description

This Power MOSFET is produced using Msemitek's advanced Shielding Gate MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters and high efficiency switching for power management in portable and battery operated products.

Features

- N-Channel: 100V 90A
 - $R_{DS(on)Typ} = 6.2m\Omega @ V_{GS} = 10V$
 - $R_{DS(on)Typ} = 8.6m\Omega @ V_{GS} = 4.5V$
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLD90N10G	Units
V_{DSS}	Drain-Source Voltage	100	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	90	A
		56	A
I_{DM}	Drain Current - Pulsed (Note 1)	270	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	80	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	250	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD90N10G	SLD90N10G	D-Pak	Tape & Reel	2500	25000

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.5	2.0	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	--	6.2	7.7	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	--	8.6	10	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 500\text{ KHz}$	--	2600	-	pF
C_{oss}	Output Capacitance		--	641	-	pF
C_{riss}	Reverse Transfer Capacitance		--	22	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V},$ $R_G = 1\text{ }\Omega, I_D = 45\text{ A}, T_J = 25^\circ\text{C}$ (Note 3)	--	20	--	ns
t_r	Turn-On Rise Time		--	16	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	32	--	ns
t_f	Turn-Off Fall Time		--	8	--	ns
Q_g	Total Gate Charge	$V_{DS} = 50\text{ V}, I_D = 45\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 3)	--	44.4	--	nC
Q_{gs}	Gate-Source Charge		--	9.1	--	nC
Q_{gd}	Gate-Drain Charge		--	9.4	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	90	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	270	A
V_{SD}	Drain to Source Diode Forward Voltage, $V_{GS} = 0\text{ V}, I_{SD} = 45\text{ A}, T_J = 25^\circ\text{C}$	--	--	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^\circ\text{C}, V_{DD} = 20\text{ V}, V_G = 10\text{ V}, L = 0.5\text{ mH}$.
3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 0.5\%$

N- Channel Typical Characteristics

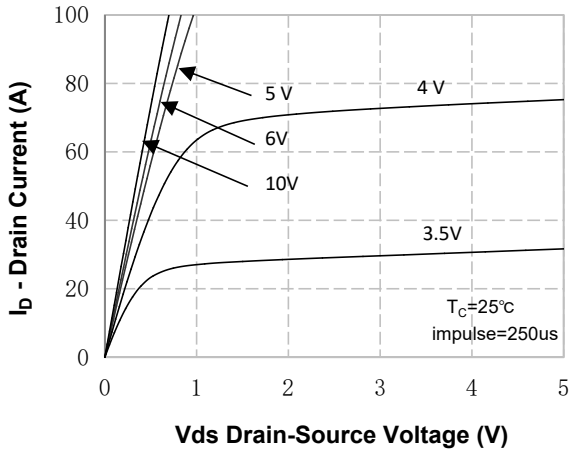


Figure 1. On-Region Characteristics

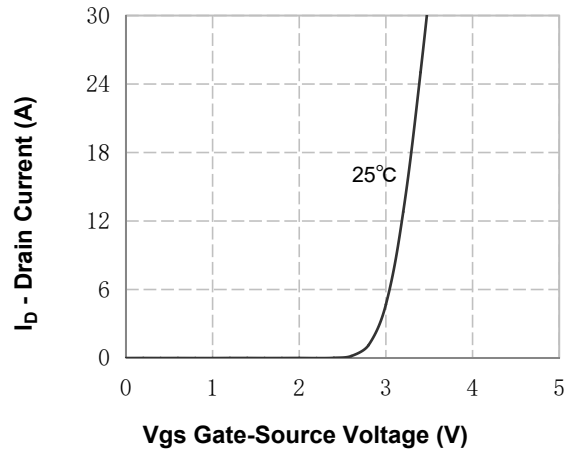


Figure 2. Transfer Characteristics

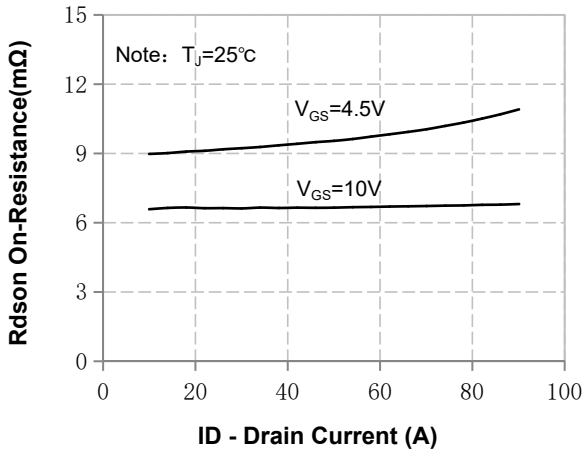


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

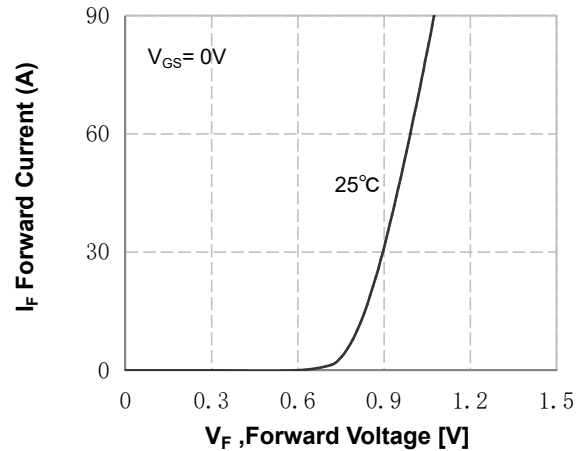


Figure 4. Body Diode Forward Voltage Variation vs Source Current

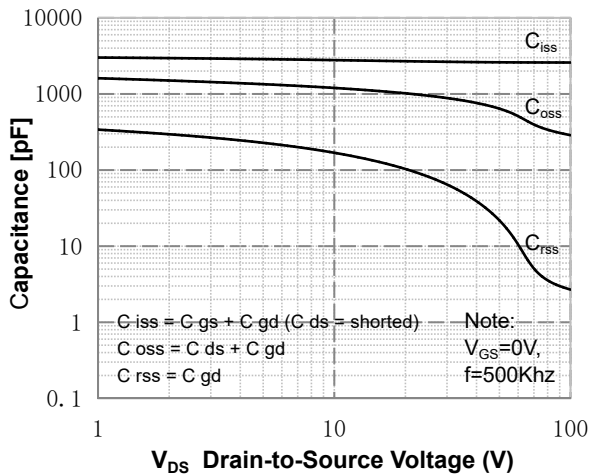


Figure 5. Capacitance Characteristics

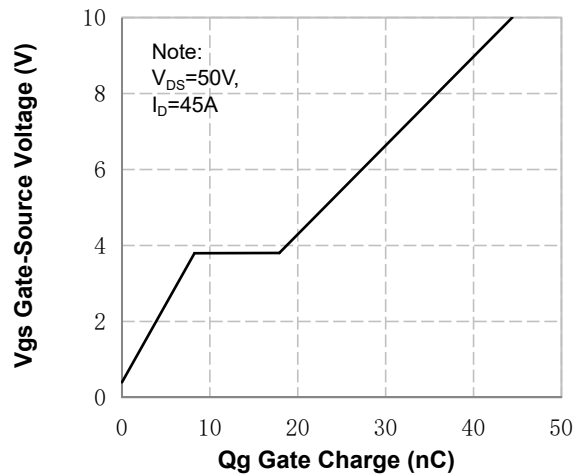


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

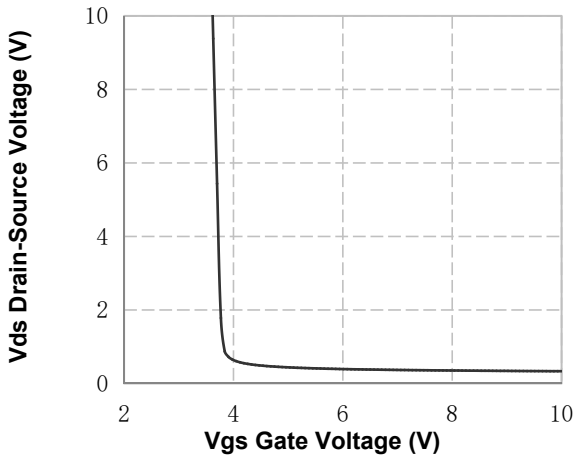


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

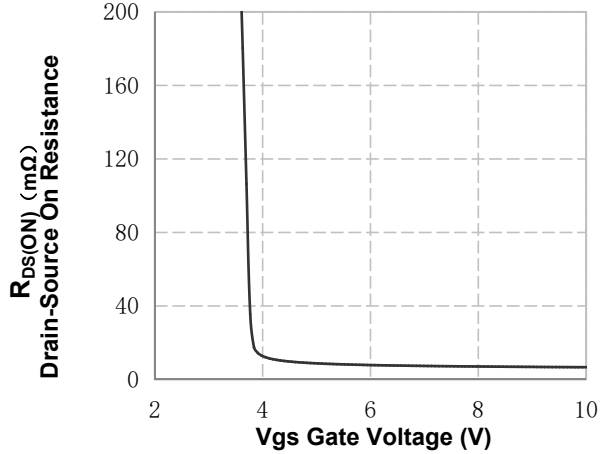


Figure 8. On-Resistance vs Gate Voltage

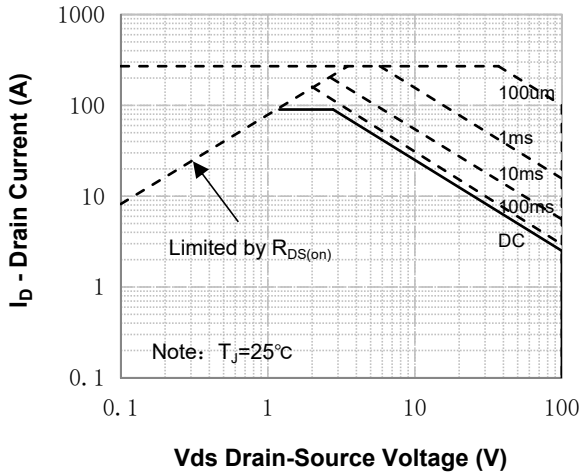


Figure 9. Maximum Safe Operating Area

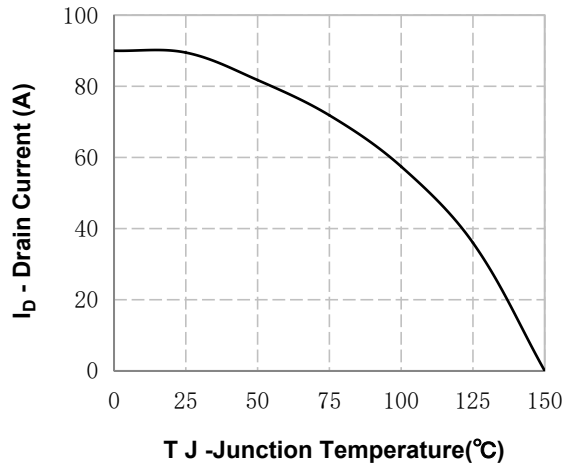


Figure 10. Maximum Continuous Drain Current vs Temperature

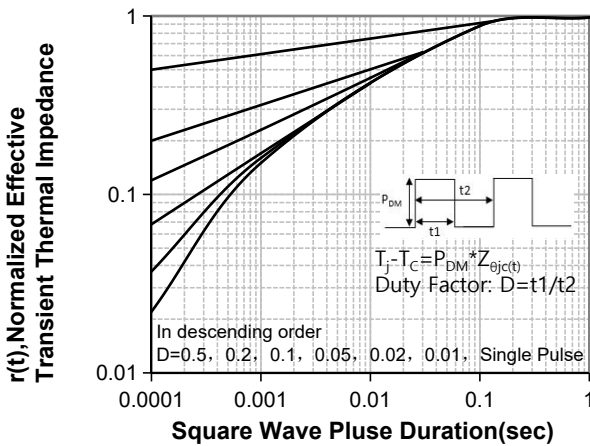


Figure 11. Transient Thermal Response Curve

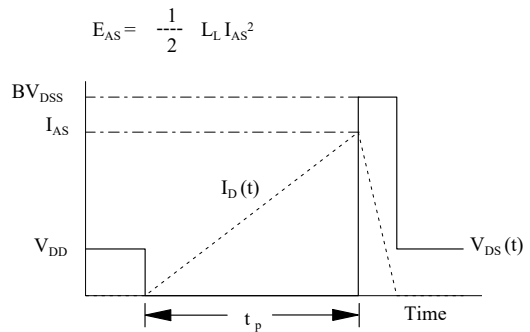
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



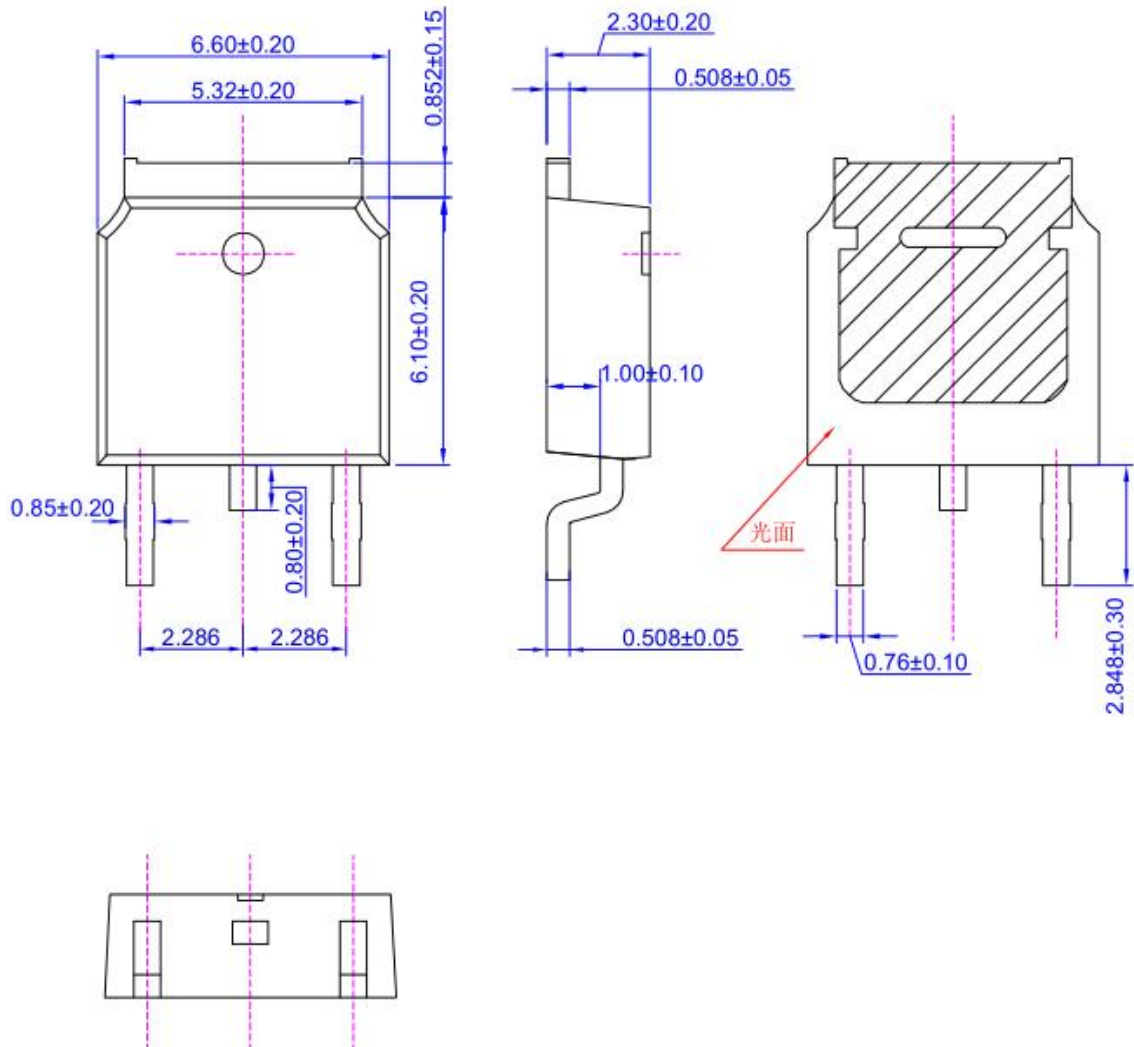
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO-252 OUTLINE



NOTE:

- 1The plastic package is not marked as smooth surface $Ra=0.1$; Subglossy surface $Ra=0.8$
- 2.Undeclared tolerance ± 0.25 , Unmarked fillet $R_{max}=0.25$

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