Power Stage

650 V GaN HEMT Power Stage

BM3G007MUV-LB

General Description

This is the product guarantees long time support in industrial market.
BM3G007MUV-LB provides an optimum solution for all electronics systems that requires high power density and efficiency.
By integrating the 650 V enhancement GaN HEMT and silicon driver to ROHM's original package, parasitic inductance caused by a PCB and wire bonding is reduced significantly compared to traditional discrete solutions.
Owing to this, a high switching slew rate up to 150 V/ns can be achieved. On the other hand, adjustable gate drive strength contributes to low EMI, and various protections and other additional functions provide optimized cost, PCB size.
This IC is designed to adapt major exist controllers, so that it also can be used to replace the traditional discrete power switches, such as super junction MOSFET.

Features

- Nano Cap™ Integrated Output Selectable 5 V LDO
- Long Time Support Product for Industrial Applications
- Wide Operating Range for VDD Pin Voltage
- Wide Operating Range for IN Pin Voltage
- Low VDD Quiescent and Operating Current
- Low Propagation Delay
- High dv/dt Immunity
- Adjustable Gate Drive Strength
- Power Good Signal Output
- VDD UVLO Protection
- Thermal Shutdown Protection

Key Specifications

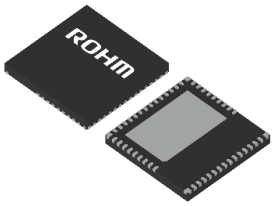
- Power Supply Voltage Range
  - VDD pin: 6.25 V to 30 V
  - D pin: 650 V (Max)
  - IN pin: -0.6 V to +30 V
- VDD Operating Current @ 130 kHz: 650 µA (Typ)
- VDD Quiescent Current: 180 µA (Typ)
- Allowable Input Switching Frequency: 2 MHz (Max)
- Turn-on Delay Time: 12 ns (Typ)
- Turn-off Delay Time: 15 ns (Typ)
- Operating Temperature Range: -40 °C to +105 °C
- GaN HEMT D-S ON State Resistance: 70 mΩ (Typ)

Package

VQFN046V8080

W (Typ) x D (Typ) x H (Max)

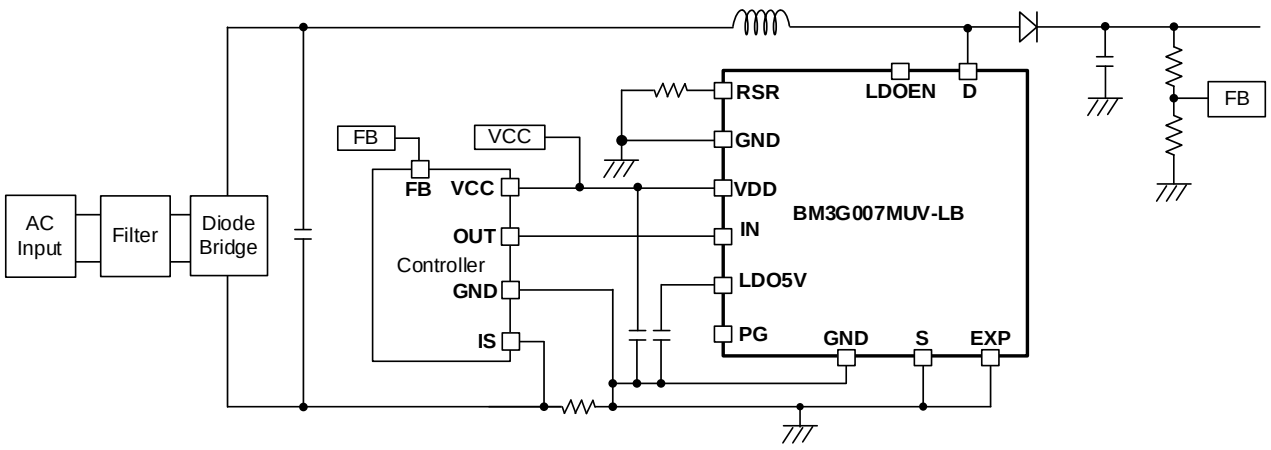
8.0 mm x 8.0 mm x 1.0 mm
pitch 0.5 mm



Applications

- Industrial Equipment, Power Supplies with High Power Density, High Efficiency Demand, or Bridge Topology such as Totem-pole PFC, LLC Power Supply, Adaptor, etc.

Typical Application Circuit



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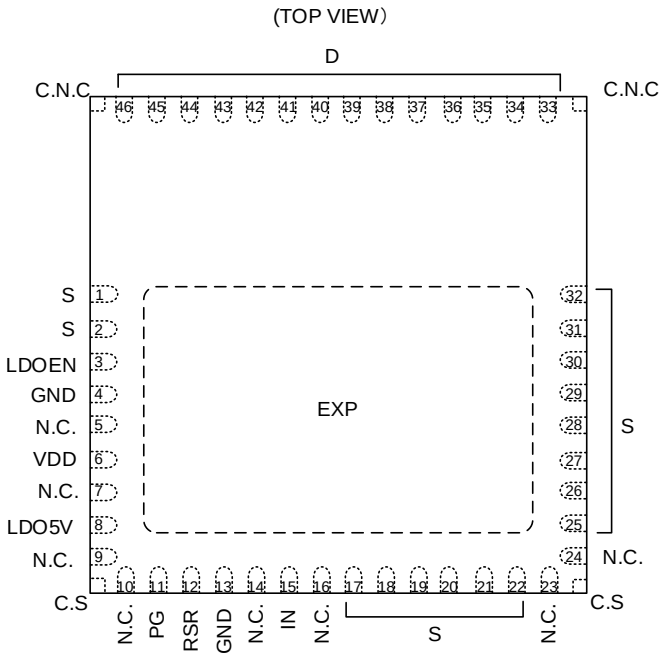
Pin Configuration

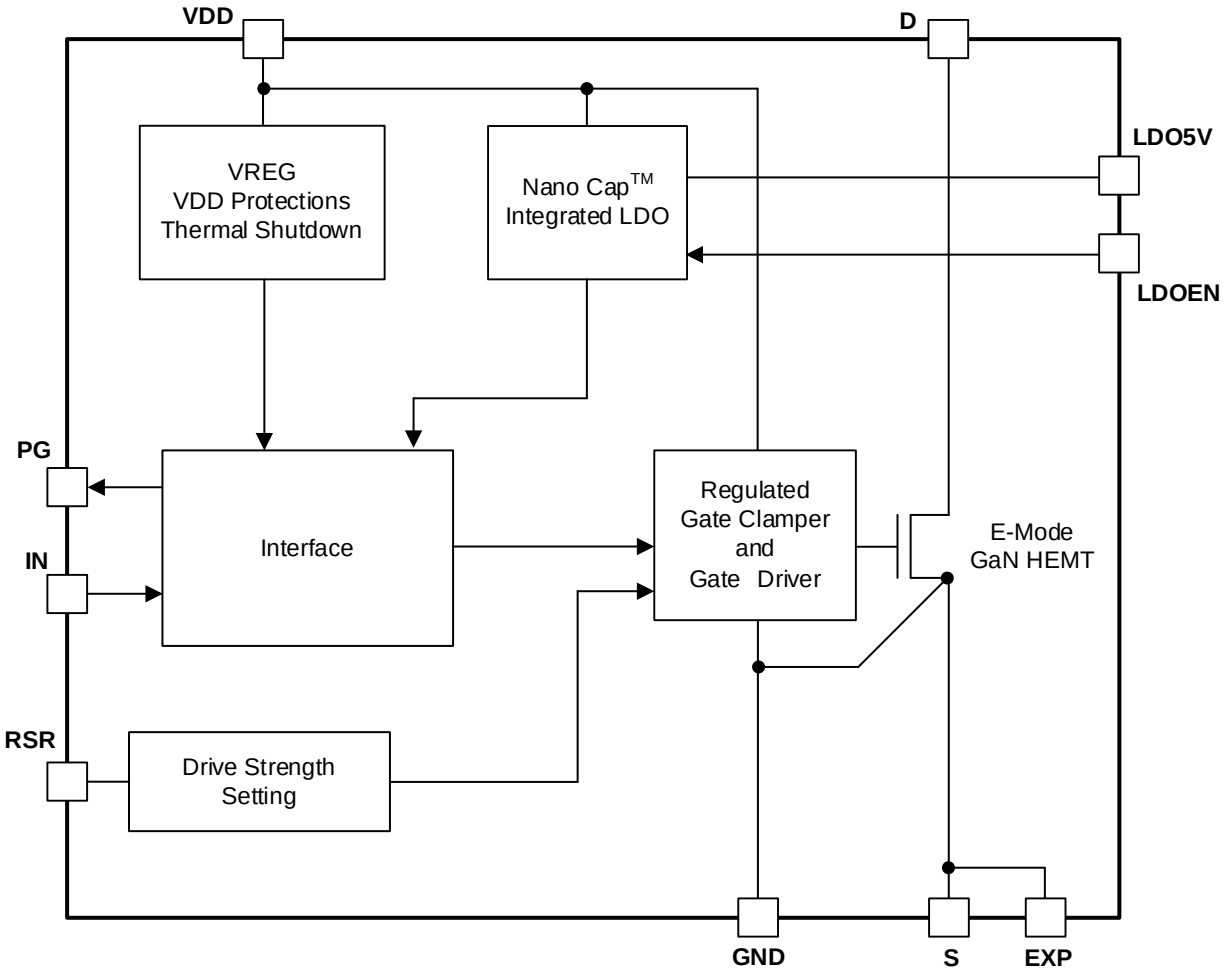


Pin Descriptions

Pin Number	Pin Name	I/O	Function
1, 2, 17-22, 25-32	S	O	GaN HEMT SOURCE pin
3	LDOEN	I	LDO function enable/disable pin
4, 13	GND	O	GND pin*(Note 1)*
5, 7, 9, 10, 14, 16, 23, 24	N.C.	-	Non-connection*(Note 2)*
6	VDD	I	Power supply input pin
8	LDO5V	O	5 V LDO output pin
11	PG	O	Power good signal output pin
12	RSR	I	Gate drive strength adjustment pin
15	IN	I	Non-inverting gate drive input
33-46	D	I	GaN HEMT DRAIN pin
-	EXP	O	GaN HEMT SOURCE pin*(Note 1)*
-	C.S	-	Corner pin*(Note 3)*
-	C.N.C	-	Corner pin, non-connection*(Note 2)*

(Note 1) It is connected to the S pin internally, but also connect to the S pin on the PCB.
(Note 2) Do not connect to other pins.
(Note 3) It is connected to the S pin internally, but do not connect to other pins on the PCB.

Block Diagram



Description of Blocks

1 Overview

The IC, which integrates GaN device, gate driver and other additional functions such as protections, offers an optimum solution for making high power density design much easier and more efficient.
Due to a zero reverse recovery and extremely low output capacitance of GaN device, the IC achieves excellent efficiency especially in bridge-based topologies. It is also possible to replace existing Si MOSFETs and heatsinks to improve the efficiency and PCB size.
The integrated gate driver with wide operating the VDD pin and IN pin input voltage range brings a remarkable switching performance such as a high drain slew rate and low propagation delay, and it also makes the GaN device even much easier to use than traditional Si MOFET discrete.
Furthermore, various protections such as VDD UVLO, LDO output UVP, thermal shutdown (TSD) are also integrated to protect this IC from damages. A power good signal is outputted from the PG pin, and it switches to a low level if any abnormal state is detected.

2 Feature Descriptions

2.1 E-Mode GaN HEMT

This IC integrates an enhancement-mode (normally-off) GaN device.
The enhancement-mode GaN device has smaller parasitic inductance and less switching loss than the cascode topology which connects a depletion-mode (normally-on) GaN device and a Si MOSFET in series because the cascode topology has additional parasitic inductance between a depletion-mode GaN device and Si MOSFET.
These characteristics offer advanced switching performance physically, and that is significant especially in large current applications.

2.2 Regulated Gate Clamper and Gate Driver

This IC integrates an original gate driver for the enhancement-mode GaN device, and the driver keeps off until VDD UVLO and TSD are judged as normal.
The internal regulated gate clamper allows a wide operating range of the VDD pin voltage.

2.3 Nano Cap™ Integrated LDO

Nano Cap™ is a combination of technologies which allow stage operation even if output capacitance is connected with the range of nF unit.
This IC integrates a selectable LDO regulator with 5 V output voltage.
It is designed to be used as a power supply for other components such as a digital isolator for the high side IN pin's input signal in bridge applications. It is recommended to use an output capacitor C_{LDO5V} of at least 0.1 µF or more between the LDO5V pin and the GND pin if this function is used.
Use ceramic capacitor which has low ESR as the output capacitor C_{LDO5V}.
LDO regulator is valid when LDOEN pin state is open. It can be also disabled by shorting the LDOEN pin to the GND pin if it is not necessary.

2.4 Interface

It is possible to use the output of most of general MCUs or ACDC controllers as the IN pin's input signal directly, due to the original IN input interface circuit.
The PG pin is an open drain output for a power good signal of this IC.
If all protections are judged as normal, and the IN pin state for input signal is valid (after t_{D_IN} from VDD UVLO release), the PG pin voltage keeps a high impedance state.
If one or more protections are detected, the PG pin is pulled down to low level by internal resistor R_{PG_PD}. It can be outputted to the digital isolator or the controller IC to report the abnormal state of this IC.
The protections and abnormal states, and corresponding PG pin state are shown in Table 1.
However, VDD pin voltage is V_{OFF} or less, the PG pin is forcibly high impedance state.

Table 1. Protections Introducing the PG Pin Low Level

Protections and Abnormal States ("1" = Detected, "0" = Non-detected, "X" = Don't care)			PG Pin State ("L" = Pulled down to GND, "Hi-Z" = High Impedance)	
VDD UVLO	LDO5V UVP	TSD	LDOEN Pin = OPEN	LDOEN Pin = GND
1	X	X	Hi-Z	Hi-Z
0	0	0	Hi-Z	Hi-Z
0	0	1	L	L
0	1	0	L	Hi-Z
0	1	1	L	L

2 Feature Descriptions – continued

2.5 Drive Strength Setting

Generally, there is a tradeoff between efficiency and EMI. A higher switching slew rate reduces the switching loss, in the other hand, it also increases the switching noise.
By adjusting a resistor R_{SR} between the RSR pin and the GND pin, the turn-on slew rate SR_{ON} can be selected freely from 20 V/ns to 80 V/ns.
The larger the value of R_{SR}, the higher the value of SR_{ON}.
When the value of R_{SR} is 100 kΩ or more, the value of SR_{ON} is clamped to a constant value.
It allows users to optimize the switching speed according to specific circumstance, such as an EMI filter space, PCB layout, etc.
Refer to Figure 28 for the relationship between R_{SR} and SR_{ON}.

2.6 VREG, VDD Protections, Thermal Shutdown

This IC has internal regulators, some protection circuits.

Description of Blocks – continued

3 Start Sequence

Start sequence is shown in Figure 1, Figure 2 and see the sections below for detailed descriptions.

3.1 Start Sequence (LDOEN pin = OPEN)

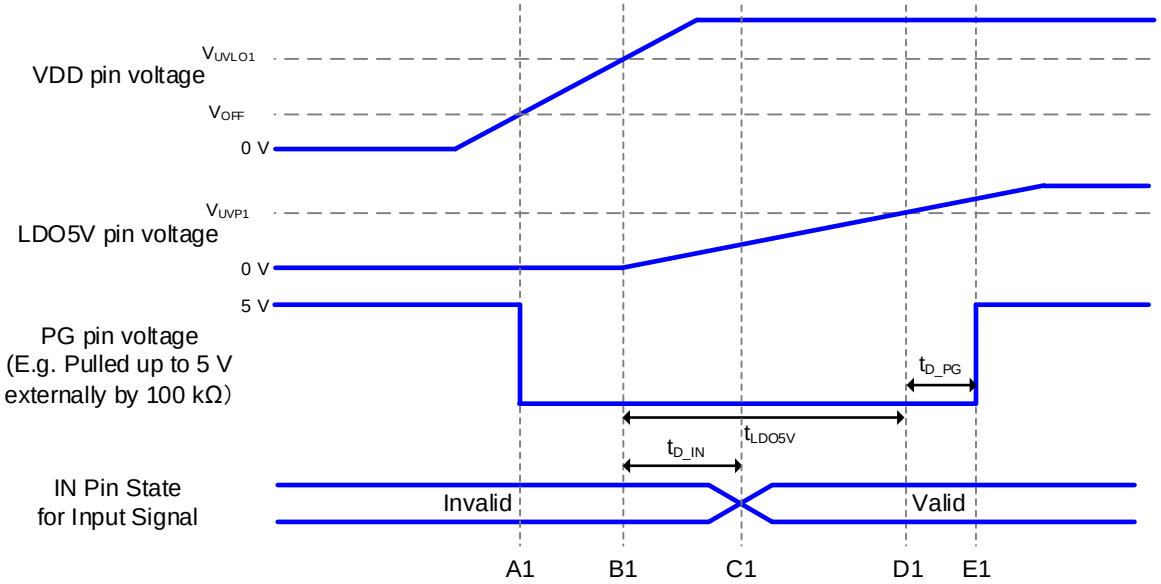


Figure 1. Start Sequences Timing Chart (LDOEN pin = OPEN)

A1: When the VDD pin voltage exceeds V_{OFF}, the IC becomes to operational state, and the PG pin state becomes pulled down internally.
B1: When the VDD pin voltage exceeds V_{UVLO1}, the IC starts to operate, and the LDO5V pin voltage starts to rise.
C1: The IC is ready for an input signal from the IN pin after t_{D_IN} from B1. It becomes possible to drive the integrated GaN HEMT.
D1: When the LDO5V pin voltage exceeds V_{UVP1}, the conditions for outputting power good signal are satisfied. The time from B1 to D1 is defined as t_{LDO5V}.
E1: The PG pin state changes from internally pulled down to a high impedance after t_{D_PG} from D1.

3.2 Start Sequence (LDOEN pin = GND)

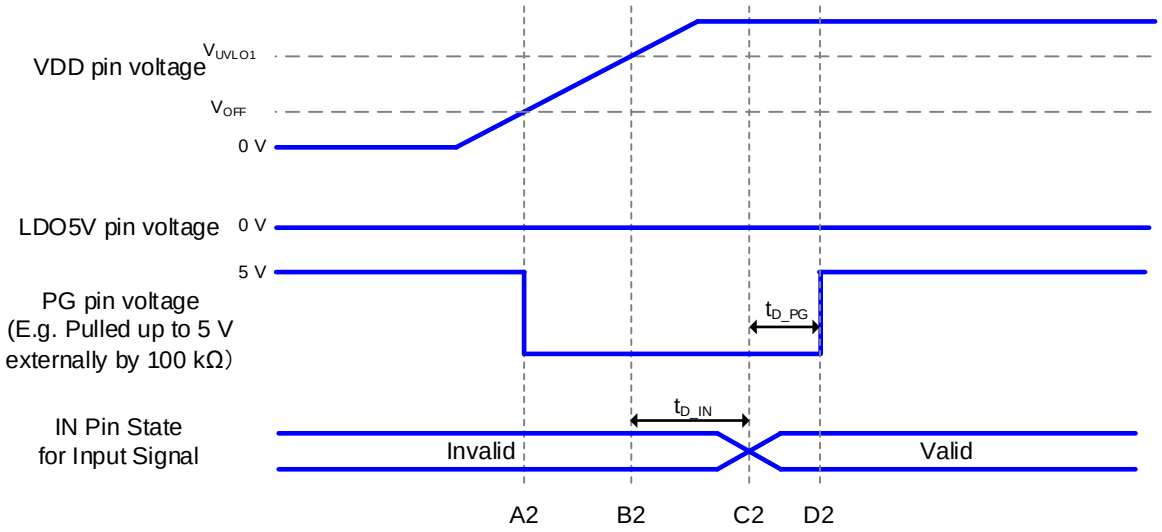


Figure 2. Start Sequences Timing Chart (LDOEN pin = GND)

A2: Same as A1.
B2: When the VDD pin voltage exceeds V_{UVLO1}, the IC starts to operate.
C2: Same as C1.
D2: The PG pin state changes from internally pulled down to a high impedance after t_{D_PG} from C2.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{MAX1A}	-0.3 to +650	V	D pin voltage, DC
	V_{MAX1B}	-0.3 to +730	V	D pin voltage, tpulse < 1 μs *(Note 1)*
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +35	V	VDD pin voltage
Maximum Applied Voltage 3	V_{MAX3}	-0.6 to +35	V	IN pin voltage
Maximum Applied Voltage 4	V_{MAX4}	-0.3 to +6.0	V	LDOEN, LDO5V, RSR, PG pin voltage
Maximum Inflow Current	I_{MAX}	5.0	mA	PG pin Inflow current
DRAIN Pin Current	$I_{D(RMS)}$	20.9	A	RMS, Tc = 25 °C
	$I_{D(PULSE)}$	66.1	A	tpulse < 1 μs *(Note 1)*, Tc = 25 °C
DRAIN dv/dt	dv/dt	150	V/ns	V_D = 0 V to 400 V
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Duty is less than 1 %.

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 4)*	2s2p *(Note 5)*	
VQFN046V8080				
Junction to Ambient	θ_{JA}	90.5	25.8	°C/W
Junction to Top Characterization Parameter *(Note 3)*	Ψ_{JT}	13	6	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain Voltage Range	V_{DRAIN}	-	-	650	V	D pin voltage, DC
Power Supply Voltage Range	V_{DD}	6.25	15	30	V	VDD pin voltage
Input Voltage Range 1	V_{IN_H}	2.5	5	30	V	IN pin high voltage
Input Voltage Range 2	V_{IN_L}	-0.6	0	+0.3	V	IN pin low voltage
LDO5V Load Current Range	I_{LDO5V}	-	-	10	mA	V_{DD} = 15 V
LDO5V Pin Output Capacitance Range	C_{LDO5V}	0.1	-	100	µF	LDOEN = OPEN
RSR Pin Pull-down Resistance Range	R_{SR}	0	-	OPEN	Ω	
Operating Temperature	Topr	-40	-	+105	°C	Surrounding temperature

Electrical Characteristics (Unless noted otherwise, V_{DD} = 15 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
GaN HEMT						
D-S Withstand Voltage	$V_{(BR)DDS1}$	650	-	-	V	V_{IN} = 0 V
	$V_{(BR)DDS2}$	730	-	-	V	V_{IN} = 0 V, tpulse < 1 µs *(Note 1)*
D Pin Leak Current	I_{DSS1}	-	-	100	µA	V_{DS} = 650 V, V_{IN} = 0 V, Ta = 25 °C
	I_{DSS2}	-	10	-	µA	V_{DS} = 650 V, V_{IN} = 0 V, Ta = 150 °C
D-S ON State Resistance	R_{ON1}	-	70	100	mΩ	I_D = 0.5 A, V_{IN} = 5 V, Ta = 25 °C
	R_{ON2}	-	175	-	mΩ	I_D = 0.5 A, V_{IN} = 5 V, Ta = 150 °C
S-D Reverse Voltage	V_{SD}	-	2.4	-	V	I_D = -8.0 A, V_{IN} = 0 V
Output Capacitance	C_{OSS}	-	49.9	-	pF	V_{IN} = 0 V, V_D = 400 V, f = 1 MHz
Energy Related Effective Output Capacitance	$C_{O(ER)}$	-	74.5	-	pF	V_{IN} = 0 V, V_D = 0 V to 400 V
Time Related Effective Output Capacitance	$C_{O(TR)}$	-	116.6	-	pF	V_{IN} = 0 V, V_D = 0 V to 400 V
Reverse Recovery Charge	Q_{RR}	-	0	-	nC	
Circuit Current						
VDD Operating Current	I_{ON1}	-	650	1000	µA	D pin = open, R_{SR} = 0 Ω operating at 130 kHz, duty = 50 %
VDD Quiescent Current	I_{ON2}	-	180	240	µA	V_{IN} = 0 V, R_{SR} = 0 Ω
VDD Standby Current	I_{STB}	-	80	160	µA	V_{DD} = 5 V
VDD Pin						
VDD Operating Limit Voltage	V_{OFF}	-	-	3	V	
VDD UVLO Release Voltage	V_{UVLO1}	5.65	5.95	6.25	V	VDD pin voltage rising
VDD UVLO Detection Voltage	V_{UVLO2}	5.15	5.30	5.45	V	VDD pin voltage dropping
VDD UVLO Hysteresis	V_{UVLO3}	-	0.65	-	V	V_{UVLO3} = V_{UVLO1} - V_{UVLO2}
VDD UVLO Timer	t_{UVLO}	50	100	200	µs	

(Note 1) Duty is less than 1 %.

Electrical Characteristics – continued (Unless noted otherwise, V_{DD} = 15 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Thermal Shutdown						
TSD Temperature 1	T_{SD1}	150	175	200	°C	Temperature rising *(Note 1)*
TSD Temperature 2	T_{SD2}	-	100	-	°C	Temperature dropping *(Note 1)*
TSD Hysteresis	T_{SD3}	-	75	-	°C	$T_{SD3} = T_{SD1} - T_{SD2}$ *(Note 1)*
TSD Timer	t_{TSD}	50	100	150	µs	
LDOEN Pin						
LDOEN Internal Pull-up Resistor	R_{LDOEN_PU}	350	500	650	kΩ	
LDOEN External Pull-down Resistor Setting Range	R_{LDOEN_PD}	-	0	10	kΩ	In case of disabling LDO function
LDO5V Pin						
LDO5V Output Voltage	V_{LDO5V}	4.90	5.00	5.10	V	
LDO5V Maximum Output Current	I_{LDO5V}	10	-	-	mA	
LDO5V UVP Release Voltage	V_{UVP1}	-	85	-	%	Percentage of V_{LDO5V}
LDO5V UVP Detection Voltage	V_{UVP2}	-	80	-	%	Percentage of V_{LDO5V}
LDO5V UVP Hysteresis	V_{UVP3}	-	5	-	%	Percentage of V_{LDO5V}
LDO5V Internal Pull-down Resistor	R_{LDO5V_PD}	0.5	1.0	1.5	kΩ	Short LDOEN to GND
PG Pin						
PG Internal Pull-down Resistor	R_{PG_PD}	-	110	200	Ω	
IN Pin						
Positive-going Input Threshold	V_{IN_POS}	1.60	1.80	2.00	V	
Negative-going Input Threshold	V_{IN_NEG}	1.05	1.30	1.55	V	
Input threshold Hysteresis	V_{IN_HYS}	-	0.50	-	V	
Input Leakage Current	I_{IN_LEAK}	-	40	-	µA	V_{IN} = 5 V
Allowable Input Switching Frequency	f_{SW}	-	-	2.0	MHz	
RSR Pin						
Turn-on Slew Rate 1	SR_{ON1}	-	20	-	V/ns	R_{SR} = 0 Ω V_{BUS} = 400 V *(Note 1) (Note 2)*
Turn-on Slew Rate 2	SR_{ON2}	-	80	-	V/ns	R_{SR} = OPEN, V_{BUS} = 400 V *(Note 1) (Note 2)*
Switching Items						
Turn-on Delay Time	$t_{D(ON)}$	-	12	-	ns	R_{SR} = OPEN, V_{BUS} = 400 V *(Note 1) (Note 2)*
Drain Fall Time	t_F	-	3	-	ns	R_{SR} = OPEN, V_{BUS} = 400 V *(Note 1) (Note 2)*
Turn-off Delay Time	$t_{D(OFF)}$	-	15	-	ns	V_{BUS} = 400 V *(Note 1) (Note 2)*
Drain Rise Time	t_R	-	5	-	ns	V_{BUS} = 400 V *(Note 1) (Note 2)*
Minimum IN Pin High Pulse-width for GaN HEMT Turn-on	t_{IN_MIN}	-	-	24	ns	

(Note 1) No shipping inspection.
(Note 2) Refer to “Switching Parameter Measurement Information”.

Electrical Characteristics – continued (Unless noted otherwise, V_{DD} = 15 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Startup Items						
Input Validation Delay Time	t_{D_IN}	-	15	30	µs	
PG Signal Delay Time	t_{D_PG}	-	10	20	µs	
LDO5V Rise Time	t_{LDO5V}	-	400	800	µs	LDOEN = OPEN, C_{LDO5V} = 0.1 µF

Switching Parameter Measurement Information

Figure 3 shows the circuit for measurements of switching parameters.
Figure 4 shows instruction of them.

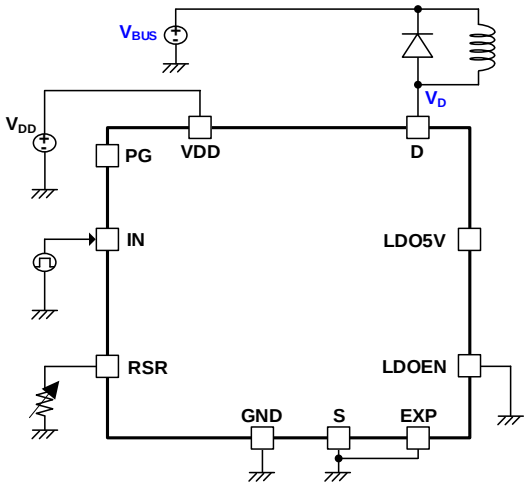


Figure 3. Switching Parameters Measurement Circuit

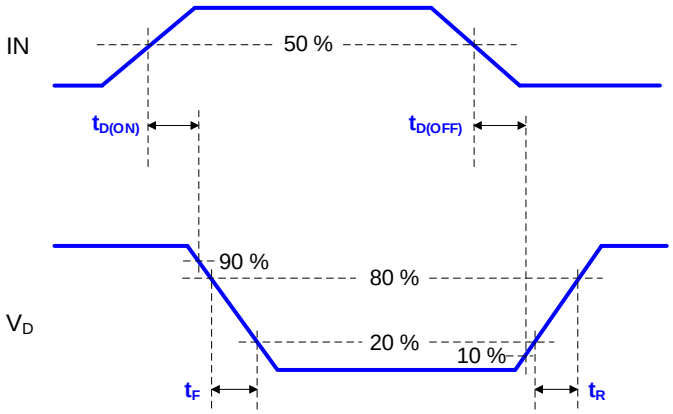


Figure 4. Instruction of Switching Parameters

1 Turn-on Delay Time: $t_{D(ON)}$
The turn-on delay time is the time from rising edge of the IN pin voltage (represented by 50 % of IN pin high voltage level) to when the GaN HEMT starts turning on (represented by V_D falling to 90 % of V_{BUS}).

2 Drain Fall Time: t_F
The drain fall time is the time it takes for V_D falls from 80 % to 20 % of V_{BUS}.

3 Turn-off Delay Time: $t_{D(OFF)}$
The turn-off delay time is the time from falling edge of the IN pin voltage (represented by 50 % of IN pin high voltage level) to when the GaN HEMT starts turning off (represented by V_D rising to 10 % of V_{BUS}).

4 Drain Rise Time: t_R
The drain rise time is the time it takes for V_D rises from 20 % to 80 % of V_{BUS}.

5 Turn-on Slew Rate: SR_{ON}
The turn-on slew rate is the slew rate which is when V_D falls from 80 % to 20 % of V_{BUS}.
It is calculated by the formula below.

$$SR_{ON} = \frac{V_{BUS} \times 60\ \%}{t_F}$$

where:
SR_{ON} is the turn-on slew rate.
V_{BUS} is the DC bus voltage.
t_F is the drain fall time.

Application Examples

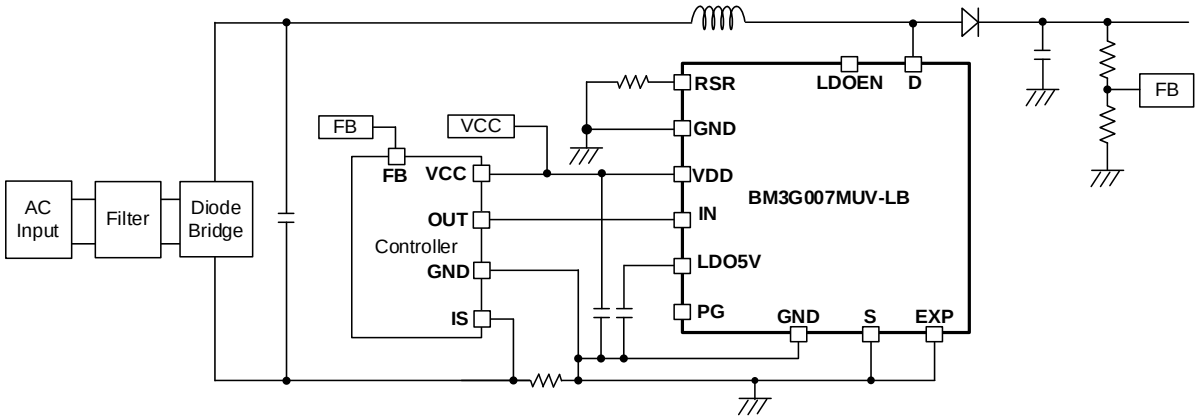


Figure 5. PFC Converter Application Example

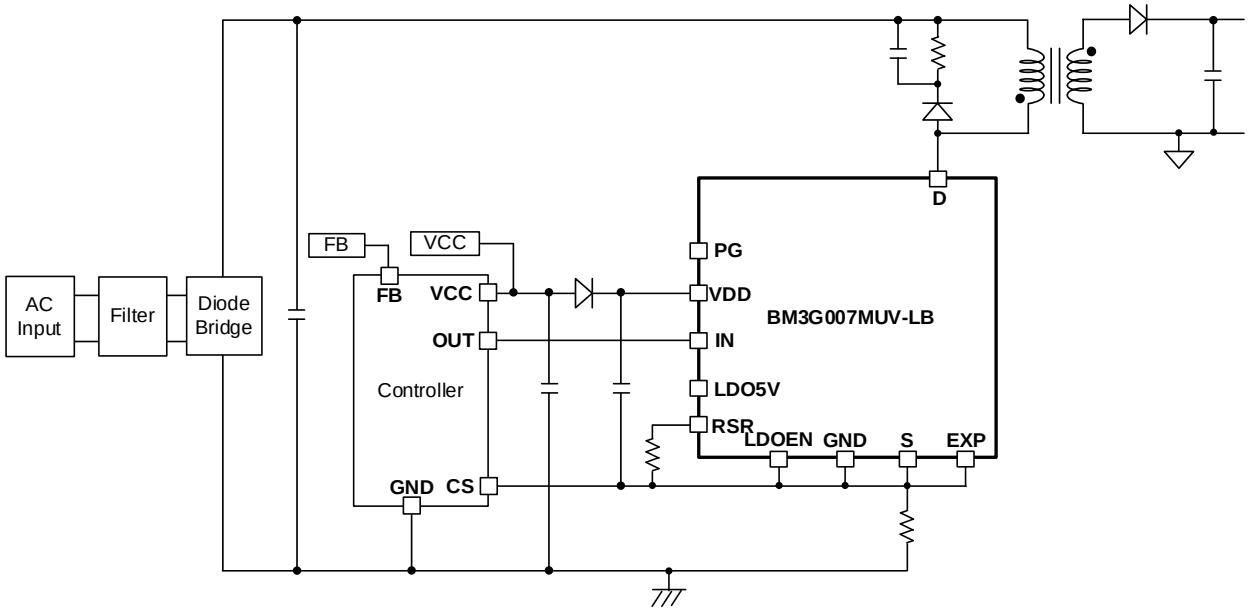


Figure 6. Flyback Converter Application Example

Application Examples - continued

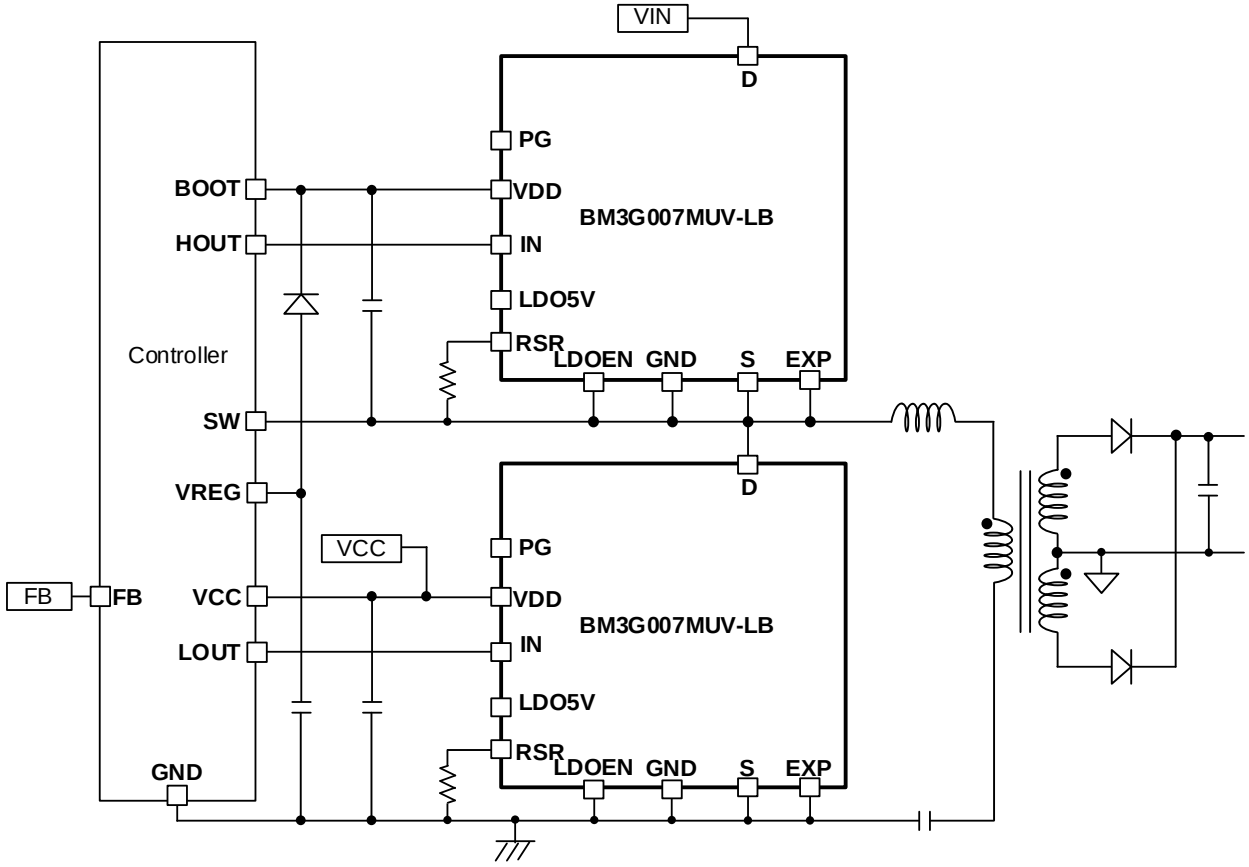


Figure 7. LLC Resonant Converter Application Example

Typical Performance Curves (Reference Data)

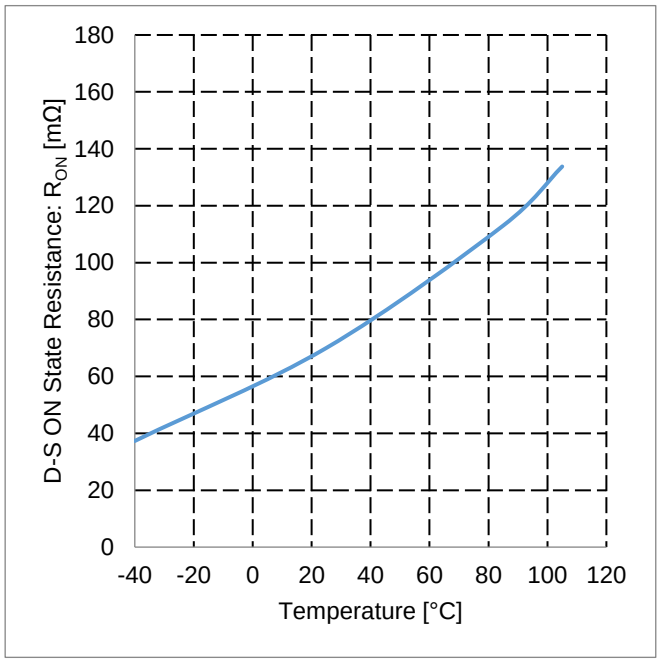


Figure 8. D-S ON State Resistance vs Temperature

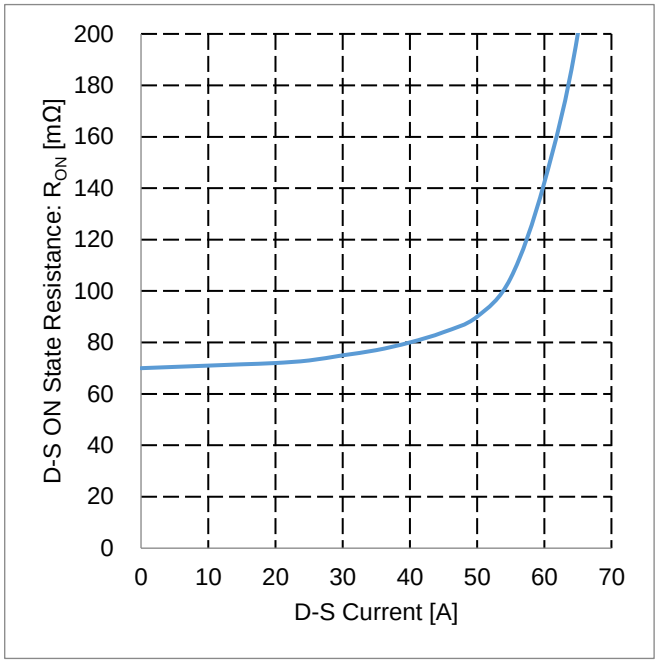


Figure 9. D-S ON State Resistance vs D-S Current

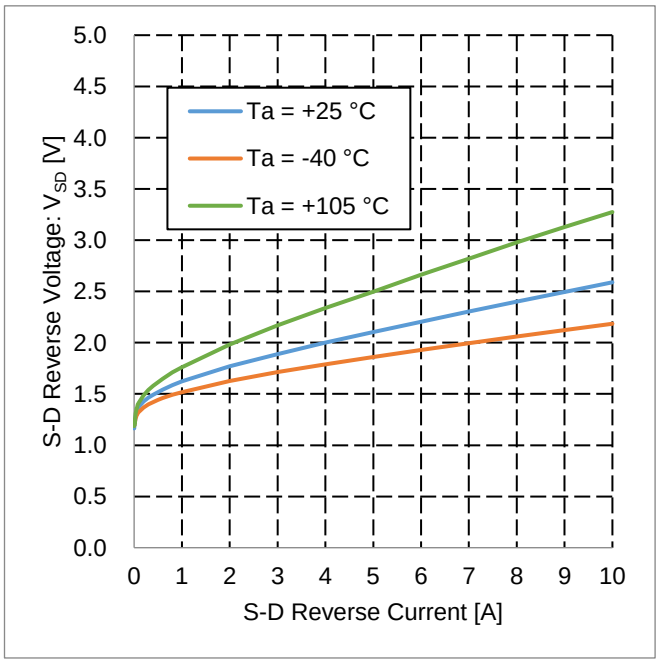


Figure 10. S-D Reverse Voltage vs S-D Reverse Current

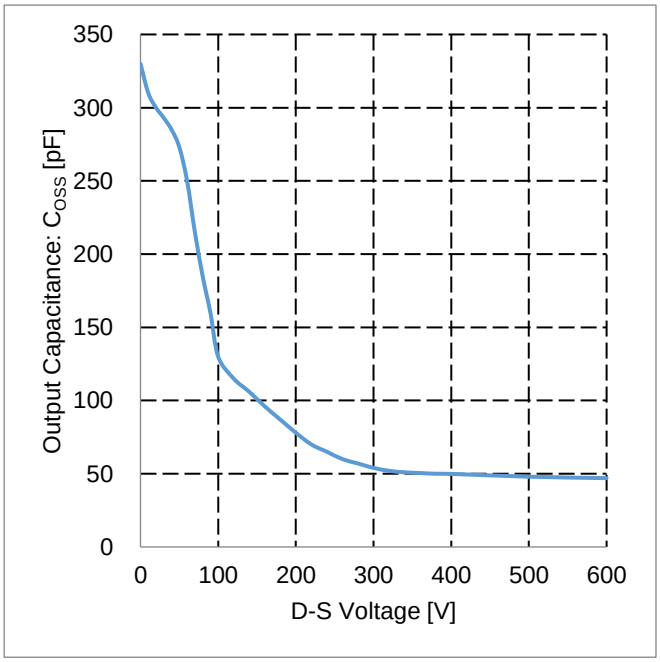


Figure 11. Output Capacitance vs D-S Voltage

Typical Performance Curves (Reference Data) - continued

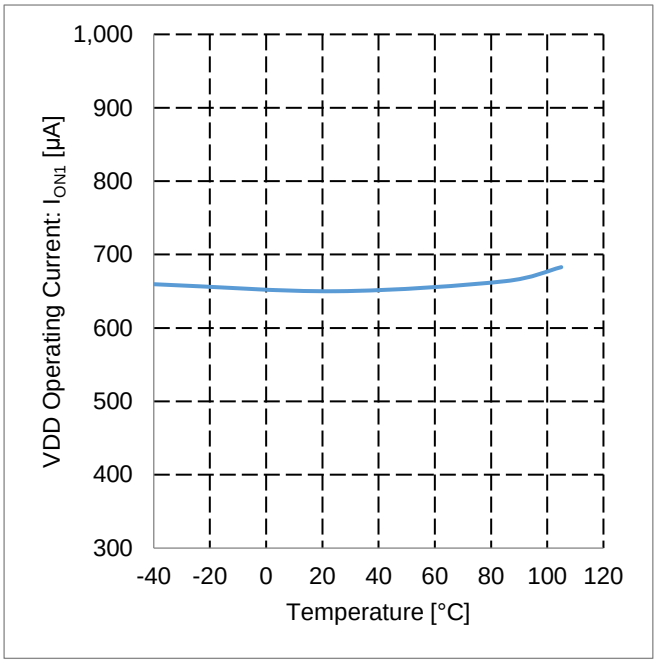


Figure 12. VDD Operating Current vs Temperature

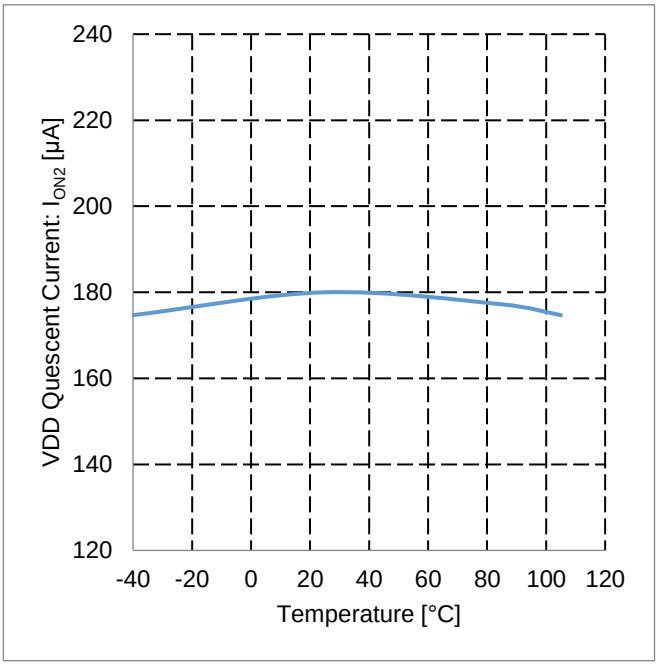


Figure 13. VDD Quiescent Current vs Temperature

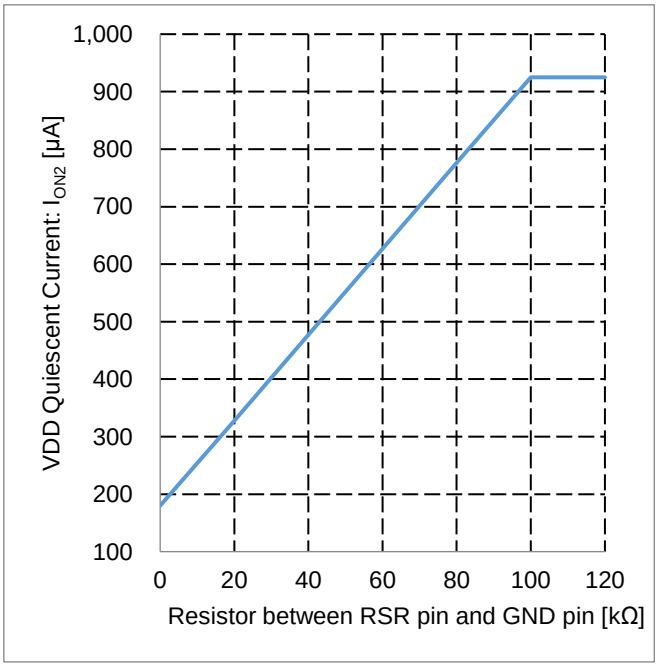


Figure 14. VDD Quiescent Current vs Resistor between RSR pin and GND pin

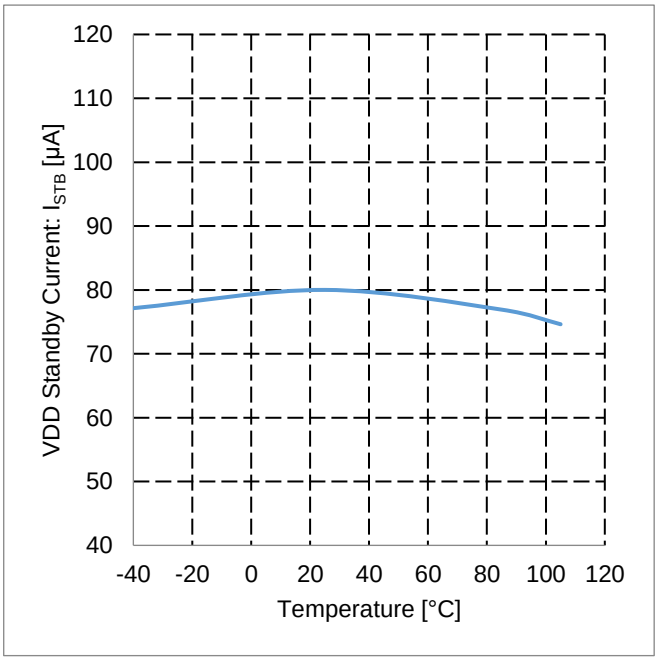


Figure 15. VDD Standby Current vs Temperature

Typical Performance Curves (Reference Data) - continued

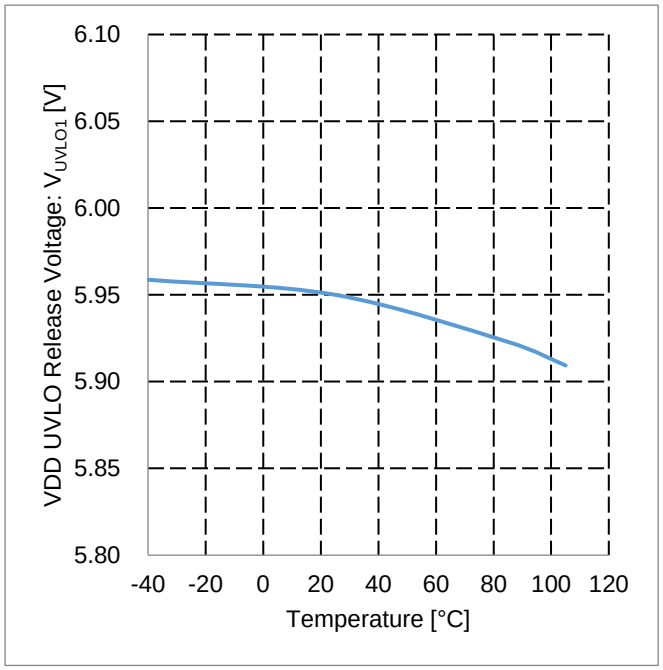


Figure 16. VDD UVLO Release Voltage vs Temperature

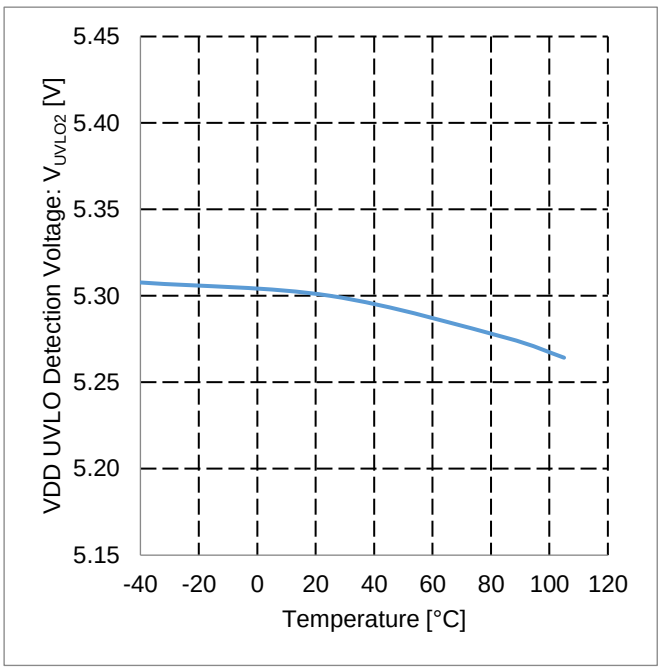


Figure 17. VDD UVLO Detection Voltage vs Temperature

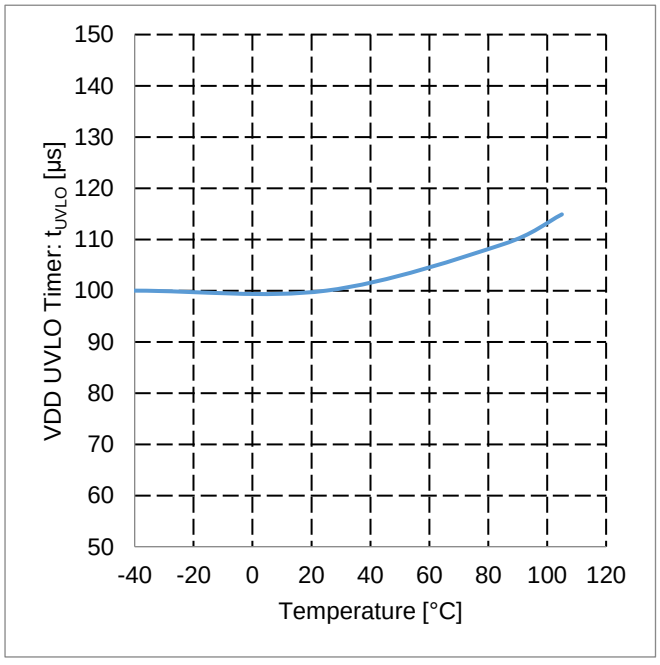


Figure 18. VDD UVLO Timer vs Temperature

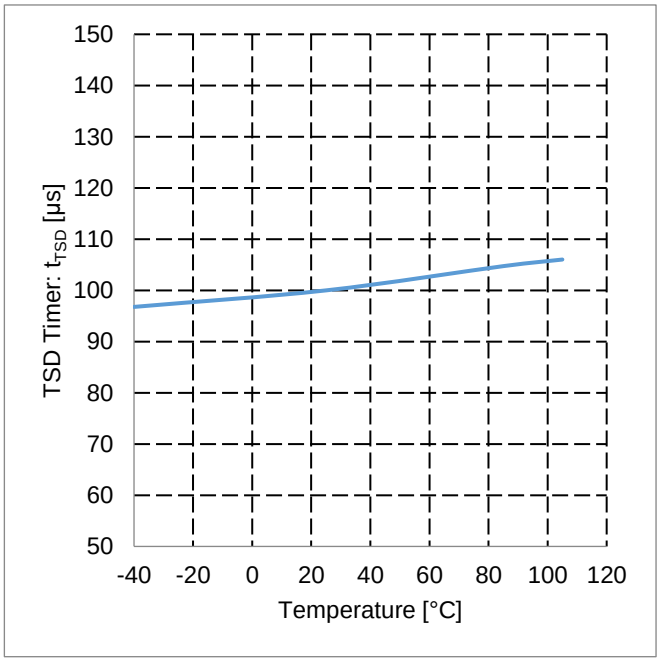


Figure 19. TSD Timer vs Temperature

Typical Performance Curves (Reference Data) - continued

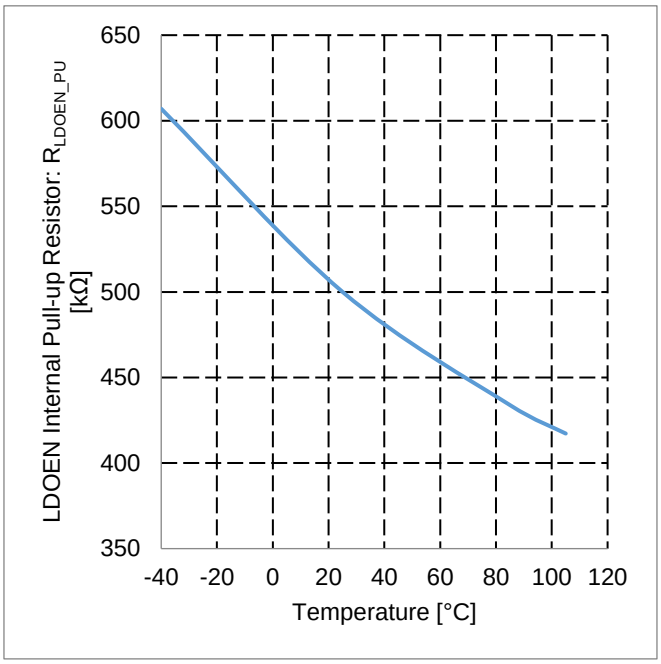


Figure 20. LDOEN Internal Pull-up Resistor vs Temperature

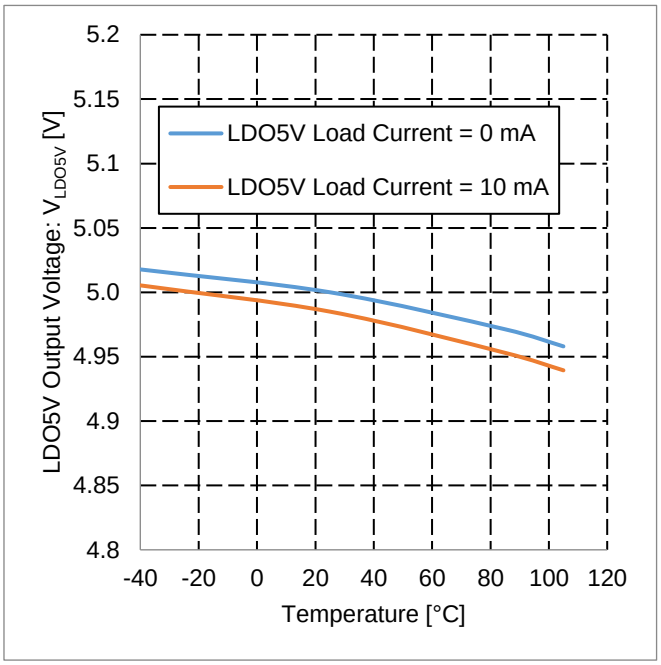


Figure 21. LDO5V Output Voltage vs Temperature

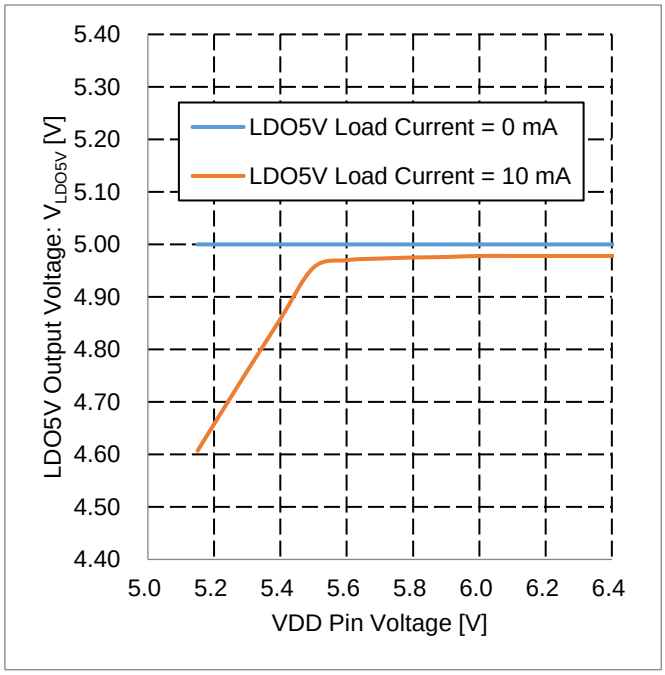


Figure 22. LDO5V Output Voltage vs VDD Pin Voltage

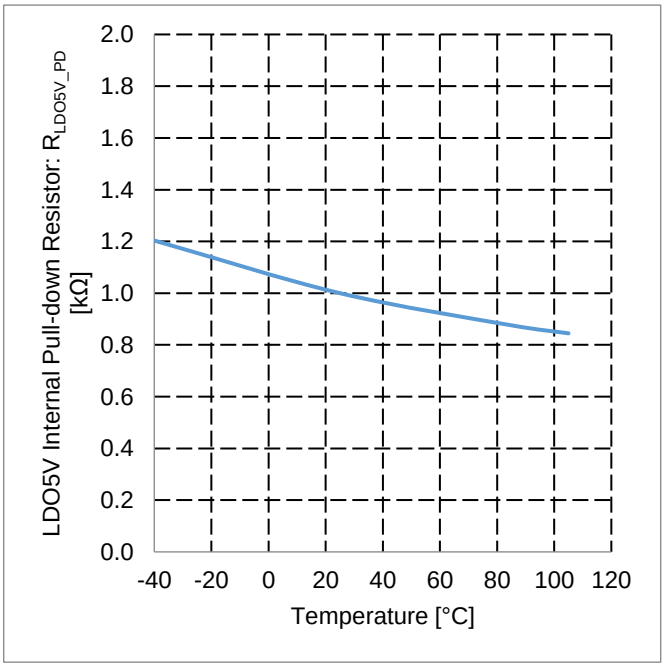


Figure 23. LDO5V Internal Pull-down Resistor vs Temperature

Typical Performance Curves (Reference Data) - continued

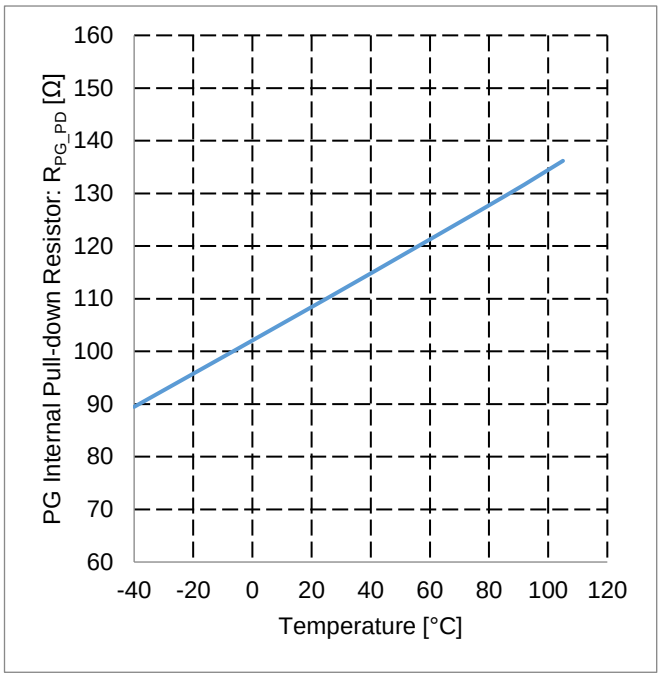


Figure 24. PG Internal Pull-down Resistor vs Temperature

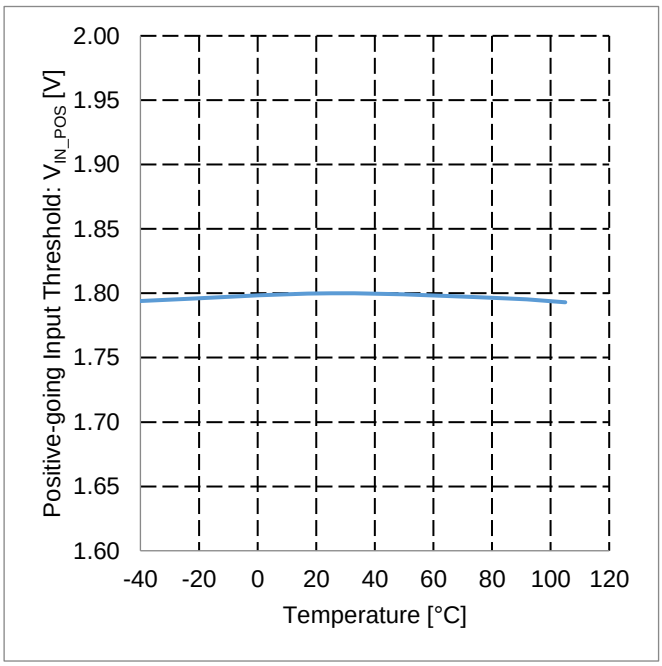


Figure 25. Positive-going Input Threshold vs Temperature

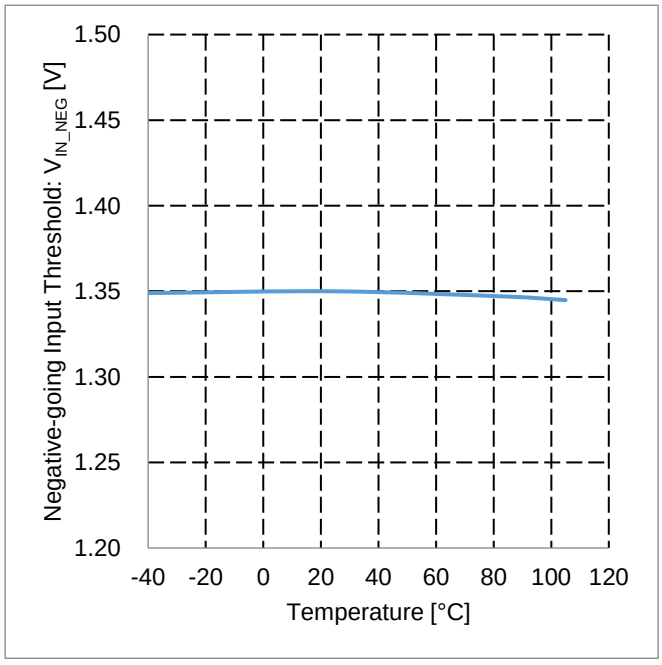


Figure 26. Negative-going Input Threshold vs Temperature

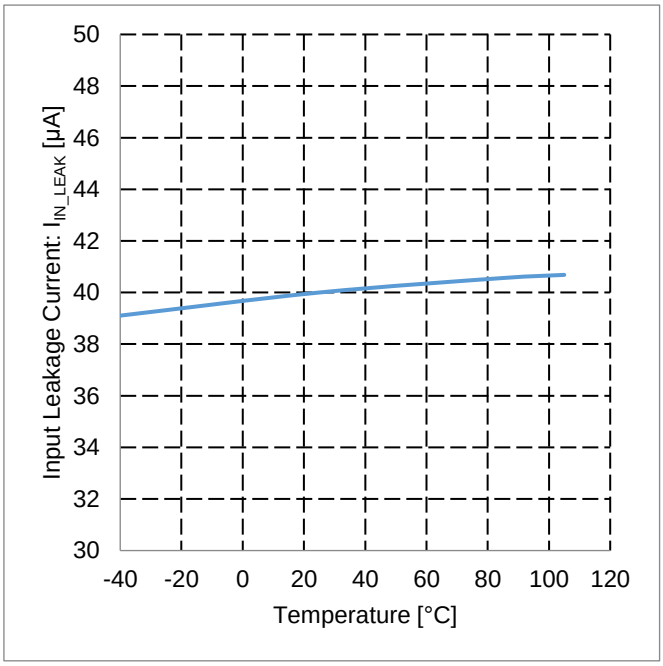


Figure 27. Input Leakage Current vs Temperature

Typical Performance Curves (Reference Data) - continued

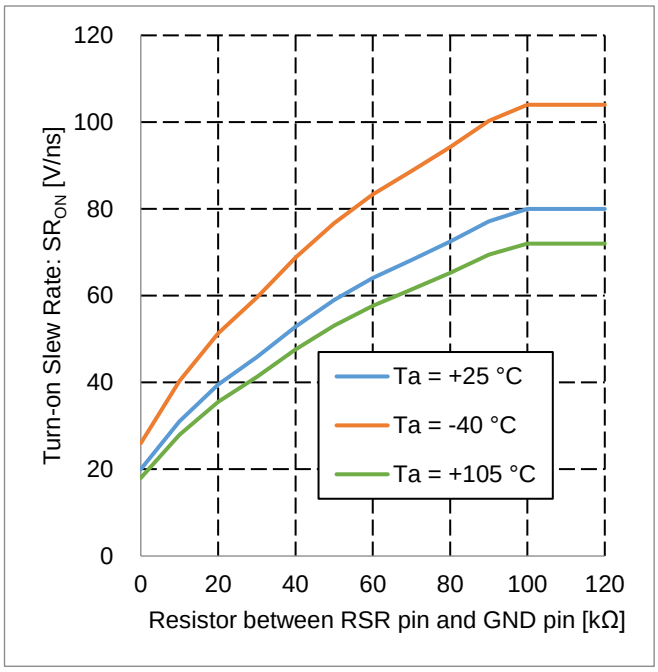


Figure 28. Turn-on Slew Rate vs Resistor between RSR pin and GND pin

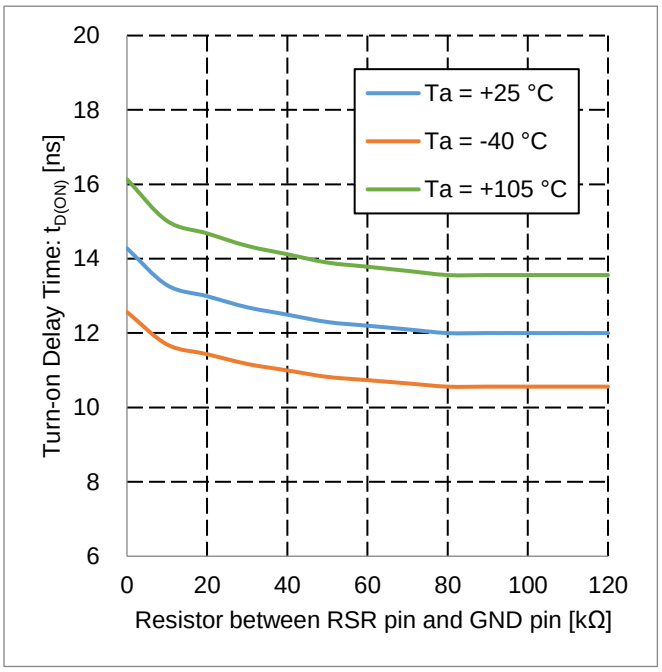


Figure 29. Turn-on Delay Time vs Resistor between RSR pin and GND pin

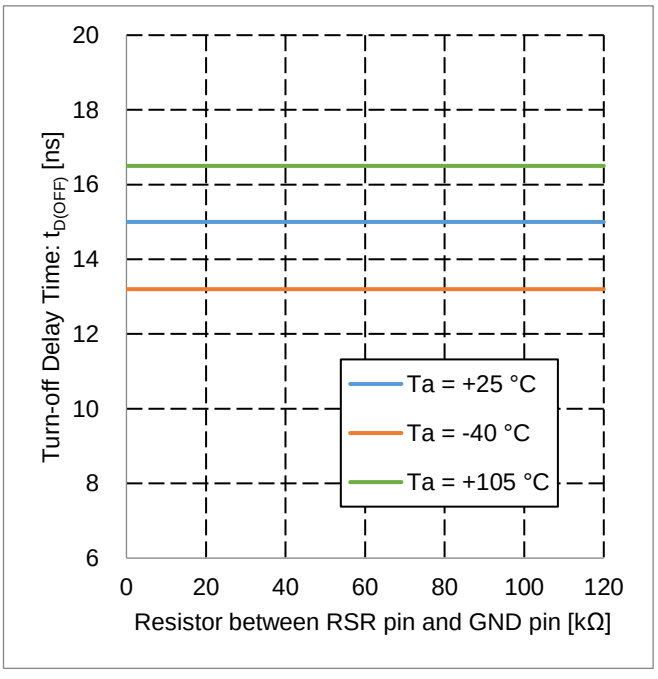


Figure 30. Turn-off Delay Time vs Resistor between RSR pin and GND pin

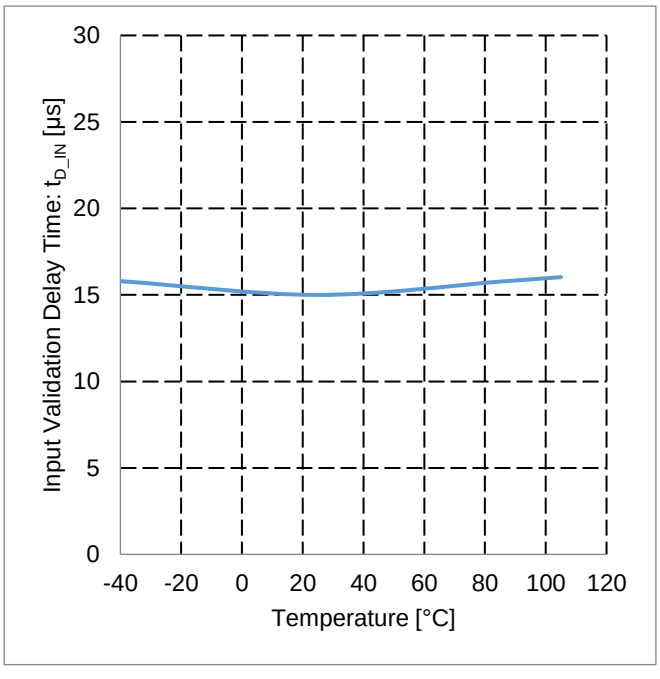


Figure 31. Input Validation Delay Time vs Temperature

Typical Performance Curves (Reference Data) - continued

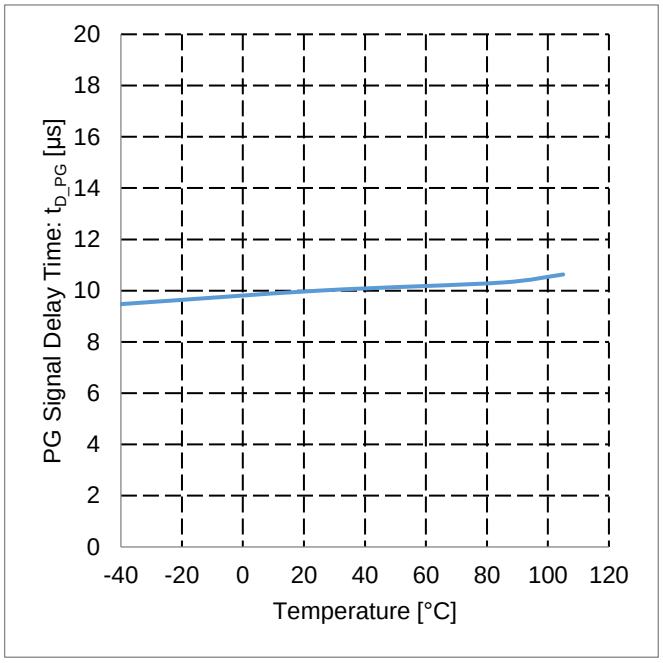


Figure 32. PG Signal Delay Time vs Temperature

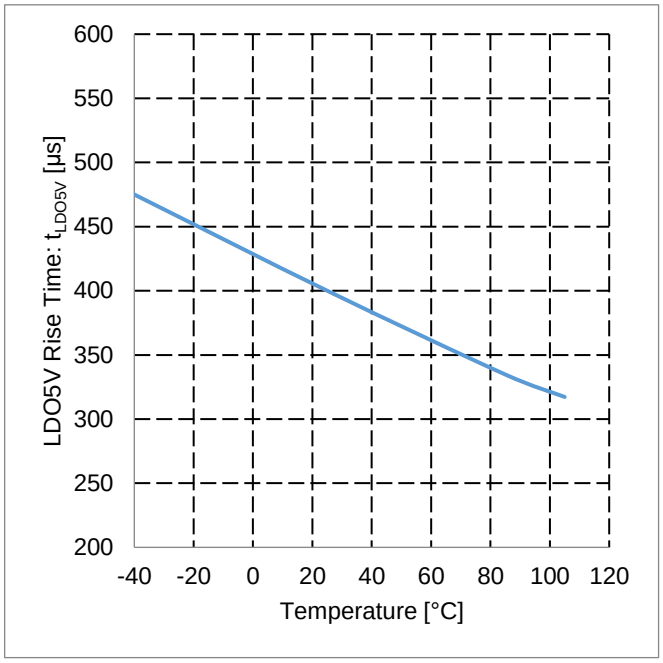


Figure 33. LDO5V Rise Time vs Temperature

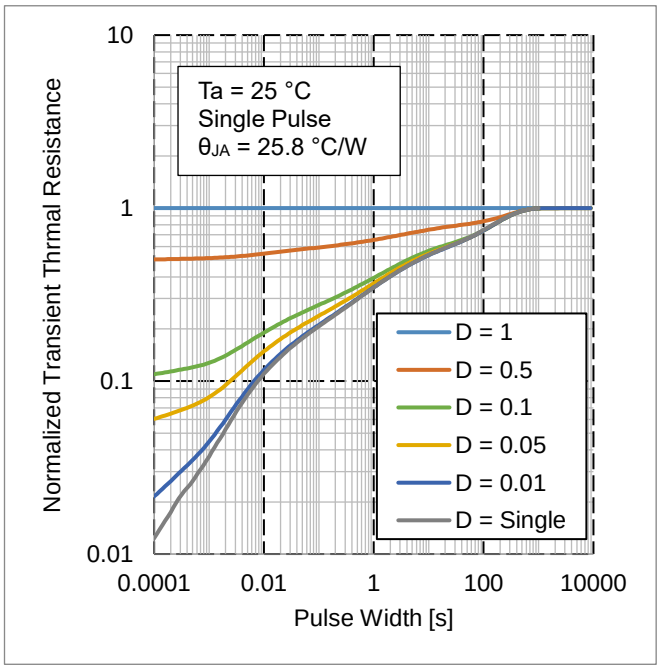


Figure 34. Normalized Transient Thermal Resistance vs Pulse Width

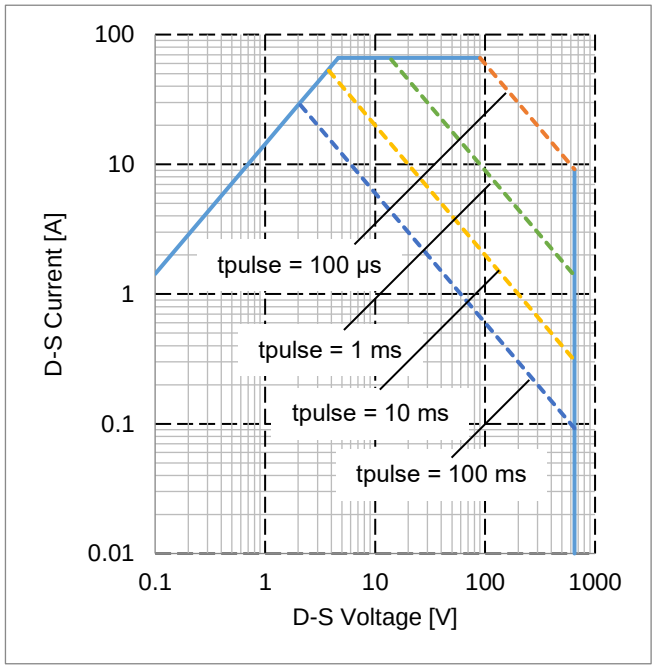
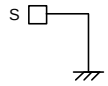
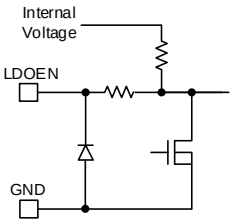
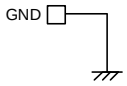
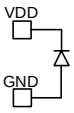
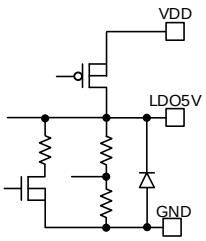
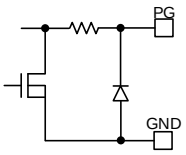
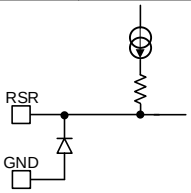
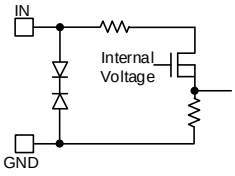
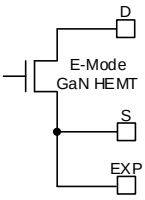
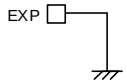


Figure 35. Maximum Safe Operating Area

I/O Equivalence Circuit

1, 2, 17-22, 25-32	S	3	LDOEN	4, 13	GND	5, 7, 9, 10, 14, 16, 23, 24	N.C.
						–	
6	VDD	8	LDO5V	11	PG	12	RSR
							
15	IN	33-46	D	-	EXP		
							

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

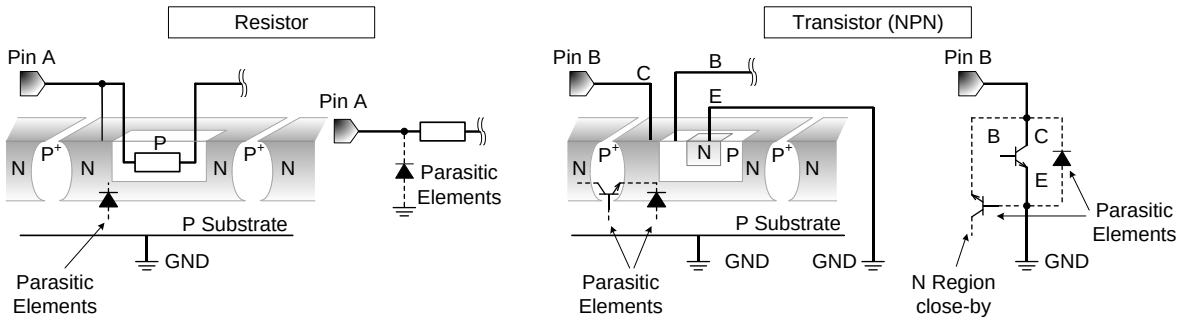


Figure 36. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

B	M	3	G	0	0	7	M	U	V	-	L	B	E	2

GaN HEMT D-S ON State Resistance (Typ)
07: 70 mΩ

Package

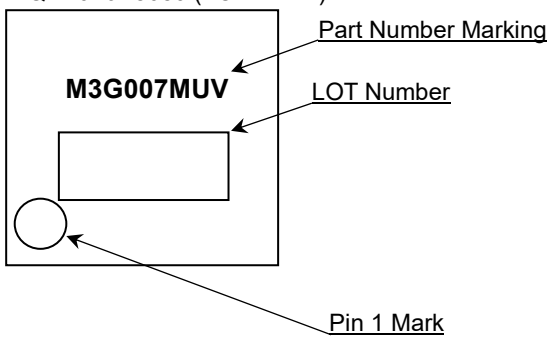
MUV:
VQFN046V8080

Product Class
LB: Industrial Applications

Packaging and forming specification
E2: Embossed tape and reel

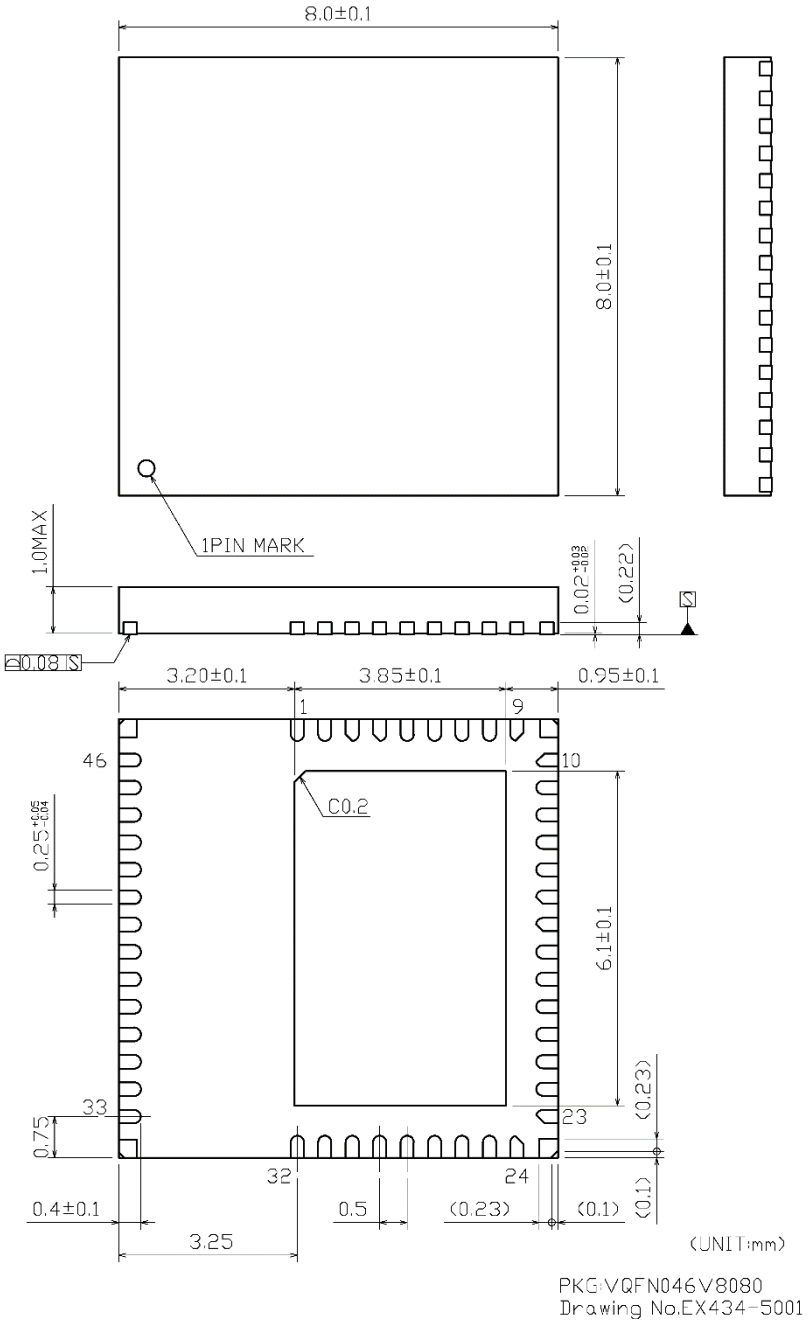
Marking Diagram

VQFN046V8080 (TOP VIEW)



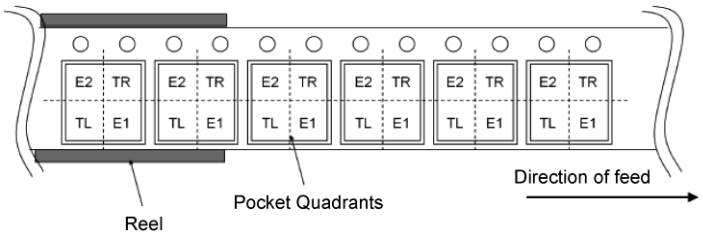
Physical Dimension and Packing Information

Package Name	VQFN046V8080



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
13.Jan.2023	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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