



# MPQ4326/4326J

## 36V, 6A, Low Quiescent Current, Synchronous Step-Down Converter, AEC-Q100 Qualified

### DESCRIPTION

The MPQ4326/4326J is a configurable-frequency (200kHz to 2.5MHz), synchronous, step-down switching regulator with an integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). The device provides up to 6A of highly efficient output current ( $I_{OUT}$ ) with peak current mode control.

The MPQ4326/4326J can maintain a regulated output voltage ( $V_{OUT}$ ) across a wide input voltage ( $V_{IN}$ ) up to 36V. It provides a load dump tolerance up to 42V via the input over-voltage protection (OVP). A 1 $\mu$ A quiescent current ( $I_Q$ ) in shutdown mode allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency ( $f_{SW}$ ) under light-load conditions to reduce switching and gate driving losses. An open-drain power good (PG) signal indicates whether  $V_{OUT}$  is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current ( $I_L$ ) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. A high duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4326 is available in a QFN-14 (4mmx4mm) package. The MPQ4326J is available in a QFN-16 (4mmx4mm) package.

### FEATURES

- Designed for Automotive Applications
  - 42V Load Dump Tolerance
  - Operating Input Voltage ( $V_{IN}$ ) Up to 36V
  - Up to 6A of Continuous  $I_{OUT}$
  - Low-Dropout Mode
  - 50ns Minimum On Time ( $t_{ON\_MIN}$ )
  - Operating Junction Temperature ( $T_J$ ) from -40°C to +150°C
  - Available in AEC-Q100 Grade 1
- Increases Battery Life
  - 1 $\mu$ A Low Shutdown Supply Current

### FEATURES (continued)

- 24 $\mu$ A  $I_Q$  in Sleep Mode
- 28 $\mu$ A  $I_Q$  with Switching
- AAM Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals
  - Internal 45m $\Omega$  High-Side and 25m $\Omega$  Low-Side MOSFETs
- Optimized for EMC/EMI
  - Configurable 200kHz to 2.5MHz  $f_{SW}$
  - FSS Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features
  - Fixed Output Options <sup>(1)</sup>: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, or 5V
  - Power Good (PG) Output
  - Synchronizable to External Clock
  - OCP in Hiccup Mode
  - Available in a QFN-14 (4mmx4mm) Package (MPQ4326) and a QFN-16 (4mmx4mm) Package (MPQ4326J) with Wettable Flanks
- Functional Safety System Design Capability
  - Documents Available for MPSafe™ QM System Design



### APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver-Assistance Systems (ADAS)
- Industrial Power Systems

#### Note:

- 1) See the Ordering Information section on page 3 regarding the fixed-output versions. Additional output voltages may be available. Contact MPS for details.

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## TYPICAL APPLICATION

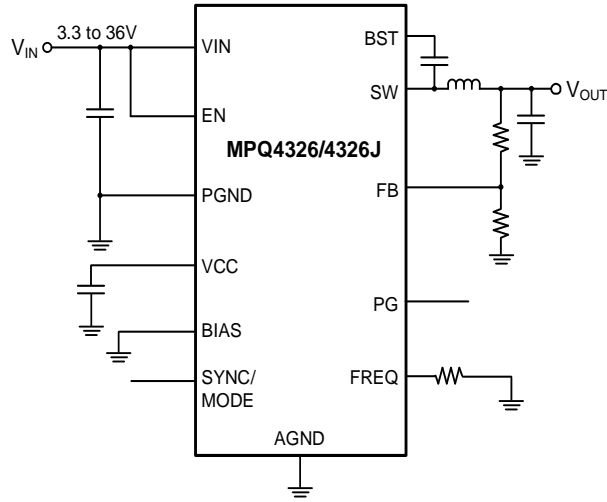


Figure 1: Typical Application (Adjustable Output)

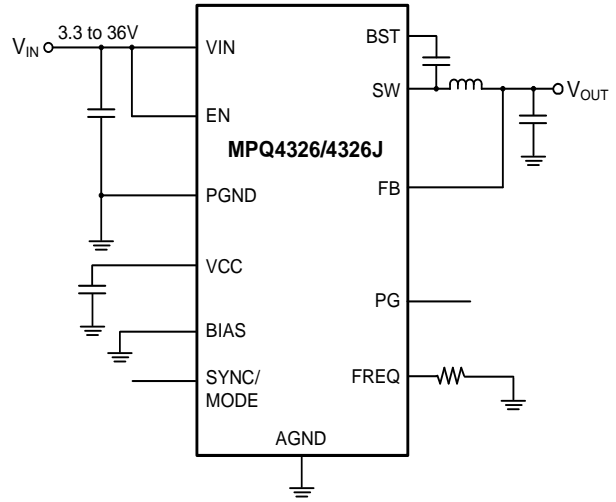
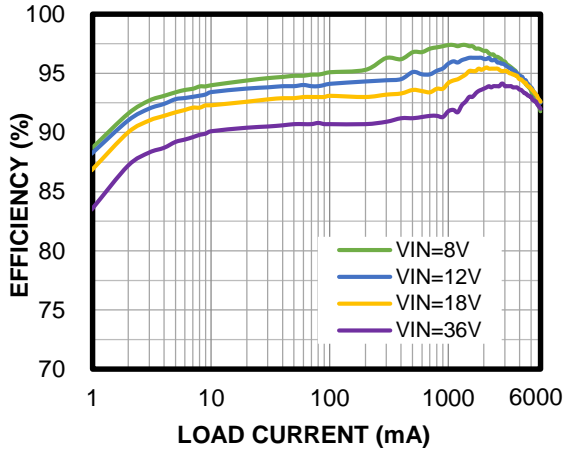


Figure 2: Typical Application (Fixed Output)

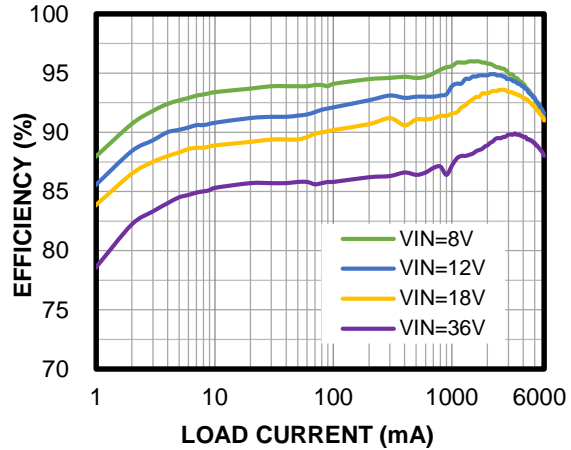
### Efficiency vs. Load Current

$V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  $L = 4.7\mu H$   
(DCR = 15m $\Omega$ ), AAM mode



### Efficiency vs. Load Current

$V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 1\mu H$   
(DCR = 9.4m $\Omega$ ), AAM mode



### ORDERING INFORMATION

| Part Number <sup>(2)*</sup> | Package          | Top Marking | MSL Rating** |
|-----------------------------|------------------|-------------|--------------|
| MPQ4326GRE***               | QFN-14 (4mmx4mm) | See Below   | 1            |
| MPQ4326GRE-AEC1***          | QFN-14 (4mmx4mm) | See Below   | 1            |
| MPQ4326GRE-5-AEC1***        | QFN-14 (4mmx4mm) | See Below   | 1            |
| MPQ4326GRE-33-AEC1***       | QFN-14 (4mmx4mm) | See Below   | 1            |
| MPQ4326JGRE-AEC1***         | QFN-16 (4mmx4mm) | See Below   | 1            |

\* For Tape & Reel, add suffix -Z (e.g. MPQ4326GRE-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* Wettable flank

**Note:**

2) Contact MPS for additional details on the fixed-output versions.

### TOP MARKING

(MPQ4326GRE, MPQ4326GRE-AEC1, MPQ4326GRE-5-AEC1 and MPQ4326GRE-33-AEC1)

**MPSYWW**  
**MP4326**  
**LLLLLL**  
**E**

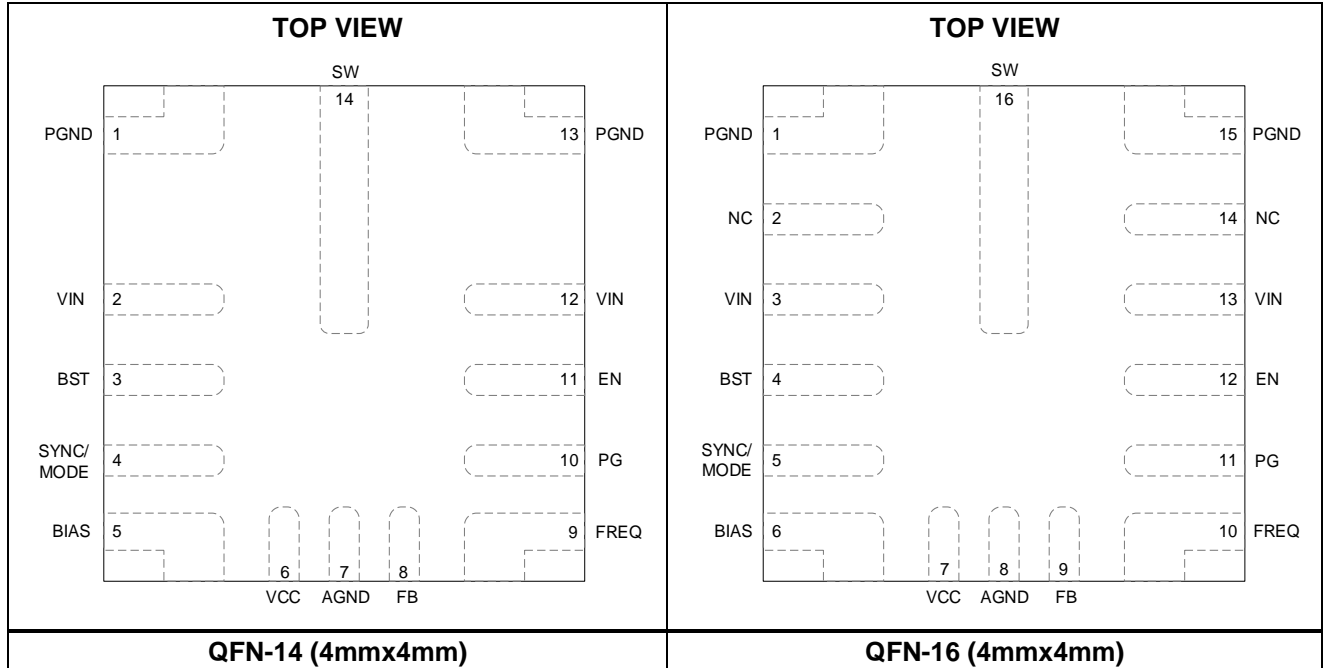
MPS: MPS prefix  
 Y: Year code  
 WW: Week code  
 MP4326: Part number  
 LLLLLL: Lot number  
 E: Wettable flank

### TOP MARKING (MPQ4326JGRE-AEC1)

**MPSYWW**  
**M4326J**  
**LLLLLL**  
**E**

MPS: MPS prefix  
 Y: Year code  
 WW: Week code  
 M4326J: Part number  
 LLLLLL: Lot number  
 E: Wettable flank

### PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #<br>QFN-16 | Pin #<br>QFN-14 | Name          | Description   |
|-----------------|-----------------|---------------|---|
| 1, 15           | 1, 13           | PGND          | <b>Power ground.</b>  |
| 2, 14           | -               | NC            | <b>Not connected.</b> Float the NC pin.   |
| 3, 13           | 2, 12           | VIN           | <b>Input supply.</b> The VIN pin supplies power to all the internal control circuitry as well as the power MOSFET connected to SW. The two VIN pins are connected internally. Place decoupling capacitors from VIN to ground to minimize the input voltage ripple ( $\Delta V_{IN}$ ) and switching spikes. The capacitors should be placed close to each VIN pin.  |
| 4               | 3               | BST           | <b>Bootstrap.</b> The BST pin is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between the BST and SW pins. See the Application Information section on page 39 to calculate the size of this capacitor.  |
| 5               | 4               | SYNC/<br>MODE | <b>SYNC input and MODE selection.</b> Pull the SYNC/MODE pin below the specified threshold (0.4V) to enter advanced asynchronous modulation (AAM) mode; pull the pin above the specified threshold (1.4V) to enter forced continuous conduction mode (FCCM). Connect SYNC/MODE to an external 200kHz to 2.5MHz clock source to synchronize the converter to the external clock and enter FCCM. This pin has an internal, 100k $\Omega$ pull-down resistor. If SYNC/MODE is floated, the device enters AAM mode. |
| 6               | 5               | BIAS          | <b>External bias.</b> Connect the BIAS pin to a 5V output voltage ( $V_{OUT}$ ) supply to achieve lower quiescent current ( $I_Q$ ). For the 5V output version, connect BIAS to $V_{OUT}$ directly. For other output versions, connect BIAS to an external 5V source or ground. It is recommended to avoid providing external bias voltage before $V_{IN}$ . Do not float this pin.   |
| 7               | 6               | VCC           | <b>Internal bias supply.</b> The VCC pin is the output of the internal regulator that supplies power to the internal control circuit and gate drivers. VCC is typically 5V. Place a decoupling capacitor exceeding 1 $\mu$ F between VCC and ground. The capacitor should be placed as close to VCC as possible.  |
| 8               | 7               | AGND          | <b>Analog ground.</b>   |
| 9               | 8               | FB            | <b>Feedback input.</b> For the fixed-output versions, connect the FB pin directly to $V_{OUT}$ . For the adjustable-output version, connect FB to the middle point of the external feedback divider between the output and AGND to set $V_{OUT}$ . The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.  |
| 10              | 9               | FREQ          | <b>Switching frequency configuration.</b> Connect a resistor from the FREQ pin to ground to set the switching frequency ( $f_{SW}$ ).   |
| 11              | 10              | PG            | <b>Power good output.</b> The PG pin is an open-drain output. If PG is used, connect a pull-up resistor to the power source. PG goes high if $V_{OUT}$ is within 94.5% to 105.5% of the nominal voltage. PG goes low if $V_{OUT}$ is above 107% or below 93% of the nominal voltage. Float this pin if not used.  |
| 12              | 11              | EN            | <b>Enable.</b> Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Pull EN above the specified threshold (1.02V) to enable the chip. Do not float this pin.  |
| 16              | 14              | SW            | <b>Switch node.</b> The SW pin is the source of the HS-FET and the drain of the low-side MOSFET (LS-FET).   |

**ABSOLUTE MAXIMUM RATINGS** <sup>(3)</sup>

|  |   |
|--|---|
| VIN, EN.....   | -0.3V to +40V                               |
| VIN, EN.....   | 42V for automotive load dump <sup>(4)</sup> |
| SW.....  | -0.3V to V <sub>IN_MAX</sub> + 0.3V         |
| BST.....   | V <sub>SW</sub> +5.5V                       |
| FREQ.....  | -0.3V to +5.5V                              |
| All other pins.....  | -0.3V to +6V                                |
| Continuous power dissipation (T <sub>A</sub> = 25°C) <sup>(5)</sup> <sup>(9)</sup> |   |
| QFN-14 (4mmx4mm).....  | 4.86W                                       |
| QFN-16 (4mmx4mm).....  | 4.42W                                       |
| Junction temperature (T <sub>J</sub> ).....  | 150°C                                       |
| Lead temperature.....  | 260°C                                       |
| Storage temperature.....   | -65°C to +150°C                             |

**ESD Ratings**

|                                 |                          |
|---------------------------------|--------------------------|
| Human body model (HBM).....     | Class 2 <sup>(6)</sup>   |
| Charged-device model (CDM)..... | Class C2b <sup>(7)</sup> |

**Recommended Operating Conditions**

|   |                                |
|---|--------------------------------|
| Continuous supply voltage (V <sub>IN</sub> )..... | 3.3V to 36V                    |
| Output voltage (V <sub>OUT</sub> ).....           | 0.8V to 0.95 x V <sub>IN</sub> |
| Operating junction temp (T <sub>J</sub> )....     | -40°C to +150°C                |

| <b>Thermal Resistance</b> | <b>θ<sub>JA</sub></b> | <b>θ<sub>JC</sub></b>       |
|---------------------------|-----------------------|-----------------------------|
| QFN-14 (4mmx4mm)          |                       |                             |
| JESD51-7.....             | 46.7.....             | 7.9.....°C/W <sup>(8)</sup> |
| EVQ4326-R-00A.....        | 25.7.....             | °C/W <sup>(9)</sup>         |
| QFN-16 (4mmx4mm)          |                       |                             |
| JESD51-7.....             | 50.2.....             | 5.6.....°C/W <sup>(8)</sup> |
| EVQ4326J-R-00A.....       | 28.3.....             | °C/W <sup>(9)</sup>         |
|                           |                       | <b>Ψ<sub>JT</sub></b>       |
| QFN-14 (4mmx4mm)          |                       |                             |
| JESD51-7.....             | 2.6.....              | °C/W <sup>(8)</sup>         |
| EVQ4326-R-00A.....        | 2.2.....              | °C/W <sup>(9)</sup>         |
| QFN-16 (4mmx4mm)          |                       |                             |
| JESD51-7.....             | 2.3.....              | °C/W <sup>(8)</sup>         |
| EVQ4326J-R-00A.....       | 2.....                | °C/W <sup>(9)</sup>         |

**Notes:**

- 3) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
- 4) Refer to ISO16750.
- 5) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) / θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation may produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 6) Per AEC-Q100-002.
- 7) Per AEC-Q100-011.
- 8) Measured on a JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ<sub>JC</sub> value shows the thermal resistance from the junction-to-case bottom, and the Ψ<sub>JT</sub> value shows the characterization parameter from the junction-to-case top.
- 9) Measured on an MPS standard EVB, a 2oz copper thickness, 4-layer PCB (8.3cmx8.3cm). The Ψ<sub>JT</sub> value shows the characterization parameter from the junction-to-case top.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 2V, T<sub>J</sub> = -40°C to +150°C, typical values are at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter   | Symbol                       | Condition   | Min  | Typ  | Max  | Units |
|---|------------------------------|---|------|------|------|-------|
| <b>Input Supply</b>   |                              |   |      |      |      |       |
| Minimum operating input voltage (V <sub>IN</sub> )            | V <sub>IN_MIN</sub>          |   |      |      | 3.3  | V     |
| V <sub>IN</sub> under-voltage lockout (UVLO) rising threshold | V <sub>IN_UVLO_RISING</sub>  |   | 3.5  | 3.7  | 3.9  | V     |
| V <sub>IN</sub> UVLO falling threshold                        | V <sub>IN_UVLO_FALLING</sub> |   | 2.75 | 2.9  | 3.15 | V     |
| V <sub>IN</sub> UVLO hysteresis                               | V <sub>IN_UVLO_HYS</sub>     |   |      | 750  |      | mV    |
| V <sub>IN</sub> quiescent current                             | I <sub>Q</sub>               | V <sub>FB</sub> = 0.85V, no load, sleep mode, without BIAS connection, T <sub>J</sub> = 25°C            |      | 24   | 35   | μA    |
|   |                              | V <sub>FB</sub> = 0.85V, no load, sleep mode, without BIAS connection, T <sub>J</sub> = -40°C to +150°C |      | 24   | 80   | μA    |
|   |                              | V <sub>FB</sub> = 0.85V, no load, connect BIAS to 5V  |      | 3    |      | μA    |
| V <sub>IN</sub> quiescent current (switching)                 | I <sub>Q_SLEEP</sub>         | SYNC/MODE = ground, AAM mode, switching, no load  |      | 28   |      | μA    |
| V <sub>IN</sub> active current (no switching) <sup>(10)</sup> | I <sub>Q_ACTIVE</sub>        | SYNC/MODE = VCC, CCM, non-switching   |      | 950  |      | μA    |
| V <sub>IN</sub> shutdown current                              | I <sub>SHDN</sub>            | EN = 0V   |      | 1    | 10   | μA    |
| V <sub>IN</sub> over-voltage protection (OVP) threshold       | V <sub>IN_OVP_RISING</sub>   |   | 36   | 38   | 40   | V     |
| V <sub>IN</sub> OVP hysteresis                                | V <sub>IN_OVP_HYS</sub>      |   |      | 1    |      | V     |
| <b>Switches and Frequency</b>                                 |                              |   |      |      |      |       |
| Switching frequency   | f <sub>SW</sub>              | R <sub>FREQ</sub> = 49.9kΩ  | 350  | 410  | 460  | kHz   |
|   |                              | R <sub>FREQ</sub> = 19.6kΩ  | 900  | 1000 | 1100 | kHz   |
|   |                              | R <sub>FREQ</sub> = 8.66kΩ  | 1980 | 2200 | 2420 | kHz   |
| Minimum on time <sup>(10)</sup>                               | t <sub>ON_MIN</sub>          |   |      | 50   | 65   | ns    |
| Minimum off time <sup>(10)</sup>                              | t <sub>OFF_MIN</sub>         |   |      | 40   | 55   | ns    |
| Switch leakage current  | I <sub>SW_LKG</sub>          | T <sub>J</sub> = 25°C   |      | 0.01 | 1    | μA    |
|   |                              | T <sub>J</sub> = -40°C to +150°C  |      | 0.01 | 5    | μA    |
| High-side MOSFET (HS-FET) on resistance                       | R <sub>DS(ON)_HS</sub>       | V <sub>BST</sub> - V <sub>SW</sub> = 5V   |      | 45   |      | mΩ    |
| Low-side MOSFET (LS-FET) on resistance                        | R <sub>DS(ON)_LS</sub>       | V <sub>CC</sub> = 5V  |      | 25   |      | mΩ    |
| <b>BIAS</b>   |                              |   |      |      |      |       |
| BIAS voltage (V <sub>BIAS</sub> ) takeover threshold          | V <sub>BIAS_RISING</sub>     |   |      | 4.6  |      | V     |
| V <sub>BIAS</sub> takeover hysteresis                         | V <sub>BIAS_HYS</sub>        |   |      | 240  |      | mV    |

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter   | Symbol                | Condition   | Min  | Typ  | Max  | Units         |
|---|-----------------------|---|------|------|------|---------------|
| <b>Output and Regulation</b>                          |                       |   |      |      |      |               |
| FB voltage (adjustable-output version)                | $V_{FB}$              | $T_J = 25^{\circ}C$                                       | 794  | 800  | 806  | mV            |
|   |                       | $T_J = -40^{\circ}C$ to $+150^{\circ}C$                   | 790  | 800  | 810  | mV            |
| Output regulation voltage (3.3V fixed-output version) | $V_{OUT}$             | $T_J = 25^{\circ}C$                                       | 3250 | 3300 | 3350 | mV            |
|   |                       | $T_J = -40^{\circ}C$ to $+150^{\circ}C$                   | 3234 | 3300 | 3366 | mV            |
| FB input current                                      | $I_{FB}$              | Adjustable-output version                                 |      | 0    | 100  | nA            |
|   |                       | Fixed-output version, $V_{OUT} = V_{OUT\_REG}$            |      | 3.3  |      | $\mu A$       |
| Output voltage ( $V_{OUT}$ ) discharge current        | $I_{DISCHARGE}$       | $V_{EN} = 0V$ , $V_{OUT} = 0.3V$                          | 2    |      |      | mA            |
| <b>Bootstrap (BST)</b>                                |                       |   |      |      |      |               |
| BST to SW refresh rising threshold                    | $V_{BST-SW\_RISING}$  |   | 2.2  | 2.7  | 3.2  | V             |
| BST to SW refresh falling threshold                   | $V_{BST-SW\_FALLING}$ |   | 2    | 2.5  | 3    | V             |
| BST to SW refresh hysteresis                          | $V_{BST-SW\_HYS}$     |   |      | 0.2  |      | V             |
| <b>Enable (EN)</b>                                    |                       |   |      |      |      |               |
| EN rising threshold                                   | $V_{EN\_RISING}$      |   | 0.97 | 1.02 | 1.07 | V             |
| EN falling threshold                                  | $V_{EN\_FALLING}$     |   | 0.80 | 0.85 | 0.90 | V             |
| EN hysteresis voltage                                 | $V_{EN\_HYS}$         |   |      | 170  |      | mV            |
| <b>Soft Start and VCC</b>                             |                       |   |      |      |      |               |
| Soft-start time                                       | $t_{SS}$              | EN high to PG high  | 4.5  | 6    | 7.5  | ms            |
| VCC voltage   | $V_{CC}$              | $I_{VCC} = 0mA$   | 4.7  | 5    | 5.3  | V             |
| VCC regulation  |                       | $I_{VCC} = 30mA$ , AAM mode                               |      | 1    |      | %             |
| VCC current limit                                     | $I_{LIMIT\_VCC}$      | $V_{CC} = 4V$   | 50   | 65   |      | mA            |
| <b>SYNC/MODE</b>                                      |                       |   |      |      |      |               |
| SYNC/MODE voltage rising threshold                    | $V_{SYNC\_RISING}$    |   | 1.4  |      |      | V             |
| SYNC/MODE voltage falling threshold                   | $V_{SYNC\_FALLING}$   |   |      |      | 0.4  | V             |
| SYNC/MODE timeout                                     | $t_{MODE}$            | SYNC/MODE low to DCM                                      |      | 55   | 80   | $\mu s$       |
| SYNCIN clock range                                    | $f_{SYNC}$            | Percentage of free-running frequency                      | 90   |      | 110  | % of $f_{sw}$ |
| SYNCIN clock locking time                             | $t_{SYNC\_LOCK}$      | SYNC clock locking time                                   |      |      | 128  | cycle         |
| SYNCIN clock duty                                     | $D_{SYNC\_DUTY}$      | SYNC clock duty for minimum input clock pulse width >40ns | 20   |      | 80   | %             |
| $f_{sw}$ after SYNC                                   |                       | $f_{sw}$ accuracy compared to $f_{SYNC}$                  | -5   |      | +5   | %             |



**ELECTRICAL CHARACTERISTICS (continued)**
**V<sub>IN</sub> = 12V, V<sub>EN</sub> = 2V, T<sub>J</sub> = -40°C to +150°C, typical values are at T<sub>J</sub> = 25°C unless otherwise noted.**

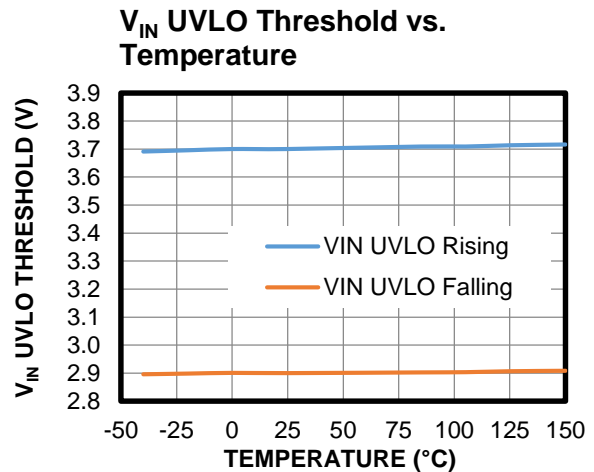
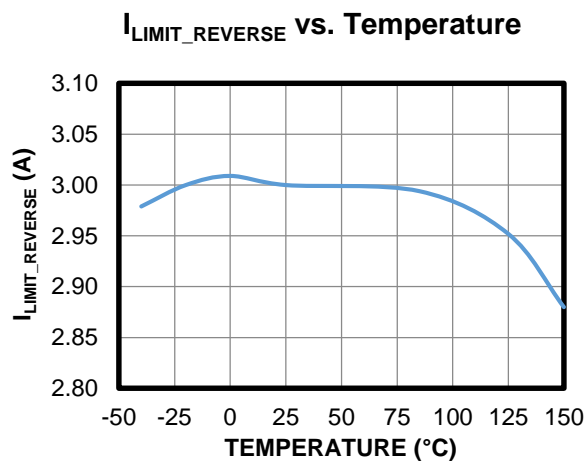
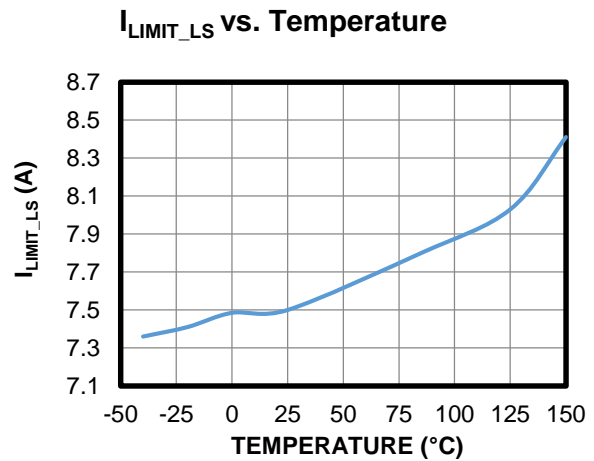
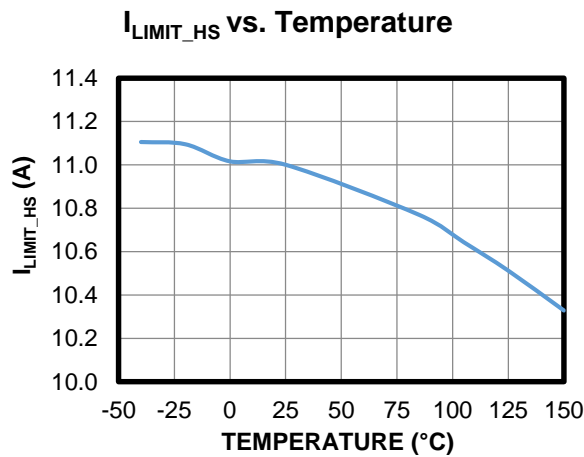
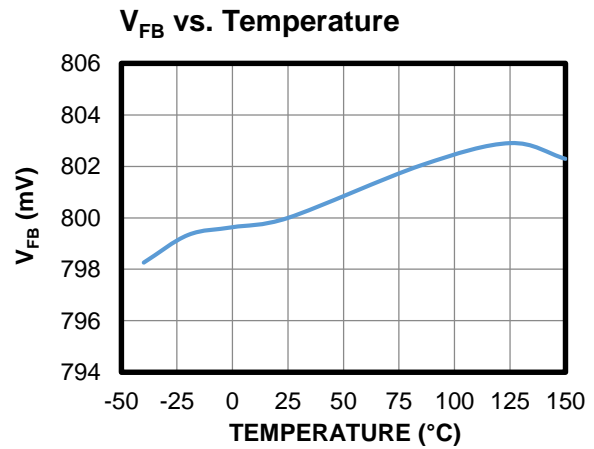
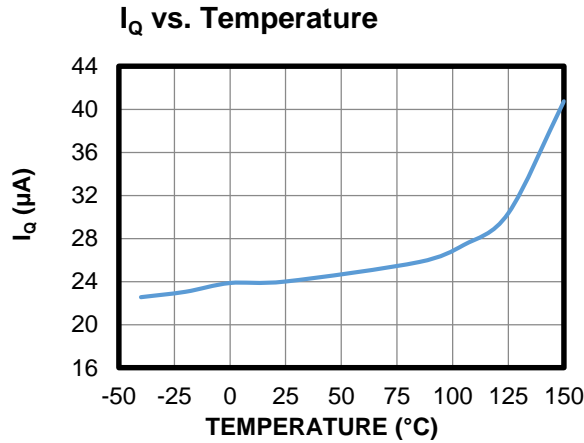
| Parameter                                   | Symbol                      | Condition                | Min   | Typ   | Max   | Units                 |
|---|-----------------------------|--------------------------|-------|-------|-------|-----------------------|
| <b>Power Good (PG)</b>                      |                             |                          |       |       |       |                       |
| PG rising threshold                         | V <sub>PG_VTH_RISING</sub>  | V <sub>OUT</sub> rising  | 93    | 94.5  | 96    | % of V <sub>REF</sub> |
|   |                             | V <sub>OUT</sub> falling | 104   | 105.5 | 107   | % of V <sub>REF</sub> |
| PG falling threshold                        | V <sub>PG_VTH_FALLING</sub> | V <sub>OUT</sub> falling | 91.5  | 93    | 94.5  | % of V <sub>REF</sub> |
|   |                             | V <sub>OUT</sub> rising  | 105.5 | 107   | 108.5 | % of V <sub>REF</sub> |
| PG trip threshold hysteresis                | V <sub>PG_VTH_HYS</sub>     |                          |       | 1.5   |       | % of V <sub>REF</sub> |
| PG low output voltage                       | V <sub>PG_LOW</sub>         | I <sub>SINK</sub> = 1mA  |       | 0.1   | 0.3   | V                     |
| PG start-up rising delay time               | t <sub>PG_R_DELAY</sub>     |                          |       | 1.2   |       | ms                    |
| PG rising deglitch time                     | t <sub>PG_R_DEGLITCH</sub>  |                          |       | 160   |       | μs                    |
| PG falling deglitch time                    | t <sub>PG_F_DEGLITCH</sub>  |                          |       | 160   |       | μs                    |
| <b>Protections</b>                          |                             |                          |       |       |       |                       |
| High-side (HS) current limit                | I <sub>LIMIT_HS</sub>       | Duty cycle = 30%         | 8.5   | 11    | 13    | A                     |
| Low-side (LS) valley current limit          | I <sub>LIMIT_LS</sub>       |                          | 6     | 7.5   | 9     | A                     |
| Zero-current detection (ZCD) current        | I <sub>ZCD</sub>            | AAM mode                 | 0     | 200   |       | mA                    |
| LS reverse current limit                    | I <sub>LIMIT_REVERSE</sub>  | FCCM                     |       | 3     |       | A                     |
| Thermal shutdown <sup>(10)</sup>            | T <sub>SD</sub>             |                          | 155   | 170   | 185   | °C                    |
| Thermal shutdown hysteresis <sup>(10)</sup> | T <sub>SD_HYS</sub>         |                          |       | 20    |       | °C                    |

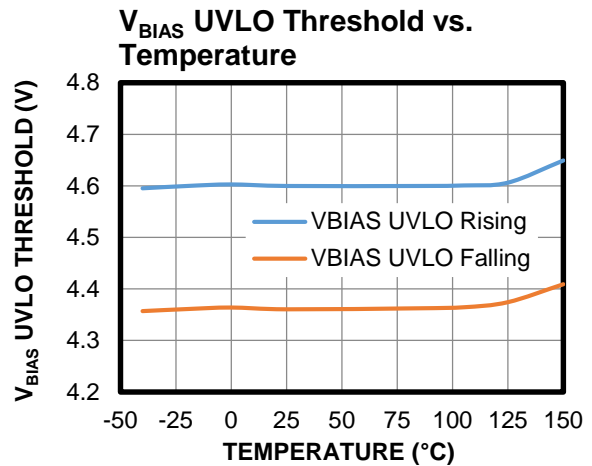
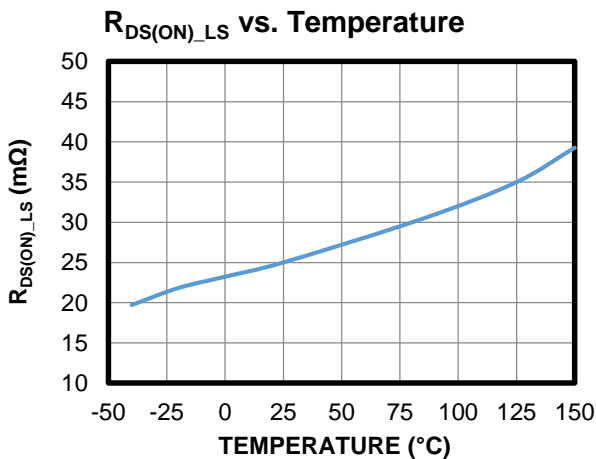
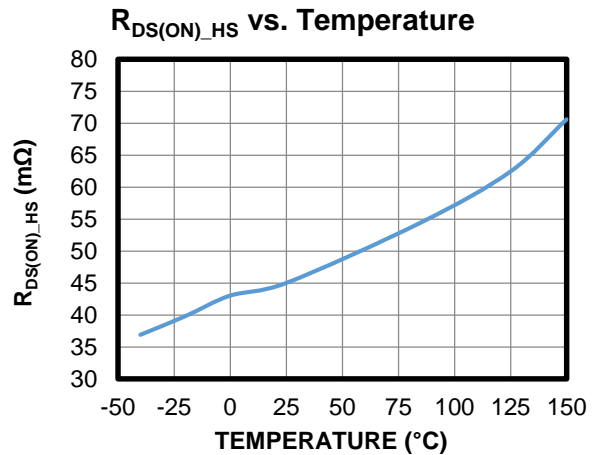
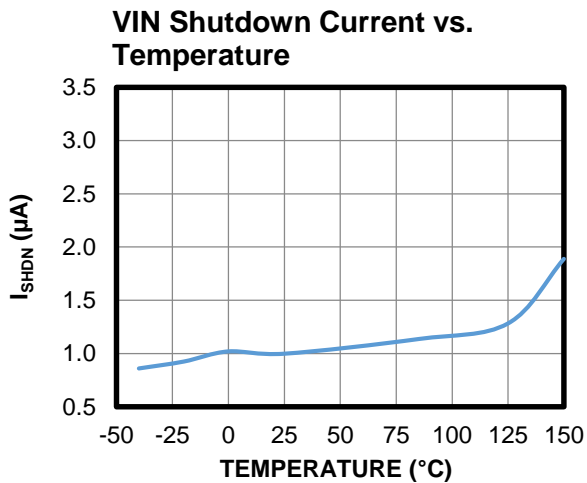
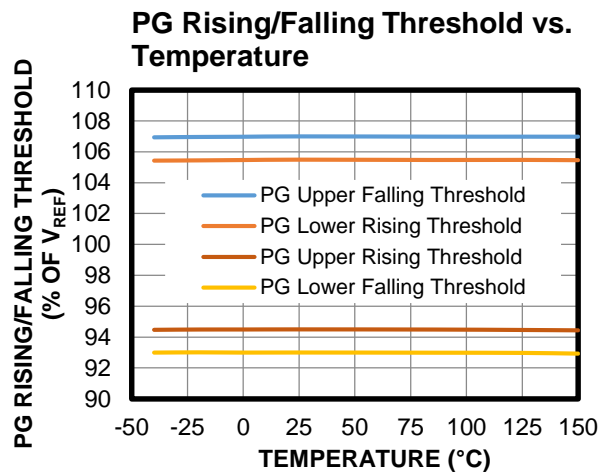
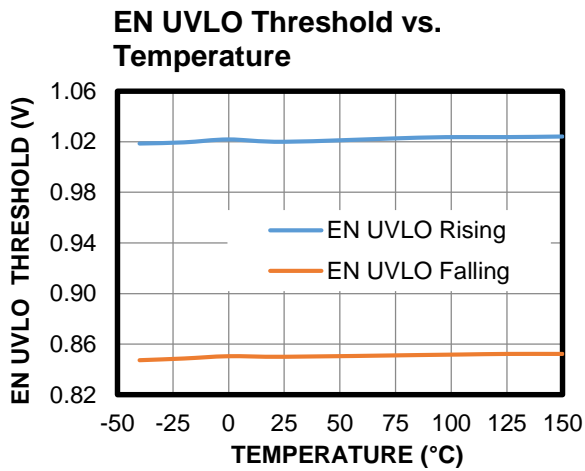
**Note:**

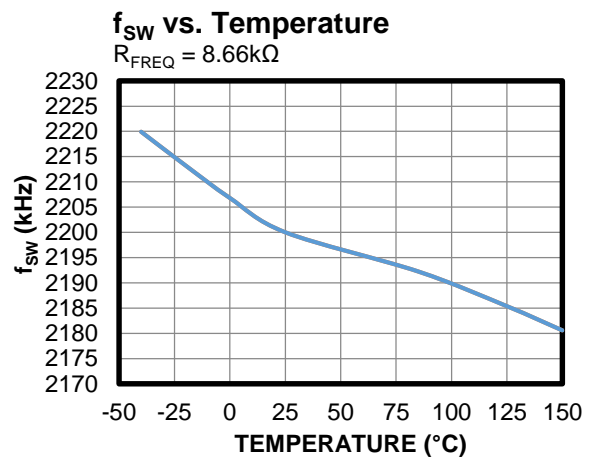
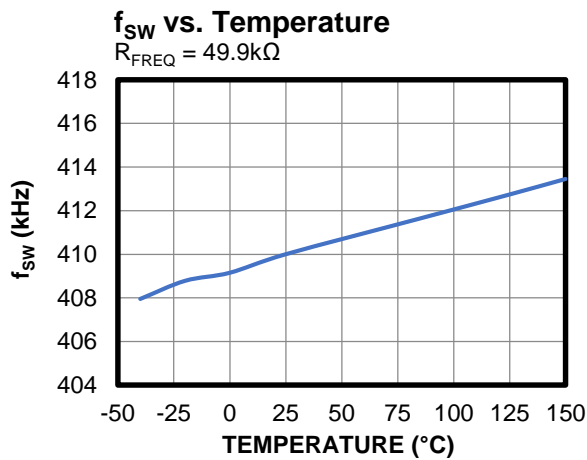
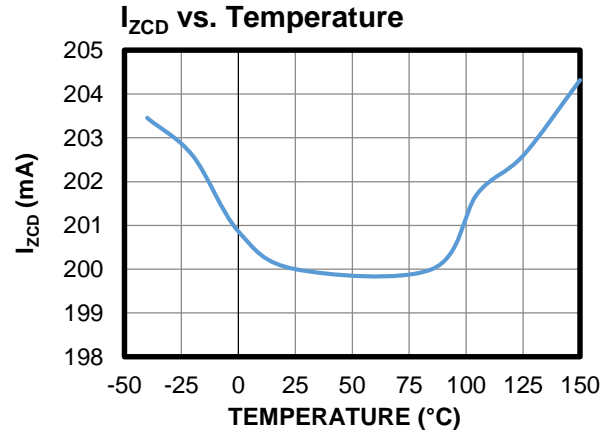
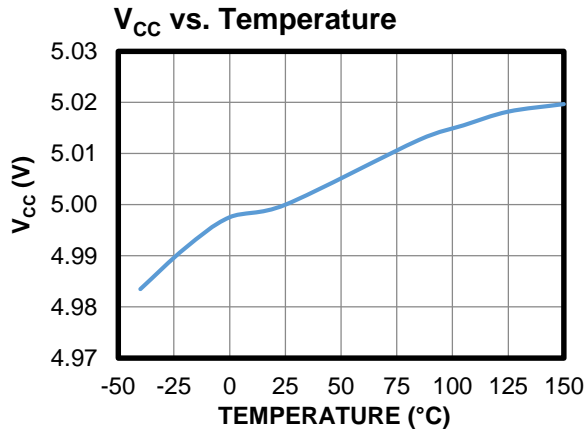
10) Guaranteed by design and characterization. Not tested in production.

## TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.


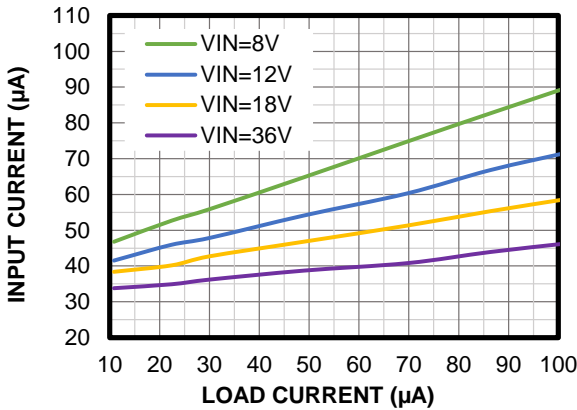
**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode, BIAS connected to  $V_{OUT}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

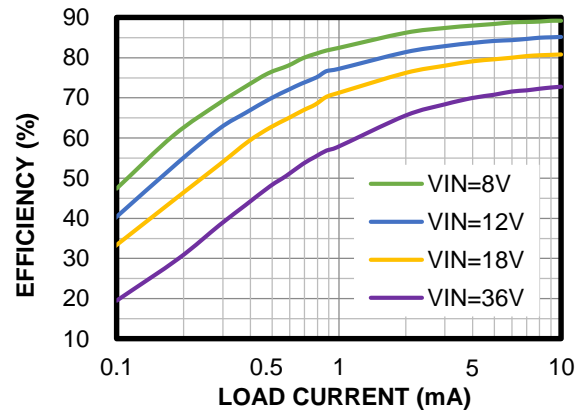
### Input Current vs. Load Current

AAM mode,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )



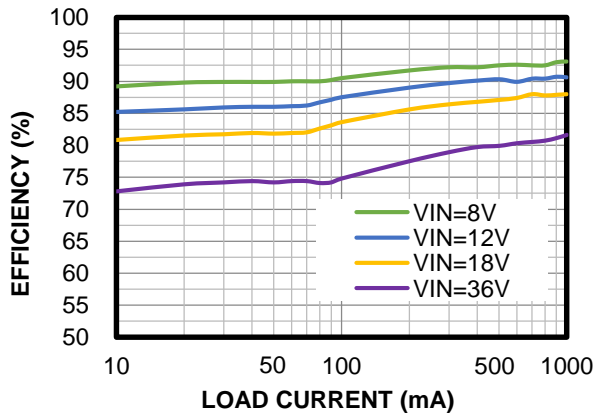
### Efficiency vs. Load Current

AAM mode,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )



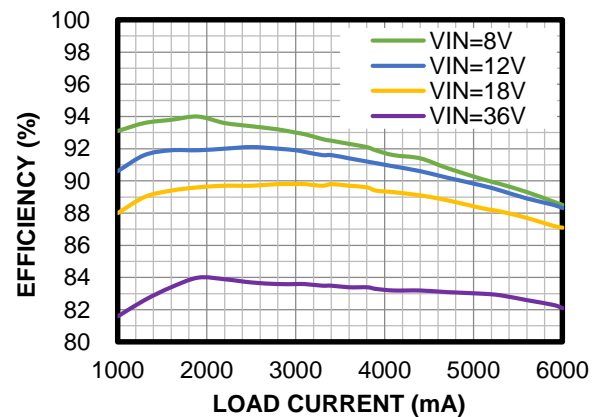
### Efficiency vs. Load Current

AAM mode,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )



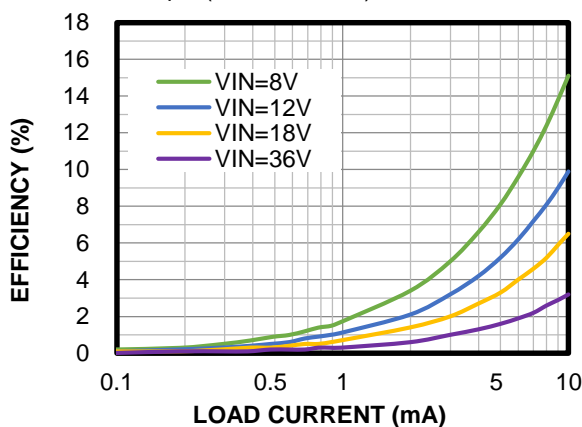
### Efficiency vs. Load Current

AAM mode,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )



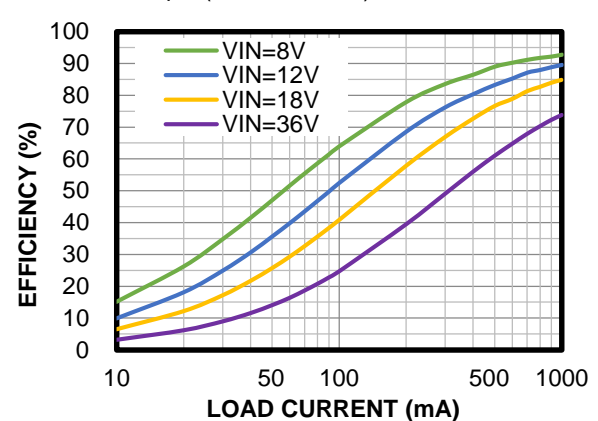
### Efficiency vs. Load Current

FCCM,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )



### Efficiency vs. Load Current

FCCM,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )

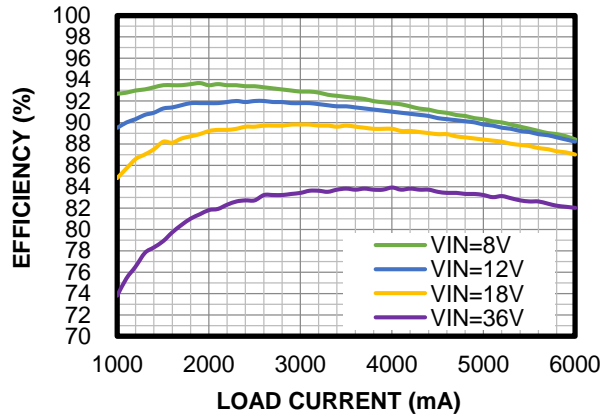


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

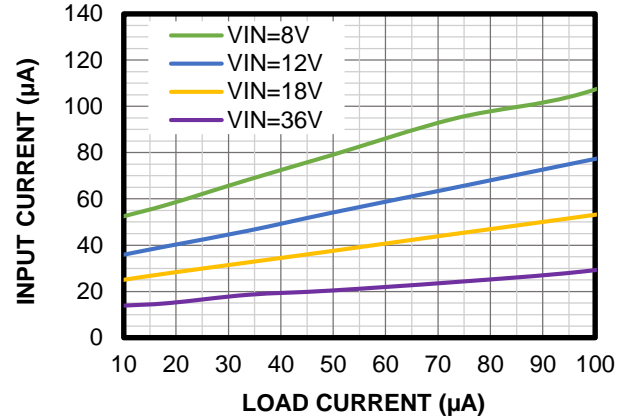
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode, BIAS connected to  $V_{OUT}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Efficiency vs. Load Current**

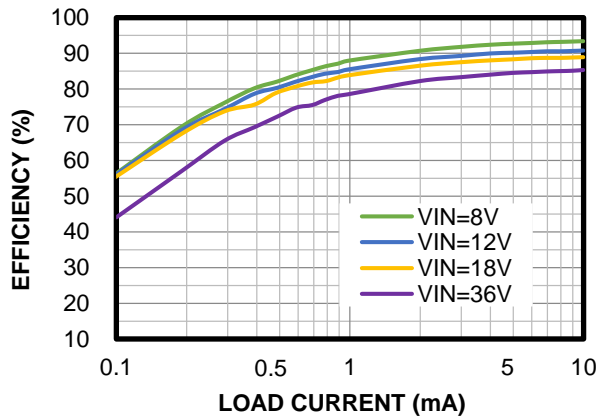
FCCM,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )


**Input Current vs. Load Current**

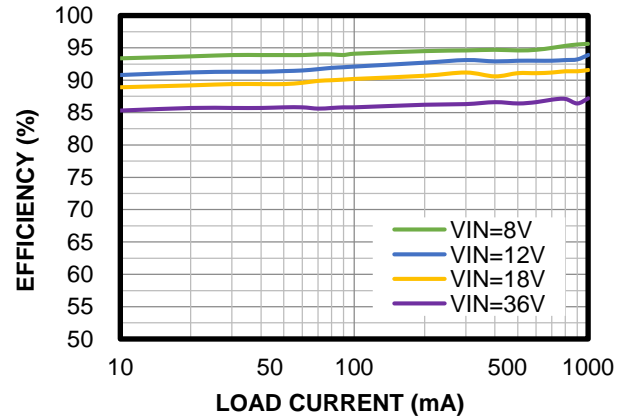
AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )


**Efficiency vs. Load Current**

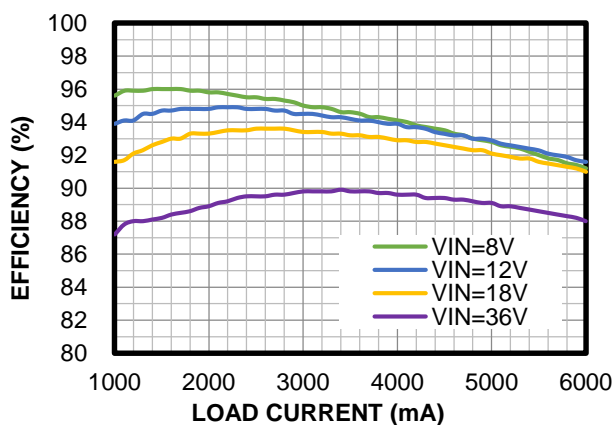
AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )


**Efficiency vs. Load Current**

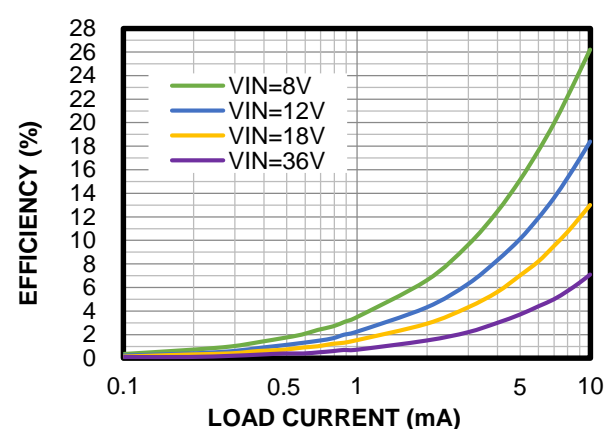
AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )


**Efficiency vs. Load Current**

AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )

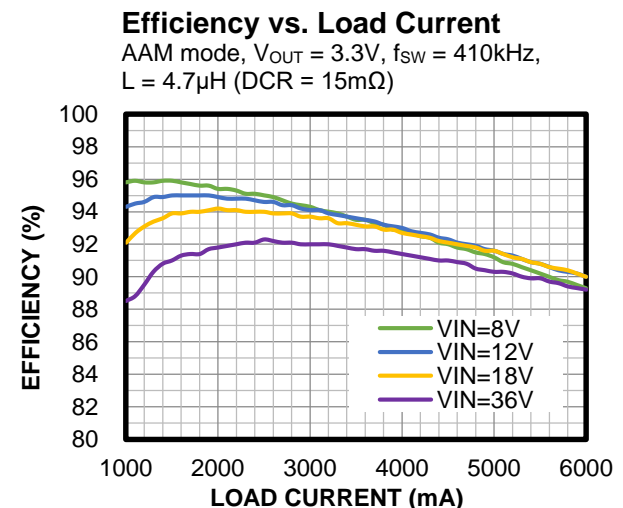
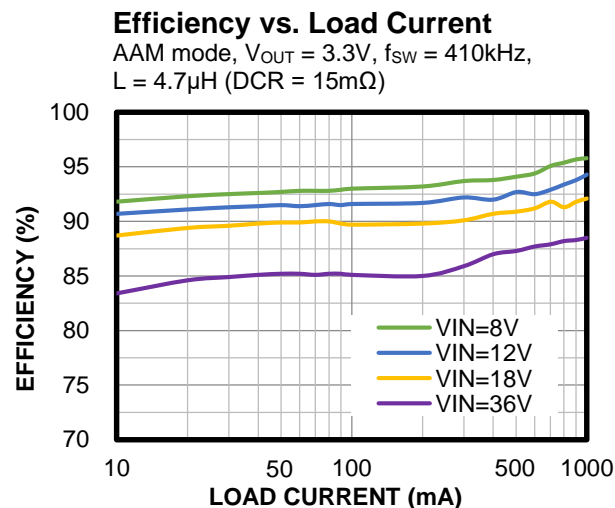
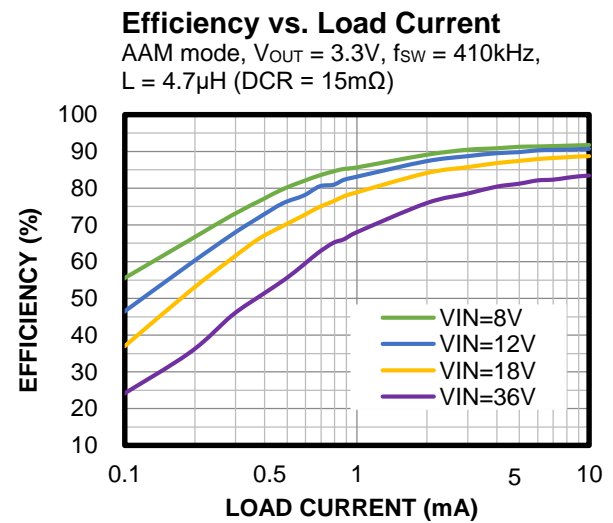
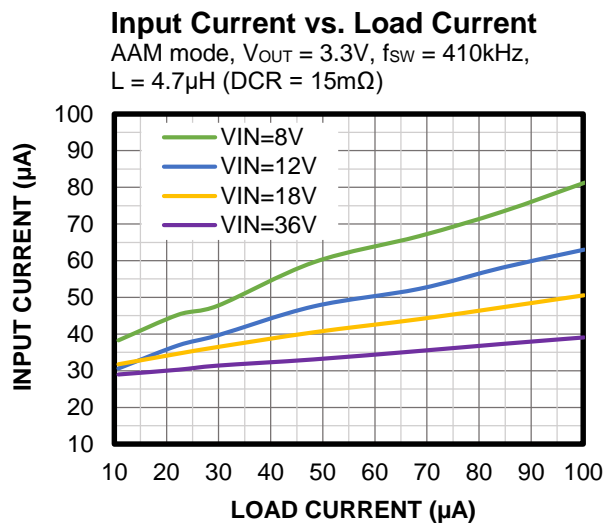
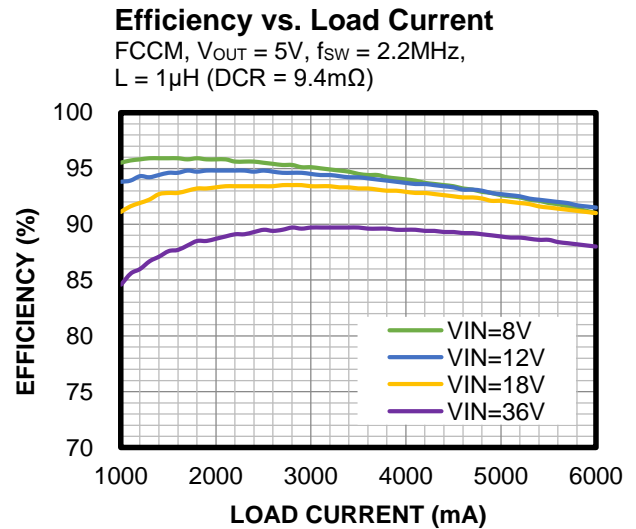
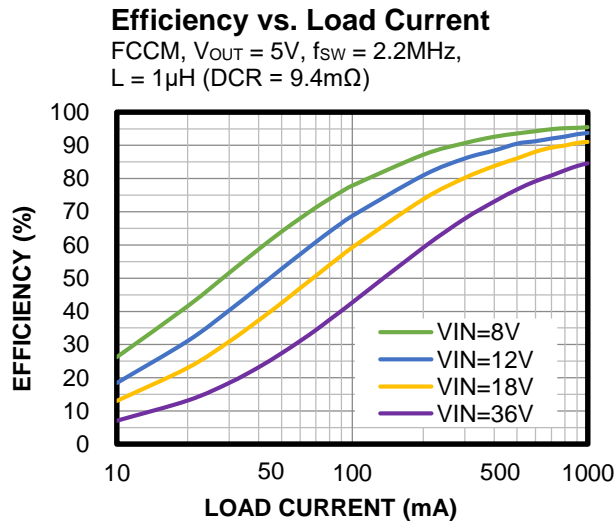

**Efficiency vs. Load Current**

FCCM,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )



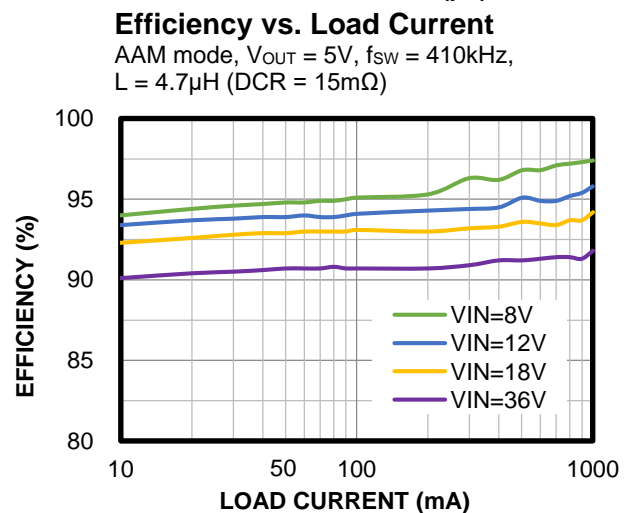
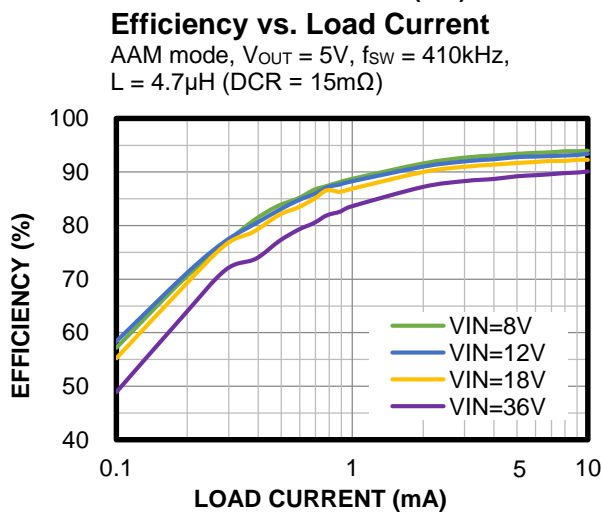
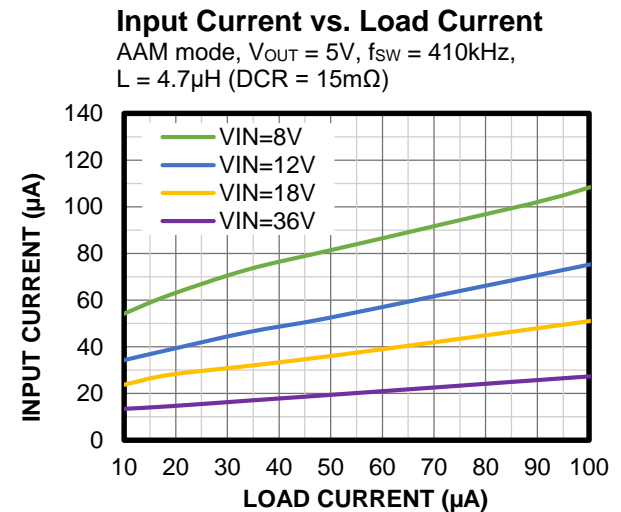
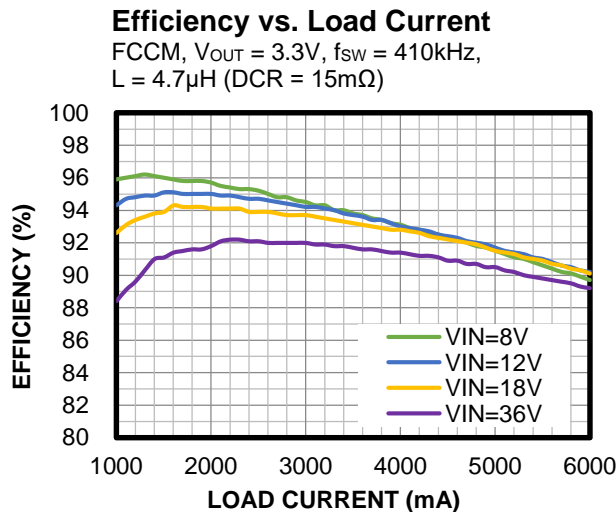
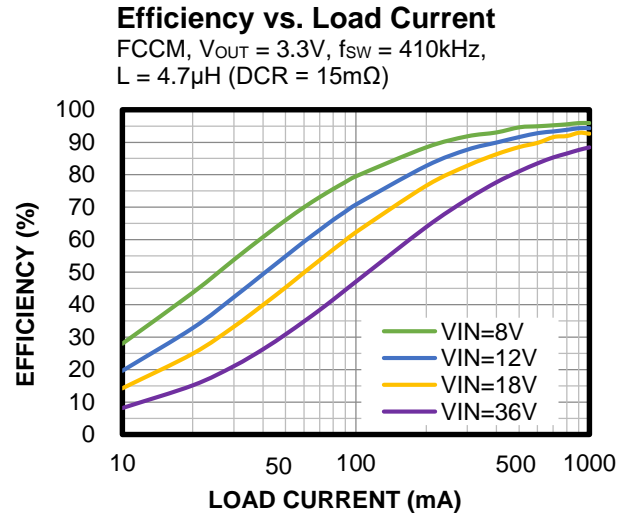
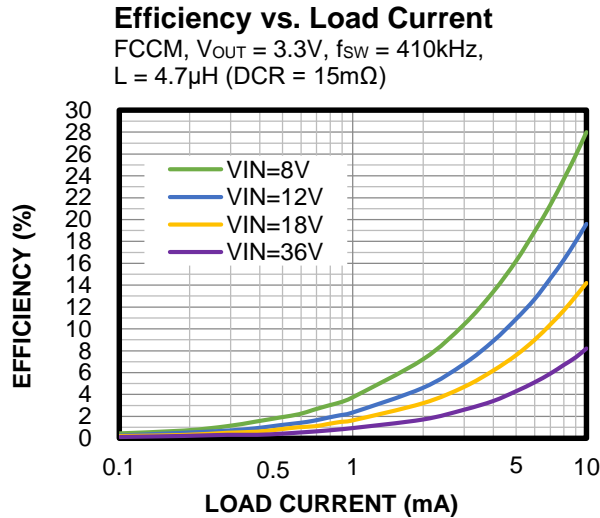
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 1μH, f<sub>sw</sub> = 2.2MHz, AAM mode, T<sub>A</sub> = 25°C, BIAS connected to V<sub>OUT</sub>, unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode, BIAS connected to  $V_{OUT}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



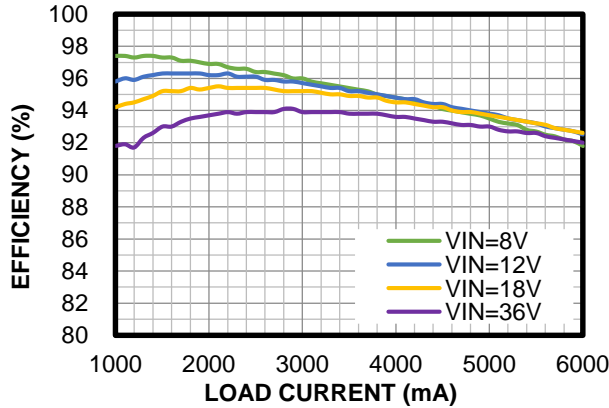


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

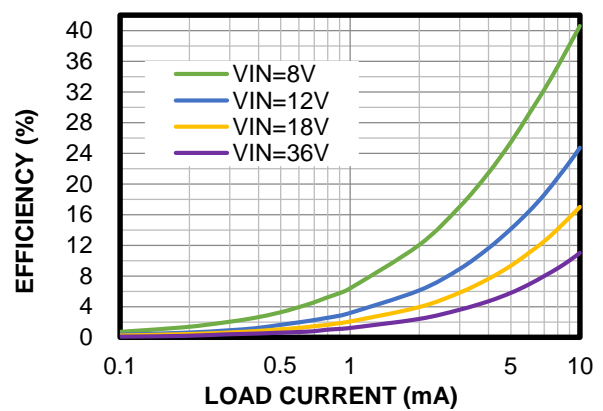
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode, BIAS connected to  $V_{OUT}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Efficiency vs. Load Current**

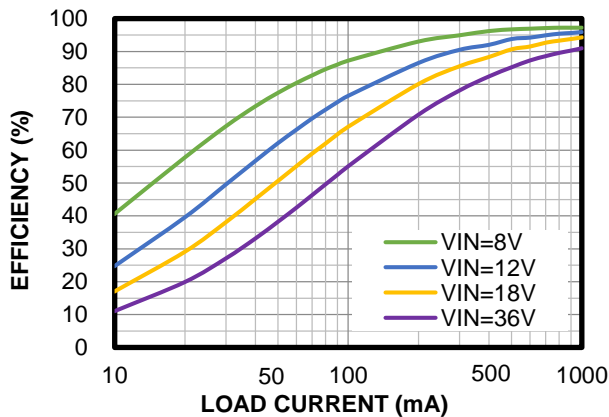
AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR = 15m $\Omega$ )


**Efficiency vs. Load Current**

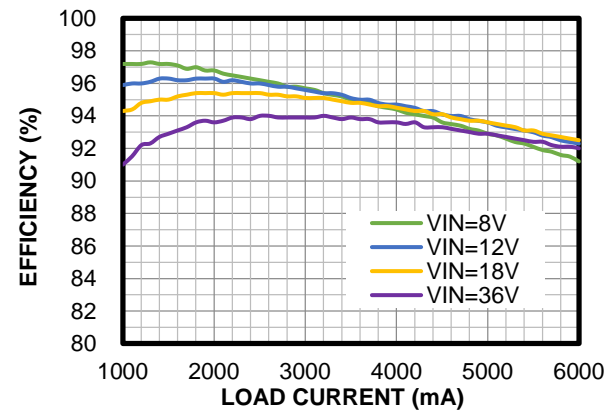
FCCM,  $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR = 15m $\Omega$ )


**Efficiency vs. Load Current**

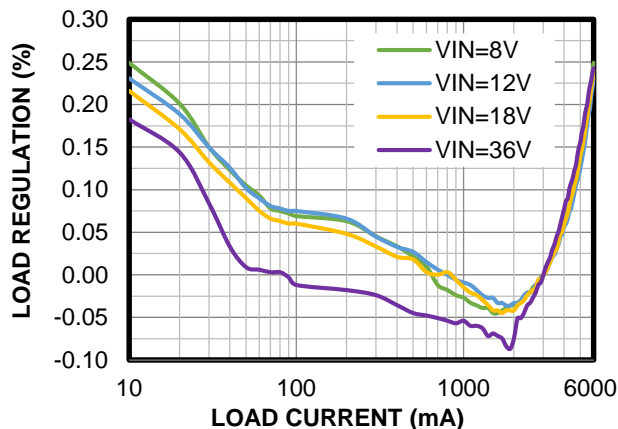
FCCM,  $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR = 15m $\Omega$ )


**Efficiency vs. Load Current**

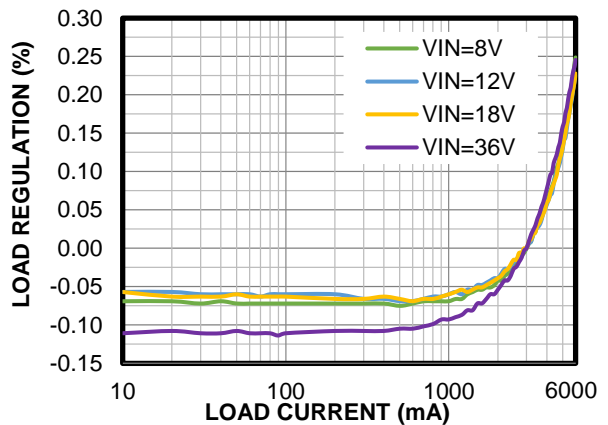
FCCM,  $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR = 15m $\Omega$ )


**Load Regulation**

AAM mode,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )


**Load Regulation**

FCCM,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR = 9.4m $\Omega$ )

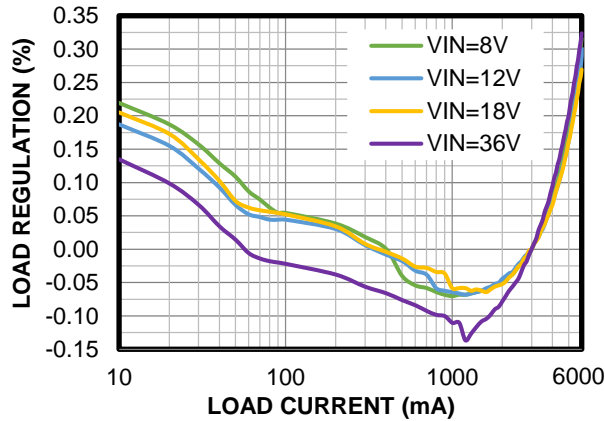


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

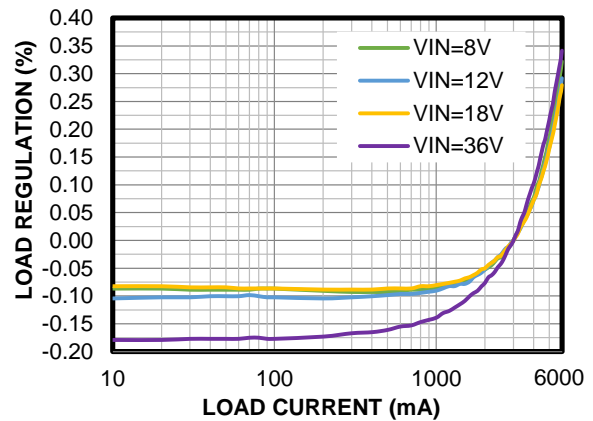
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{sw} = 2.2MHz$ , AAM mode, BIAS connected to  $V_{OUT}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Load Regulation**

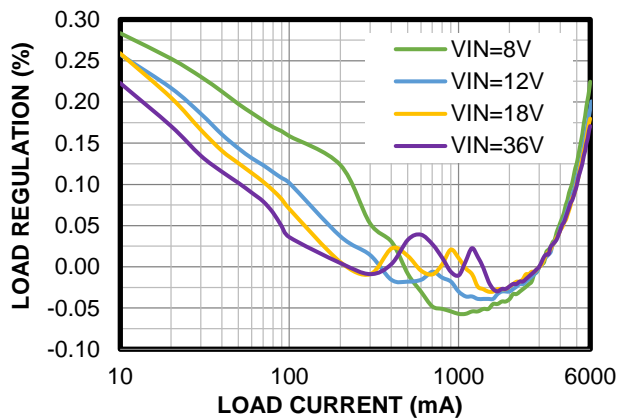
AAM mode,  $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR =  $9.4m\Omega$ )


**Load Regulation**

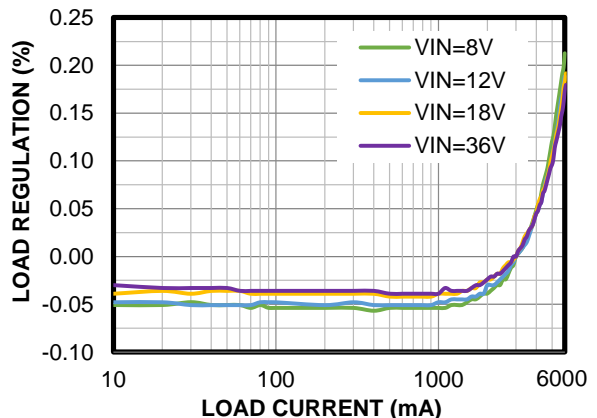
FCCM,  $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$ ,  
 $L = 1\mu H$  (DCR =  $9.4m\Omega$ )


**Load Regulation**

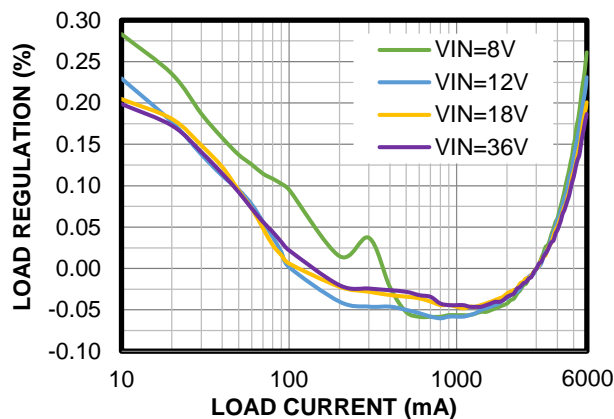
AAM mode,  $V_{OUT} = 3.3V$ ,  $f_{sw} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR =  $15m\Omega$ )


**Load Regulation**

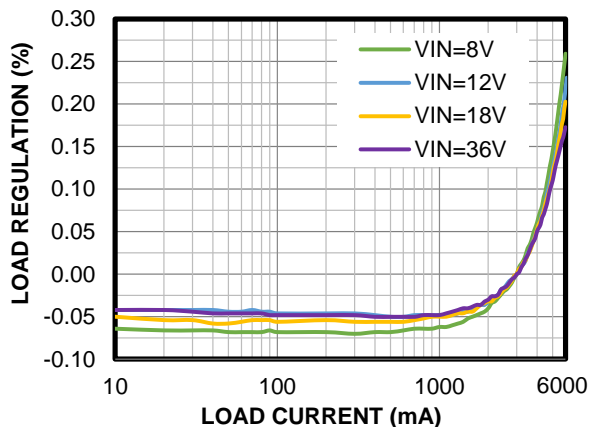
FCCM,  $V_{OUT} = 3.3V$ ,  $f_{sw} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR =  $15m\Omega$ )


**Load Regulation**

AAM mode,  $V_{OUT} = 5V$ ,  $f_{sw} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR =  $15m\Omega$ )

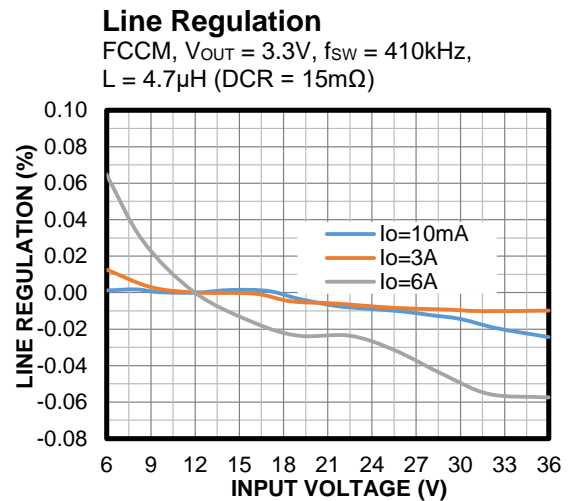
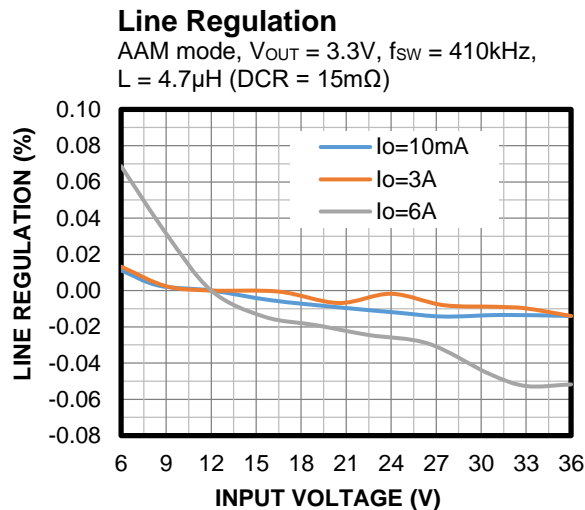
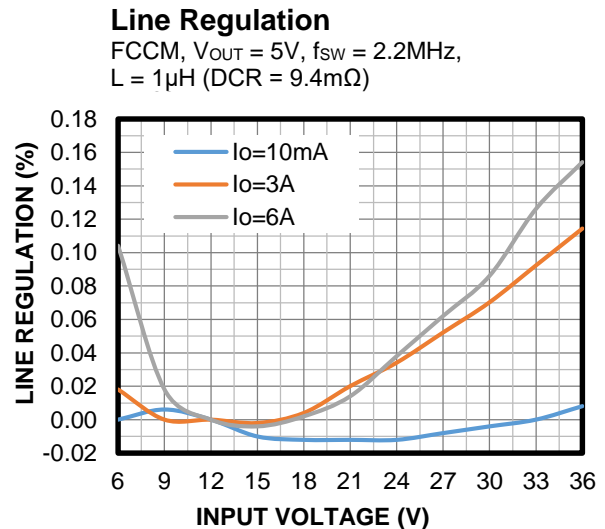
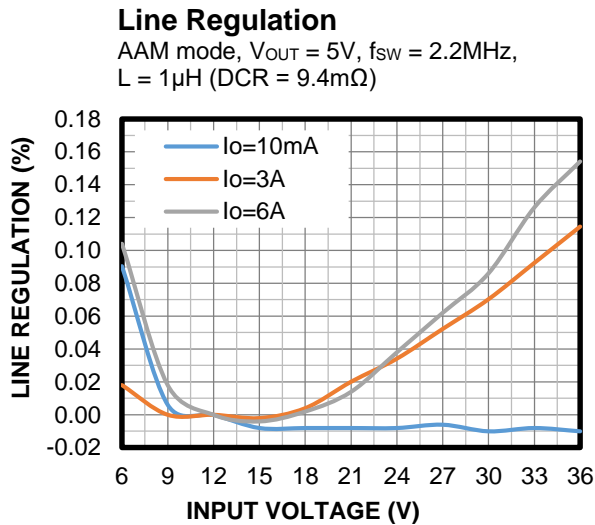
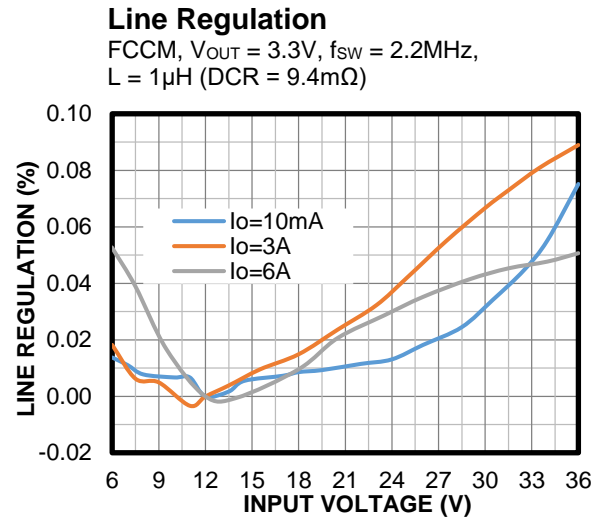
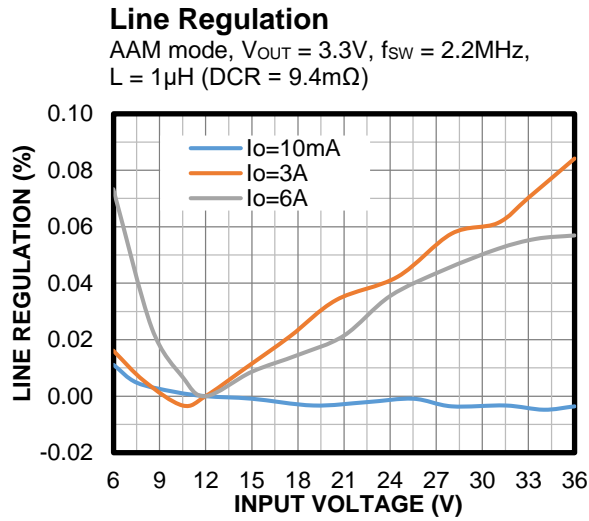

**Load Regulation**

FCCM,  $V_{OUT} = 5V$ ,  $f_{sw} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR =  $15m\Omega$ )



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{sw} = 2.2MHz$ , AAM mode, BIAS connected to  $V_{OUT}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

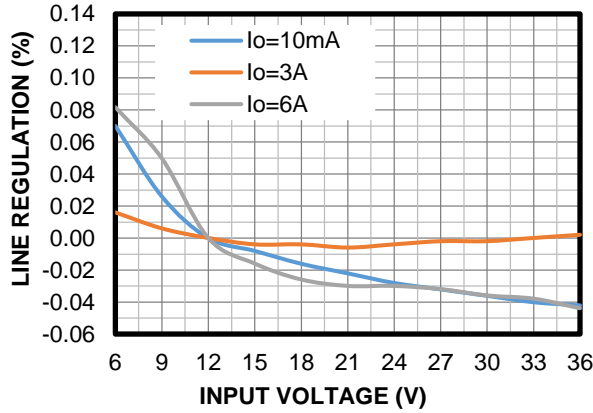


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

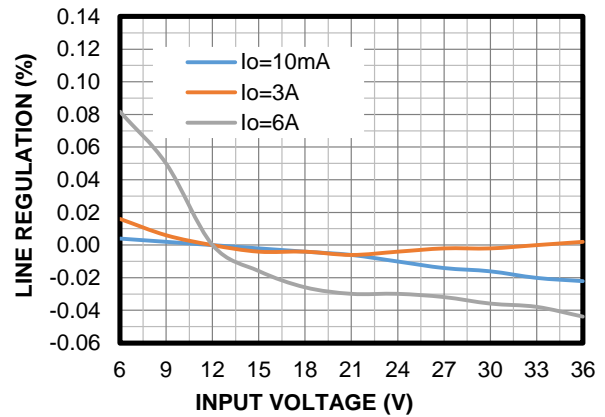
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode, BIAS connected to  $V_{OUT}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Line Regulation**

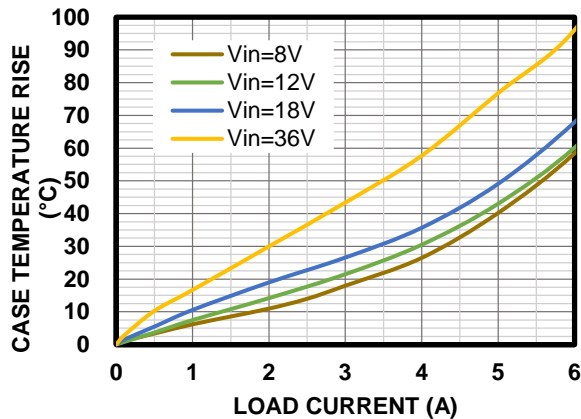
AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR =  $15m\Omega$ )


**Line Regulation**

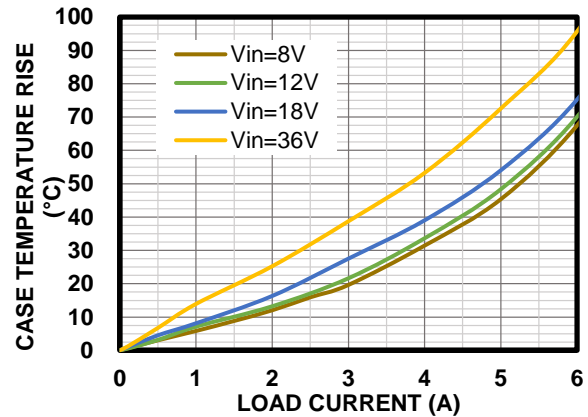
FCCM,  $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  
 $L = 4.7\mu H$  (DCR =  $15m\Omega$ )


**Case Temperature Rise**

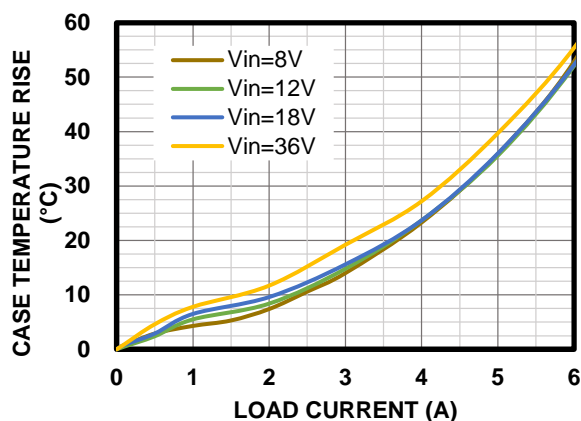
$V_{OUT} = 3.3V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 1\mu H$   
 (DCR =  $9.4m\Omega$ )


**Case Temperature Rise**

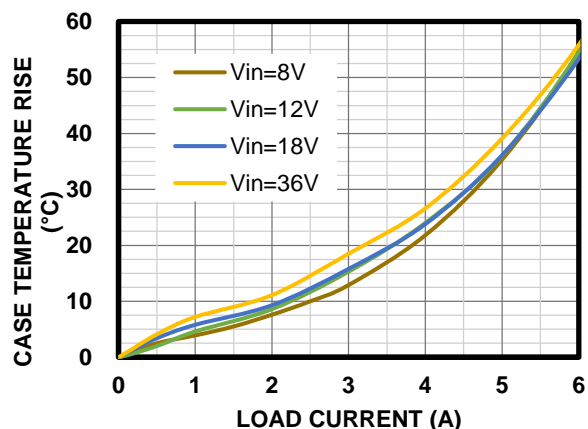
$V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 1\mu H$   
 (DCR =  $9.4m\Omega$ )


**Case Temperature Rise**

$V_{OUT} = 3.3V$ ,  $f_{SW} = 410kHz$ ,  $L = 4.7\mu H$   
 (DCR =  $15m\Omega$ )

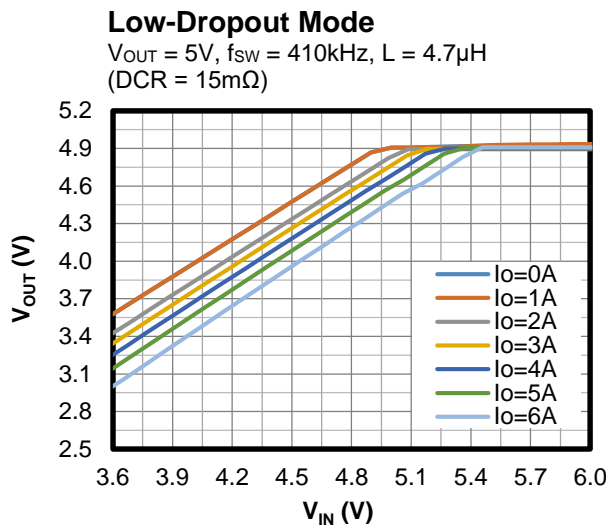
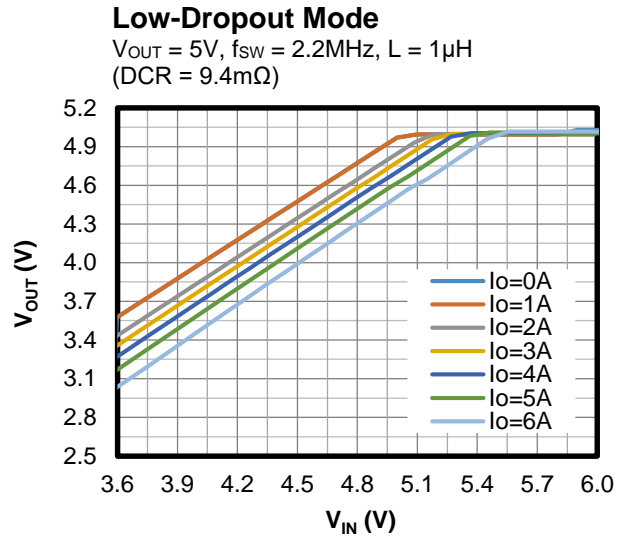
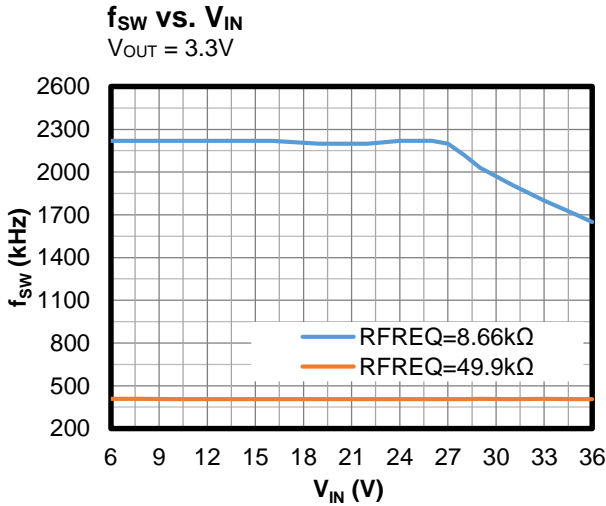

**Case Temperature Rise**

$V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  $L = 4.7\mu H$   
 (DCR =  $15m\Omega$ )



## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

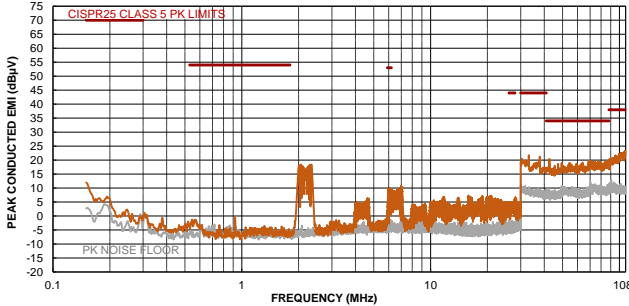
V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 1μH, f<sub>sw</sub> = 2.2MHz, AAM mode, BIAS connected to V<sub>OUT</sub>, T<sub>A</sub> = 25°C, unless otherwise noted.



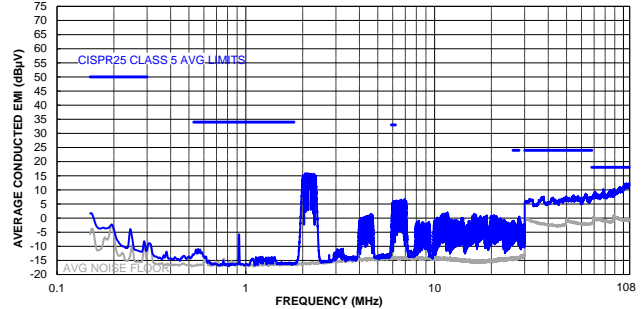
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 6A$ ,  $L = 1\mu H$  <sup>(11)</sup>,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted. <sup>(12)</sup>

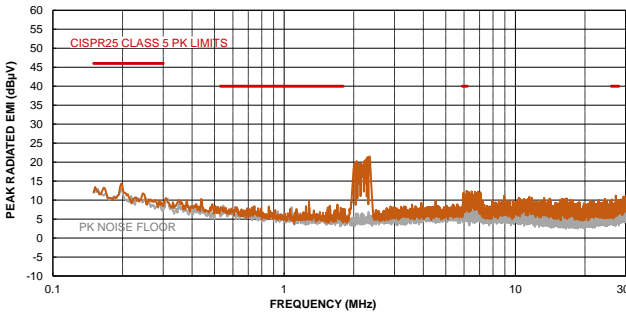
**CISPR25 Class 5 Peak Conducted Emissions**  
150kHz to 108MHz



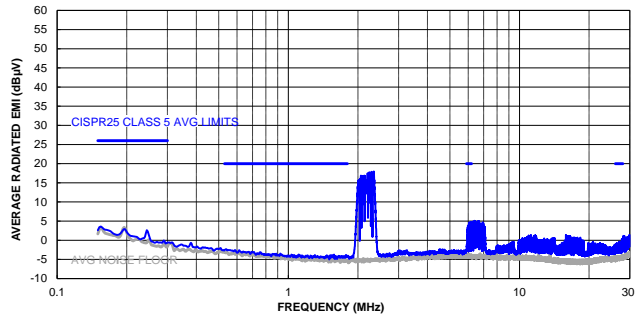
**CISPR25 Class 5 Average Conducted Emissions**  
150kHz to 108MHz



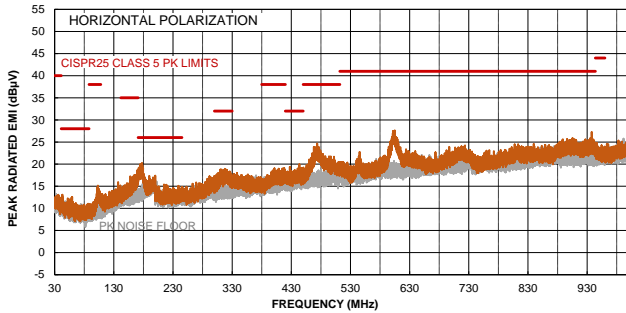
**CISPR25 Class 5 Peak Radiated Emissions**  
150kHz to 30MHz



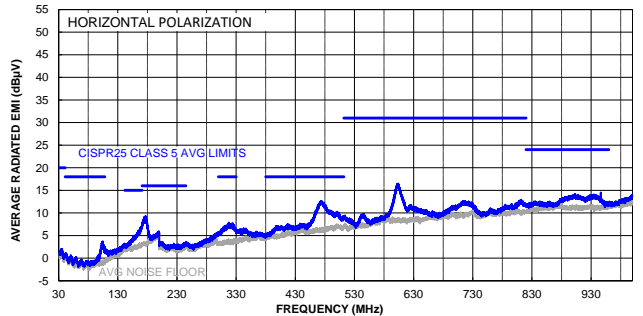
**CISPR25 Class 5 Average Radiated Emissions**  
150kHz to 30MHz



**CISPR25 Class 5 Peak Radiated Emissions**  
Horizontal, 30MHz to 1GHz



**CISPR25 Class 5 Average Radiated Emissions**  
Horizontal, 30MHz to 1GHz

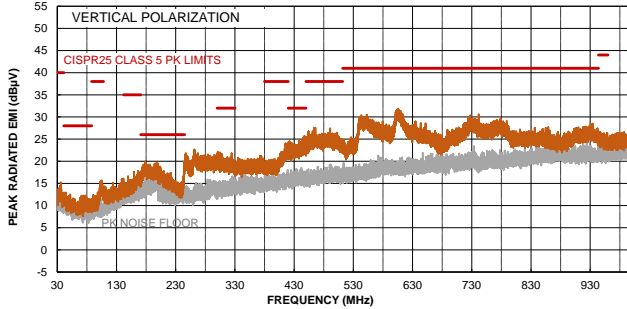


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, I<sub>OUT</sub> = 6A, L = 1μH<sup>(11)</sup>, f<sub>SW</sub> = 2.2MHz, T<sub>A</sub> = 25°C, unless otherwise noted.<sup>(12)</sup>

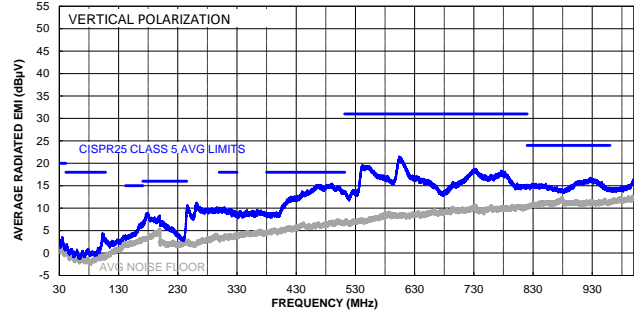
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



#### Notes:

11) Inductor part number: XEL4020-102MEB; DCR = 14.6mΩ.

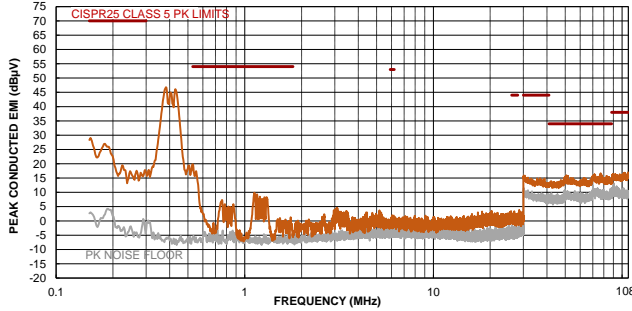
12) The EMC test results are based on the application circuit with EMI filters (see Figure 17 on page 47).

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 6A$ ,  $L = 4.7\mu H$  <sup>(13)</sup>,  $f_{SW} = 410kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted. <sup>(14)</sup>

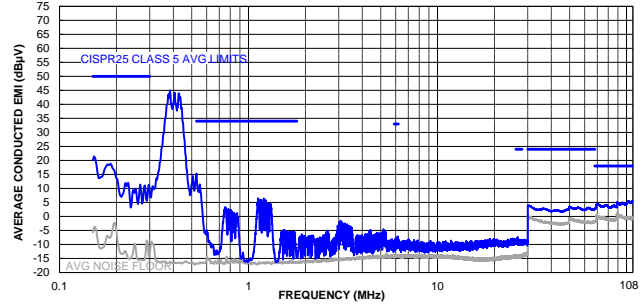
### CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



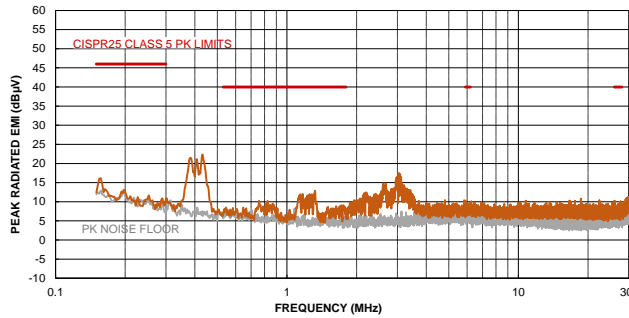
### CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



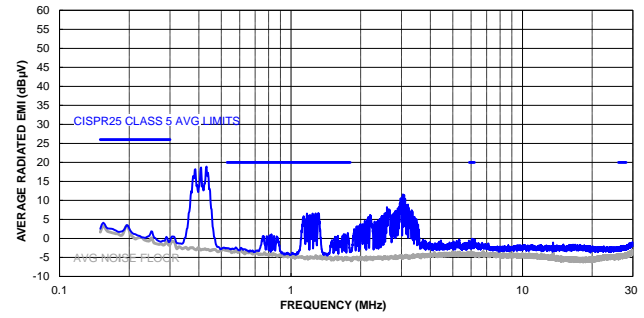
### CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



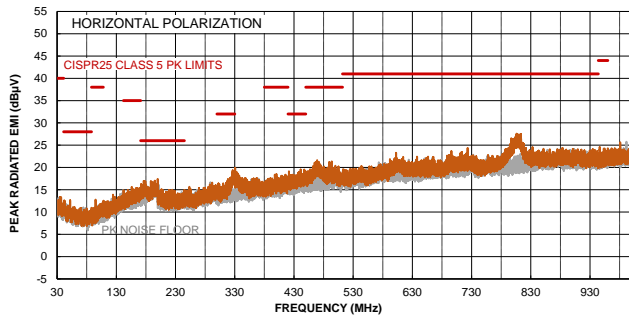
### CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



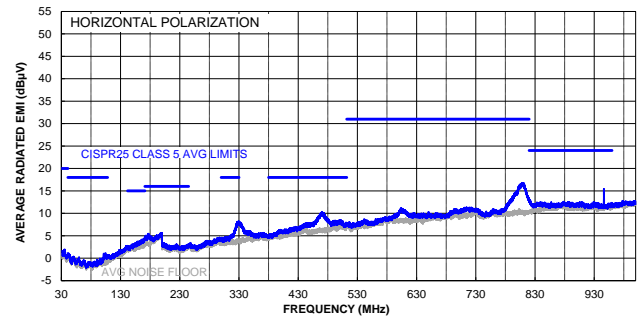
### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



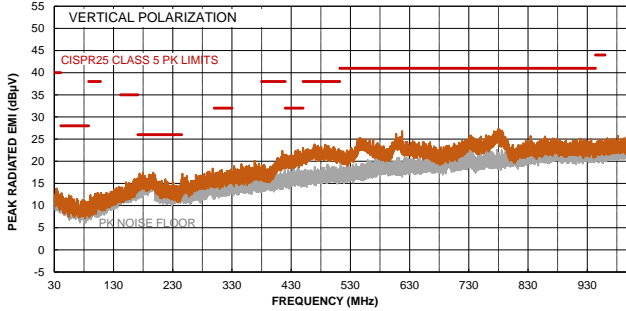


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, I<sub>OUT</sub> = 6A, L = 4.7μH<sup>(13)</sup>, f<sub>SW</sub> = 410kHz, T<sub>A</sub> = 25°C, unless otherwise noted.<sup>(14)</sup>

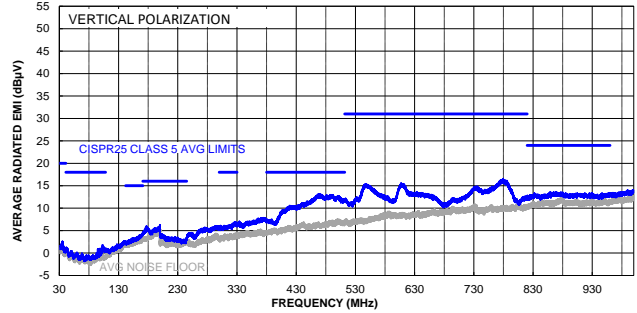
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz

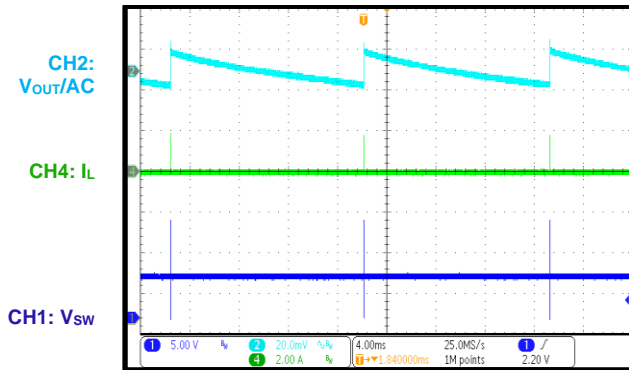
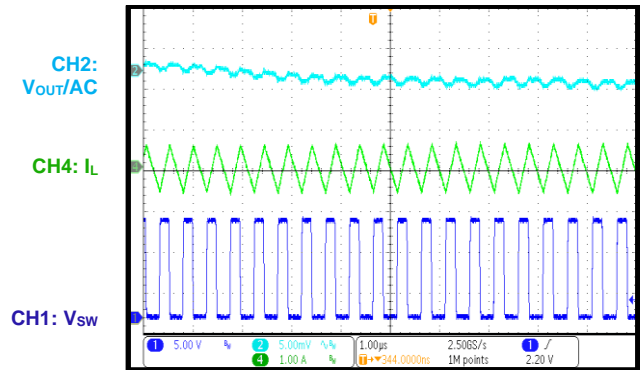
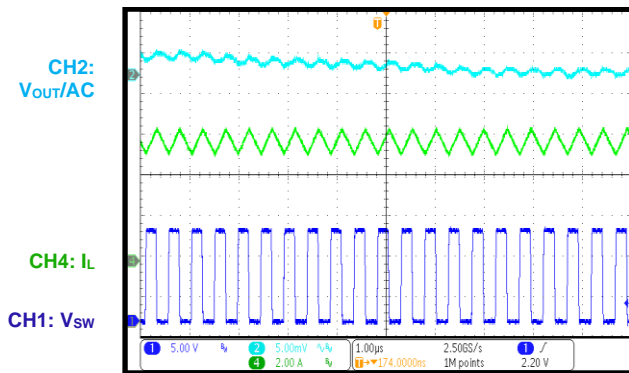
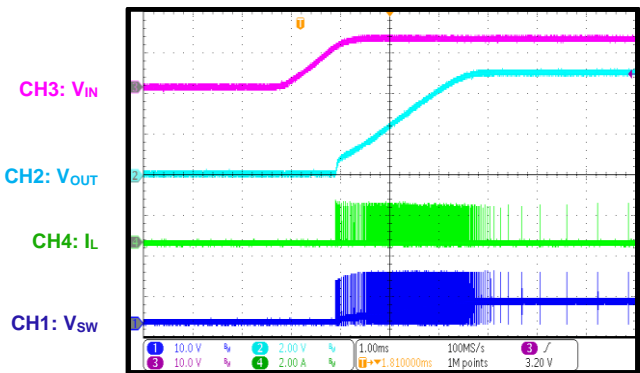
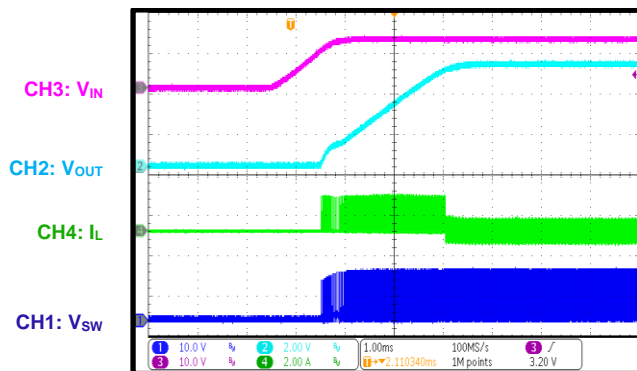
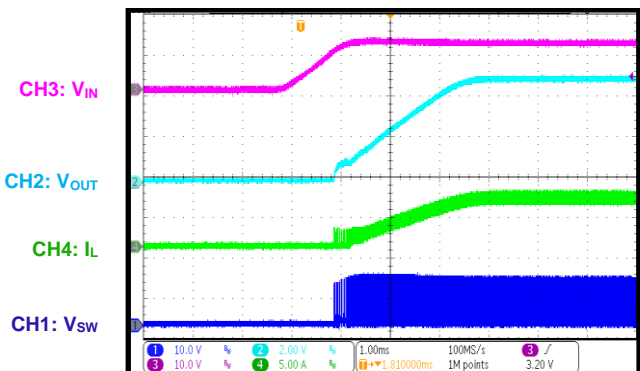


#### Notes:

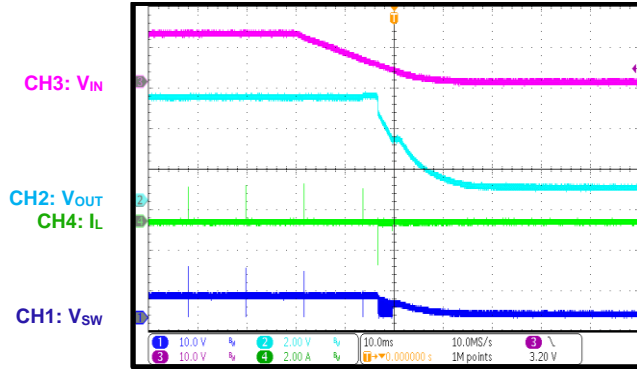
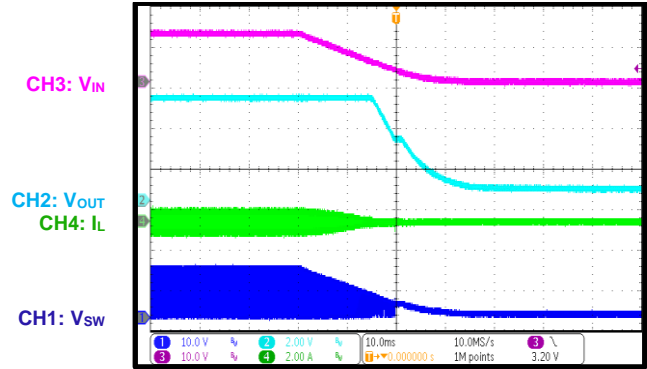
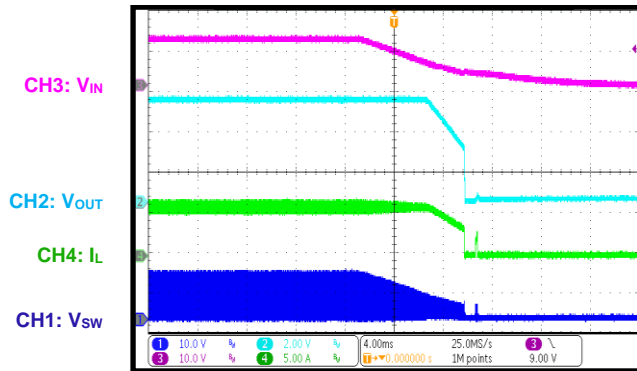
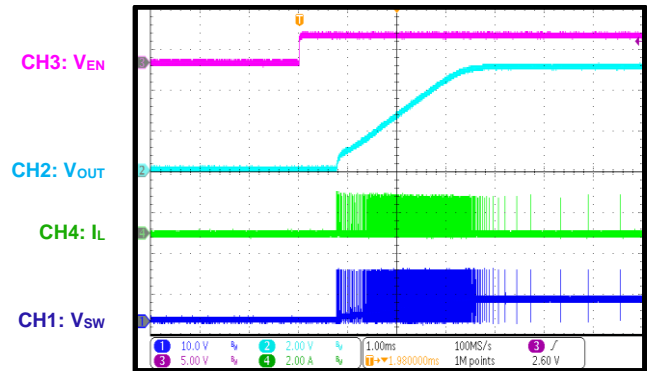
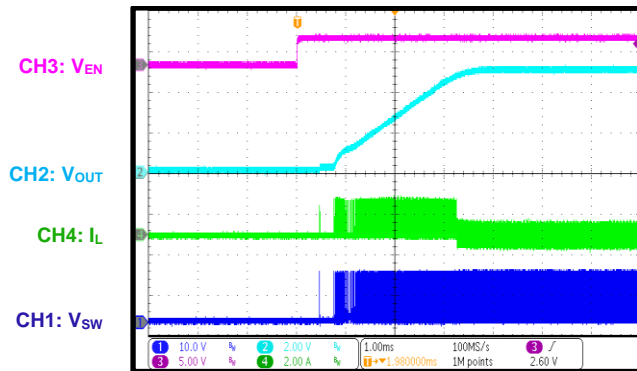
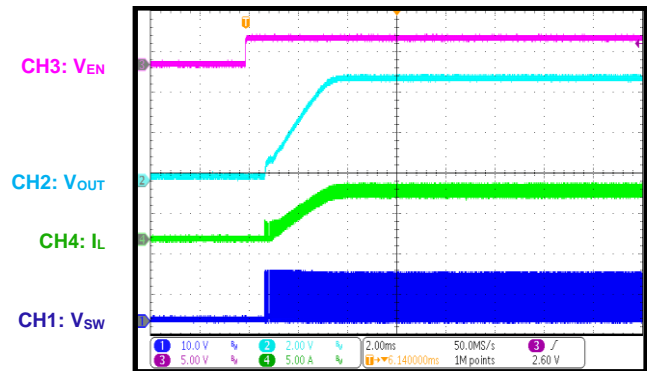
13) Inductor part number: XEL6060-472MEB/C; DCR = 15.02mΩ.

14) The EMC test results are based on the application circuit with EMI filters (see Figure 18 on page 48).

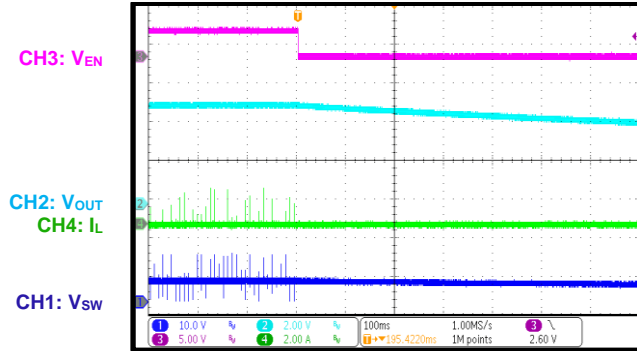
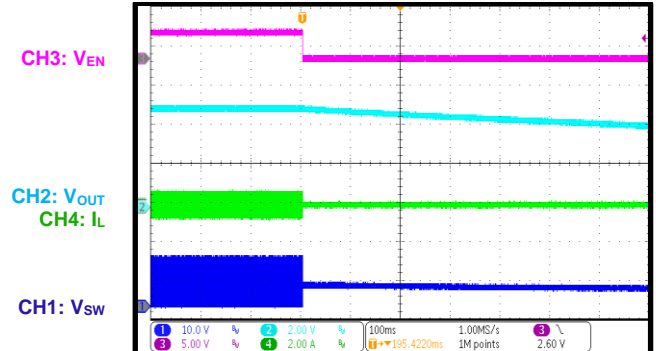
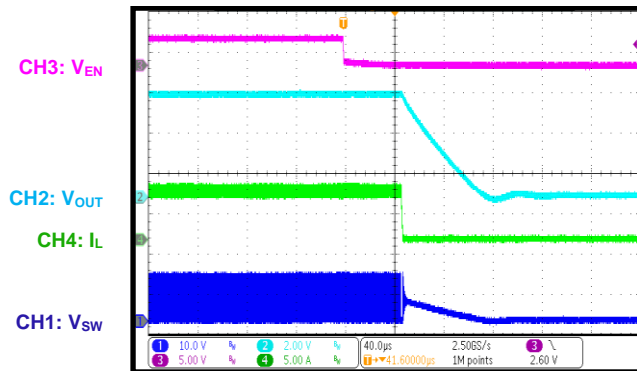
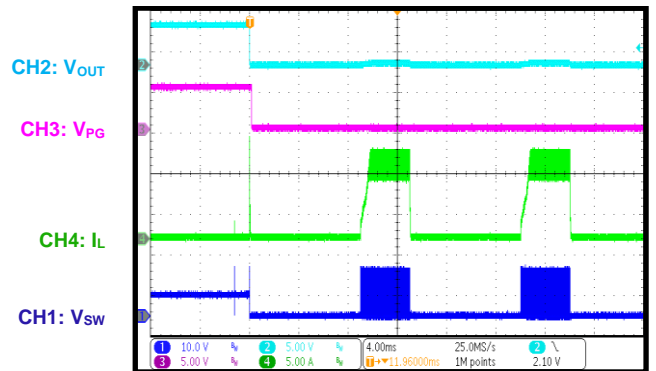
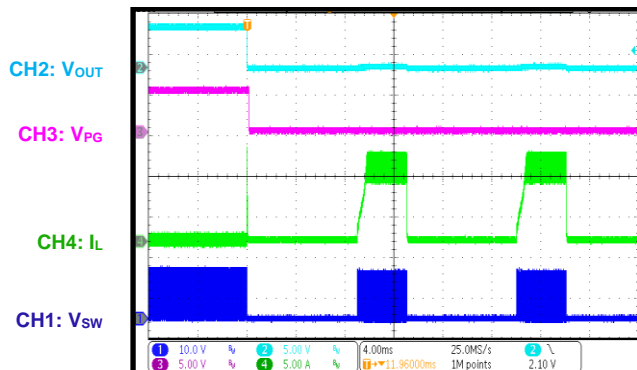
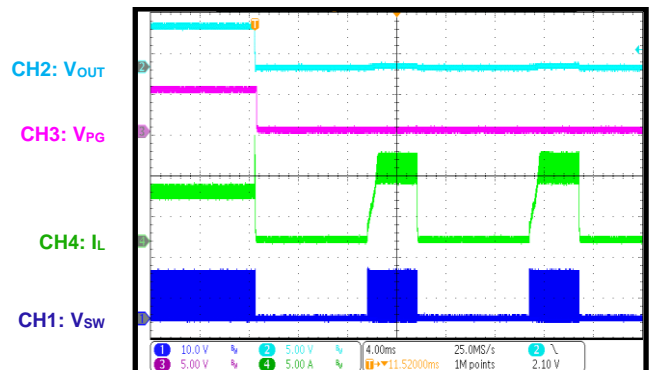
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

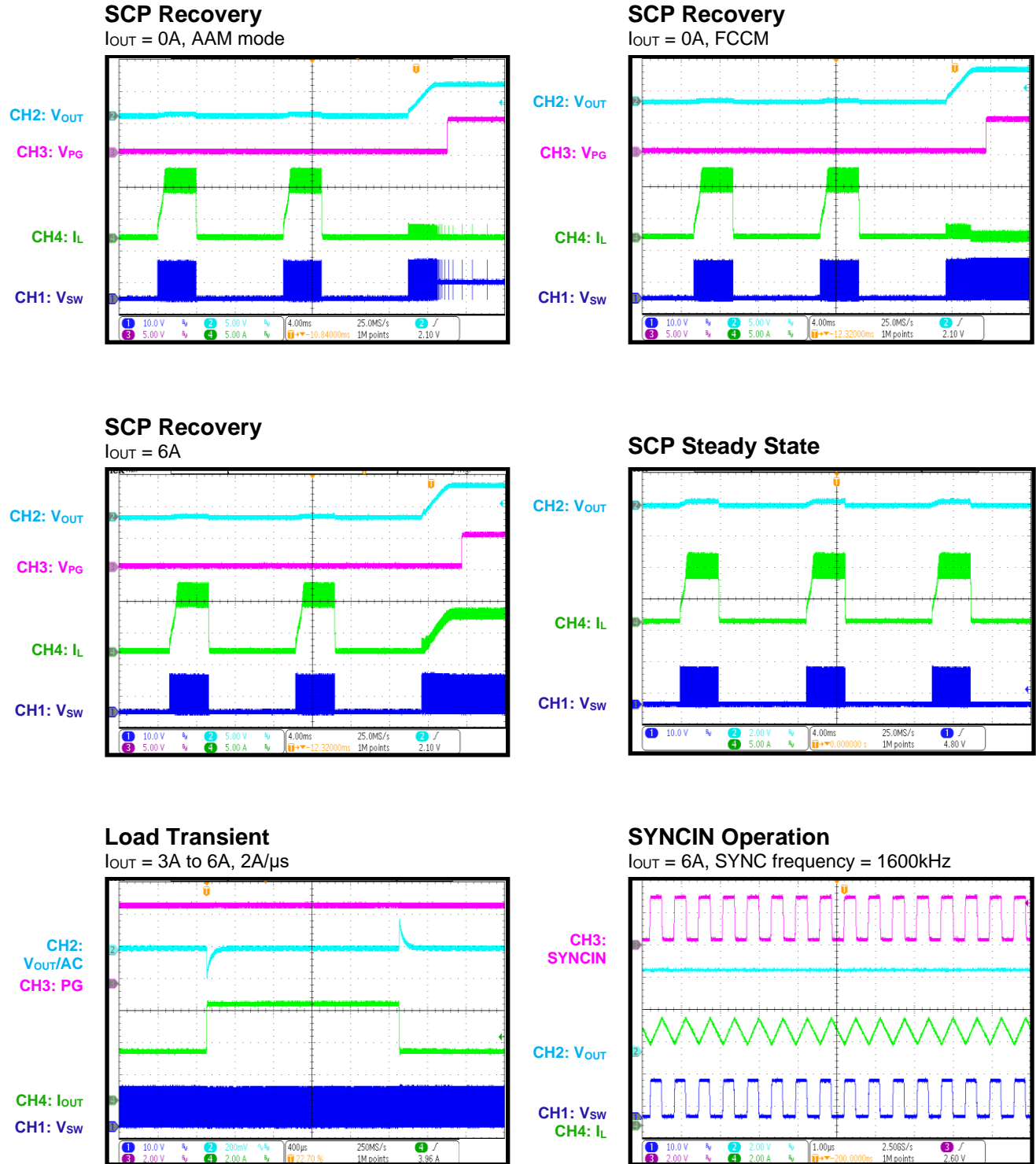
**Steady State**
 $I_{OUT} = 0A$ , AAM mode

**Steady State**
 $I_{OUT} = 0A$ , FCCM

**Steady State**
 $I_{OUT} = 6A$ 

**Start-Up through  $V_{IN}$** 
 $I_{OUT} = 0A$ , AAM mode

**Start-Up through  $V_{IN}$** 
 $I_{OUT} = 0A$ , FCCM

**Start-Up through  $V_{IN}$** 
 $I_{OUT} = 6A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

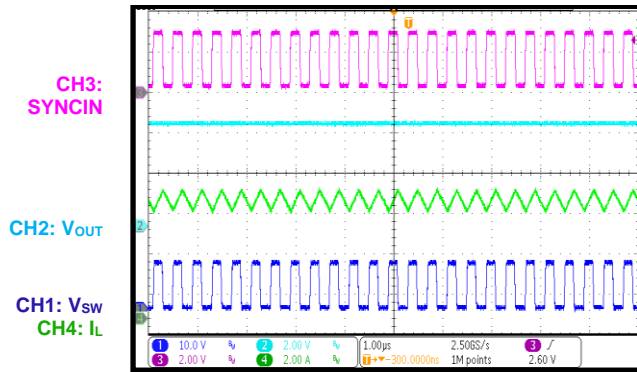
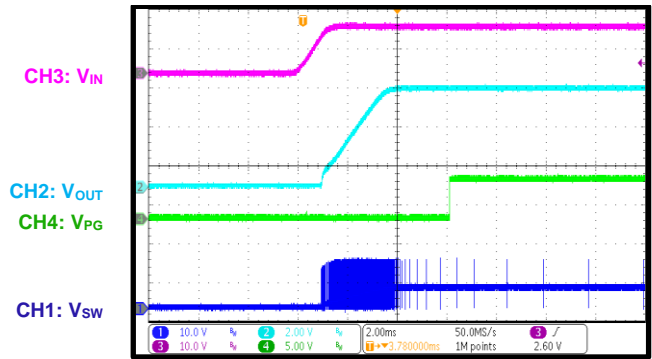
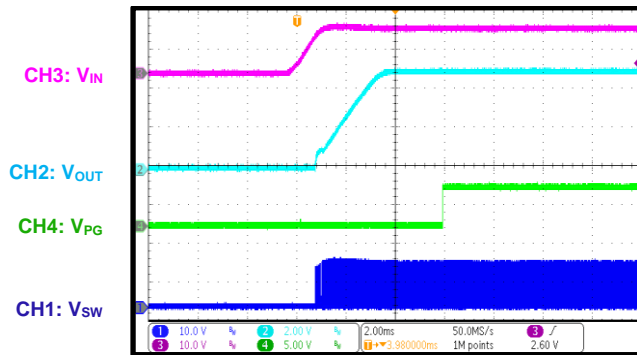
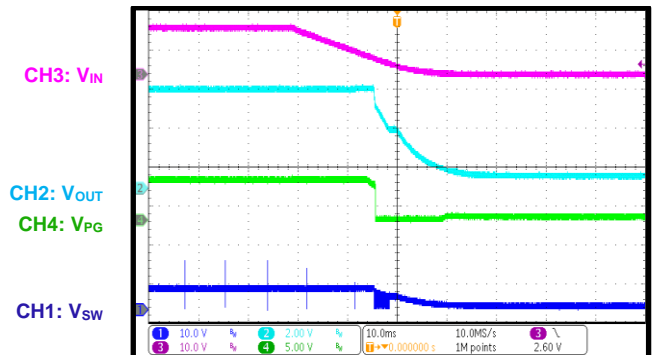
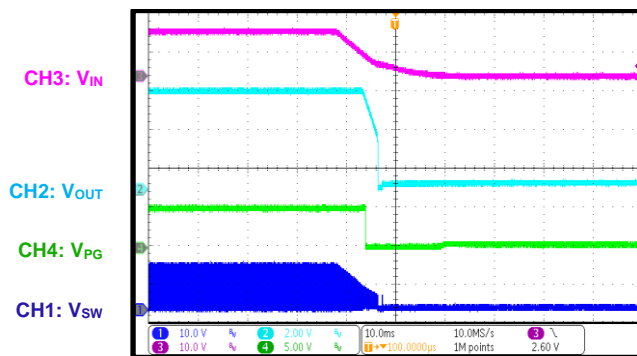
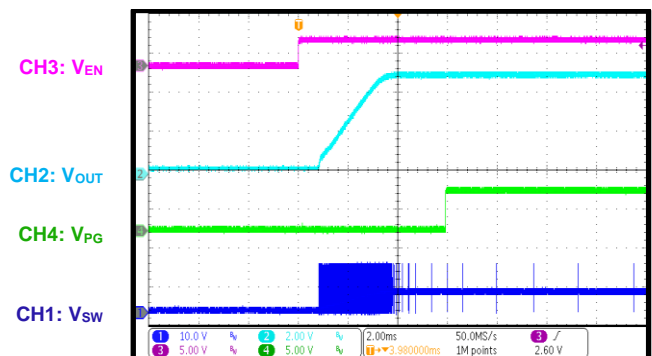
**Shutdown through VIN**
 $I_{OUT} = 0A$ , AAM mode

**Shutdown through VIN**
 $I_{OUT} = 0A$ , FCCM

**Shutdown through VIN**
 $I_{OUT} = 6A$ 

**Start-Up through EN**
 $I_{OUT} = 0A$ , AAM mode

**Start-Up through EN**
 $I_{OUT} = 0A$ , FCCM

**Start-Up through EN**
 $I_{OUT} = 6A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^{\circ}C$ , unless otherwise noted.

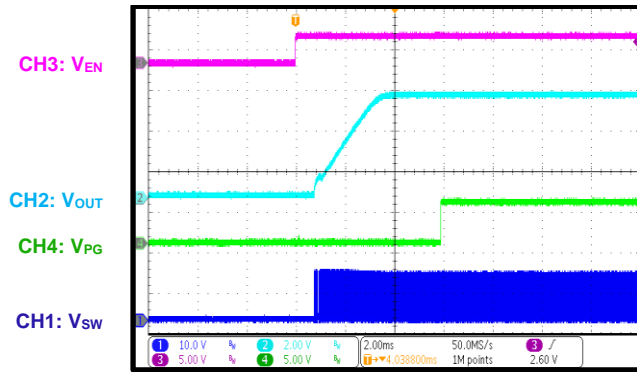
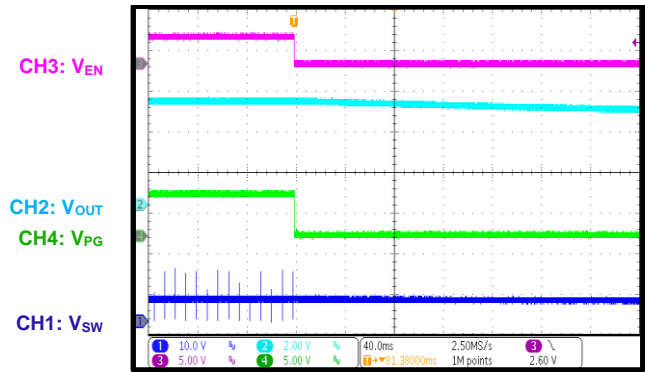
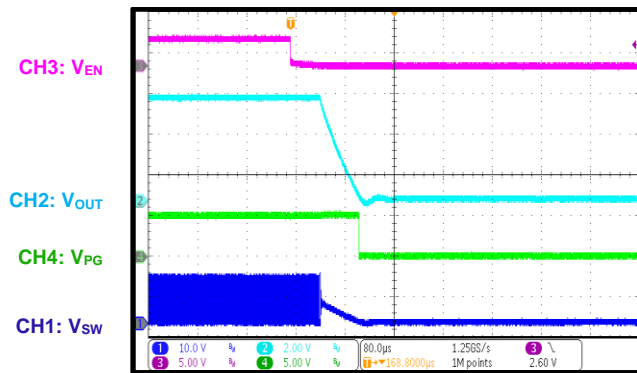
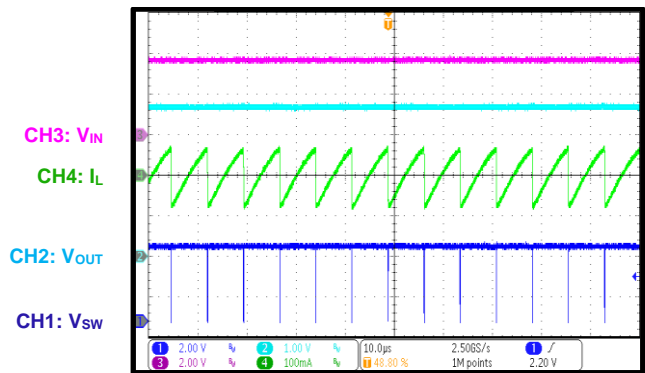
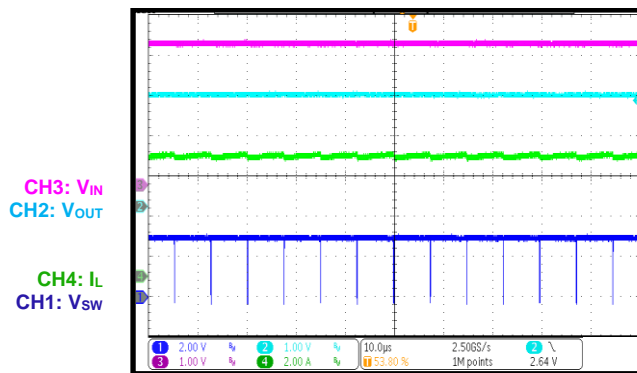
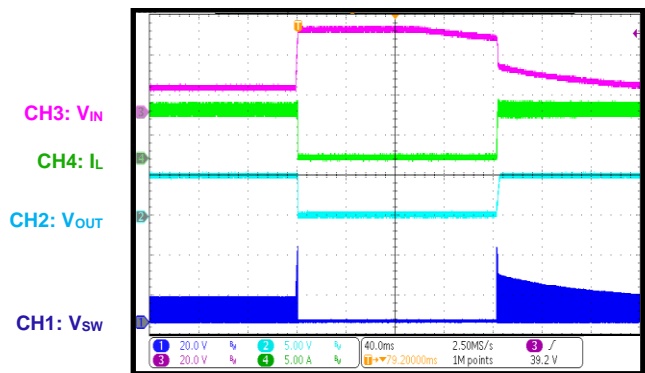
**Shutdown through EN**
 $I_{OUT} = 0A$ , AAM mode

**Shutdown through EN**
 $I_{OUT} = 0A$ , FCCM

**Shutdown through EN**
 $I_{OUT} = 6A$ 

**SCP Entry**
 $I_{OUT} = 0A$ , AAM mode

**SCP Entry**
 $I_{OUT} = 0A$ , FCCM

**SCP Entry**
 $I_{OUT} = 6A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.


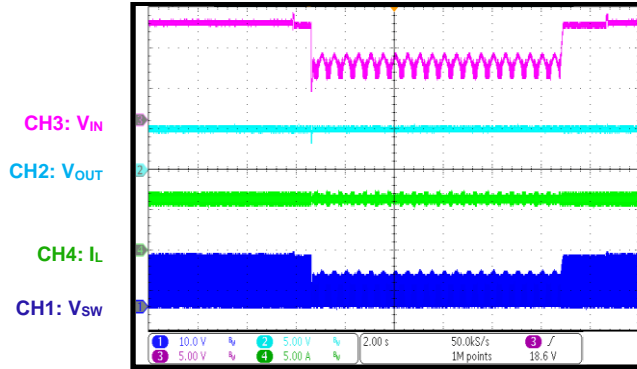
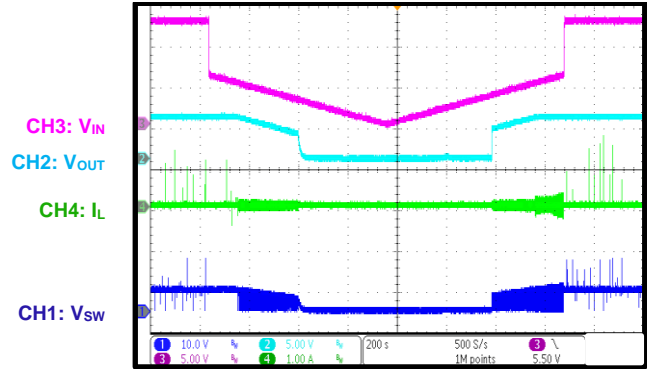
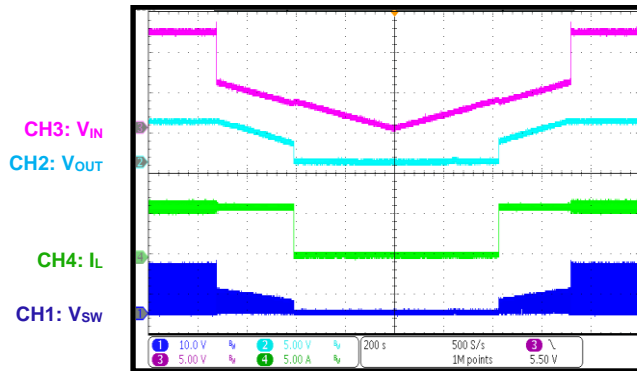
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

**SYNCIN Operation**
 $I_{OUT} = 6A$ , SYNC frequency = 2500kHz

**PG in Start-Up through VIN**
 $I_{OUT} = 0A$ , AAM mode

**PG in Start-Up through VIN**
 $I_{OUT} = 6A$ 

**PG in Shutdown through VIN**
 $I_{OUT} = 0A$ , AAM mode

**PG in Shutdown through VIN**
 $I_{OUT} = 6A$ 

**PG in Start-Up through EN**
 $I_{OUT} = 0A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

**PG in Start-Up through EN**
 $I_{OUT} = 6A$ 

**PG in Shutdown through EN**
 $I_{OUT} = 0A$ 

**PG in Shutdown through EN**
 $I_{OUT} = 6A$ 

**Low-Dropout Mode**
 $V_{IN} = 3.7V$ ,  $I_{OUT} = 0A$ 

**Low-Dropout Mode**
 $V_{IN} = 3.7V$ ,  $I_{OUT} = 6A$ 

**Load Dump**
 $V_{IN} = 12V$  to  $42V$ ,  $I_{OUT} = 6A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 1\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

**Cold Crank**
 $V_{IN} = 12V$  to 3.3V to 5V,  $I_{OUT} = 6A$ 

 **$V_{IN}$  Ramping Down and Up**
 $I_{OUT} = 0A$ , AAM mode

 **$V_{IN}$  Ramping Down and Up**
 $I_{OUT} = 6A$ 




## FUNCTIONAL BLOCK DIAGRAM

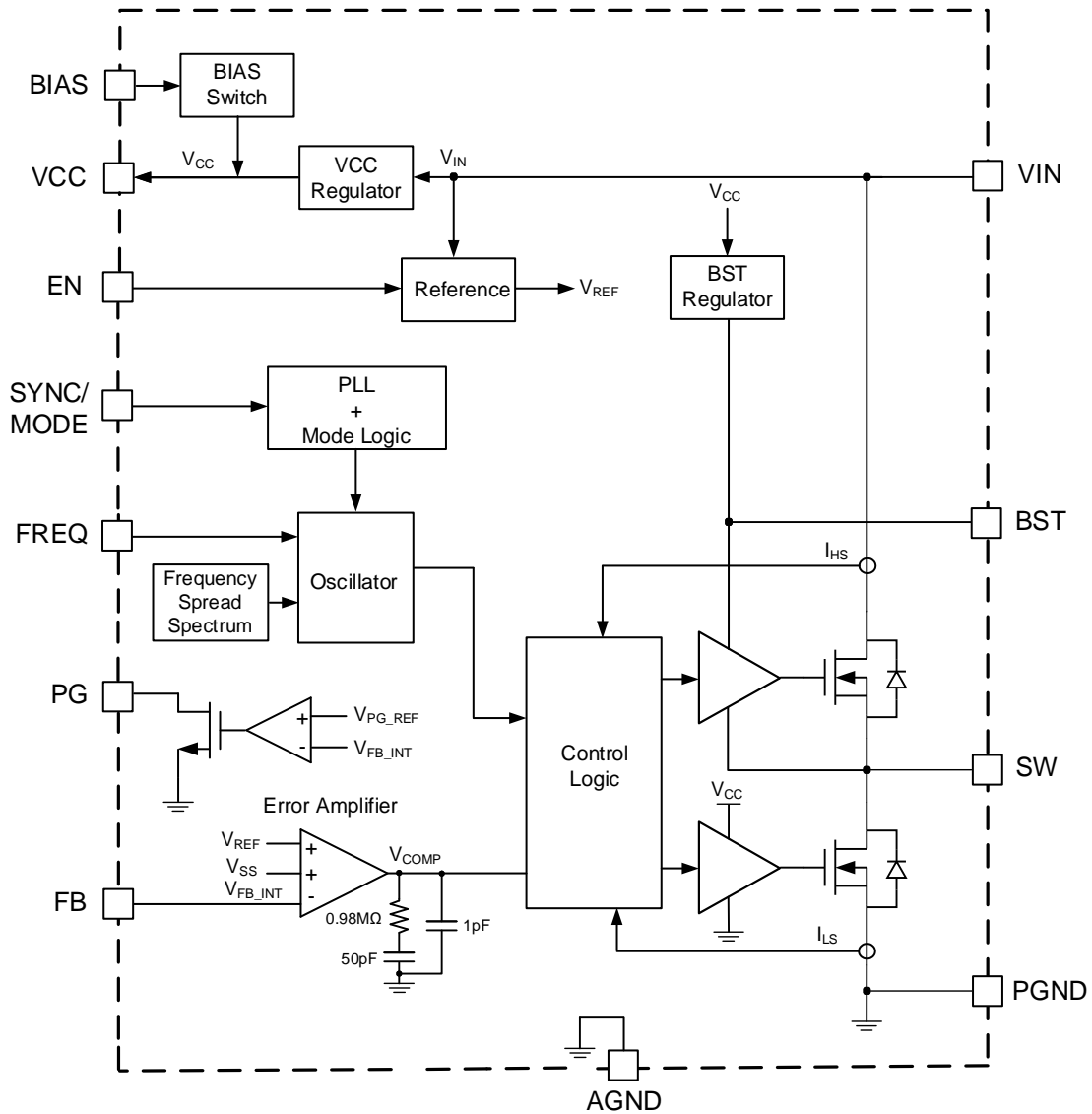
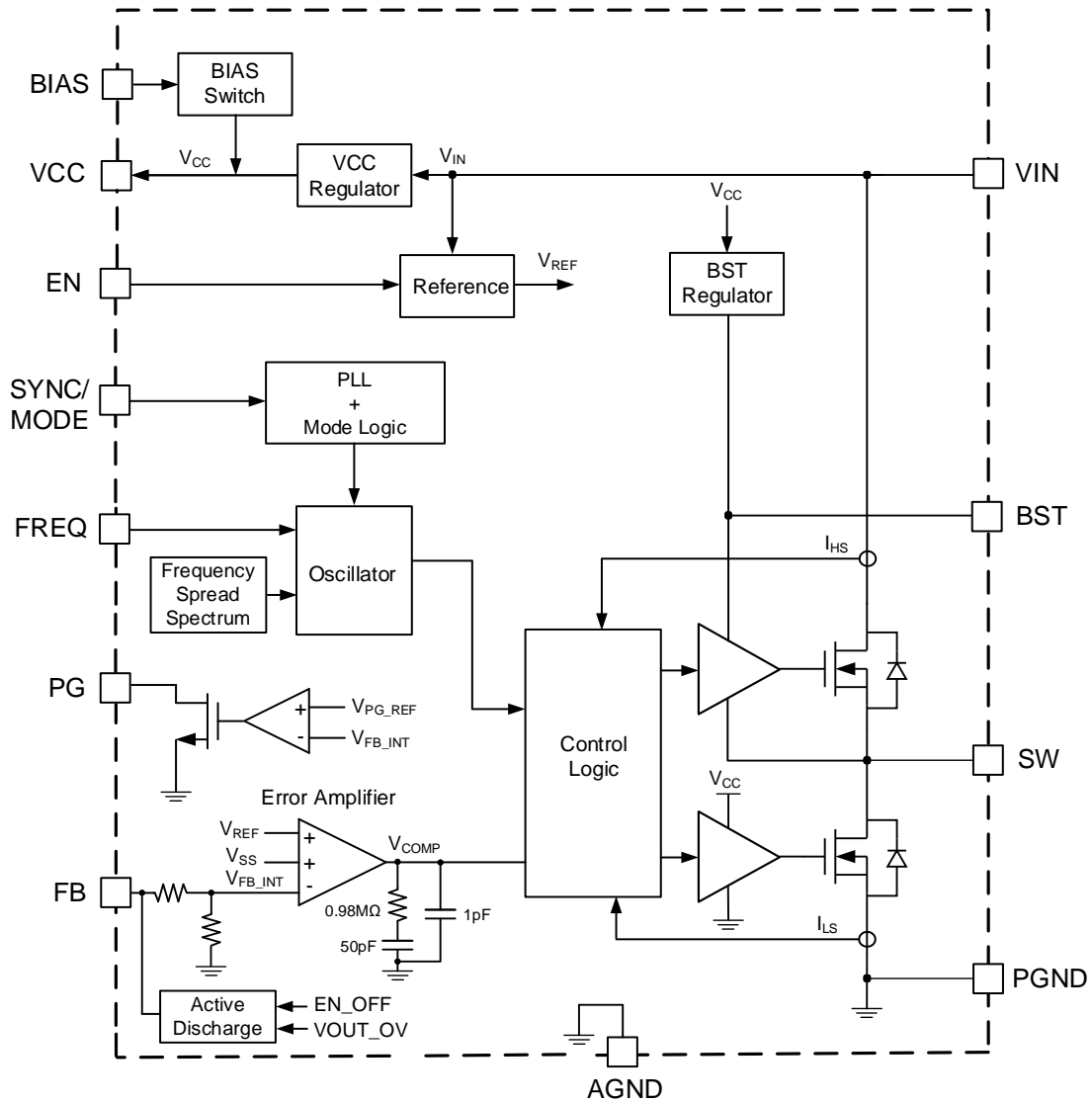


Figure 3: Functional Block Diagram (Adjustable Output)

**FUNCTIONAL BLOCK DIAGRAM (continued)**

**Figure 4: Functional Block Diagram (Fixed Output)**

## OPERATION

The MPQ4326/4326J is a synchronous, step-down switching regulator with an integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). It provides up to 6A of highly efficient output current ( $I_{OUT}$ ) with peak current mode control.

The MPQ4326/4326J features a wide input voltage ( $V_{IN}$ ) range, configurable 200kHz to 2.5MHz switching frequency ( $f_{SW}$ ), internal soft start (SS), and precise current limiting. The MPQ4326/4326J's very low operational quiescent current ( $I_Q$ ) makes it well-suited for battery-powered applications.

### Pulse-Width Modulation (PWM) Control

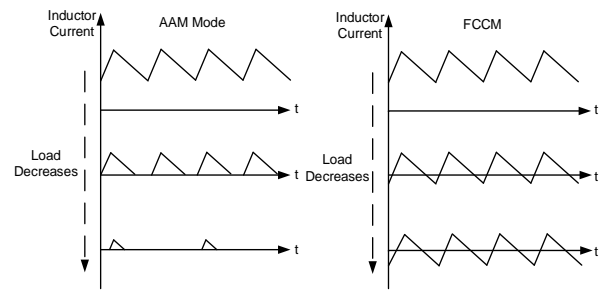
At moderate to high output currents, the MPQ4326/4326J operates with fixed-frequency, peak current mode control to regulate the output voltage ( $V_{OUT}$ ). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage ( $V_{COMP}$ ).

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts or until the inductor current ( $I_L$ ) drops below the zero-current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time ( $t_{OFF\_MIN}$ ) before the next cycle starts.

If the current in the HS-FET cannot reach the value set by  $V_{COMP}$  within one PWM period, then the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off until current reaches the value set by  $V_{COMP}$ , or once its 7 $\mu$ s maximum on time ( $t_{ON\_MAX}$ ) is reached. This mode extends the duty cycle, which achieves low dropout when  $V_{IN} \approx V_{OUT}$ .

### Mode Selection and Light-Load Operation

The MPQ4326/4326J provides forced continuous conduction mode (FCCM), advanced asynchronous modulation (AAM) mode, and on the fly mode selection (see Figure 5).



**Figure 5: AAM Mode and FCCM**

Under light-load conditions, the MPQ4326/4326J can work in two different modes by setting the state of the SYNC/MODE pin.

If SYNC/MODE is pulled above 1.4V or an external clock is used, then the MPQ4326/4326J enters FCCM. In FCCM, the device works with a fixed frequency from no-load to full-load conditions. The advantage of FCCM is the constant frequency and lower output ripple at light loads.

If SYNC/MODE is pulled below 0.4V, then the MPQ4326/4326J enters AAM mode, which optimizes efficiency under light-load and no-load conditions.

The MPQ4326/4326J enters asynchronous operation as  $I_L$  approaches 0A under light-load conditions. If the load decreases further,  $V_{COMP}$  drops to its set value, and the device enters AAM mode. In AAM mode, the internal clock resets once  $V_{COMP}$  reaches its set value. The crossover time is used as a benchmark for the next clock. If the load increases and  $V_{COMP}$  exceeds its set value, the device operates in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) with a constant  $f_{SW}$ .

### Error Amplifier (EA)

The error amplifier (EA) compares the FB pin voltage ( $V_{FB}$ ) with the internal reference ( $V_{REF}$ ) (typically 0.8V) and outputs a current proportional to the difference between the two voltages. This current charges the compensation network to form  $V_{COMP}$ , which controls the power MOSFET's duty cycle.

During normal operation, the minimum  $V_{COMP}$  is clamped to 0.9V, and the maximum  $V_{COMP}$  is clamped to 2V. If the IC shuts down,  $V_{COMP}$  is internally pulled down to ground.

### Frequency Spread Spectrum (FSS)

The MPQ4326/4326J employs a 7.5kHz modulation frequency with a 128-step triangular profile to spread the internal oscillator frequency across a 20% ( $\pm 10\%$ ) window. The steps vary with the set oscillator frequency to ensure that the exact  $f_{SW}$  steps cycle by cycle (see Figure 6).

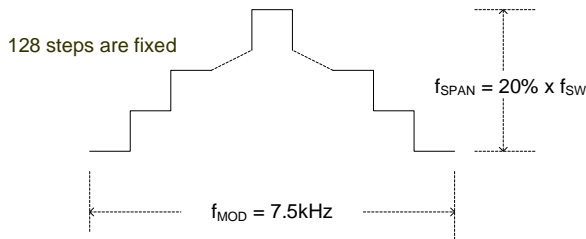


Figure 6: Frequency Spread Spectrum

Sidebands are created by modulating  $f_{SW}$  via the triangle modulation waveform. The emission power of the fundamental  $f_{SW}$  and its harmonics are distributed into smaller pieces. This significantly reduces peak EMI noise.

### Low-Dropout Operation

To improve dropout, the MPQ4326/4326J is designed to operate at close to 100% duty cycle when the BST-to-SW voltage exceeds 2.7V.

Once the device exits low-dropout mode, it initiates SS again to prevent  $V_{COMP}$  from rising too high during this period. Even  $V_{IN}$  rapidly increases, inductor spikes are also minimized.

The effective duty cycle during the regulator's dropout period is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side (LS) diode, and the PCB resistance.

### Soft Start (SS)

Soft start (SS) prevents  $V_{OUT}$  from overshooting during start-up, where the SS time ( $t_{SS}$ ) is fixed internally.

Once  $t_{SS}$  starts, the SS voltage ( $V_{SS}$ ) rises from 0V to 1.2V with a set slew rate. If  $V_{SS}$  drops below the 0.8V internal reference voltage ( $V_{REF}$ ), then  $V_{SS}$  takes over and the EA uses  $V_{SS}$  as its reference. If  $V_{SS}$  exceeds  $V_{REF}$ , the EA uses  $V_{REF}$  as its reference. During  $t_{SS}$ , the converter operates in AAM mode for smooth SS regardless of the MODE setting.

During start-up through EN, the first pulse occurs after about 710 $\mu$ s. During this period, the VCC voltage ( $V_{CC}$ ) is regulated, the internal bias is generated, and the compensator network is charged. After another 2.9ms,  $V_{OUT}$  ramps up and reaches its set value. SS is complete after another 2.3ms. PG is also pulled high after a 160 $\mu$ s glitch.

### Pre-Biased Start-Up

If  $V_{FB}$  exceeds  $V_{SS}$  during start-up ( $V_{FB} > V_{SS} - 150\text{mV}$ ), this means that the output has a pre-biased voltage. Both the HS-FET and LS-FET remain off until  $V_{SS}$  exceeds  $V_{FB}$ .

### $V_{IN}$ Over-Voltage Protection (OVP)

The MPQ4326/4326J can operate across a wide  $V_{IN}$  range up to 36V. If  $V_{IN}$  exceeds its over-voltage protection (OVP) rising threshold ( $V_{IN\_OVP\_RISING}$ ) (typically 38V), then the device stops switching. If  $V_{IN}$  drops to the OVP falling threshold (typically 37V), then the device resumes switching and normal regulation. This ensures the device can survive in load dump conditions up to 42V.

### Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (170 $^{\circ}$ C), the power MOSFETs shut down. Once the temperature drops below its lower threshold (150 $^{\circ}$ C), the thermal shutdown condition is removed and the chip starts up again.

### Start-Up and Shutdown

If both  $V_{IN}$  and the EN voltage ( $V_{EN}$ ) exceed their respective thresholds, the chip starts up. The reference block starts up first to generate a stable  $V_{REF}$  and reference currents. Then the internal regulator is enabled to provide a stable supply for the remaining circuitries.

Once the internal supply rail is up, the LS-FET turns on to charge the BST pin if the voltage between BST and SW ( $V_{BST-SW}$ ) does not exceed the BST refresh rising threshold (typically 2.7V).

The HS-FET remains off during this time. When the SS block is enabled, it first holds its SS output low to ensure that the remaining circuits are ready. Then the SS block slowly ramps up.

Three events can shut down the chip: EN going low,  $V_{IN}$  falling below its under-voltage lockout (UVLO) threshold, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then  $V_{COMP}$  is pulled down and the floating driver disables the HS-FET.

## APPLICATION INFORMATION

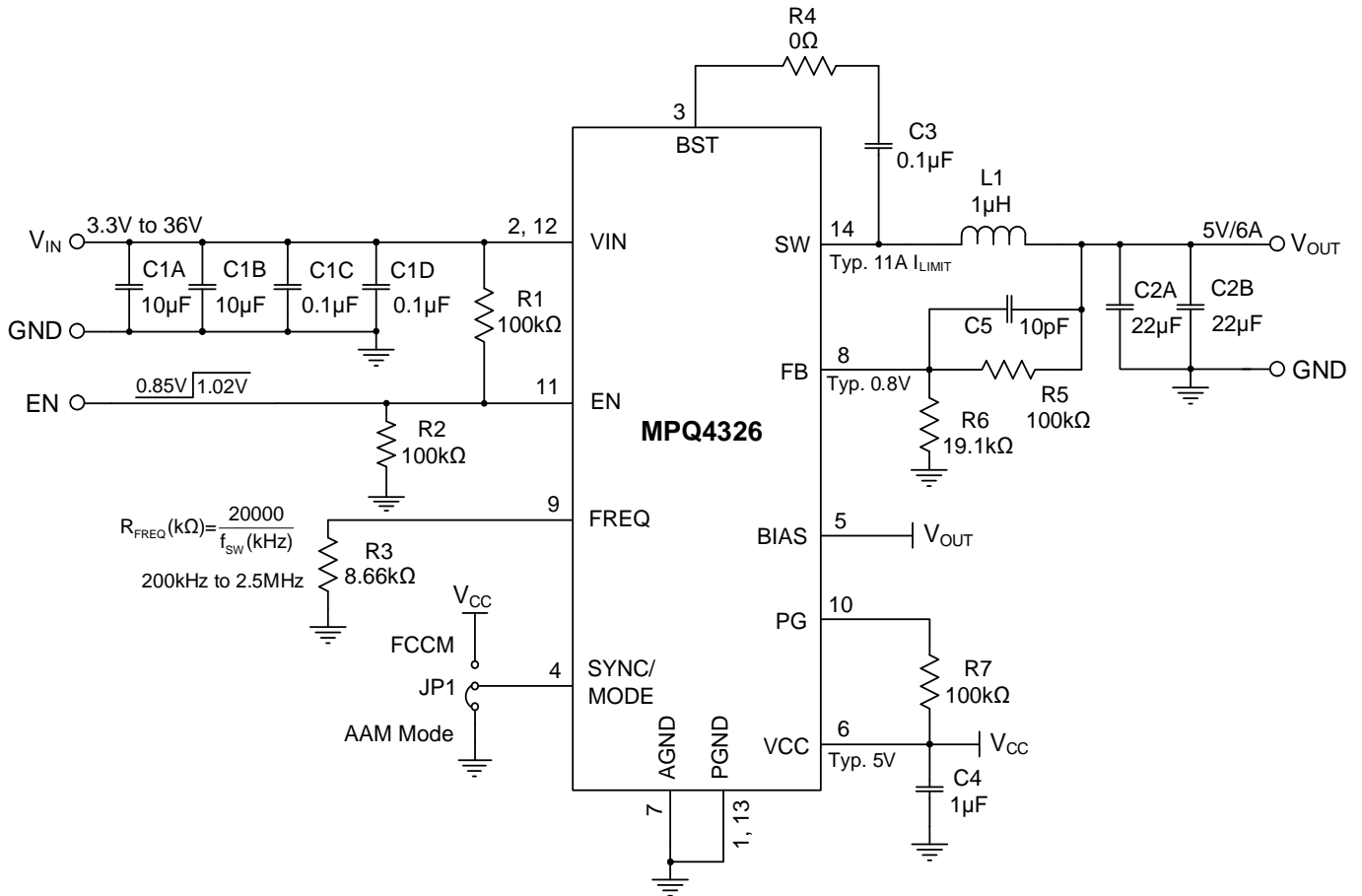


Figure 7: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$ )

Table 1: Design Guide Index

| Pin # | Pin Name  | Component          | Design Guide Index   |
|-------|-----------|--------------------|--|
| 1, 13 | PGND      | -                  | Ground Connection (PGND, Pins 1 and 13; AGND, Pin 7)       |
| 2, 12 | VIN       | C1A, C1B, C1C, C1D | Selecting the Input Capacitors (VIN, Pins 2 and 12)        |
| 3     | BST       | R4, C3             | Floating Driver and Bootstrap Charging (BST, Pin 3)        |
| 4     | SYNC/MODE | -                  | SYNC Input and MODE Selection (SYNC/MODE, Pin 4)           |
| 5     | BIAS      | -                  | External Bias for Low Quiescent Current (BIAS, Pin 5)      |
| 6     | VCC       | C4                 | Input Bias Supply (VCC, Pin 6)                             |
| 7     | AGND      | -                  | Ground Connection (PGND, Pins 1 and 13; AGND, Pin 7)       |
| 8     | FB        | R5, R6, C5         | Feedback (FB, Pin 8)                                       |
| 9     | FREQ      | R3                 | Setting the Switching Frequency ( $f_{sw}$ ) (FREQ, Pin 9) |
| 10    | PG        | R7                 | Power Good (PG) Indicator (PG, Pin 10)                     |
| 11    | EN        | R1, R2             | Enable (EN) and Under-Voltage Lockout (UVLO) (EN, Pin 11)  |
| 14    | SW        | L1, C2A, C2B       | Selecting the Inductor and Output Capacitors (SW, Pin 14)  |

### Ground Connection (PGND, Pins 1 and 13; AGND, Pin 7)

See the PCB Layout Guidelines section on page 44 for more details.

### Selecting the Input Capacitors (VIN, Pins 2 and 12)

The step-down converter has a discontinuous input current ( $I_{IN}$ ) and requires a capacitor to supply AC current to the converter while maintaining the DC  $V_{IN}$ . Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7 $\mu$ F to 10 $\mu$ F capacitor is sufficient. It is strongly recommended to use an additional, lower-value capacitor (e.g. 0.1 $\mu$ F) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and PGND as possible.

Since the input capacitor ( $C_{IN}$ ) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in  $C_{IN}$  ( $I_{CIN}$ ) can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (1)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose  $C_{IN}$  with an RMS current rating greater than half of the maximum load current ( $I_{LOAD\_MAX}$ ).  $C_{IN}$  can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1 $\mu$ F) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge that prevents excessive voltage ripple at the input. The input voltage ripple ( $\Delta V_{IN}$ ) caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

### Floating Driver and Bootstrap Charging (BST, Pin 3)

The bootstrap (BST) capacitor ( $C_{BST}$ , also called  $C_{BST}$ ) is recommended to be between 0.1 $\mu$ F and 0.22 $\mu$ F.

It is not recommended to place a resistor ( $R_{BST}$ ) in series with  $C_{BST}$ , unless there is a strict EMI requirement.  $R_{BST}$  reduces EMI and voltage stress at high input voltages. A higher resistance is better for switching spike reduction but compromises efficiency. If necessary,  $R_{BST}$  should be less than 5 $\Omega$ .

The voltage between the BST and SW pins ( $V_{BST-SW}$ ) is regulated to about 5V by the dedicated internal bootstrap regulator. If  $V_{BST-SW}$  drops below its regulated value, then a N-channel MOSFET pass transistor connected between VCC and BST turns on to charge  $C_{BST}$ . The external circuit should provide enough voltage headroom to facilitate charging.

When the HS-FET is on,  $V_{BST}$  exceeds  $V_{CC}$  so  $C_{BST}$  cannot charge. At higher duty cycle operation, the time available for bootstrap charging is shorter, so  $C_{BST}$  may not be charged sufficiently. If the external circuit has an insufficient voltage and time to charge  $C_{BST}$ , additional external circuitry can be used to ensure that  $V_{BST}$  remains within its normal operating region.

If  $V_{BST}$  reaches its UVLO threshold, then the HS-FET turns off, and the LS-FET turns on for  $t_{OFF\_MIN}$  to refresh  $V_{BST}$  via the set  $f_{SW}$ .

### SYNC Input and MODE Selection (SYNC/MODE, Pin 4)

The switching frequency ( $f_{SW}$ ) can be synchronized to the rising edge of a clock signal applied at SYNCIN. The recommended SYNCIN frequency range is between 200kHz and 2.5MHz.

Switching can be synchronized to an external clock within a SCYNCIN clock locking time (128 cycles), ranging from  $\pm 10\%$  of the set clock frequency.

When SYNC/MODE is used for mode selection, pull this pin high to allow the part to enter FCCM; pull this pin low to allow the part to enter AAM mode. Table 2 on page 40 shows the details for mode selection.

**Table 2: Mode Selection**

| SYNC/MODE Input   | Operation |
|-------------------|-----------|
| <0.4V             | AAM mode  |
| >1.4V             | FCCM      |
| External clock in | FCCM      |

### External Bias for Low Quiescent Current (BIAS, Pin 5)

BIAS is the external bias pin. When BIAS is connected to the 5V voltage, the internal LDO turns off, and a smaller input supply current enables higher efficiency. If the BIAS pin voltage ( $V_{BIAS}$ ) exceeds 4.6V, the pin starts to work; if  $V_{BIAS}$  drops below 4.36V, the pin is disabled. For the 5V output version, connect BIAS to  $V_{OUT}$  directly. For the other lower (<4.6V) or higher (>6V) output versions, connect BIAS to the external 5V source to achieve a lower input supply current, or connect BIAS to ground to disable the bias function. It is recommended to avoid providing  $V_{BIAS}$  before  $V_{IN}$ .

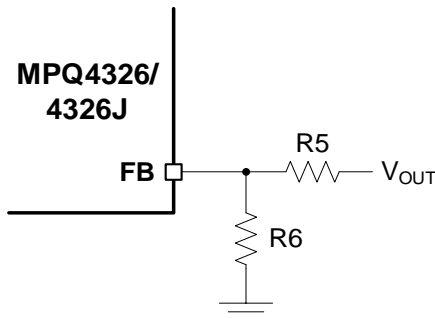
### Internal Bias Supply (VCC, Pin 6)

The VCC capacitance (C4) is recommended to be 1 $\mu$ F.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses  $V_{IN}$  as its input and operates across the entire  $V_{IN}$  range. If  $V_{IN}$  exceeds 5V, then  $V_{CC}$  is in full regulation. If  $V_{IN}$  drops below 5V, then the VCC output degrades.

### Feedback (FB, Pin 8)

For the adjustable-output version, the typical feedback voltage ( $V_{FB}$ ) is 0.8V. The external resistor dividers (R5 and R6) connected to FB sets  $V_{OUT}$  (see Figure 8).


**Figure 8: Feedback Divider Network for Adjustable-Output Version**

R6 can be calculated with Equation (4):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

Table 3 lists the recommended feedback resistances for common output voltages.

**Table 3: Resistor Selection for Output Voltages**

| $V_{OUT}$ (V) | R5 (k $\Omega$ ) | R6 (k $\Omega$ ) |
|---------------|------------------|------------------|
| 3.3           | 100 (0.1%)       | 31.6 (0.1%)      |
| 5             | 100 (0.1%)       | 19.1 (0.1%)      |

For the fixed-output version, the FB resistor dividers ( $R_{FB1}$  and  $R_{FB2}$ ) are integrated internally (see Figure 9). Connect FB directly to the output to set  $V_{OUT}$ . The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, or 5V.

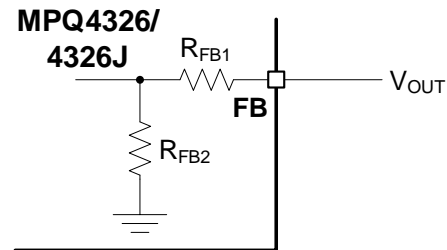

**Figure 9: Feedback Divider Network for Fixed-Output Version**

Table 4 shows the relationship between the internal  $R_{FB}$  and  $V_{OUT}$ .

**Table 4:  $R_{FB}$  vs.  $V_{OUT}$** 

| $V_{OUT}$ (V) | $R_{FB1}$ (k $\Omega$ ) | $R_{FB2}$ (k $\Omega$ ) |
|---------------|-------------------------|-------------------------|
| 1             | 64                      | 256                     |
| 1.8           | 320                     | 256                     |
| 2.5           | 544                     | 256                     |
| 3.0           | 704                     | 256                     |
| 3.3           | 800                     | 256                     |
| 3.8           | 960                     | 256                     |
| 5             | 1344                    | 256                     |

### Setting the Switching Frequency ( $f_{sw}$ ) (FREQ, Pin 9)

A frequency resistor (R3, also called  $R_{FREQ}$ ) can be used to set  $f_{sw}$  (see Figure 10 on page 41).



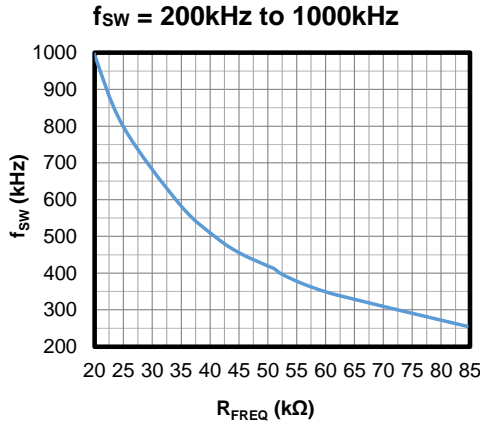
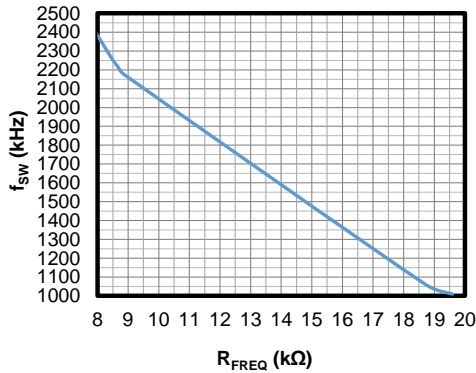

**Figure 10: f<sub>SW</sub> vs. R<sub>FREQ</sub>**

Table 5 shows the relationship between f<sub>SW</sub> and R<sub>FREQ</sub>.

**Table 5: f<sub>SW</sub> vs. R<sub>FREQ</sub>**

| R <sub>FREQ</sub> (kΩ) | f <sub>SW</sub> (kHz) |
|------------------------|-----------------------|
| 7.87                   | 2500                  |
| 8.66                   | 2200                  |
| 14.3                   | 1500                  |
| 18.7                   | 1060                  |
| 19.6                   | 1000                  |
| 24.9                   | 800                   |
| 34.8                   | 590                   |
| 43.2                   | 470                   |
| 49.9                   | 410                   |
| 52.3                   | 400                   |
| 56.2                   | 370                   |
| 62                     | 340                   |
| 84.5                   | 255                   |
| 100                    | 210                   |

### Power Good (PG) Indicator (PG, Pin 10)

The PG resistor (R7, also called R<sub>PG</sub>) is recommended to have a resistance around 100kΩ.

The MPQ4326/4326J includes an open-drain power good output that indicates whether V<sub>OUT</sub> is

within a specific window of its nominal range.

If PG is used, connect it to a logic high power source in the system via a pull-up resistor. If V<sub>OUT</sub> is within 94.5% to 105.5% of the nominal voltage, PG goes high; if V<sub>OUT</sub> exceeds 107% or drops below 93% of the nominal voltage, PG goes low. Float PG if it is not used.

### Enable (EN) and Under-Voltage Lockout (UVLO) (EN, Pin 11)

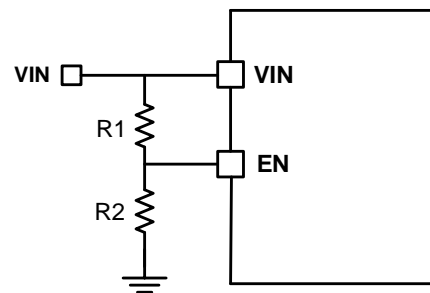
EN is a digital control pin that turns the regulator on and off.

#### Enabled by an External Logic High/Low Signal

If V<sub>EN</sub> reaches about 0.7V, the bandgap (BG) does not turn on until V<sub>IN</sub> exceeds about 2.7V. The BG then provides an accurate V<sub>REF</sub> for the EN threshold. Pull EN above its rising threshold (1.02V) to enable the device. Pull EN below 0.85V to shut down the device. There is no internal pull-up or pull-down resistor connected to EN. Do not float EN to avoid uncertain states. If the control signal cannot give an accurate high or low logic, then an external pull-up or pull-down resistor is required.

#### Configurable V<sub>IN</sub> Under-Voltage Lockout (UVLO) Threshold

The MPQ4326/4326J has an internal, fixed UVLO threshold. The rising threshold is 3.7V, and the falling threshold is about 2.9V. For applications that require a higher UVLO level, place an external resistor divider between V<sub>IN</sub> and EN to raise the equivalent UVLO threshold (see Figure 11).


**Figure 11: Adjustable UVLO via the EN Divider**

The UVLO rising threshold (V<sub>IN\_UVLO\_RISING</sub>) can be calculated with Equation (5):

$$V_{IN\_UVLO\_RISING} = \left(1 + \frac{R1}{R2}\right) \times V_{EN\_RISING} \quad (5)$$

Where  $V_{EN\_RISING}$  is 1.02V.

The UVLO falling threshold ( $V_{IN\_UVLO\_FALLING}$ ) can be calculated with Equation (6):

$$V_{IN\_UVLO\_FALLING} = \left(1 + \frac{R1}{R2}\right) \times V_{EN\_FALLING} \quad (6)$$

Where  $V_{EN\_FALLING}$  is 0.85V.

If EN is not used to turn the device on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

### Selecting the Inductor and Output Capacitors (SW, Pin 14)

The inductance (L) can be calculated with Equation (7):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Where  $\Delta I_L$  is the peak-to-peak inductor ripple current.

A 1 $\mu$ H to 10 $\mu$ H inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A small-size inductor provides benefits for EMI. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current ( $I_{L\_PEAK}$ ) can be calculated with Equation (8):

$$I_{L\_PEAK} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Choose an inductor that does not saturate under  $I_{L\_PEAK}$ .

### Peak and Valley Current Limits

Both the HS-FET and LS-FET have cycle-by-cycle current limit protection. If  $I_L$  reaches the high-side (HS) peak current limit (typically 11A) while the HS-FET is on, then the HS-FET is immediately forced off to prevent the current from rising further.

When the LS-FET is on, the next clock's rising edge is held until  $I_L$  drops below the LS valley current limit (typically 7.5A). Once the HS-FET turns on again,  $I_L$  drops to a sufficiently low value. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

### Short-Circuit Protection (SCP)

If the output is shorted to ground, and  $V_{OUT}$  drops below 70% of its nominal output, then the MPQ4326/4326J shuts down momentarily and discharges  $V_{SS}$ . Once  $V_{SS}$  is fully discharged, the device initiates SS. This hiccup process is repeated until the fault is removed.

During the hiccup period, if  $V_{FB}$  reaches 50% of the internal  $V_{REF}$ , the device triggers short-circuit protection (SCP) recovery and initiates SS to avoid large spikes. When applying SCP function,  $V_{IN}$  is recommended to be lower than 24V.

The output voltage ripple ( $\Delta V_{OUT}$ ) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (9)$$

Where  $R_{ESR}$  is the equivalent series resistance (ESR) of the output capacitor ( $C_{OUT}$ ).

$C_{OUT}$  maintains the DC  $V_{OUT}$ . Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep  $\Delta V_{OUT}$  low.

For ceramic capacitors, the capacitance dominates the impedance at  $f_{SW}$  and causes the majority of  $\Delta V_{OUT}$ . For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at  $f_{SW}$ . For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

When selecting  $C_{OUT}$ , consider the allowable overshoot in  $V_{OUT}$  if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to  $C_{OUT}$ , causing its voltage to rise. To

achieve an optimal overshoot relative to the regulated voltage, C<sub>OUT</sub> can be estimated with Equation (12):

$$C_{OUT} = \frac{(I_{OUT})^2 \times L}{(V_{OUT})^2 \times ((V_{OUT\_MAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V<sub>OUT\_MAX</sub> / V<sub>OUT</sub> is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance.

The C<sub>OUT</sub> characteristics also affect the stability of the regulation system. The MPQ4326/4326J can be optimized for a wide range of capacitances and ESR values.

### Output Over-Voltage Protection (OVP) and Discharge

If V<sub>OUT</sub> exceeds 130% of its nominal regulation value, the MPQ4326/4326J stops switching. An internal 75Ω discharge path from FB to ground discharges V<sub>OUT</sub>. This discharge path is only activated if the output is fixed. Once V<sub>OUT</sub> drops back to 125% of its nominal voltage, the discharge path is disabled, and the device resumes switching.

For the fixed-output version, the V<sub>OUT</sub> discharge path is also activated if a shutdown through EN occurs. Once V<sub>CC</sub> drops to its UVLO threshold, the discharge path is disabled.

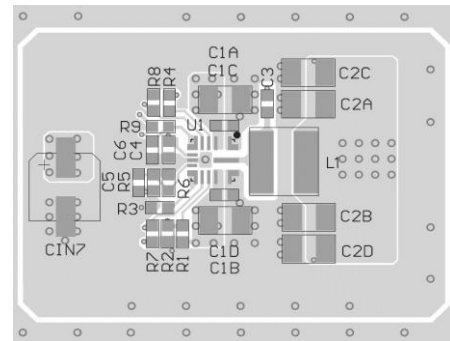
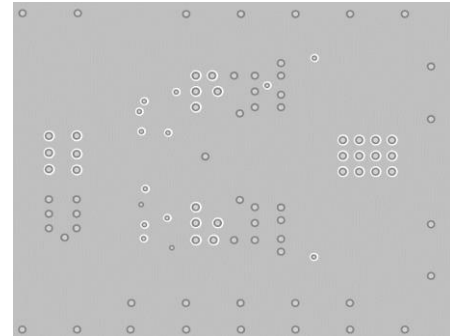
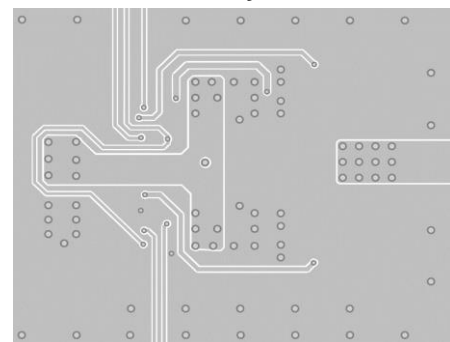
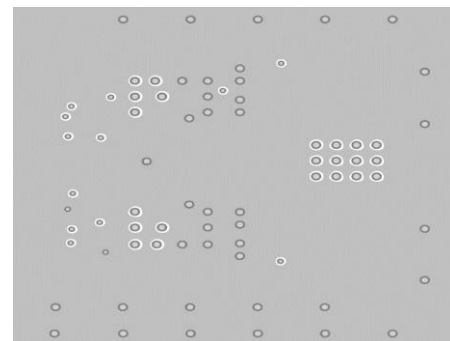
**PCB Layout Guidelines** <sup>(15)</sup>

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to achieve improved thermal performance. For the best results, refer to Figure 12 and follow the guidelines below:

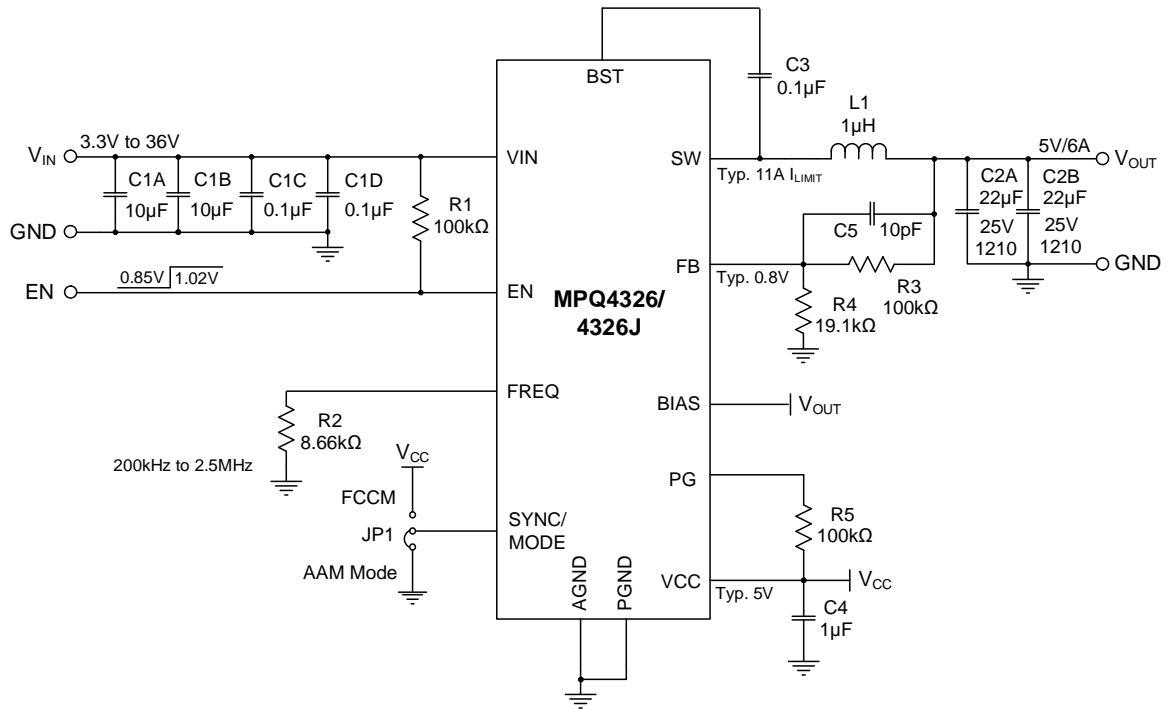
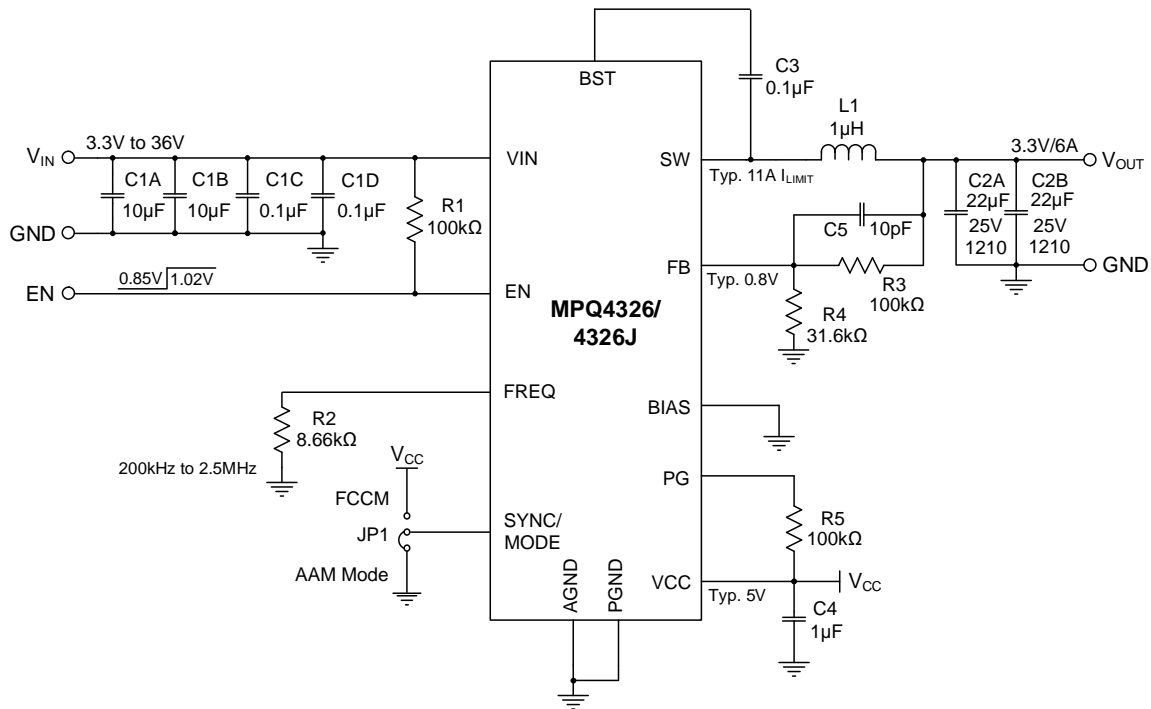
1. Place symmetric input capacitors as close to VIN and PGND as possible.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at ground and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Reduce the SW node routing size for improved EMI.
10. Place the feedback resistors close to the chip to ensure that the trace connected to FB is as short as possible.
11. Use multiple vias to connect the power planes to the internal layers.

**Note:**

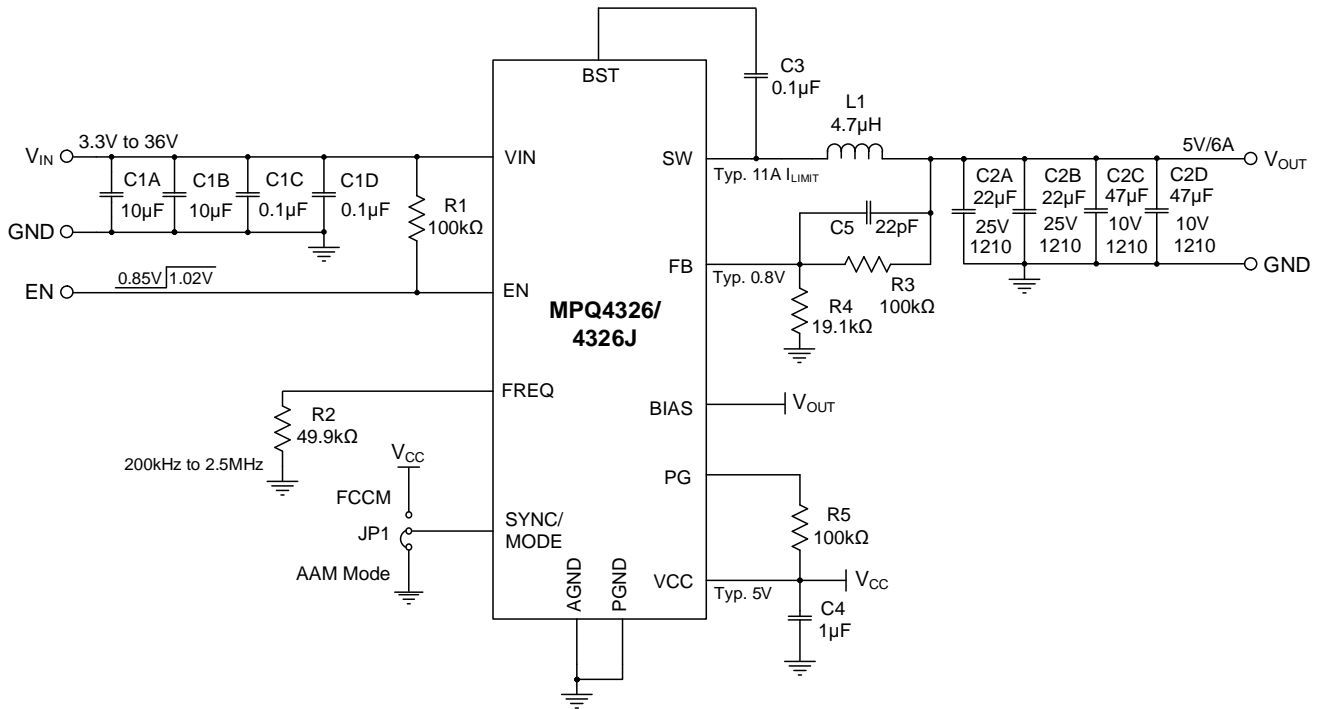
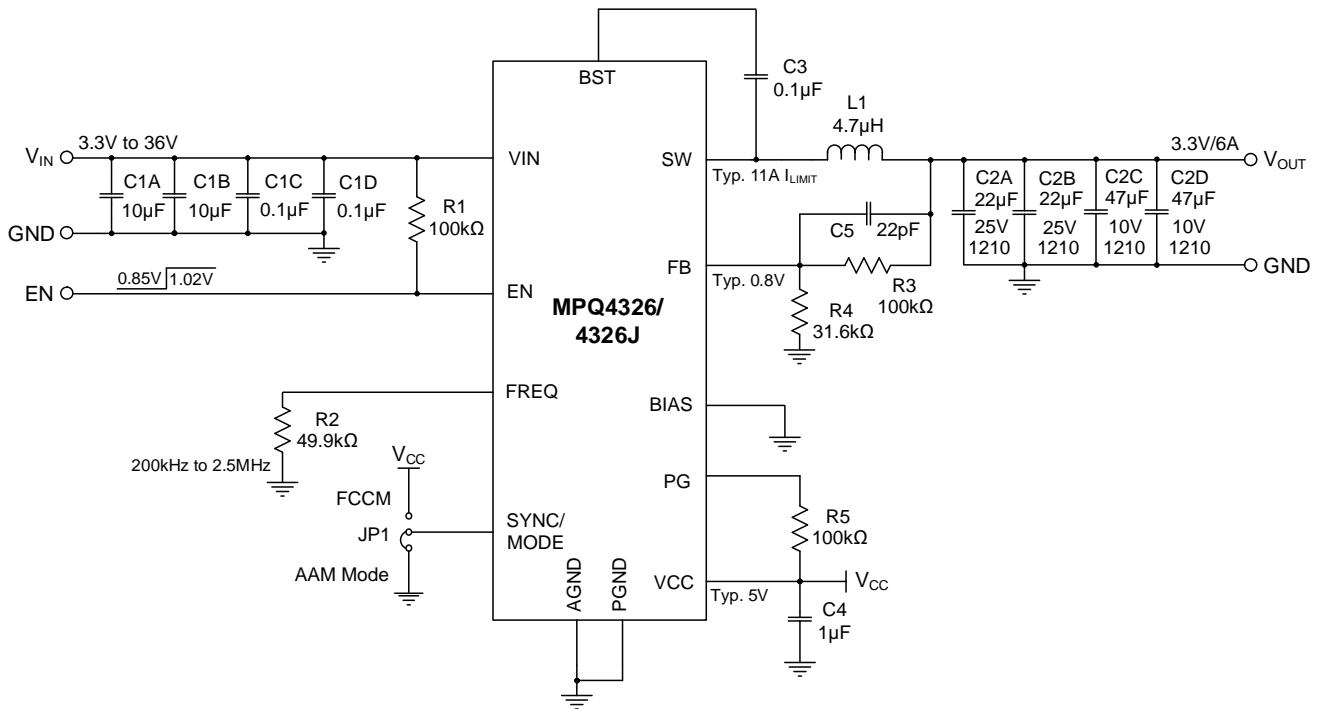
15) The recommended PCB layout is based on Figure 13 on page 45.

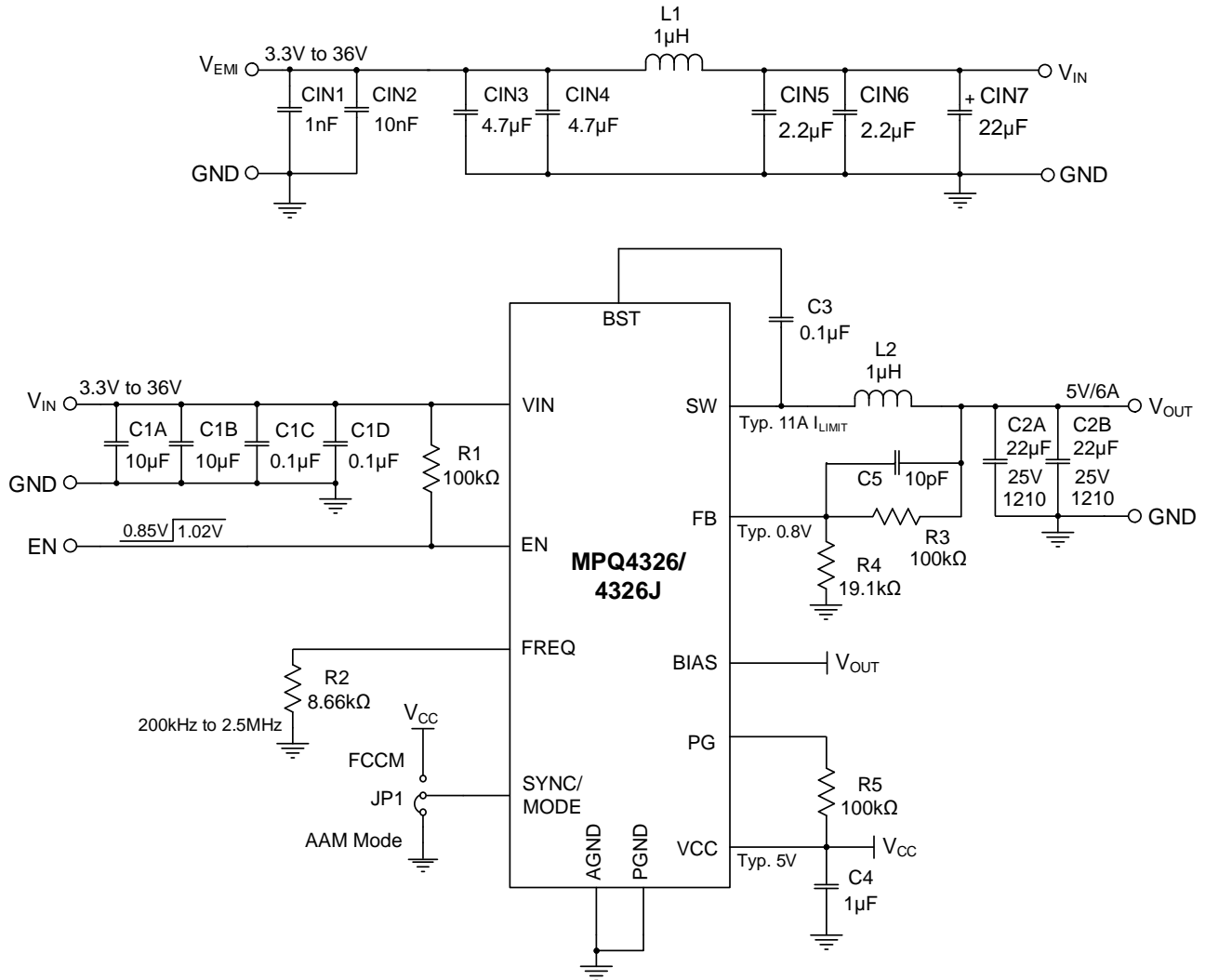

**Top Layer**

**Mid-Layer 1**

**Mid-Layer 2**

**Bottom Layer**
**Figure 12: Recommended PCB Layout**

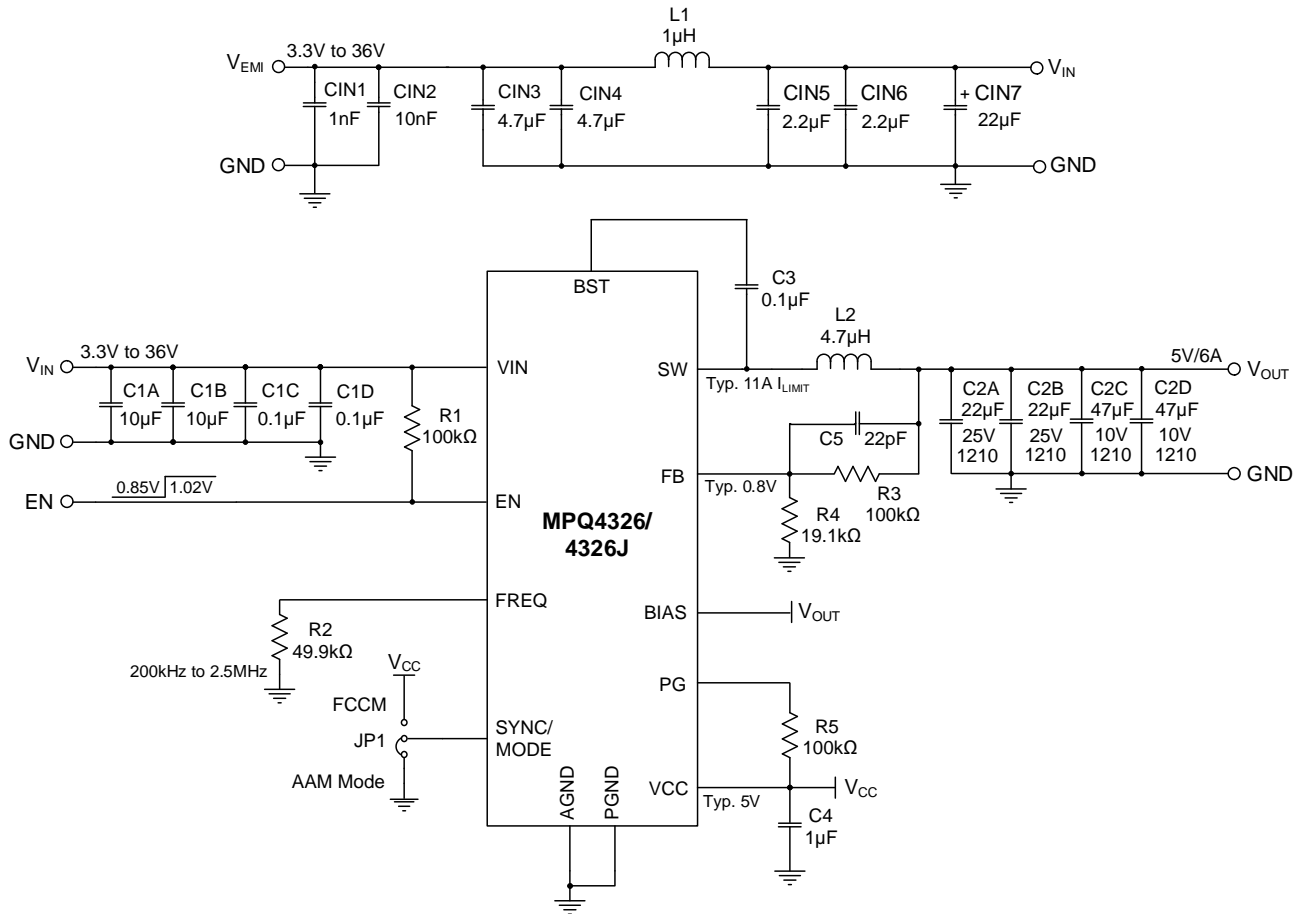
## TYPICAL APPLICATION CIRCUITS


 Figure 13: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$ )

 Figure 14: Typical Application Circuit ( $V_{OUT} = 3.3V$ ,  $f_{sw} = 2.2MHz$ )

## TYPICAL APPLICATION CIRCUITS (continued)


 Figure 15: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 410kHz$ )

 Figure 16: Typical Application Circuit ( $V_{OUT} = 3.3V$ ,  $f_{sw} = 410kHz$ )

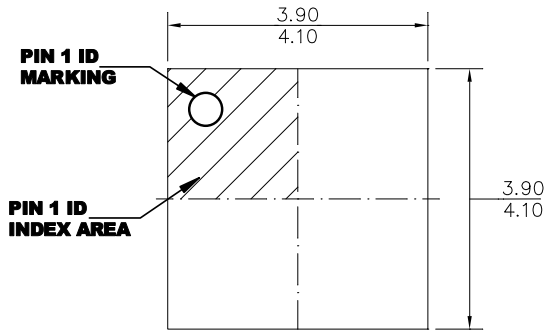
**TYPICAL APPLICATION CIRCUITS (continued)**

**Figure 17: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$  with EMI Filters)**

**TYPICAL APPLICATION CIRCUITS (continued)**

**Figure 18: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 410kHz$  with EMI Filters)**

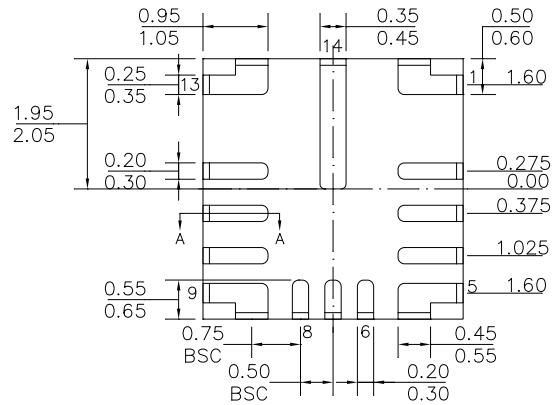


# PACKAGE INFORMATION

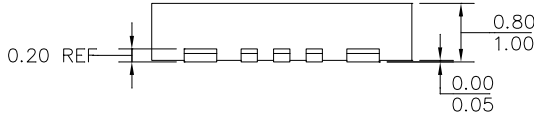
## QFN-14 (4mmx4mm) Wettable Flank



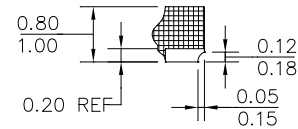
**TOP VIEW**



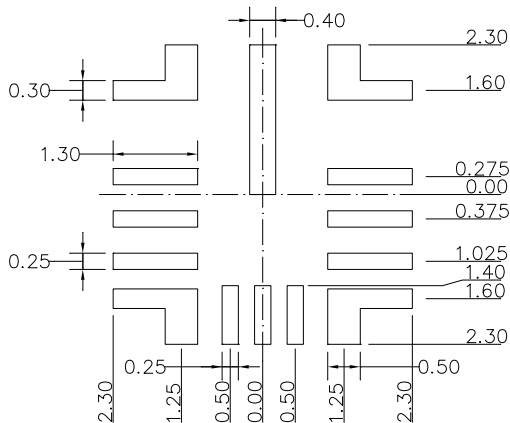
**BOTTOM VIEW**



**SIDE VIEW**



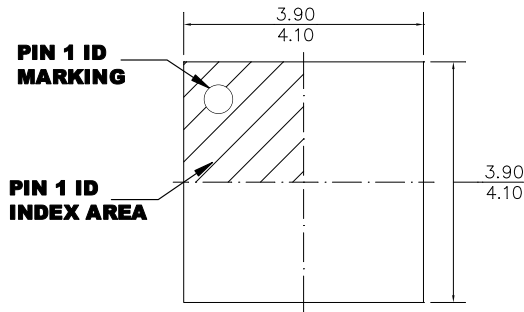
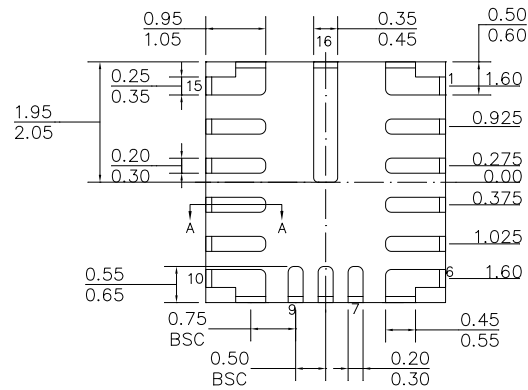
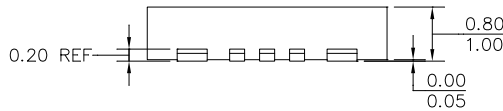
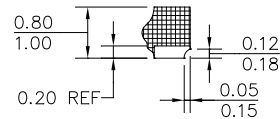
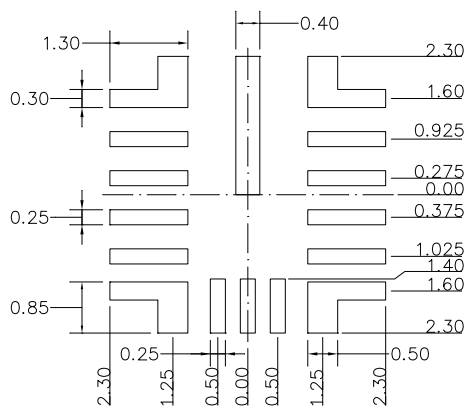
**SECTION A-A**



**RECOMMENDED LAND PATTERN**

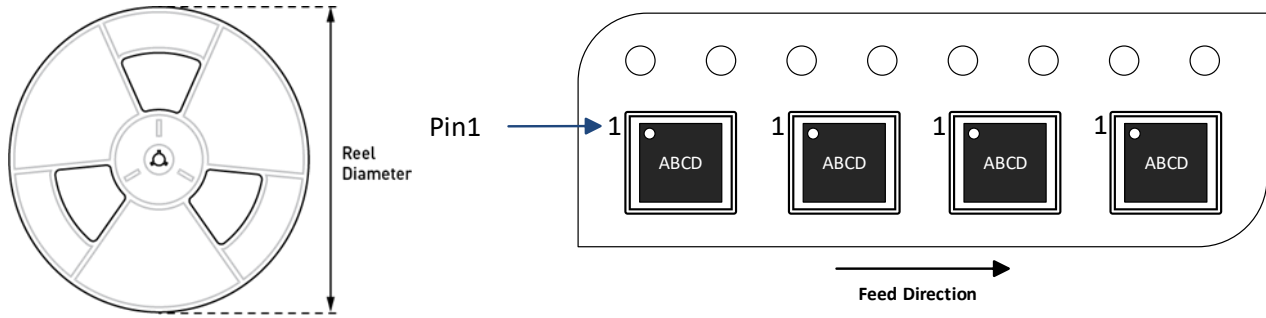
**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

**PACKAGE INFORMATION (continued)**
**QFN-16 (4mmx4mm)  
Wettable Flank**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**SECTION A-A**

**RECOMMENDED LAND PATTERN**
**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.**
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.**
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.**
- 4) JEDEC REFERENCE IS MO-220.**
- 5) DRAWING IS NOT TO SCALE.**

## CARRIER INFORMATION



| Part Number          | Package Description | Quantity/ Reel | Quantity/ Tube <sup>(16)</sup> | Quantity/ Tray <sup>(16)</sup> | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|----------------------|---------------------|----------------|--------------------------------|--------------------------------|---------------|--------------------|--------------------|
| MPQ4326GRE-Z         | QFN-14 (4mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |
| MPQ4326GRE-AEC1-Z    | QFN-14 (4mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |
| MPQ4326GRE-5-AEC1-Z  | QFN-14 (4mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |
| MPQ4326GRE-33-AEC1-Z | QFN-14 (4mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |
| MPQ4326JGRE-AEC1-Z   | QFN-16 (4mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |

**Note:**

16) N/A indicates "not available" in tube and tray. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for a 500-piece partial reel is "-P"; tape & reel dimensions are the same as the full reel.)

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 9/6/2023      | Initial Release | -             |

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