3A Ultra-small Load Switch with Slew Rate Control

Features

- Integrated P-channel MOSFET load switch
- Input voltage: 1.2V to 5.5V
- 3A maximum continuous switch current
- Switch on-resistance(typ.):
  Rdson=17mΩ at VIN=5.5V
  Rdson=22mΩ at VIN=3.3V
  Rdson=81mΩ at VIN=1.2V
- Controlled slew rate to limit inrush currents
- Ultra low shutdown current
- Internal EN pull-down resistor
- Quick output discharge(QOD)
- WLCSP 1.355mm×0.855mm×0.55mm-6B

General Description

The AW35131ACSR is a load switch with output slew rate control. The device integrates a 22mΩ (typ.) P-channel MOSFET, which can operate over a wide input range of 1.2V to 5.5V.

The AW35131ACSR features output slew rate control, limiting inrush currents during turn-on to protect downstream devices. In addition, AW35131ACSR has QOD function which can prevent the output from floating when the switch is disabled.

Applications

Smart Wear
Vehicle Module
High-Definition Television(HDTV)

Typical Application Circuit

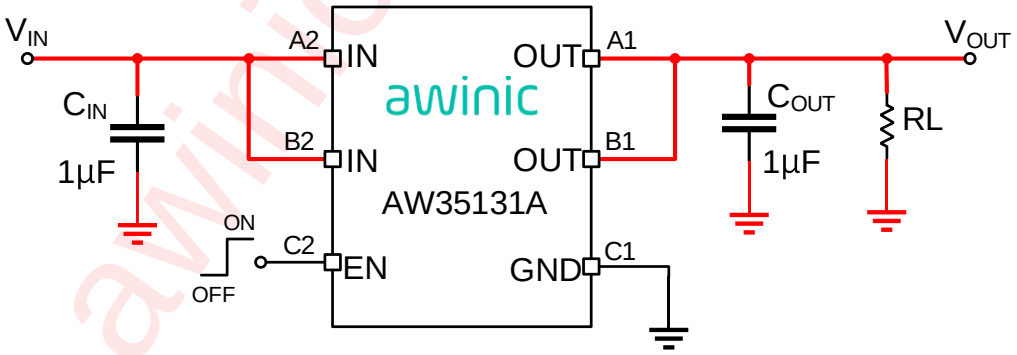
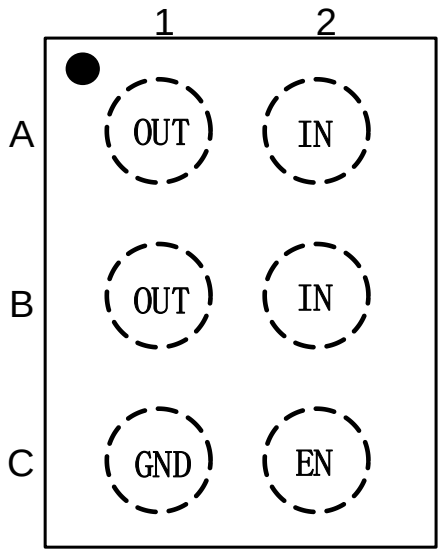


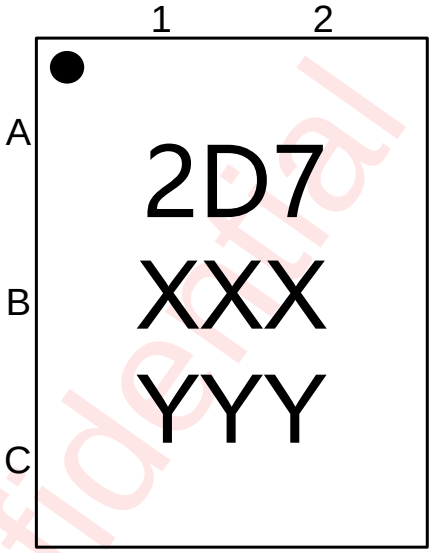
Figure 1 Typical Application circuit of AW35131ACSR

Pin Configuration And Top Mark

AW35131ACSR
(Top View)



AW35131ACSR Marking
(Top View)



2D7 – AW35131ACSR
XXX YYY – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
A1	OUT	Switch output
B1		
C1	GND	Device ground
A2	IN	Switch input and power supply
B2		
C2	EN	Switch control input, active high

Functional Block Diagram

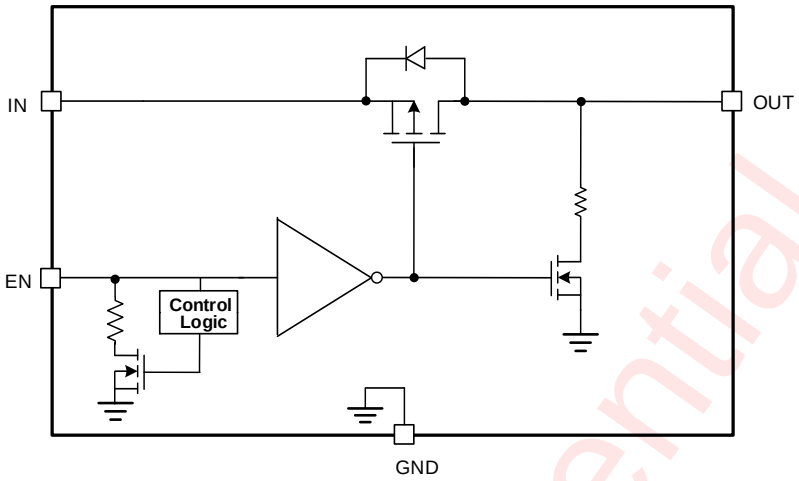


Figure 3 Functional Block Diagram

Typical Application Circuits

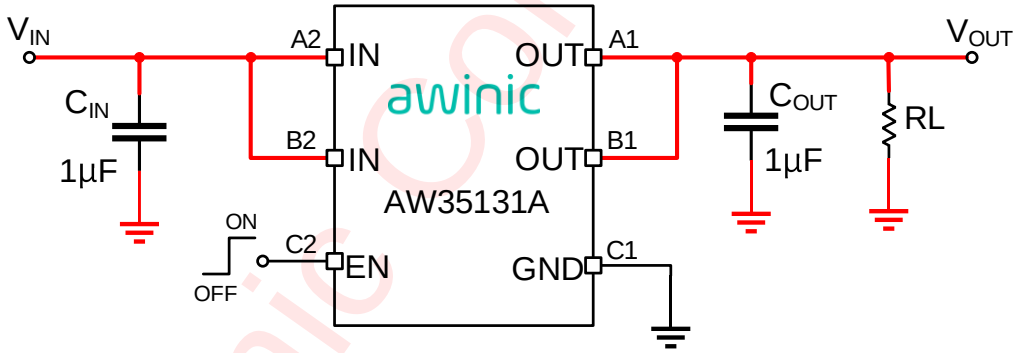


Figure 4 Typical Application circuit of AW35131ACSR

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35131ACSR	-40℃～85℃	WLCSP 1.355mm×0.855mm×0.55mm -6B	2D7	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 6V
Enable Voltage Range	EN	-0.3V to 6V
Output Voltage Range	OUT	-0.3V to 6V
Maximum Continuous Switch Current for VIN ≥ 1.5V		3A
Maximum Continuous Switch Current for 1.2 ≤VIN < 1.5V(NOTE 2)		2A
Maximum Peak Switch Current for VIN ≥ 2.5V(NOTE 3)		4A
Junction-to-ambient Thermal Resistance θ_{JA}(NOTE 4)		100°C/W
Operating Free-air Temperature Range		-40°C to 85°C
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD		
HBM (Human Body Model) (NOTE 5)		±2kV
CDM(Charged Device Model) (NOTE 6)		±1.5kV
Latch-Up		
Latch-Up (NOTE 7)		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The power mos enters saturation region, load capacity is reduced.

NOTE3: Limited by thermal design, and tested in 10ms width pulse current.

NOTE4: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE6: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE7: Test Condition: JESD78E.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	1.2		5.5	V
V_{EN}	EN Voltage	0		5.5	V
V_{OUT}	Output Voltage	0		V_{IN}	V
C_{IN}	Input capacitance	0.1	1		μF
C_{OUT}	Output load capacitance	0.1	1		μF

Electrical Characteristics

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 3.3V, C_{IN} = 1μF, I_{IN}≤ 3A.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_Q	Input quiescent current	V_{IN}=3.3V, V_{EN}=3.3V,I_{OUT}=0A, T_A=25°C		3		nA
		V_{IN}=3.3V, V_{EN}=3.3V,I_{OUT}=0A, T_A=85°C		11		nA
		V_{IN}=5.5V, V_{EN}=5.5V,I_{OUT}=0A, T_A=25°C		5	600	nA
		V_{IN}=5.5V, V_{EN}=5.5V,I_{OUT}=0A, T_A=85°C		17		nA
I_{SD}	Shutdown current from IN to GND	V_{IN}=1.2V, V_{EN}=0V, T_A=25°C		3		nA
		V_{IN}=1.8V, V_{EN}=0V, T_A=25°C		4		nA
		V_{IN}=3.3V, V_{EN}=0V, T_A=25°C		6		nA
		V_{IN}=3.3V, V_{EN}=0V, T_A=85°C		11		nA
		V_{IN}=4.5V, V_{EN}=0V, T_A=25°C		8		nA
		V_{IN}=5.5V, V_{EN}=0V, T_A=25°C		15	600	nA
		V_{IN}=5.5V, V_{EN}=0V, T_A=85°C		18		nA
I_{LEAKEN}	EN pin leakage current	V_{IN}=0V, V_{EN}=5.5V		546	1000	nA
R_{EN}	EN pin pull down resistor	V_{EN}=5.0V		9.2		MΩ
POWER SWITCH						
R_{dson}	Internal switch MOSFET on-state resistance	V_{IN}=5.5V, V_{EN}=high, I_{OUT}=200mA, T_A=25°C		17		mΩ
		V_{IN}=3.3V, V_{EN}=high, I_{OUT}=200mA, T_A=25°C		22		
		V_{IN}=1.8V, V_{EN}=high, I_{OUT}=200mA, T_A=25°C		37		
		V_{IN}=1.2V, V_{EN}=high, I_{OUT}=200mA, T_A=25°C		81		
R_{DIS}	Output discharge resistance	V_{IN}=3.3V, V_{EN}=low, T_A=25°C, I_{OUT} Sinking 2mA		87		Ω
t_R	Output rise time	V_{IN}=3.3V, C_{OUT}=1μF, R_{OUT}=5Ω		320		μs
t_F	Output fall time	V_{IN}=3.3V, C_{OUT}=1μF, R_{OUT}=5Ω		10		μs
t_{ON}	Switch turn on time	V_{IN}=3.3V, C_{OUT}=1μF, R_{OUT}=5Ω		405		μs
t_{OFF}	Switch turn off time	V_{IN}=3.3V, C_{OUT}=1μF, R_{OUT}=5Ω		4.1		μs
t_{EN}	Enable time	V_{IN}=3.3V, C_{OUT}=1μF, R_{OUT}=5Ω		253		μs
V_{IH}	EN input high threshold level		1.2			V
V_{IL}	EN input low threshold level				0.4	V

Timing Diagram

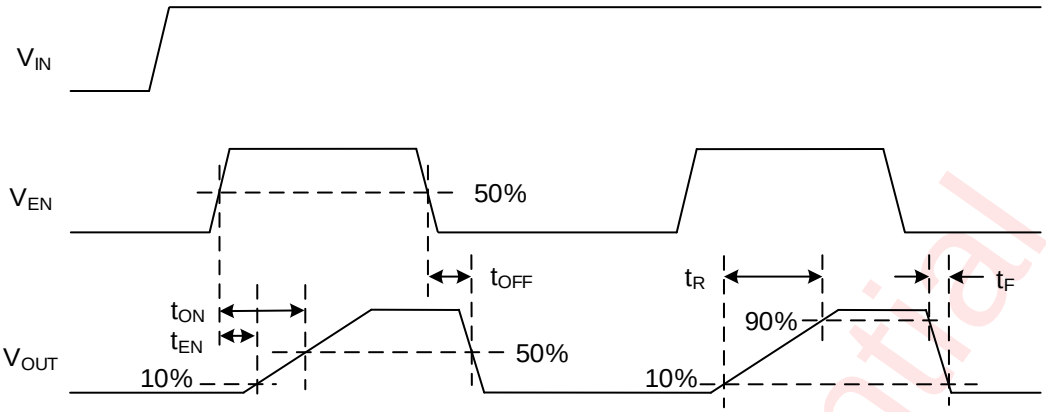


Figure 5 AW35131ACSR Timing Diagram

Typical Characteristics

Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.

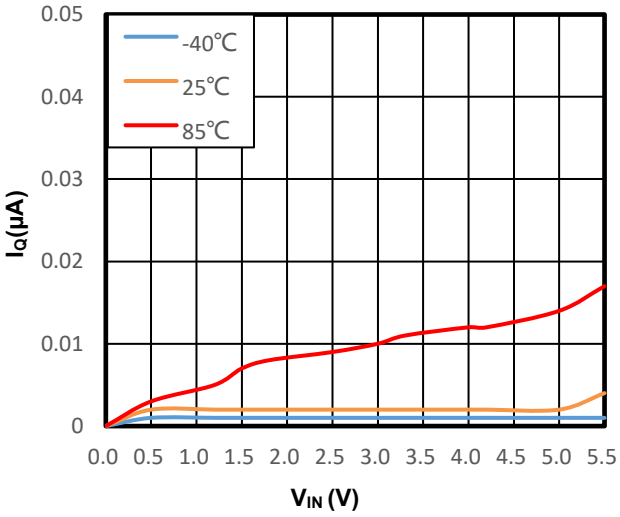


Figure 6 Quiescent Current vs. V_{IN}, No load

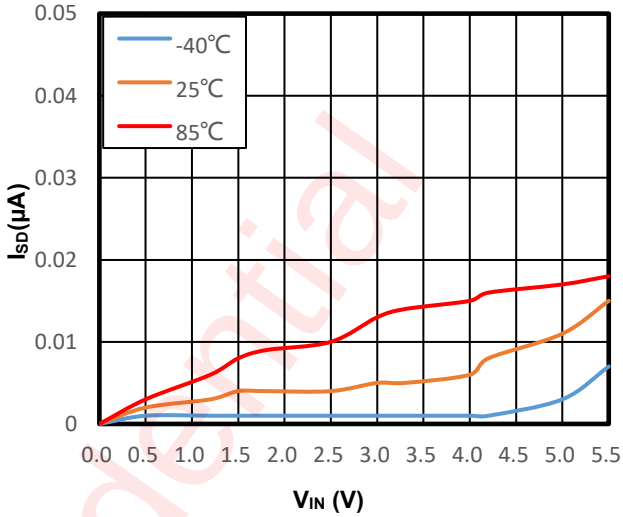


Figure 7 IN Shutdown Current vs. V_{IN}

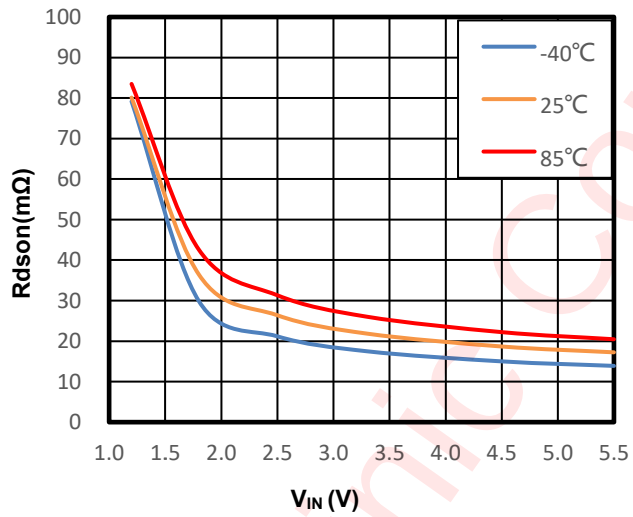


Figure 8 Rdson vs. V_{IN}(I_{OUT}=200mA)

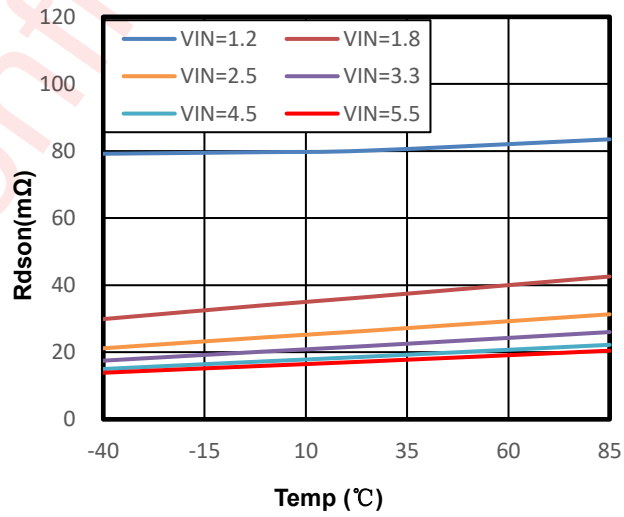


Figure 9 Rdson vs. Temperature(I_{OUT}=200mA)

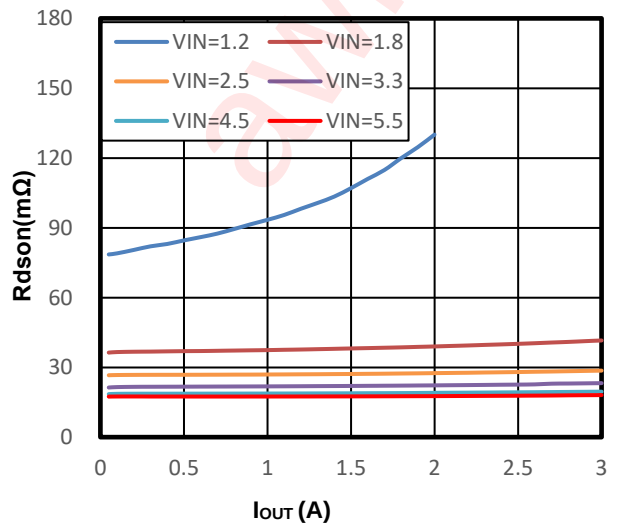


Figure 10 Rdson vs. I_{OUT}

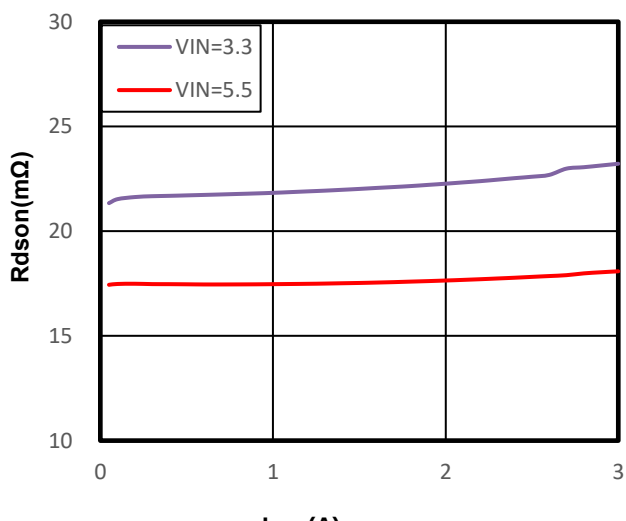
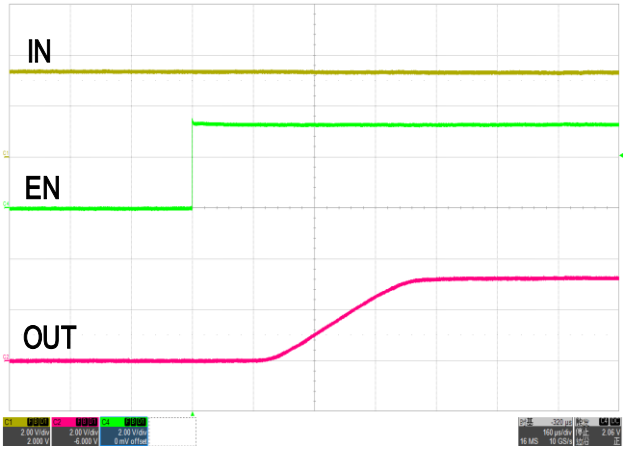
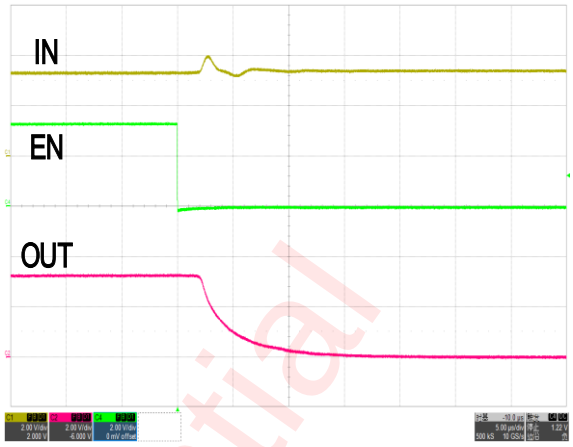


Figure 11 Rdson vs. I_{OUT}



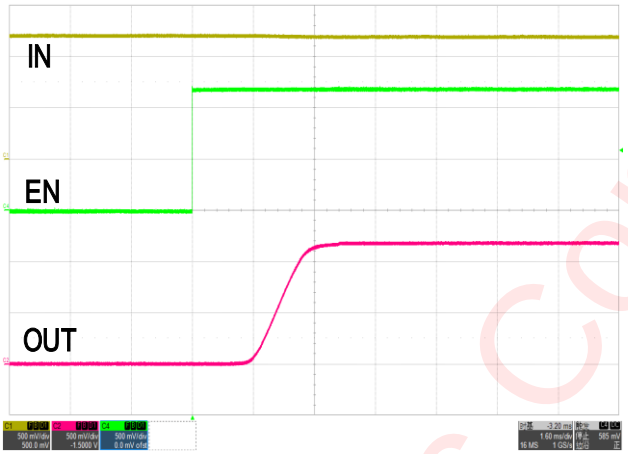
C1: 2.00V/div C2: 2.00V/div t=160μs/div
C4: 2.00V/div
V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=5Ω

Figure 12 Turn On Response



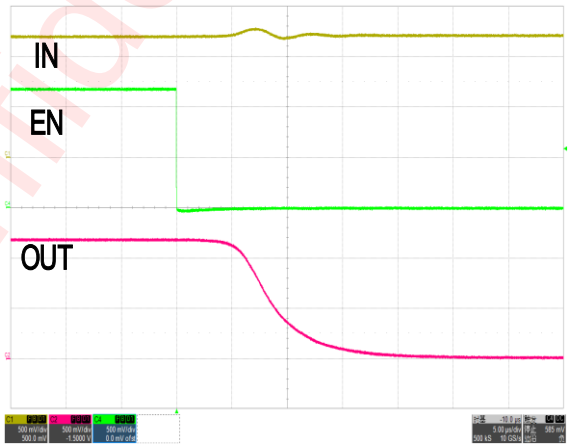
C1: 2.00V/div C2: 2.00V/div t=5μs/div
C4: 2.00V/div
V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=5Ω

Figure 13 Turn Off Response



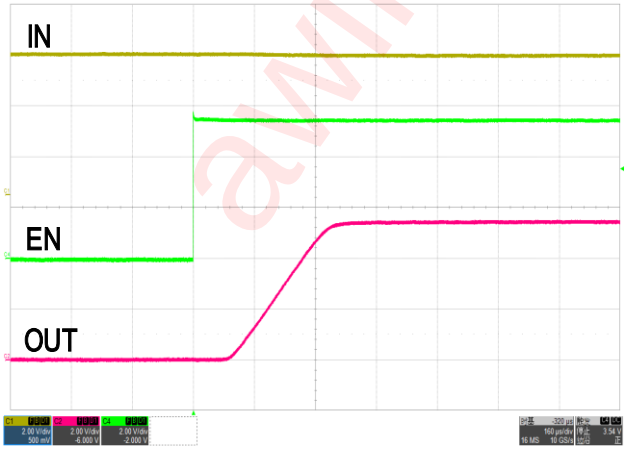
C1: 0.5V/div C2: 0.5V/div t=1.6ms/div
C4: 0.5V/div
V_{IN}=1.2V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=5Ω

Figure 14 Turn On Response



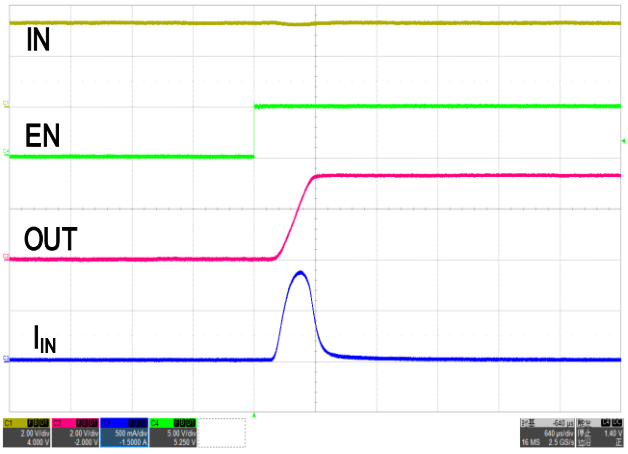
C1: 0.5V/div C2: 0.5V/div t=5μs/div
C4: 0.5V/div
V_{IN}=1.2V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=5Ω

Figure 15 Turn Off Response



C1: 2.00V/div C2: 2.00V/div t=160μs/div
C4: 2.00V/div
V_{IN}=5.5V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=5Ω

Figure 16 Turn On Response



C1: 2.00V/div C2: 2.00V/div t=640us/div
C3: 500mA/div C4: 5.00V/div
V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=100μF，no R_{load}

Figure 17 Inrush Current with C_{OUT}=100μF

Detailed Functional Description

The AW35131ACSR integrates a high side P channel MOSFET load switch, and provides a low on-resistance for a low voltage drop across the device. A controlled slew rate is used in applications to limit the inrush current. The part can be turned on, with a supply voltage from 1.2V to 5.5V.

Turn On/Off Control

Enable pin is an active high. The device is opened when EN pin is tied low (disable) or pulled down by internal 9.2MΩ resistor, forcing PMOS switch off. The IN/OUT path is activated with a minimum of V_{IN} of 1.2V and EN forced to high level.

Table 1. Functional Table

EN	IN to OUT	OUT to GND
Low	OFF	OFF
High	ON	OFF

Slew Rate Control

When the switch is enabled, the device regulates the gate voltage of MOSFET, and controls the V_{OUT} slew rate during t_R to avoid a large input inrush current. The feature reduces the interference to the power supply.

Quick Output Discharge

The AW35131ACSR includes the Quick Output Discharge (QOD) feature, in order to discharge the application capacitor connected on OUT pin. When EN pin is set to low level (disable state), a discharge resistance with a typical value of 87Ω is connected between the output and ground, pull down the output and prevent it from floating when the device is disabled.

PCB Layout Consideration

AW35131ACSR is a low ON-Resistance load switch, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW35131ACSR) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW35131ACSR) and close to OUT pin.

2. The AW35131ACSR integrate an up to 3A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R\theta_{JA}$ of the package can be decreased, allowing higher power dissipation. Blue bold paths on Figure 18 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

3. Use rounded corners on the power trace from the power supply connector to AW35131ACSR to decrease EMI coupling.

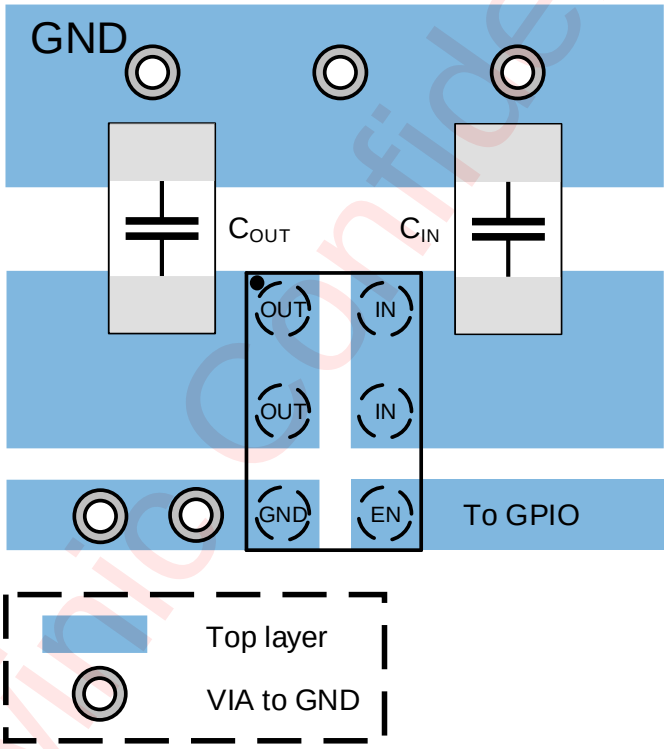
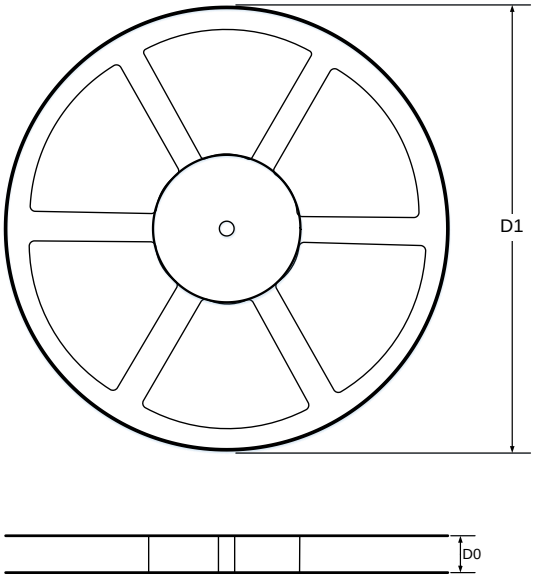


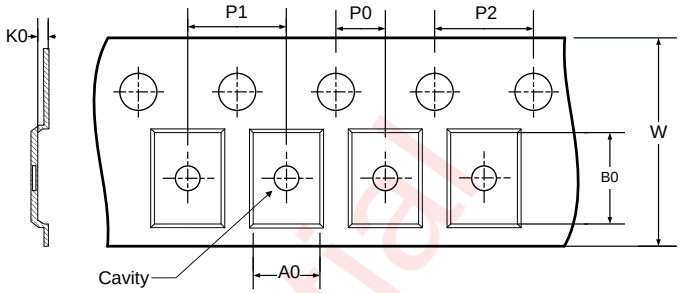
Figure 18 PCB layout example

Tape And Reel Information

REEL DIMENSIONS

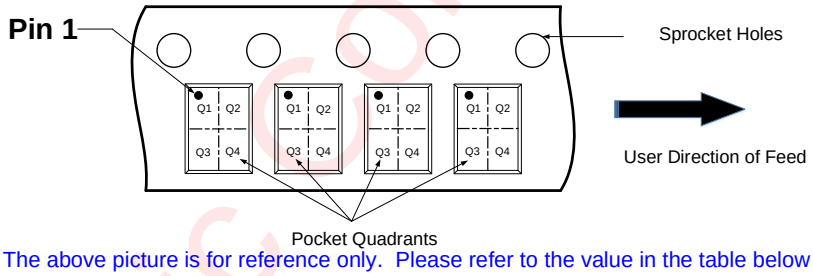


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



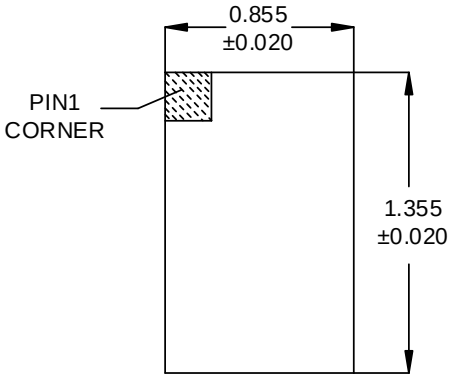
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

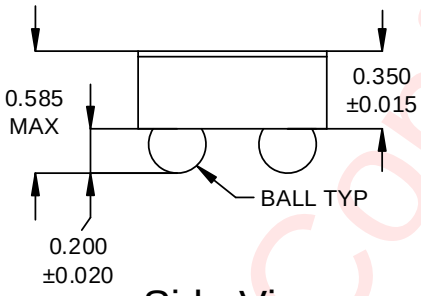
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	0.95	1.45	0.65	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

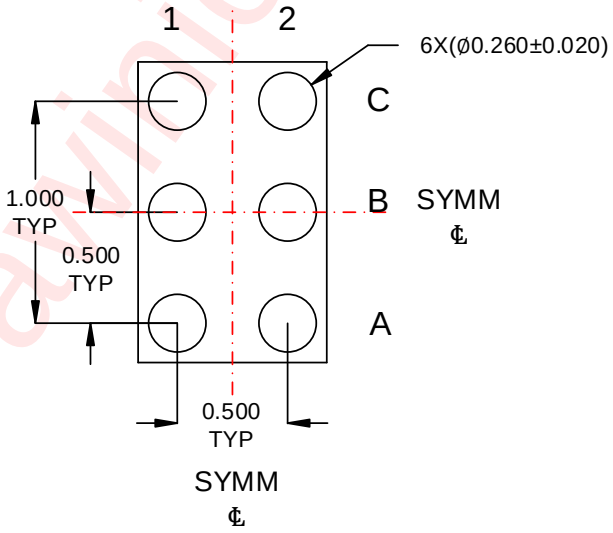
Package Description



Top View



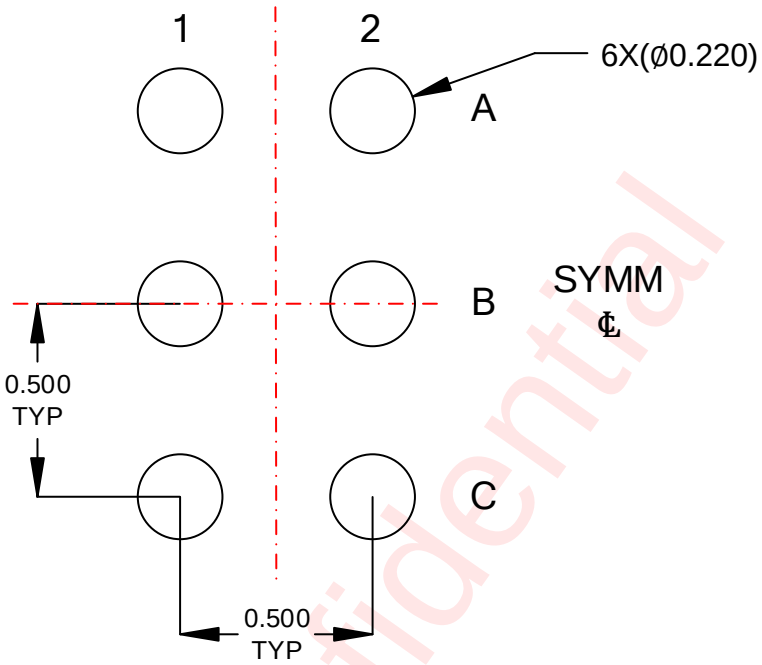
Side View

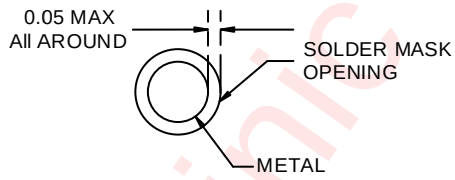


Bottom View

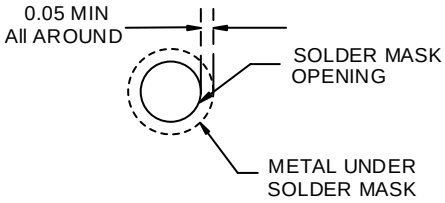
Unit: mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V0.9	Feb. 2022	Officially released
V1.0	Jun. 2022	1. Modify the parameter of Maximum Continuous Switch Current and Electrical Characteristics(P4、P5) 2. Add the Typical Characteristics(P7、P8) 3. Modify the figure of PCB layout example(P10)
V1.1	Mar. 2023	Modify the maximum value of I_Q and I_{SD} from 1000nA to 600nA(P5)

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