

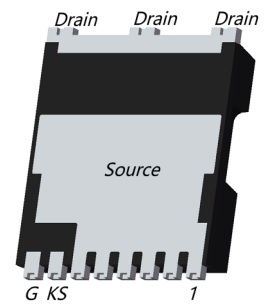
INN650TA030AH

1. General description

650V GaN-on-Silicon Enhancement-mode Power Transistor in TOLL package

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



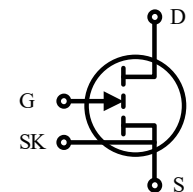
3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$ @ $V_{GS} = 6\text{ V}$	34	m Ω
$Q_{G,typ}$ @ $V_{DS} = 400\text{ V}$	16	nC
$I_{D,pulse}$	100	A
Q_{OSS} @ $V_{DS} = 400\text{ V}$	227	nC
Q_{rr} @ $V_{DS} = 400\text{ V}$	0	nC



5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	9, 10, 11	7	1, 2, 3, 4, 5, 6

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN650TA030AH	TOLL	65TA030A

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6. Maximum ratings

at $T_j = 25\text{ °C}$ unless otherwise specified

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscence sales office

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	650	V	$V_{GS} = 0\text{ V}$, $T_j = -55\text{ °C}$ to 150 °C
Drain source voltage transient ¹	$V_{DS,transient}$	800	V	$V_{GS} = 0\text{ V}$
Drain source voltage, pulsed ²	$V_{DS,pulse}$	750	V	$T_j = 25\text{ °C}$; total time < 10 h
				$T_j = 125\text{ °C}$; total time < 1 h
Continuous current, drain source	I_D	60	A	$T_c = 25\text{ °C}$
Continuous current, drain source	I_D	40	A	$T_c = 125\text{ °C}$
Pulsed current, drain source ³	$I_{D,pulse}$	100	A	$T_c = 25\text{ °C}$; $V_G = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Pulsed current, drain source ³	$I_{D,pulse}$	50	A	$T_c = 125\text{ °C}$; $V_G = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Gate source voltage, continuous	V_{GS}	-6 to +7	V	$T_j = -55\text{ °C}$ to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	$T_j = -55\text{ °C}$ to 150 °C ; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	462	W	$T_c = 25\text{ °C}$
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1 $V_{DS,transient}$ is intended for non-repetitive events, $t_{PULSE} < 200\text{ }\mu\text{s}$

2 $V_{DS,pulse}$ is intended for repetitive pulse, $t_{PULSE} < 100\text{ ns}$

3 Limit was extracted from characterization test, not measured during production

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal Resistance Junction to ambient	R_{thJA}^1	40	°C/W	
Thermal resistance, junction-case (bottom)	R_{thJC}	0.27	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

1. R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board

8. Electric characteristics

 at $T_j = 25\text{ °C}$, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	$I_D = 91\text{ mA}; V_{DS} = V_{GS}; T_j = 25\text{ °C}$
		-	1.6	-		$I_D = 91\text{ mA}; V_{DS} = V_{GS}; T_j = 150\text{ °C}$
Drain-source leakage current	I_{DSS}	-	5	100	μA	$V_{DS} = 650\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$
		-	50	-		$V_{DS} = 650\text{ V}; V_{GS} = 0\text{ V}; T_j = 150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	250	-	μA	$V_{GS} = 6\text{ V}; V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	26	34	m Ω	$V_{GS} = 6\text{ V}; I_D = 16\text{ A}; T_j = 25\text{ °C}$
		-	55	-		$V_{GS} = 6\text{ V}; I_D = 16\text{ A}; T_j = 150\text{ °C}$
Gate resistance	R_G	-	1.2	-	Ω	$f = 5\text{ MHz}; \text{open drain}$

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	655	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	309	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Reverse transfer Capacitance	C_{rss}	-	3.7	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	428	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	567	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{OSS}	-	227	-	nC	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	53	-	ns	$V_{DS} = 400\text{ V}; I_D = 30\text{ A}; L_{parasitic} = 8\text{ nH}; V_{GS} = 6\text{ V}; R_{on} = 10\text{ }\Omega; R_{off} = 2\text{ }\Omega;$ See Figure 22
Turn-off delay time	$t_{d(off)}$	-	8	-	ns	
Rise time	t_r	-	24	-	ns	
Fall time	t_f	-	9	-	ns	

 1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

 2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	16	-	nC	$V_{GS} = 0$ to 6 V; $V_{DS} = 400$ V; $I_D = 50$ A
Gate-source charge	Q_{GS}	-	2	-	nC	
Gate-drain charge	Q_{GD}	-	8	-	nC	
Gate Plateau Voltage	V_{Plat}	-	3.4	-	V	$V_{DS} = 400$ V; $I_D = 50$ A

Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	3.5	-	V	$V_{GS} = 0$ V; $I_S = 50$ A
Pulsed current, reverse	$I_{S,pulse}$	-	-	70	A	$V_{GS} = 6$ V; $t_{PULSE} = 10$ μ s
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_S = 50$ A; $V_{DS} = 400$ V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

at $T_j = 25\text{ }^\circ\text{C}$, unless specified otherwise

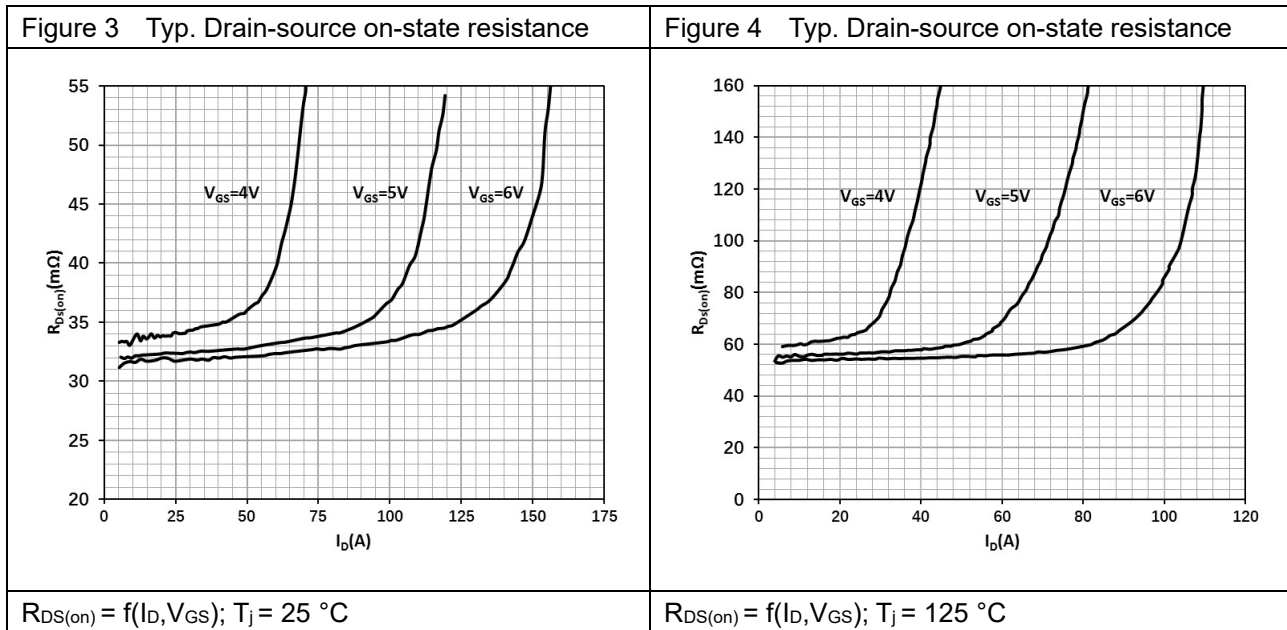
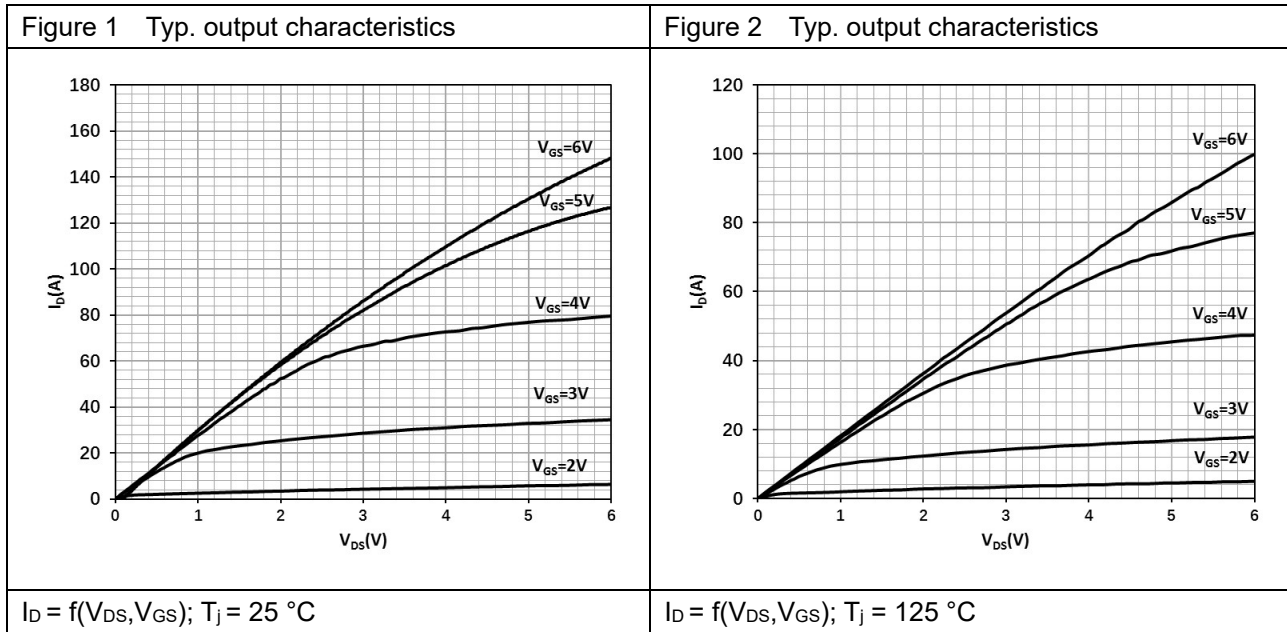
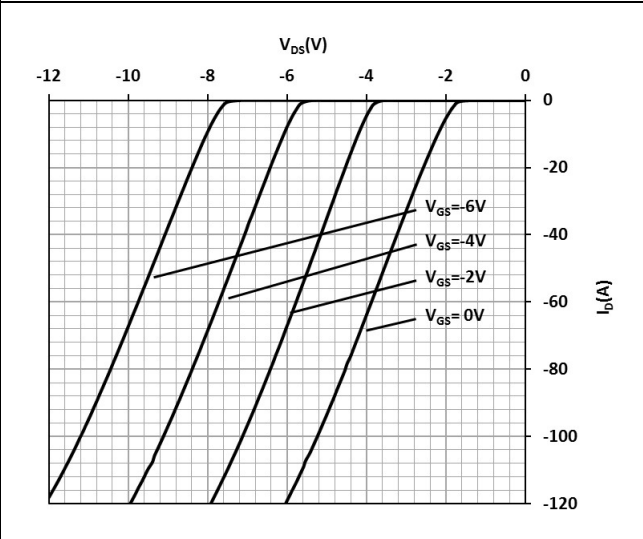
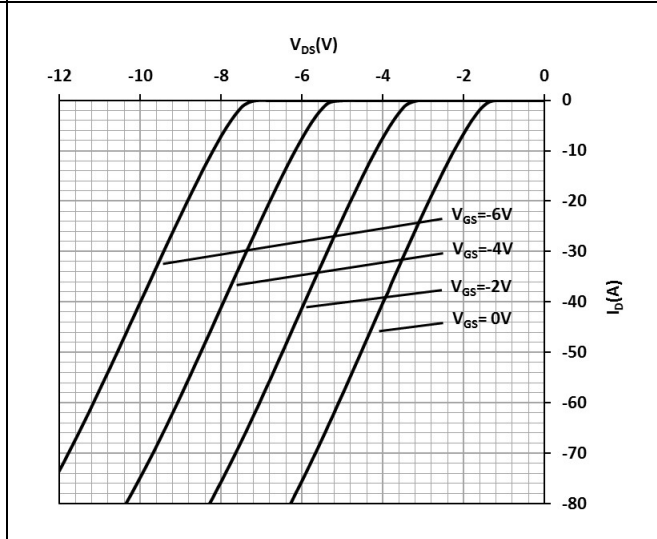


Figure 5 Typ. channel reverse characteristics



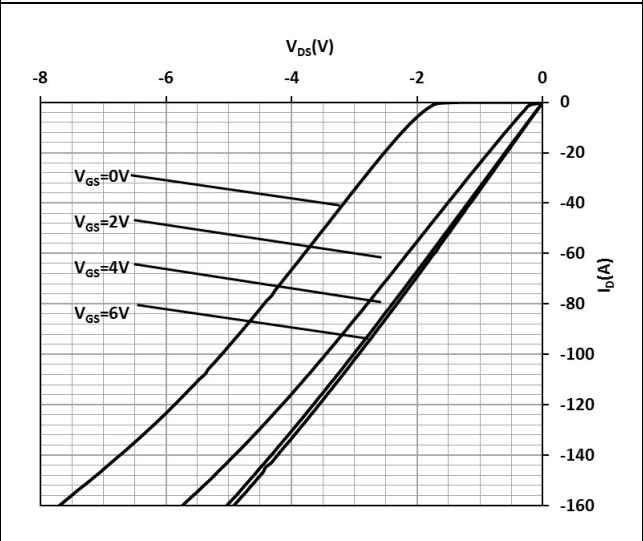
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^\circ\text{C}$

Figure 6 Typ. channel reverse characteristics



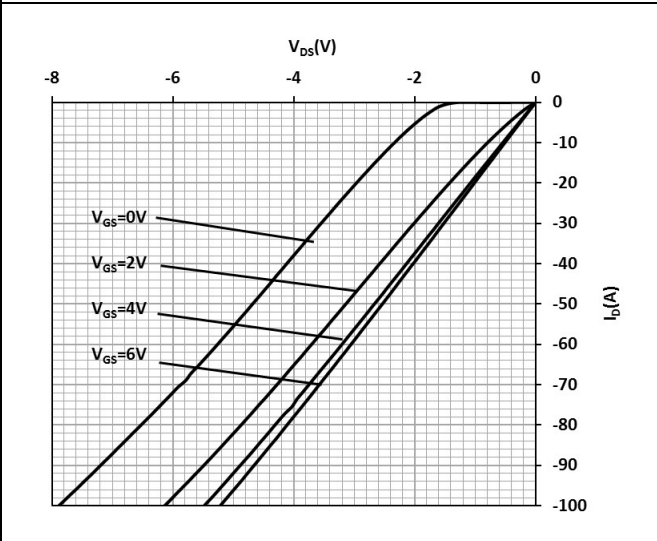
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^\circ\text{C}$

Figure 7 Typ. channel reverse characteristics



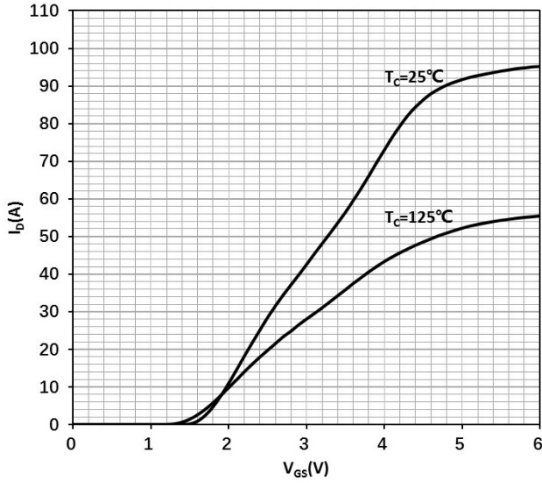
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^\circ\text{C}$

Figure 8 Typ. channel reverse characteristics



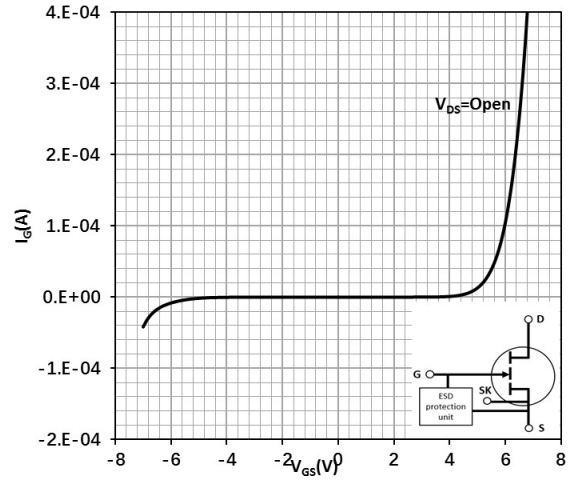
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^\circ\text{C}$

Figure 9 Typ. transfer characteristics



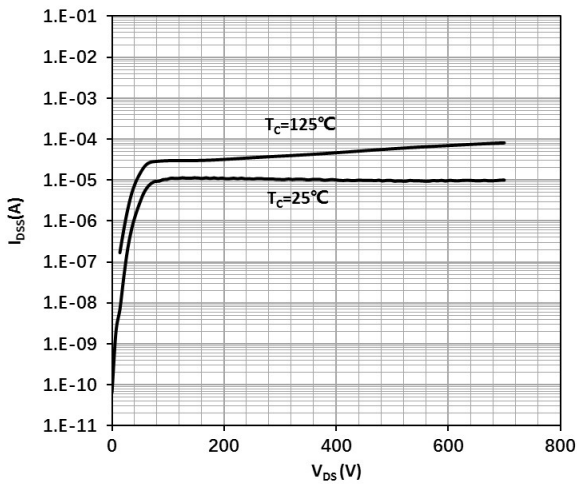
$I_D = f(V_{GS}); V_{DS} = 3 \text{ V}$

Figure 10 Typ. Gate-to-Source leakage



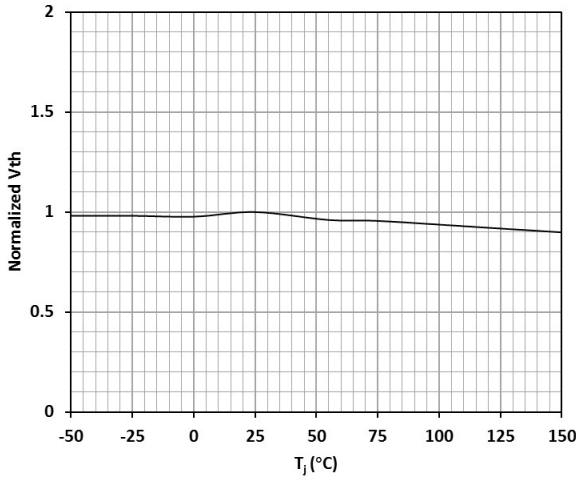
$I_G = f(V_{GS}); I_G$ reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



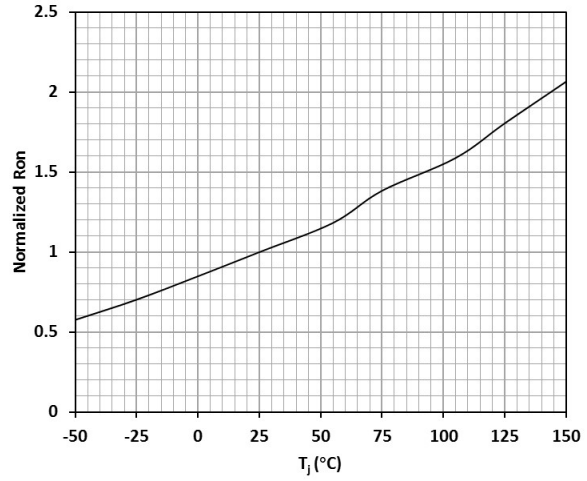
$I_{DSS} = f(V_{DS}); V_{GS} = 0 \text{ V}$

Figure 12 Gate threshold voltage



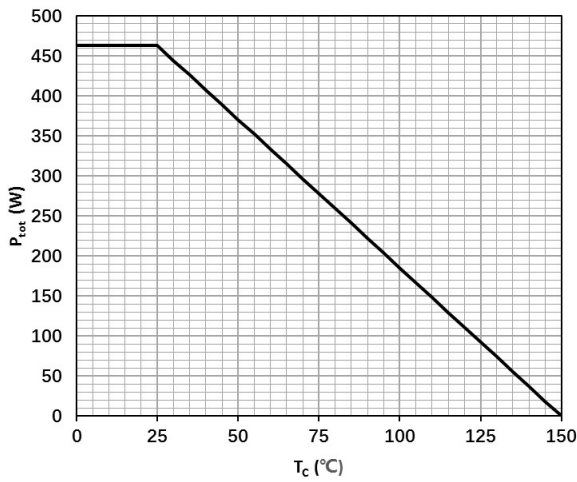
$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 91 \text{ mA}$

Figure 13 Drain-source on-state resistance



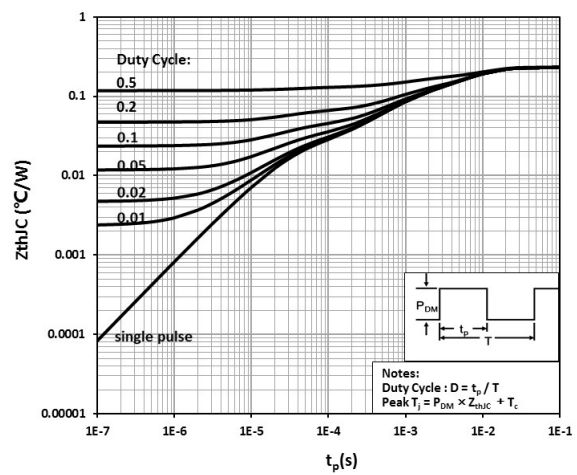
$R_{DS(on)} = f(T_j); I_D = 16 \text{ A}; V_{GS}=6\text{V}$

Figure 14 Power dissipation



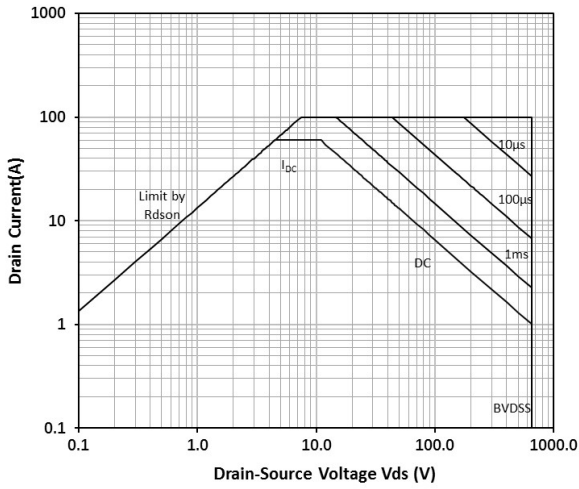
$P_{tot} = f(T_c)$

Figure 15 Max.transient thermal impedance



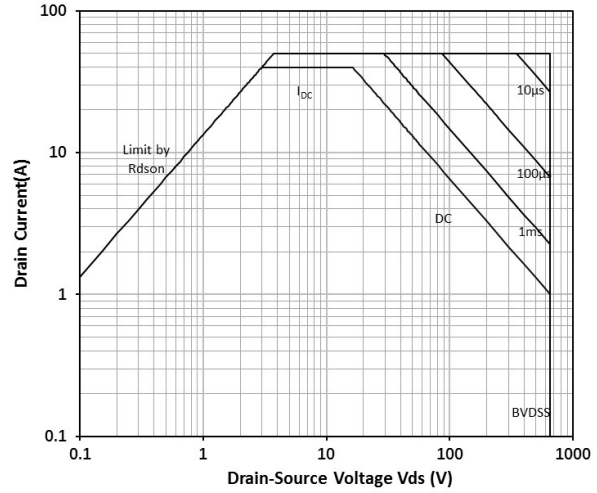
$Z_{thJC} = f(t_p, D)$

Figure 16 Safe operating area



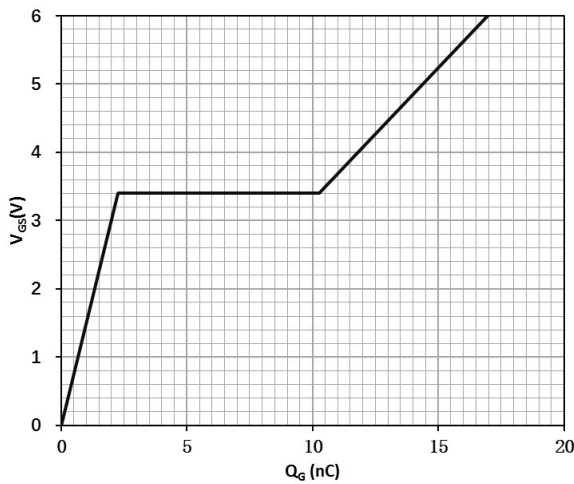
$I_D = f(V_{DS}); T_C = 25\text{ }^\circ\text{C}$

Figure 17 Safe operating area



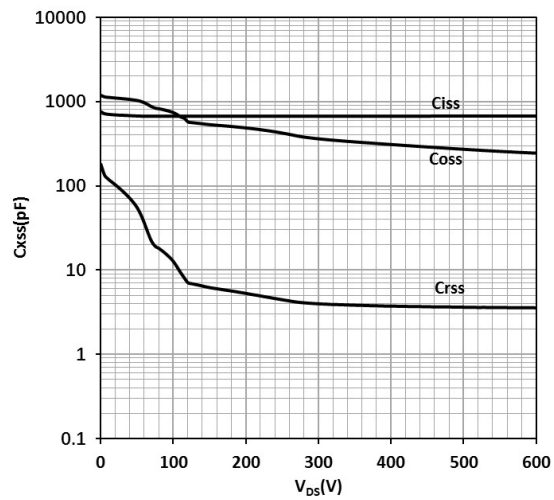
$I_D = f(V_{DS}); T_C = 125\text{ }^\circ\text{C}$

Figure 18 Typ. gate charge



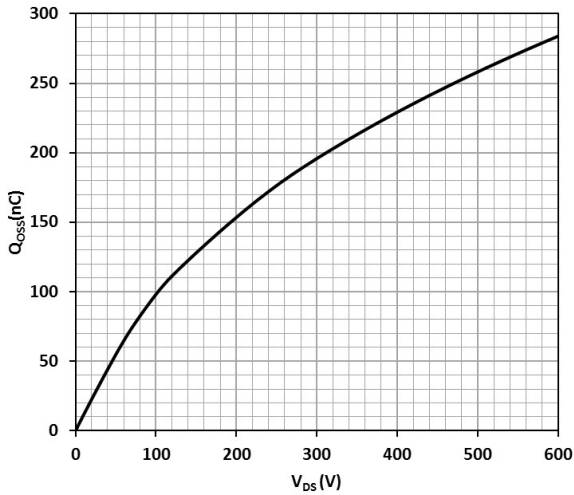
$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 16\text{ A}$

Figure 19 Typ. capacitances



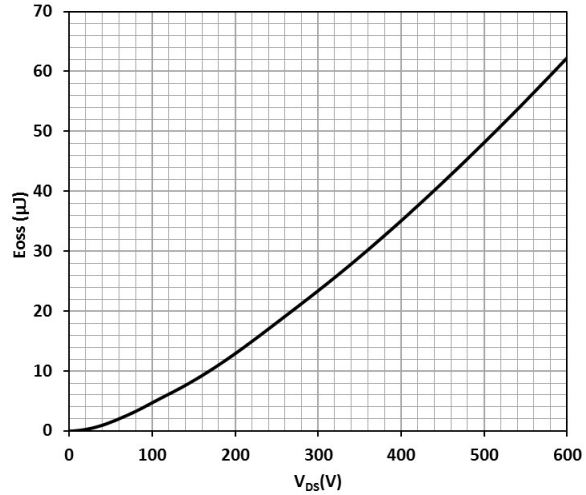
$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$

Figure 20 Typ. output charge



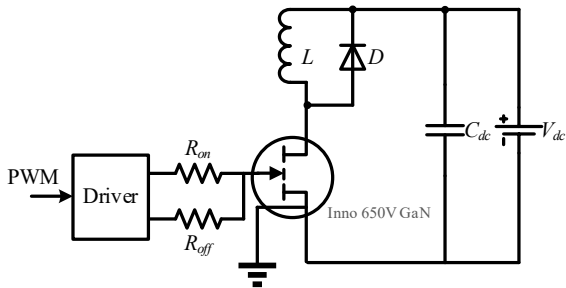
$Q_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 21 Typ. Coss stored Energy



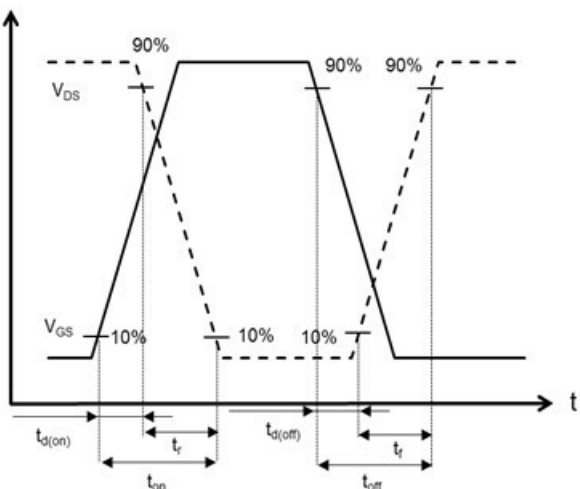
$E_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 22 Typ. Switching times with inductive load

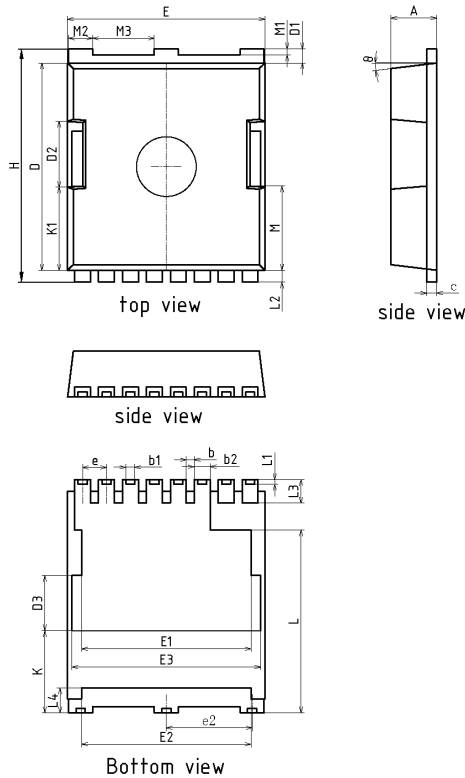


$V_{DS} = 400 \text{ V}, I_D = 30 \text{ A}, L_{\text{parasitic}} = 8 \text{ nH}, V_{GS} = 6 \text{ V},$
 $R_{on} = 10 \Omega, R_{off} = 2 \Omega$

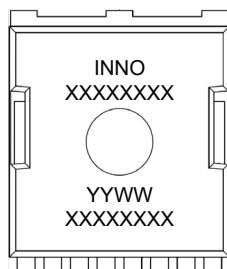
Figure 23 Typ. Switching times waveform



10. Package outlines



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.30	2.45
b	0.30	0.40	0.50
b1	0.31	0.43	0.55
b2	0.65	0.80	0.90
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	0.50	0.70	0.90
D2	3.30REF		
D3	2.77REF		
E	9.70	9.90	10.10
E1	8.50REF		
E2	8.50REF		
E3	9.46REF		
e	1.10	1.20	1.30
H	11.48	11.68	11.88
K	4.08REF		
K1	4.18REF		
L	9.13REF		
L1	0.23REF		
L2	0.50	0.60	0.70
L3	1.00	1.20	1.40
L4	1.00	1.20	1.40
M	4.18REF		
M1	0.26REF		
M2	1.10	1.20	1.30
M3	3.10REF		
Θ	10.00REF		
e2	4.20	4.30	4.40

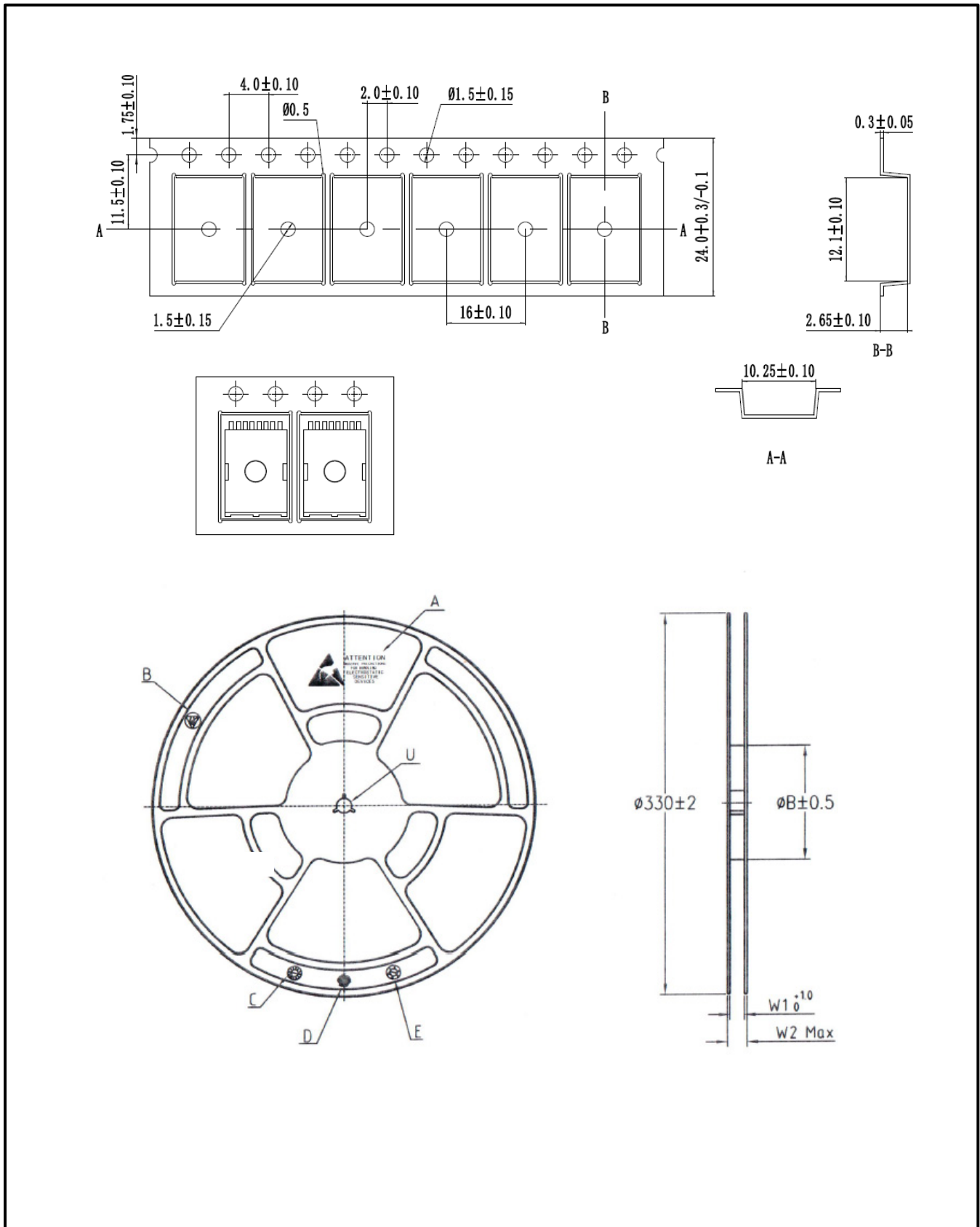


Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXXX
Row3	Date code	YYWW
Row4	ASSY lot No.	XXXXXXXX

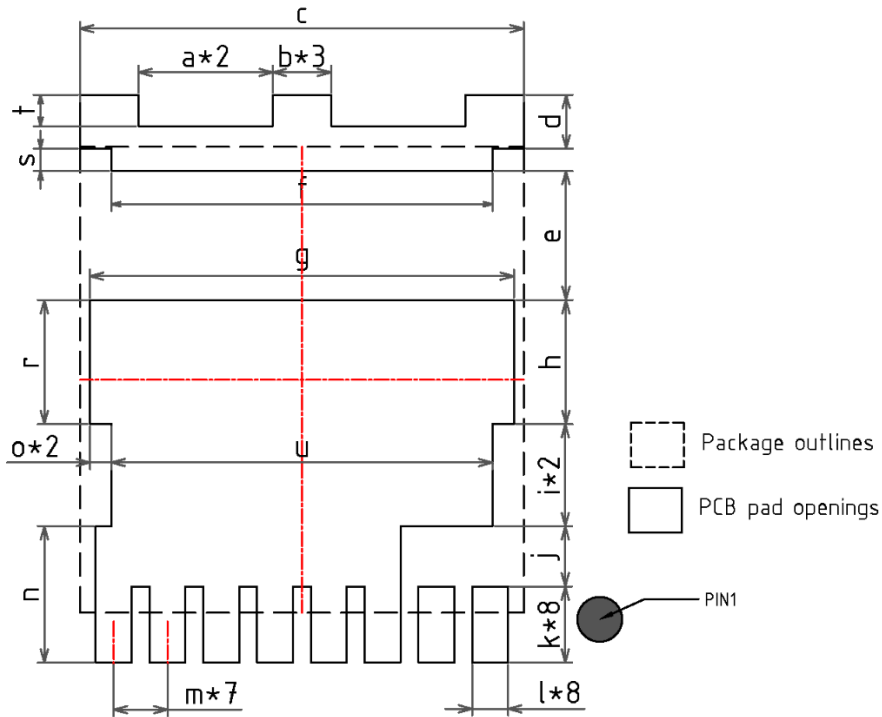
Notes:

- (1) Dimensioning and tolerancing confirm to ASME Y14.5M-1994
- (2) All dimensions are in millimeters, angles are in degrees
- (3) Coplanarity applies to the exposed heat slug as well as the terminal
- (4) Radius on terminal is optional
- (5) General tolerance: ± 0.10 mm

11. Reel information



12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	3.00	k	1.70
b	1.30	l	0.80
c	9.90	m	1.20
d	1.20	n	3.05
e	2.88	o	0.48
f	8.50	r	2.77
g	9.46	s	0.50
h	2.77	t	0.70
i	2.28	u	8.50
j	1.35	/	/

Notes:
 (1) All dimension are in millimeters.
 (2) Drawing is not to scale.

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-01-31	1.0 version release
1.1	2024-04-12	Update the reel information

Important Notice

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