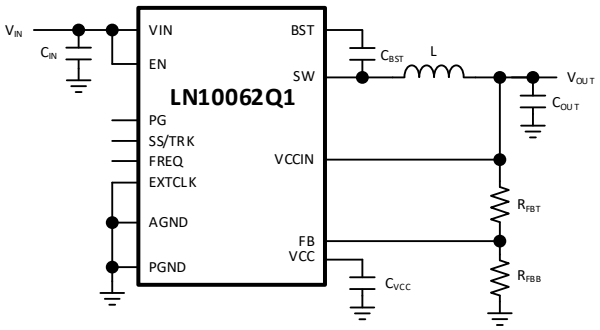
3.5V to 60V, 2.5A/3A， Synchronous Step-Down Regulator

1 FEATURES

- Automotive AEC-Q100 Grade 1 Compliance
- Ultra-Low Quiescent Current 27μA in Regulation
- Wide V_{IN} Range: 3.5V to 60V
- Wide V_{OUT} Range: 1V to V_{IN}
- Integrated both High-Side and Low-Side Power MOSFETs with up to 2.5A/3A Output Capability
- Programmable Fixed Frequency Range: 200kHz to 2.5MHz
- PLL Synchronization to External Clock
- Adjustable Soft Start and Tracking Capability
- High Efficiency Low Load DCM and PFM Operation
- Automatic Transition into Bypass LDO to Increase Low-Load Efficiency
- Near 100% Duty Cycle Operation for Low Drop Out Operation
- Low Minimum On-Time: 109 ns
- Accurate Peak and Valley Clamp and Protection
- Internal Compensation
- Spread Spectrum for Low EMI Applications
- Power Good Indicator
- Accurate VIN UVLO Protection
- Over-Temperature Shutdown and Recovery
- Output Short-Circuit Protection with Hiccup Mode
- Thermally Enhanced TSSOP-EP16 Package (5mm X 4.4mm X 1.2mm)



LN10062Q1 Typical Application Diagram

2 APPLICATIONS

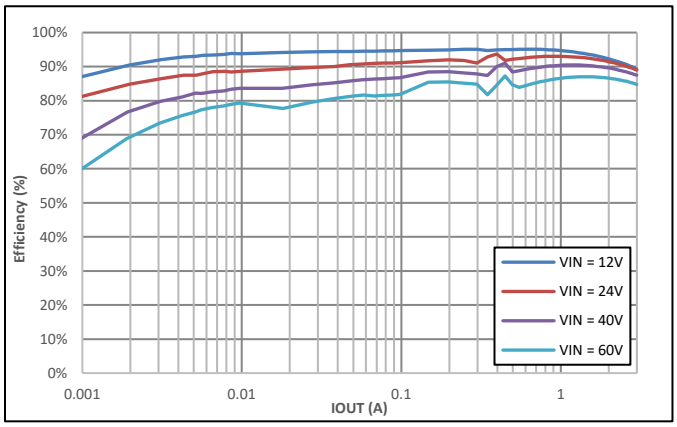
- Automotive Power Supplies
- Industrial Power Supplies
- Battery Powered Systems

3 DESCRIPTION

The LN10X62/3Q1 is a high efficiency, compact, synchronous step-down DC-DC converter employing a constant frequency, peak current mode control architecture with internal compensation. It operates from an input voltage from 3.5V to 60V, provides an adjustable output voltage from 1V to V_{IN}. LN10X62Q1 can deliver to 2.5A of output current, while LN10X63Q1 can deliver up to 3.0A. The switching frequency range is from 200kHz to 2.5MHz。

Device Information Table

Part Number	Package	Dimension
LN10062Q1	TSSOP-EP16	5mm x 4.4mm x 1.2mm
LN10063Q1	TSSOP-EP16	5mm x 4.4mm x 1.2mm
LN10162Q1	TSSOP-EP16	5mm x 4.4mm x 1.2mm
LN10163Q1	TSSOP-EP16	5mm x 4.4mm x 1.2mm



LN10063Q1 400kHz Effciency Chart

Patent Number: ZL 2017 1 0954815. 7 (China)

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4 REVISION HISTORY

Version	Change Description	Date
1.0	Initial Version	2020/07/16
1.1	Update Chapter 7.1 Table “Absolute Maximum Ratings”·····P8	2020/10/10
1.2	Update Table “order information”·····P5 Update conditions of $I_{Q-NONSW}$, $I_{VCCIN-NONSW}$ and I_{SHDN}, add maximum data·····P10 Update conditions of V_{FB-CCM}·····P10 Update typical and maximum of I_{Q-FB}·····P10 Update maximum and minimum of EN parameters·····P11 Update maximum and minimum of $V_{CCIN-ON}$·····P12 Update description of PG parameters·····P13 Update maximum and minimum of SS parameters·····P13 Update efficiency and regulation curves·····P14 Update conditions of EMI curves·····P19 Update package information·····P33	2021/08/31
1.3	Update package information·····P33	2022/04/26

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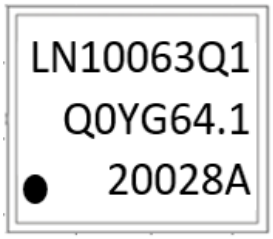
5 ORDER INFORMATION

Device	Output Current	Spread Spectrum	IC Package	MSL-Peak-Temp (1)	Material	Package	Package Qty	Top Marking (2)
LN10062Q1-AKR	2.5A	No	TSSOP-EP16	Level-3-260C	RoHS	Tape & Reel	3000	See illustration
LN10063Q1-AKR	3A	No	TSSOP-EP16	Level-3-260C	RoHS	Tape & Reel	3000	See illustration
LN10162Q1-AKR	2.5A	Yes	TSSOP-EP16	Level-3-260C	RoHS	Tape & Reel	3000	See illustration
LN10163Q1-AKR	3A	Yes	TSSOP-EP16	Level-3-260C	RoHS	Tape & Reel	3000	See illustration

(1) MSL (Moisture Sensitivity Level) and the highest solder temperature are based on JEDEC industrial standard.



Line 1: Product Mark Code

Line 2: Lot ID

Line 3: Date Code

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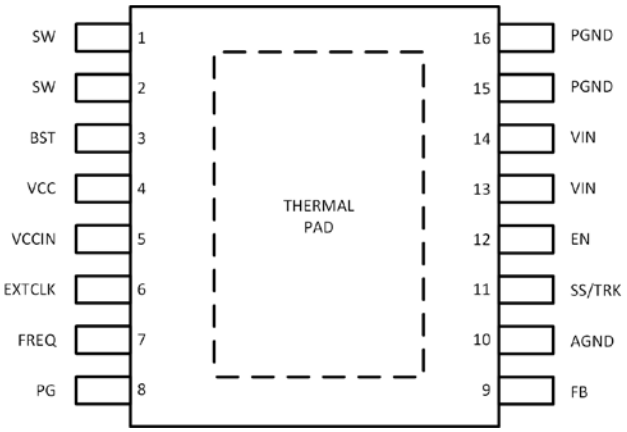
6 PIN CONFIGURATION

6.1 Pin Configuration

TSSOP-EP16 (5mm X 4.4mm X 1.2mm)

Top View



6.2 Pin Functions

Name	PIN Number	Type	Description
SW	1,2	Power	Switch node connection from the internal power MOSFETs to the external inductor.
BST	3	Power	Bootstrapped supply to the high side gate driver. Connect a 100nF ceramic capacitor between BST and SW pins.
VCC	4	Power	Voltage source that powers the gate drivers of the internal power MOSFETs and control circuits. Must be decoupled to PGND with 1-4.7µF ceramic capacitor. This voltage source is provided by one of the two internal LDO regulators with input from V_{IN} or V_{CCIN}.
VCCIN	5	Power	External power input to an auxiliary internal V_{CCIN} LDO regulator. This LDO supplies V_{CC} power from V_{CCIN}, bypassing the internal V_{IN} LDO regulator powered from V_{IN} when V_{CCIN} is above the switchover threshold.
EXTCLK	6	Signal	External synchronization clock input.
FREQ	7	Signal	Switching frequency control pin. Place a resistor between this pin and AGND to set the switching frequency between 200kHz and 2.5MHz.
PG	8	Signal	Open-drain power good output. V_{FB} is monitored and when V_{FB} is not within the regulation window. PG pin is pulled low.
FB	9	Signal	Output voltage feedback input. Use an external divider to set the desired output voltage.
AGND	10	Ground	Analog ground.

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SS/TRK	11	Signal	Soft-start and tracking pin. The voltage on this pin sets the limit for internal reference voltage for regulation target. To use the internal soft-start ramp, leave this pin open. A capacitor between this pin and the analog ground sets the ramp time for output voltage during startup. This pin can also be driven by an external voltage ramp. When the external voltage is less than the internal ramp voltage, the output voltage tracks the external voltage ramp.
EN	12	Signal	Enable pin for V_{CC} LDOs, regulator output, and input voltage for V_{IN} UVLO. Connect to V_{IN} directly, to V_{IN} through a divider, or to an external voltage source.
VIN	13,14	Power	Power supply input pin to high side power MOSFET and V_{IN} LDO regulator. Decouple this pin to PGND with ceramic capacitors.
PGND	15,16	Ground	Power ground. Connect the pins to ground plane.
THERMAL PAD	-	-	Thermal dissipation pad. Solder to ground plane.

6.3 Package Thermal Parameters

Parameter (1)		TSSOP-EP16	Units
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	38	˚C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	3	˚C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p, under no wind , 2W loss, and 25 ˚C ambient temperature.

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7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Parameters	Min	Max	Unit
VIN to PGND	-0.3	65	V
EN to PGND	-0.3	V_{IN}	
FB, FREQ, SS/TRK to AGND	-0.3	V_{CC}	
PG to AGND	-0.3	36	
EXTCLK to AGND	-0.3	5.5	
VCCIN to PGND	-0.3	36	
VCC to PGND	-0.3	5.5	
SW to PGND	-1.0	V_{IN}+0.3	
SW to PGND （Overshoot voltage less than 10ns）	-3.5	65	
BST to SW	-0.3	5.5	
AGND to PGND	-0.3	0.3	
Ambient Temperature	-40	125	˚C
Junction Temperature	-40	150	
Storage Temperature	-65	150	

7.2 ESD Ratings

Parameters	Min	Max	Unit
HBM Human Body Model		±3000	V
CDM Charge Device Model		±1000	

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7.3 Recommented Operating Condition

Parameters	Min	Max	Unit
VIN	3.5	60	V
EN	-0.3	V_{IN}	
FB	-0.3	1.1	
PG	-0.3	30	
EXTCLK	-0.3	5.5	
VCCIN	-0.3	30	
AGND to PGND	-0.1	0.1	
Output voltage	1	V_{IN}	
LN10X62Q1 output current	0	2.5	A
LN10X63Q1 output current	0	3	A
Ambient temperature	-40	125	˚C
Junction temperature	-40	125	

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7.4 Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 125˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz。

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VOUT (VIN PINS)						
V_{IN}	Operating Input Voltage Range		3.5		60	V
V_{OUT}	Operating Output Voltage Range		1		V_{IN}	V
$I_{Q-NONSW}$	VIN Supply Current	V_{EN} = 3.3V, V_{FB} = 1.5V, V_{CCIN} = 3.4V external V_{IN} = 24V		4.25	6.8	μA
$I_{VCCIN-NONSW}$	VCCIN Supply Current	V_{EN} = 3.3V, V_{FB} = 1.5V, V_{CCIN} = 3.4V external V_{IN} = 24V		58	77	μA
I_Q	During Regulation	V_{EN} = V_{IN} = 24V, V_{CCIN} = V_{OUT} = 5V, I_{OUT} = 0A		27		μA
I_{SHDN}	Shutdown Quiescent Current	V_{EN} = 0V, V_{IN} = 24V		1.3	2.2	μA
FB PIN						
V_{FB-CCM}	Regulated Feedback Voltage in CCM Mode	V_{IN} = 24V, @25C	0.992	1.0	1.008	V
		Full V_{IN} Range, Full Load Range, Full Operational Temperature Range	0.98	1.0	1.02	V
I_{Q-FB}	Feedback Input Leakage Current	V_{FB} = 1.0 V		0	100	nA
POWER MOSFETS						
$R_{DSON-HS}$ (1)	High Side MOSFET ON Resistance	I_{OUT} = 1A, V_{BST} - V_{SW} = 5V		180		mΩ
$R_{DSON-LS}$ (1)	Low Side MOSFET ON Resistance	I_{OUT} = 1A, V_{CC} = 5V		101		mΩ
PWM						
T_{ON-MIN}	Minimum ON Time			109		ns
$T_{OFF-MIN}$	Minimum OFF Time			134		ns

(1) Measured at pins.

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Electrical Characteristics (Continued)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 125˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz。

OSCILLATOR (FREQ PIN)						
$F_{OSC-INT}$	Default Frequency	FREQ Pin Floating		400		kHz
$F_{OSC-400kHz}$	Default Frequency	R_{FREQ} = 210kOhm	350	400	450	kHz
F_S	Adjustable Frequency Range	With 1% Resistor at FREQ Pin	0.2		2.5	MHz
SYNCHRONIZATION (EXTCLK PIN)						
F_{EXTCLK}	EXTCLK Frequency Range		0.2		2.5	MHz
$V_{EXTCLK-HIGH}$	EXTCLK High-Level Threshold		2.0			V
$V_{EXTCLK-LOW}$	EXTCLK Low-Level Threshold				0.4	V
$D_{EXTCLK-MAX}$	EXTCLK Maximum Duty Cycle			90%		%
$D_{EXTCLK-MIN}$	EXTCLK Minimum Duty Cycle			10%		%
$T_{EXTCLK-MIN}$	Minimum EXTCLK ON and OFF Time			80		ns
SPREAD SPECTRUM MODULATION (2)						
ΔF_S	Spread Spectrum Modulation Frequency Range			-18		%
F_{SSM}	Spread Spectrum Modulation Frequency			16		kHz
ENABLE V_{IN} UVLO (EN PIN)						
EN_{VCC-ON}	V_{EN} High-Level Threshold	V_{EN} Rising	1.83			V
$EN_{VCC-OFF}$	V_{EN} Low-Level Threshold	V_{EN} Falling			0.4	V
$EN_{VOUT-ON}$	V_{IN} UVLO Rising Threshold	V_{EN} Rising	1.92	2.08	2.25	V
$EN_{VOUT-HYS}$	V_{IN} UVLO Hysteresis	V_{EN} Falling		-200		mV
I_{Q-EN}	EN Pin Current	V_{EN} = 3.3V		0	0.2	μA

(2) This Function is available on LN1016XQ1 Only.

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Electrical Characteristics (Continued)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 125˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz。

INTERNAL VCC LDOS (VCC, VCCIN, AND VIN PINS)						
$V_{CC-TARGET}$	V_{CC} Regulation Target			4.75		V
$V_{CC-UVLO-H}$	V_{CC} UVLO Rising Threshold	V_{CCIN} Rising	2.59	2.75	2.90	V
$V_{CC-UVLO-L}$	V_{CC} UVLO Falling Threshold	V_{CCIN} Falling	2.45	2.60	2.71	V
$V_{CCIN-ON}$	V_{CCIN} Switchover Rising Threshold	V_{CCIN} Rising	2.72	3.0	3.14	V
	V_{CCIN} Switchover Hysteresis	Hysteresis		-100		mV
BOOTSTRAP (BST PIN)						
$t_{REFRESH-PER}$	Auto-Refresh Period			26		µs
OVER CURRENT PROTECTION (3)						
$I_{LIM-PEAK-2.5A}$	Peak Current Limit Threshold	LN10X62Q1		4.2		A
$I_{LIM-VALLEY-2.5A}$	Valley Current Limit Threshold			2.7		A
$I_{LIM-PEAK-3A}$	Peak Current Limit Threshold	LN10X63Q1		4.7		A
$I_{LIM-VALLEY-3A}$	Valley Current Limit Threshold			3.2		A
THERMAL SHUTDOWN (4)						
OT	Thermal Shutdown Threshold			160		˚C
OT_{HYS}	Thermal Shutdown Recovery Hysteresis			-10		˚C

(3) The current limits are measured in close-loop regulation with typical application in Figure 38. Due to inherent delays in the current limit comparators and drivers, the current limits measured in other applications may be different.

(4) Guaranteed by design.

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Electrical Characteristics (Continued)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 125˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz。

POWER GOOD (PG AND FB PINS) (5)						
V_{PG-OV}	Power Good Over-Voltage Rising Threshold	V_{FB} Ramping Up		111%	118%	%
V_{PG-UV}	Power Good Under-Voltage Falling Threshold	V_{FB} Ramping Down	81%	87%		%
$V_{PG-OV-HYS}$	Power Good Over-Voltage Recovery Hysteresis	% of FB voltage		3.7%		
$V_{PG-UV-HYS}$	Power Good Under-Voltage Recovery Hysteresis	% of FB voltage		3.7%		
V_{PG-PD}	Power Good Pull-Down Strength	I_{PG} = 1mA		40		mV
$t_{PG-RISING}$	Power Good Flag Rising Delay			320		µs
$t_{PG-FALLING}$	Power Good Flag Falling Delay			320		µs
I_{Q-PG}	PG Leakage Current	V_{PG} = 5V		10		nA
SOFT START, TRACKING (SS/TRK PIN)						
t_{SS-INT} (6)	Internal Soft-Start Time	SS Pin Float	2.4	5.1	8.4	ms
$I_{SS-CHARGE}$	Soft-Start Charge Current	V_{SS} = 0V	1.76	2.6	3.6	µA
$R_{SS-DISCHARGE}$	Soft-Start Discharge Resistance	V_{CCIN} = 0V V_{IN} = 24V	6.8	7.5	8.9	kΩ

(5) Power Good Thresholds are parameters of VFB with respect to V_{FB-CCM}

(6) Measured from $EN_{VOUT-ON}$ to soft start done.

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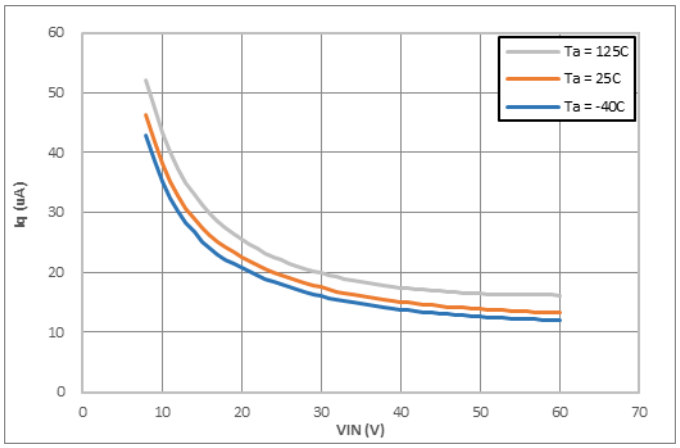
7.5 Typical Characteristics

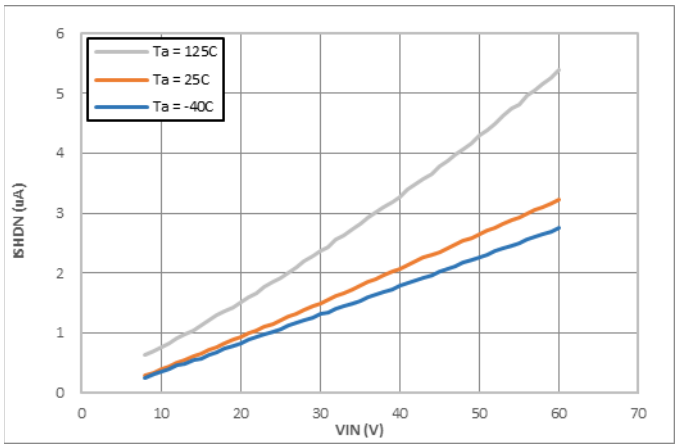
7.5.1 Characteristics Over Temperature

Unless otherwise stated, the test conditions are the same as Chapter 7.4. T_J = -40˚C 到 125˚C。



EN=5V, V_{CCIN} = V_{OUT} = 5V, No load

Figure 1. I_Q

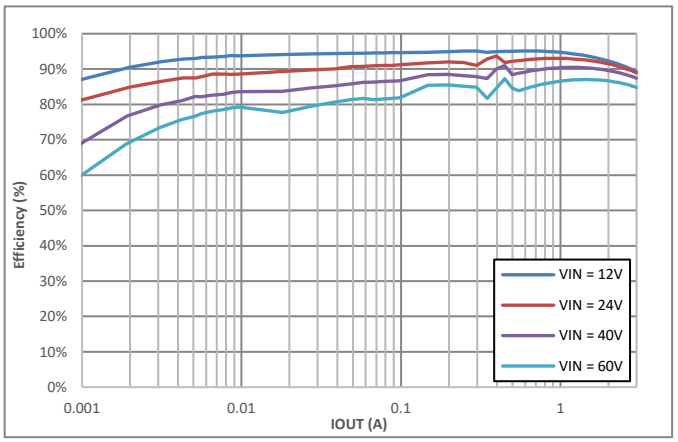


V_{EN} = 0V

Figure 2. I_{SHDN}

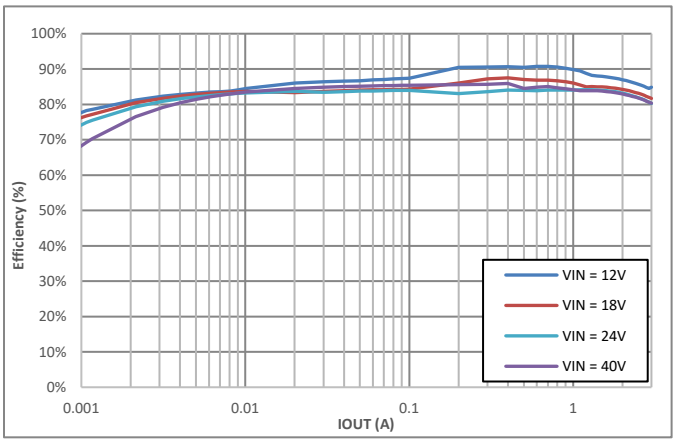
7.5.2 Typical Characteristics

Unless otherwise stated, the test conditions are： V_{IN} = 24V, V_{CCIN} = V_{OUT} = 5V, F_S = 400kHz, L = 10µH, T_A = 25˚C。



LN10063Q1, F_S = 400kHz, V_{OUT} = 5V

Figure 3. Efficiency Curves



LN10063Q1, F_S = 2.2MHz, V_{OUT} = 5V

Figure 4. Efficiency Curves

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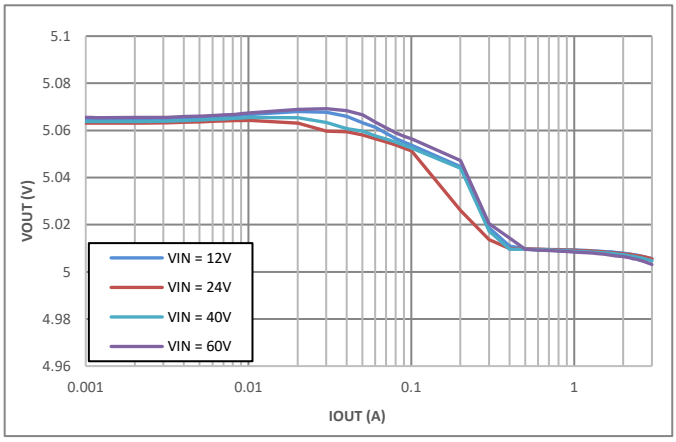
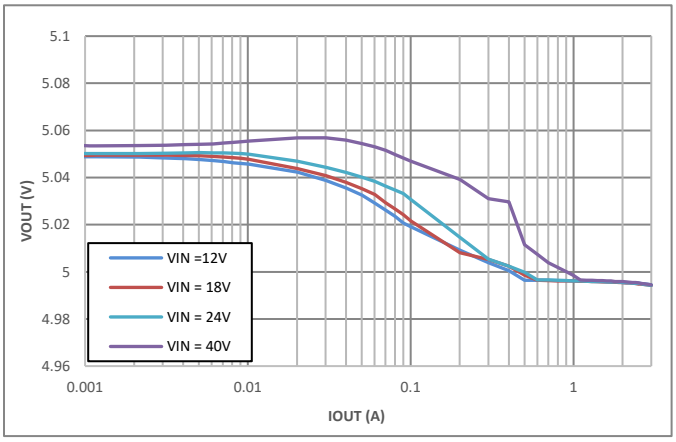
Typical Characteristics (Continued)

Unless otherwise stated, the test conditions are： V_{IN} = 24V, V_{CCIN} = V_{OUT} = 5V, F_S = 400kHz, L = 10µH, T_A = 25˚C。



LN10063Q1, F_S = 400kHz, V_{OUT} = 5V

Figure 5. Load Regulation



LN10063Q1, F_S = 2.2MHz, V_{OUT} = 5V

Figure 6. Load Regulation

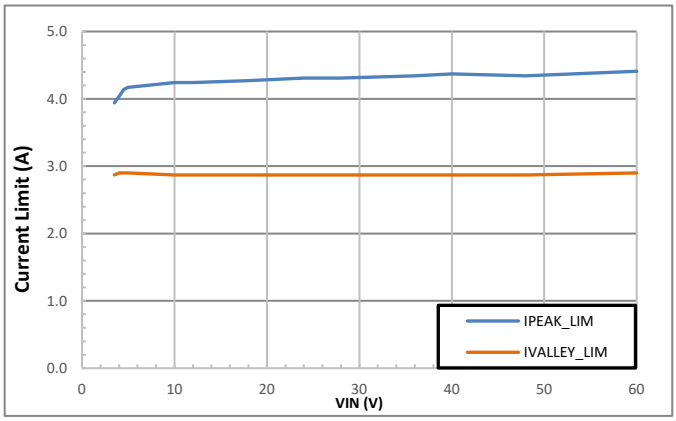


Figure 7. LN10062Q1 Peak Current and Valley Current Limit Vs. V_{IN}

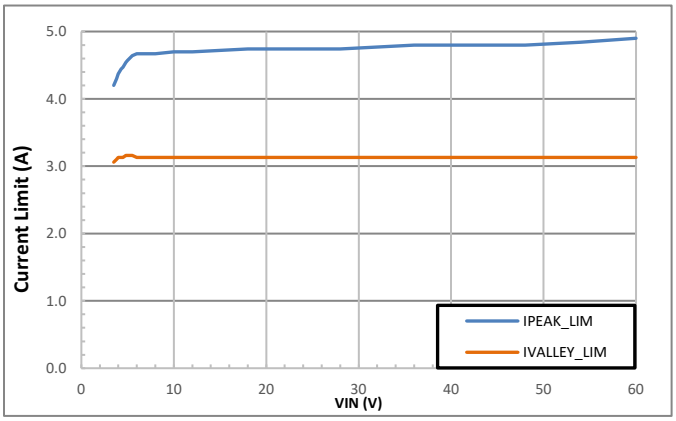
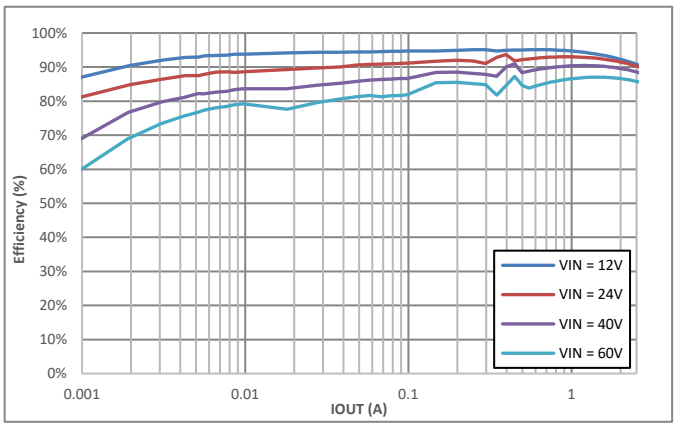
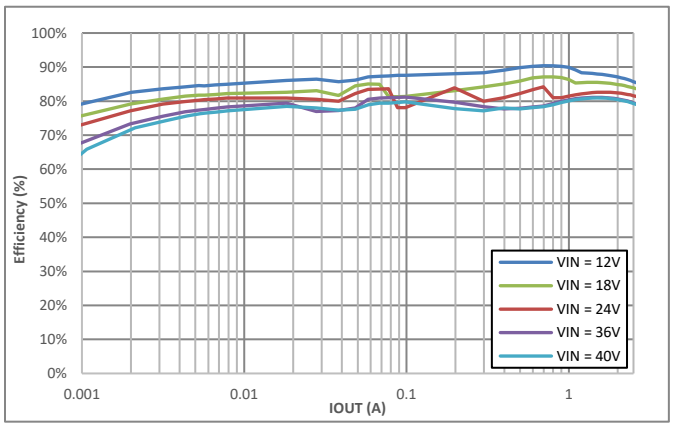


Figure 8. LN10063Q1 Peak Current and Valley Current Limit Vs. V_{IN}



LN10062Q1, F_S = 400kHz, V_{OUT} = 5V

Figure 9. Efficiency Curves



LN10062Q1, F_S = 2.2MHz, V_{OUT} = 5V

Figure 10. Efficiency Curves

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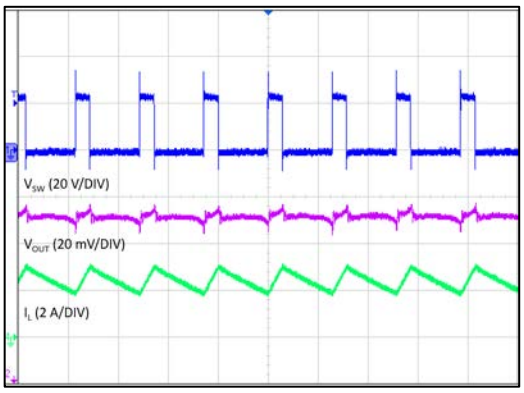
7.5.3 Typical Waveforms

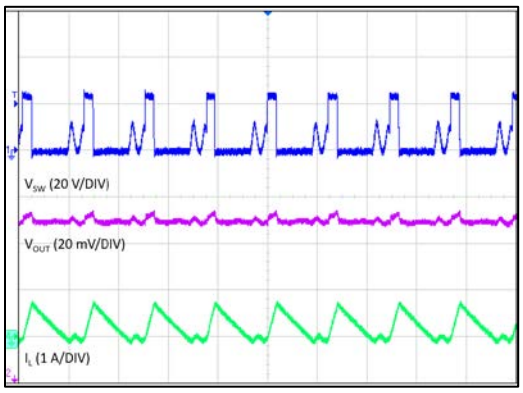
Unless otherwise stated, the test conditions are： V_{IN} = 24V, V_{CCIN} = V_{OUT} = 5V, F_S = 400kHz, L = 10μH, T_A = 25˚C。



Time (2 μs/DIV)

F_S = 400kHz, V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 2.5A

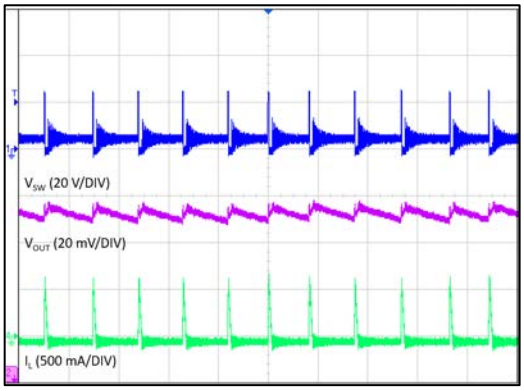
Figure 11. Switching Waveform in PWM Operation



Time (2 μs/DIV)

F_S = 400kHz, V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 250mA

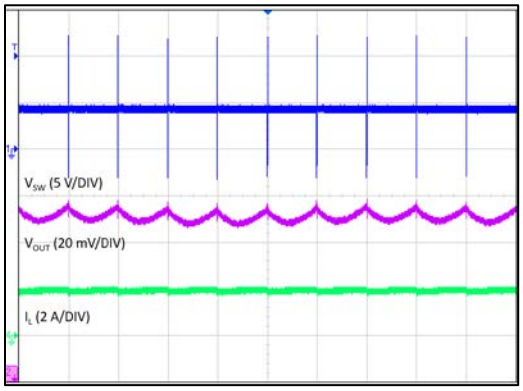
Figure 12. Switching Waveform in PWM with DCM Operation



Time (20 μs/DIV)

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 25mA

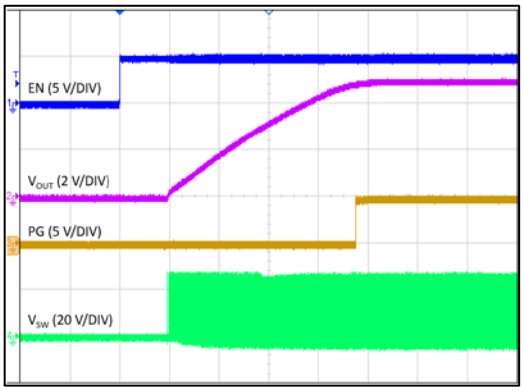
Figure 13. Switching Waveform in PFM Operation



Time (20 μs/DIV)

V_{IN} = 5V, V_{OUT} = 5V, I_{OUT} = 2A

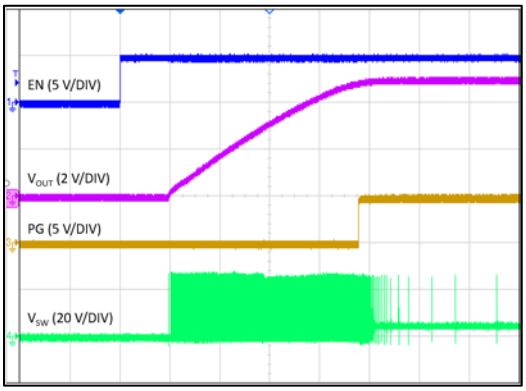
Figure 14. Switching Waveform in Dropout Operation



Time (1 ms/DIV)

V_{IN} = 24V, V_{OUT} = 5V, R_{LOAD} = 2Ω

Figure 15. Startup through EN



Time (1 ms/DIV)

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A

Figure 16. Startup through EN

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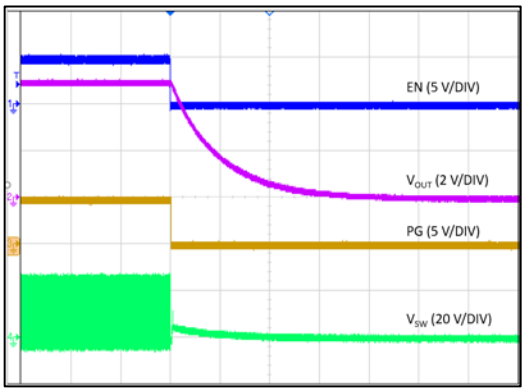
Typical Waveforms (Continued)

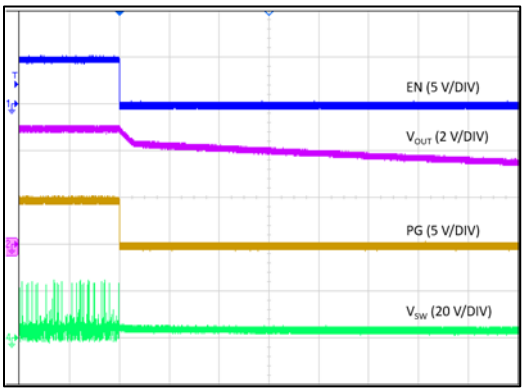
Unless otherwise stated, the test conditions are: V_{IN} = 24V, V_{CCIN} = V_{OUT} = 5V, F_S = 400kHz, L = 10µH, T_A = 25˚C。



Time (200 µs/DIV)

V_{IN} = 24V, V_{OUT} = 5V, R_{LOAD} = 2Ω

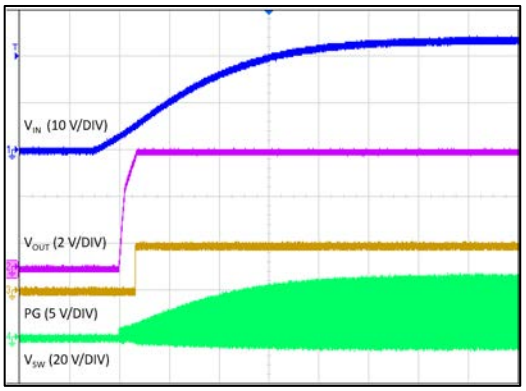
Figure 17. Shutdown through EN



Time (500 ms/DIV)

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A

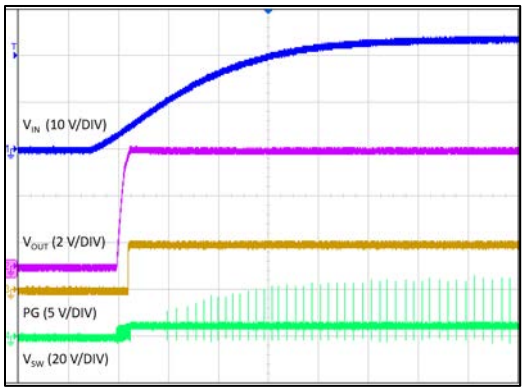
Figure 18. Shutdown through EN



Time (20 ms/DIV)

V_{IN} = 24V, V_{OUT} = 5V, R_{LOAD} = 2Ω

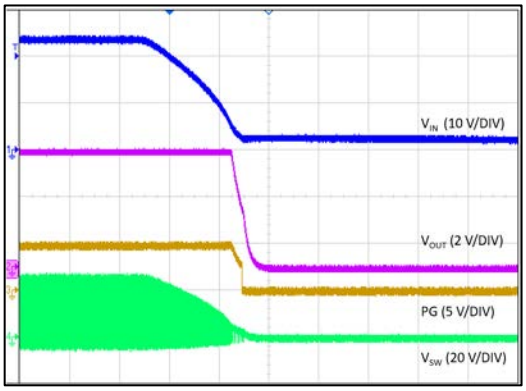
Figure 19. Startup (EN tight to V_{IN})



Time (20 ms/DIV)

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A

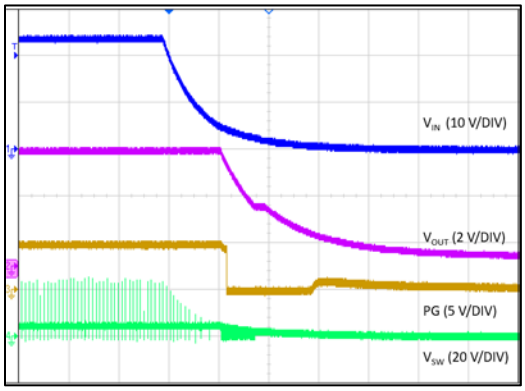
Figure 20. Startup (EN tight to V_{IN})



Time (2 ms/DIV)

V_{IN} = 24V, V_{OUT} = 5V, R_{LOAD} = 2Ω

Figure 21. Shutdown (EN tight to V_{IN})



Time (50 ms/DIV)

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A

Figure 22. Shutdown (EN tight to V_{IN})

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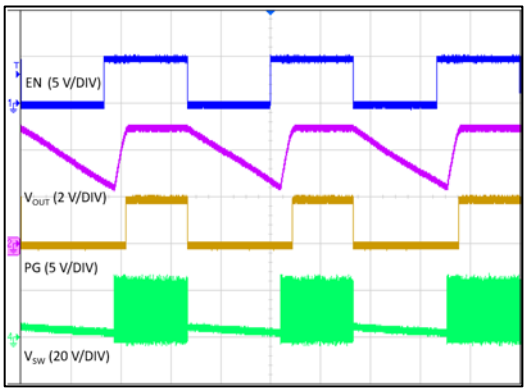
Typical Waveforms (Continued)

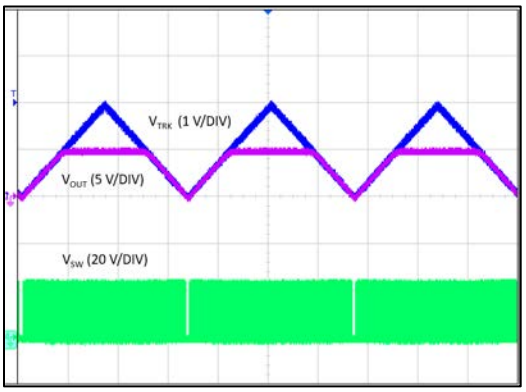
Unless otherwise stated, the test conditions are: V_{IN} = 24V, V_{CCIN} = V_{OUT} = 5V, F_S = 400kHz, L = 10µH, T_A = 25˚C。



Time (10 ms/DIV)

V_{IN} = 24V, I_{OUT} = 10mA

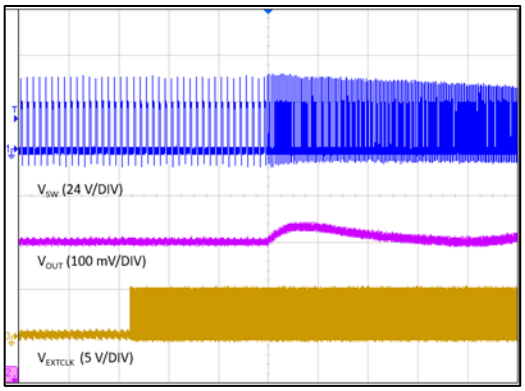
Figure 23. Startup with Pre-Charged Voltage



Time (10 ms/DIV)

V_{IN} = 24V, R_{LOAD} = 2Ω

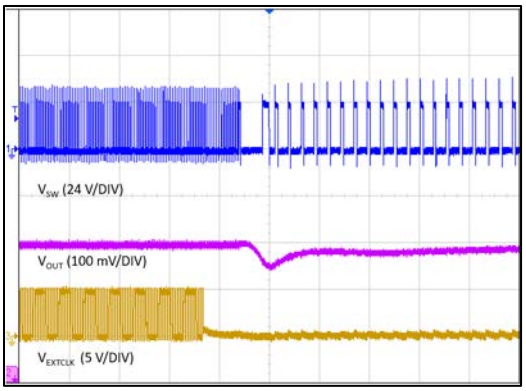
Figure 24. Tracking External Voltage



Time (20 µs/DIV)

V_{IN} = 24V, V_{OUT} = 5V, R_{LOAD} = 2Ω

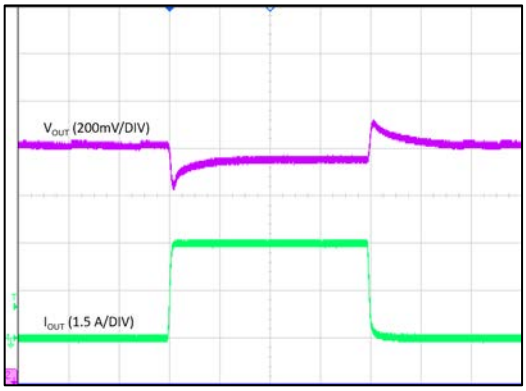
Figure 25. Synced into External 2MHz Clock



Time (10 µs /DIV)

V_{IN} = 24V, V_{OUT} = 5V, R_{LOAD} = 2Ω

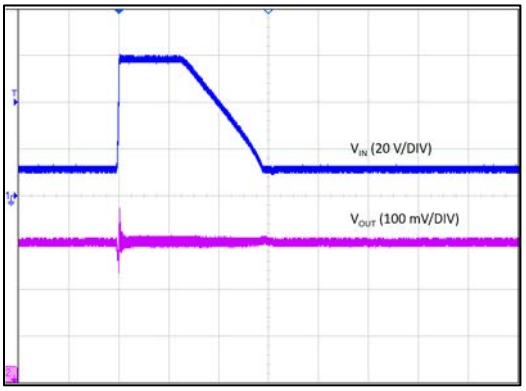
Figure 26. Synced out of External 2MHz Clock



Time (100us/DIV)

V_{IN} = 24V, V_{OUT} = 5V

Figure 27. Load Transient 0.0 <-> 3.0A



Time (500 µs/DIV)

V_{OUT} = 5V, I_{OUT} = 2.5A

Figure 28. V_{IN} Transient 12V <-> 60V

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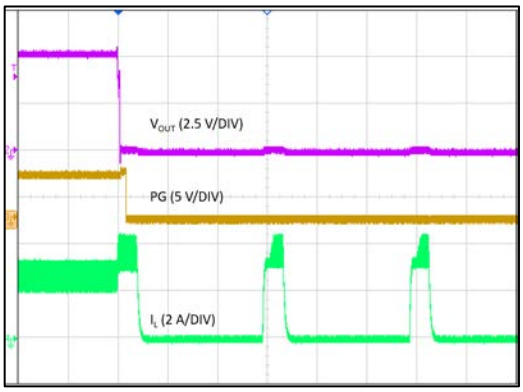
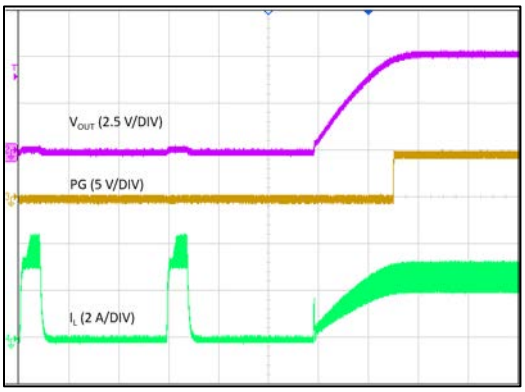
Typical Waveforms (Continued)

Unless otherwise stated, the test conditions are： V_{IN} = 24V, V_{CCIN} = V_{OUT} = 5V, F_S = 400kHz, L = 10μH, T_A = 25˚C。



Time (2 ms/DIV)

Figure 29. Into Output Short and Hiccup



Time (2 ms/DIV)

Figure 30. Out of Output Short and Recovery

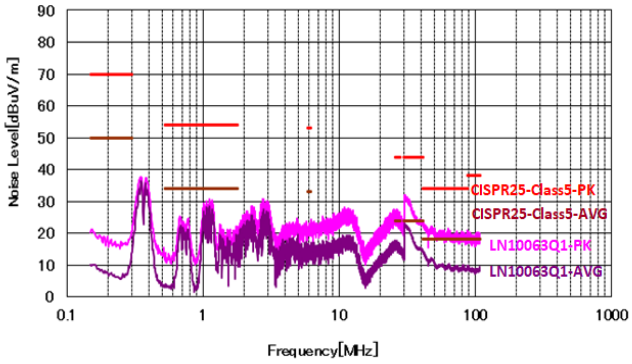


Figure 31. Conducted EMI Performance (CISPR25 Conductive Emission Test with Class 5 Limits, P(+))

LN10163Q1, V_{IN} = 12V, I_{OUT} = 3A, F_S = 400kHz

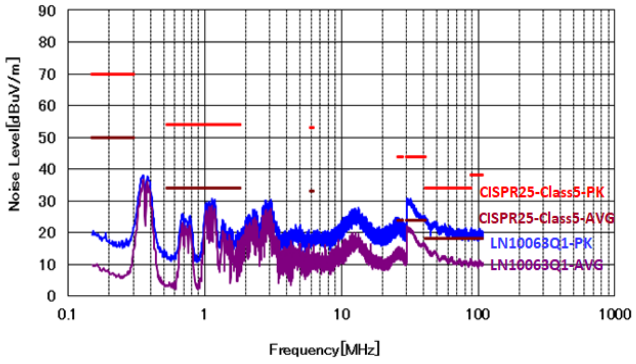


Figure 32. Conducted EMI Performance (CISPR25 Conductive Emission Test with Class 5 Limits, N(-))

LN10163Q1, V_{IN} = 12V, I_{OUT} = 3A, F_S = 400kHz

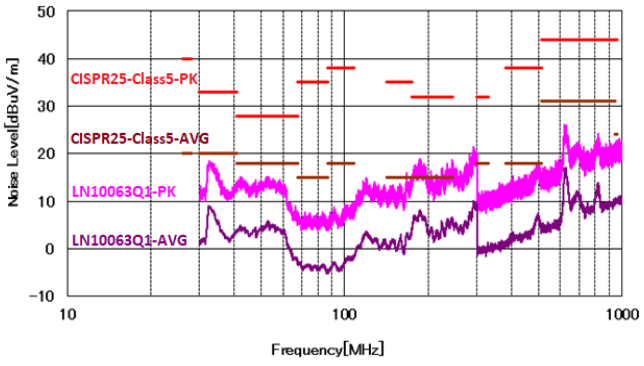


Figure 33. Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Limits, Vertical Polarization)

LN10163Q1, V_{IN} = 12V, I_{OUT} = 3A, F_S = 400kHz

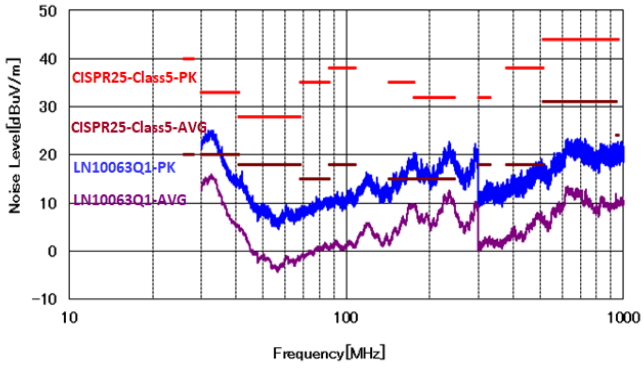


Figure 34. Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Limits, Horizontal Polarization)

LN10163Q1, V_{IN} = 12V, I_{OUT} = 3A, F_S = 400kHz

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8 FUNCTIONAL DESCRIPTION

8.1 Overview

The LN10X62/3Q1 is a high efficiency, compact, synchronous step-down DC-DC converter employing a constant frequency, peak current mode control architecture with internal compensation. It operates from an input voltage from 3.5V to 60V, provides an adjustable output voltage from 1V to V_{IN}. LN10X62Q1 can deliver up to 2.5A of output current, while LN10063Q1 can deliver up to 3.0A. The switching frequency range is from 200kHz to 2.5MHz。

The LN10X62/3Q1 features up to 2.5MHz adjustable high frequency operation through either an external resistor or synchronization with an external clock. With a low minimum on-time, it enables a very compact solution with small inductor and capacitor size and offers constant-frequency operation with very high step-down ratio. In addition, the LN10X62/3Q1 achieves the lowest possible dropout voltage with 100% maximum duty cycle operation. During light load operation, LN10X62/3Q1 operates at DCM and PFM to maximize efficiency. The LN10X62/3Q1 employs a bypass LDO which allows to generate V_{CC} from a lower voltage supply other than V_{IN} to further improve system efficiency.

The LN10X62/3Q1 also offers a plural of features include programmable output voltage, adjustable soft start and tracking capability, power good flag, and a wide array of protection features such as cycle-by-cycle peak current limit, output short-circuit protection with hiccup mode, over temperature shutdown and recovery, and adjustable system UVLO.

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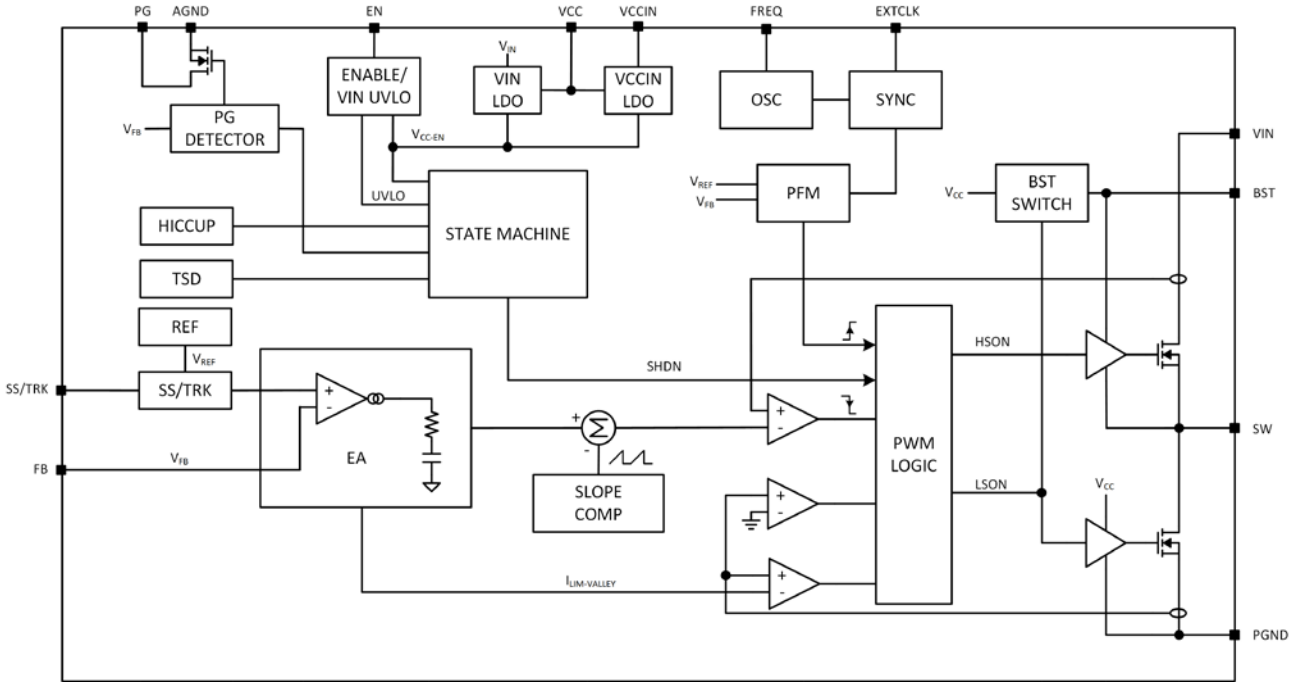
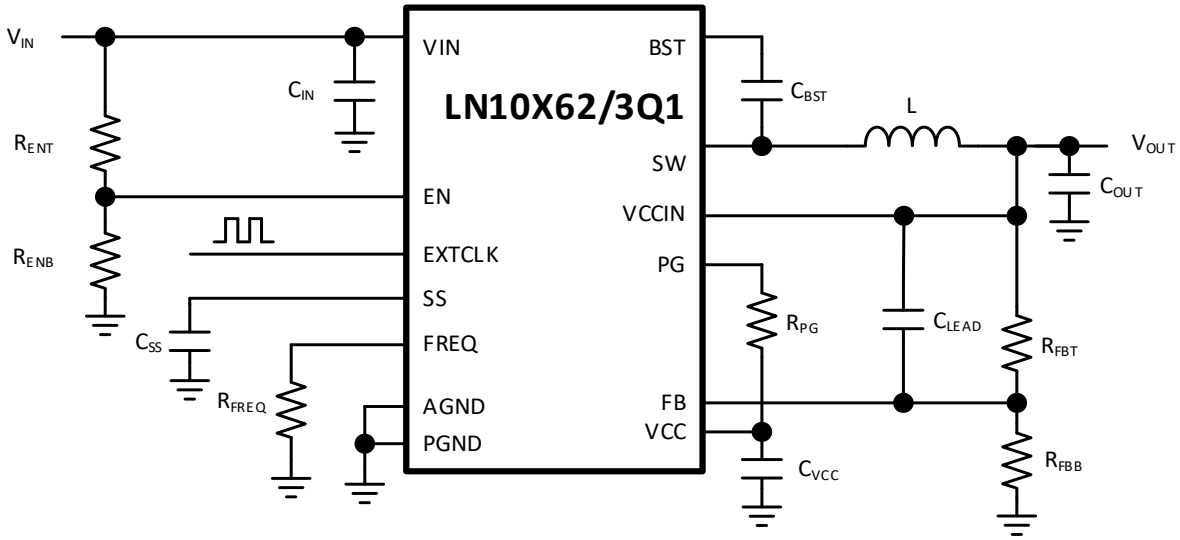
8.2 Funtional Diagram



8.3 Application Diagram with Full Features



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8.4 Funtional Description

8.4.1 Voltage Regulation Loop and FB pin

The LN10X62/3Q1 employs a peak current mode Control to regulate the output voltage. For highly efficient operation cross the whole load range. The LN10X62/3Q1 utilizes Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) at light load.

To adjust the output voltage, connect a voltage divider between V_{OUT} and GND, and connect the center of the divider to FB pin. The steady state V_{FB} is typically 1V. The output voltage can be derived from:

$$V_{OUT} = (1 + \frac{R_{FBT}}{R_{FBB}}) \times V_{FB}$$

Based on the output voltage requirements, the above equation can be re-written as:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_{FBT}$$

In general, R_{FBT} < 1MΩ is recommended. The tolerance of the divider resistance should be less than 1%, and the temperature coefficients should be less than 100ppm.

The LN10X62/3Q1 uses an internal compensation scheme to stabilize the control loop, an external RC lead compensation network can be connected between VOUT and FB to improve transient response. An external lead compensation can be achieved by adding a resistor in parallel with the upper leg resistor of the voltage divider between VOUT and FB pins.

The zero frequency of the external lead compensator is at:

$$f_z = \frac{1}{2\pi \times R_{FBT} \times C_{LEAD}}$$

While the pole frequency of the external lead compensator is at:

$$f_p = \frac{1}{2\pi \times (R_{FBT} // R_{FBB}) \times C_{LEAD}}$$

The added external lead compensator can increase the loop gain by $(1 + \frac{R_{FBT}}{R_{FBB}})$.

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8.4.2 Internal V_{CC} Regulators, V_{CC} and V_{CCIN} Pins

V_{CC} powers the internal control circuits and the gate drivers for the internal power MOSFETs. There are two LDO regulators with inputs from V_{IN} and V_{CCIN} respectively. During powerup, V_{CC} is powered by the V_{IN} LDO regulator and is regulated to 5V. When V_{CCIN} rises above the switchover threshold, V_{CC} automatically switches to the output of the output of V_{CCIN} LDO regulator. It is recommended for the applications with V_{OUT} between 3.3V and 20V to connect V_{CCIN} to V_{OUT} to utilize the higher conversion efficiency of the switching regulator. When V_{CCIN} LDO regulator is not used, connect V_{CCIN} to PGND V_{CC} must be decoupled to PGND with a 1 - 4.7µF ceramic capacitor.

8.4.3 V_{IN} UVLO and EN Pin

EN pin turns on and off the switching regulator and internal V_{CC} LDO. When the voltage on EN pin is below $EN_{VCC-OFF}$, it shuts down V_{CC} LDO and the chip goes into shutdown mode. When the voltage on EN pin is above EN_{VCC-ON} , it turns on V_{CC} LDO.

An accurate threshold is placed at typical 2.1V, when EN rises above this threshold, it turns on the switching regulator. This accurate threshold serves to provide an accurate system V_{IN} UVLO level. In the application, an enable divider can be added between V_{IN} and GND. The switching regulator can thus be turned on and off at programmable precise input voltages.

The switching regulator Enable to Disable hysteresis is at typical -200mV. The VIN UVLO threshold can be determined by:

$$V_{IN-RISING} = (1 + \frac{R_{ENT}}{R_{ENB}}) \times EN_{VOUT-ON}$$

8.4.4 Switching Frequency and FREQ Pin

The switching frequency of LN10X62/3Q1 is programmable between 200kHz to 2.5MHz by an external resistor connected between FREQ pin and AGND. R_{FREQ} is calculated from:

$$R_{FREQ}(k\Omega) = \frac{134311}{F_S(kHz)^{1.062}} - 23$$

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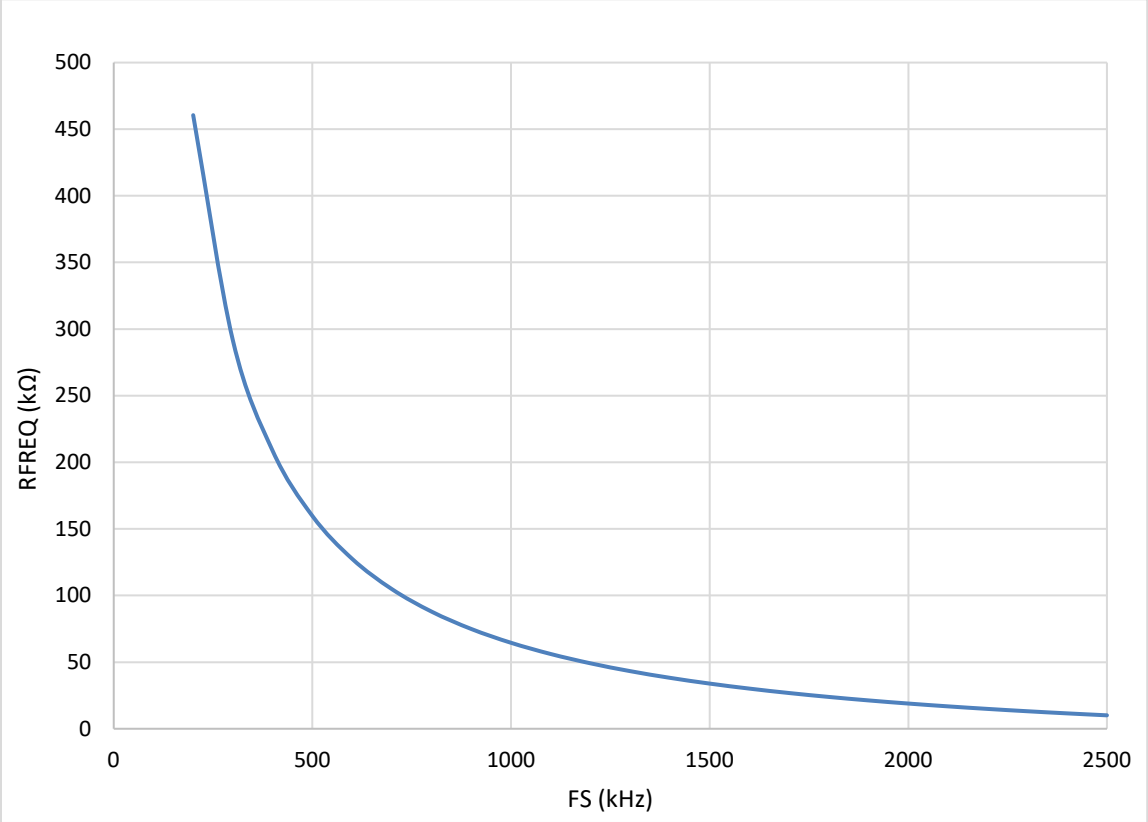
R_{FREQ} vs. Switching frequency is plotted as:



The following table lists some typical switching frequency and corresponding R_{FREQ}.

R_{FREQ} (kΩ)	F_S (kHz)
10	2500
18.7	2000
34	1500
64.9	1000
158	500
210	400
470	200

8.4.5 Synchronization to External Clock and EXTCLK Pin

LN10X62/3Q1 is capable of being synchronized to an external clock between 200kHz to 2.5MHz. Connect the external clock signal to EXTCLK pin. When this function is not used, connect EXTCLK pin to AGND through a 10kΩ resistor. Connect a R_{FREQ} that provides similar switching frequency can minimize the dynamics during the turn on and off of the external sync clock.

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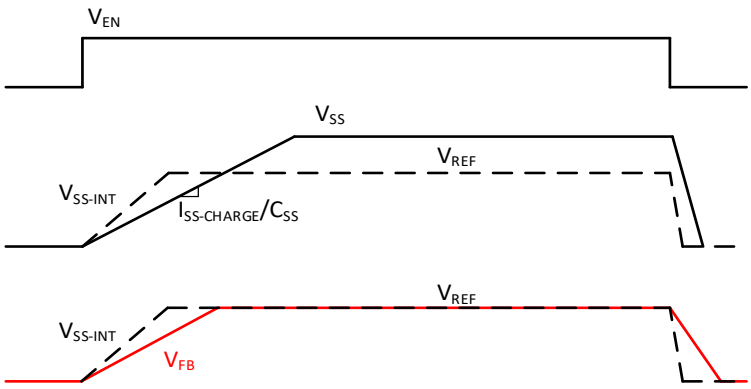
8.4.6 Power Good and PG Pin

The PG pin is connected to the open drain of an internal N-MOSFET. Externally, the PG pin needs to be pulled up to a voltage source by a resistor. Power Good goes high when V_{EN} is high and the feedback voltage V_{FB} is within the power good window defined by PG rising threshold and PG falling threshold. There is a power good rising delay $T_{PG-RISING}$ of 320μs in response to V_{FB} voltage going into the power good window and a power good falling delay $T_{PG-FALLING}$ of 320μs in response to V_{FB} voltage going outside of the window. PG pin immediately goes low when V_{EN} goes low.

8.4.7 Soft Start, Tracking, and SS/TRK Pin

LN10X62/3Q1 has an internal soft-start ramp of about 5.1ms. To use the internal soft-start ramp, leave this pin open. The device also supports externally programmable soft-start ramp and tracking mode through the SS/TRK pin. The voltage on this pin sets the limit for internal reference voltage for regulation. Connect a capacitor between this pin and AGND sets the ramp time for output voltage. An internal 2.6μA current charges the external capacitor, the internal reference voltage follows the voltage on this pin if the external ramp voltage is less than the internal ramp voltage. The soft start time can be calculated:

$$t_{SS} = C_{SS} \times \frac{V_{REF}}{I_{SS-CHARGE}}$$



Externally programmable soft-start waveforms

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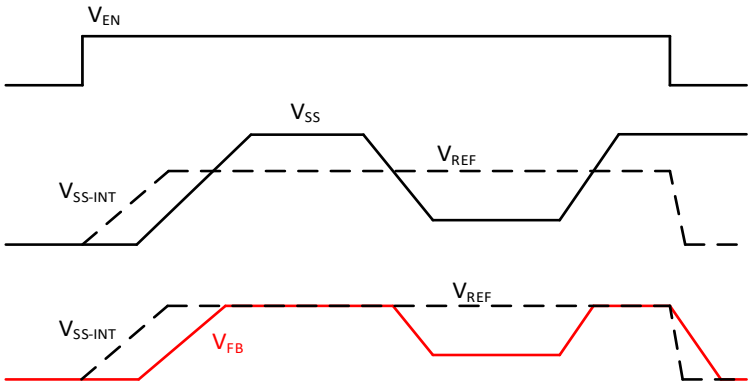
This pin can also be driven to an external voltage ramp. When the external voltage is less than the internal ramp voltage, the output voltage tracks the external voltage ramp. When the tracking voltage is above 1V, internal reference is clamped to be 1V.



Soft start waveforms for tracking external voltage

LN10X62/3Q1 supports start up into pre-biased output voltage. When the soft start ramp voltage is lower than V_{FB} voltage, the control loop does not produce PWM pulses; only when the soft start ramp voltage is close to or rises above V_{FB} voltage, the control algorithm regulates V_{FB} to follow the soft start ramp.

8.4.8 Over-Current Protection

8.4.8.1 Peak Current Protection

Peak current protection is a cycle-by-cycle protection inherited from the peak current mode control. The peak current command is clamped to the Peak Current Limit Threshold.

8.4.8.2 Valley Current Protection

During low side conduction, the low side power MOSFET current is sensed and compared to valley current threshold. When low side current is higher than the valley current threshold, high side power MOSFET is not allowed to turn on for the next cycle.

8.4.8.3 Hiccup Mode

When low side current is higher than the valley current threshold for 32 cycles, it shuts down the switching regulator. The switching regulator automatically turns back on after 5ms if EN is high. During shutdown period, the soft start ramp capacitor is discharged by an internal FET; when the switching regulator turns back on, the regulator goes through the soft start process.

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8.4.9 Thermal Shutdown and Auto-Recovery

When the junction temperature exceeds 160˚C, LN10X62/3Q1 shuts down the switching regulator to reduce thermal dissipation. It automatically restarts the switching regulator after junction temperature drops back below 150 ˚C. The V_{CC} LDO regulators remain operational during over-temperature event.

8.4.10 Bootstrap Voltage, BST, and SW Pin

The internal gate driver for the high side Power MOSFET uses a bootstrapped supply from an external capacitor C_{BST}. C_{BST} connect between BST pin and SW. The voltage on C_{BST} is charged from V_{CC} through an internal switch when the low side power MOSFET conducts.

8.4.11 Low Drop-Out

When input voltage is close to the output target voltage, LN10X62/3Q1 enters Low Drop-Out mode. The high-side MOSFET can be turned on for more than a switching period to maintain the output voltage regulation. When the input voltage is lower than the target voltage, the high-side power MOSFET is turned on for maximum allowable on time: $t_{REFRESH-PE}$. The low-side power MOSFET turns on briefly for $T_{OFF-MIN}$ to refresh the charge on C_{BST}.

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9 APPLICATION INFORMATON

9.1 Typical Applications

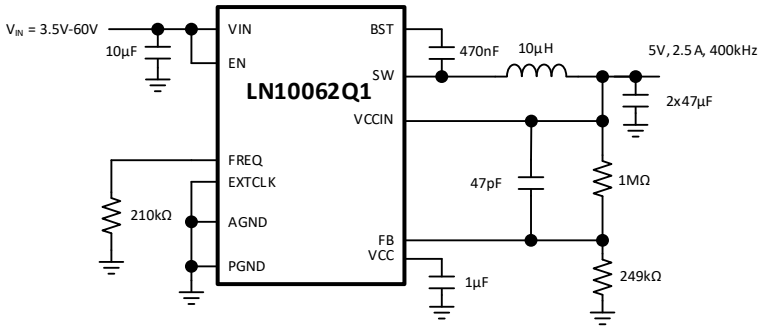

Figure 35. LN10062Q1, 400kHz, 5V, 2.5A Typical Application Diagram

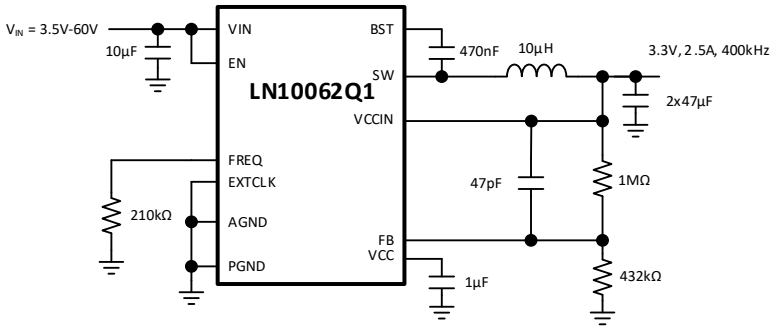

Figure 36. LN10062Q1, 400kHz, 3.3V, 2.5A Typical Application Diagram

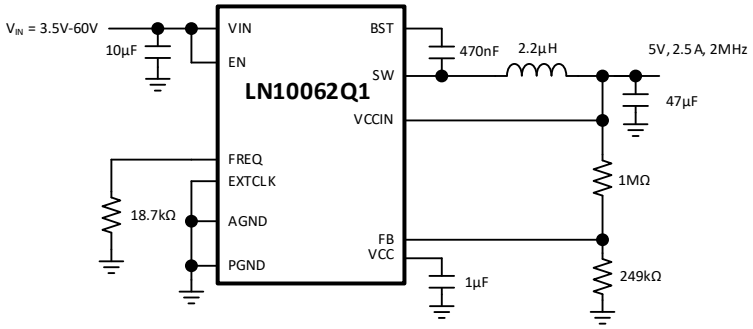

Figure 37. LN10062Q1, 2MHz, 5V, 2.5A Typical Application Diagram

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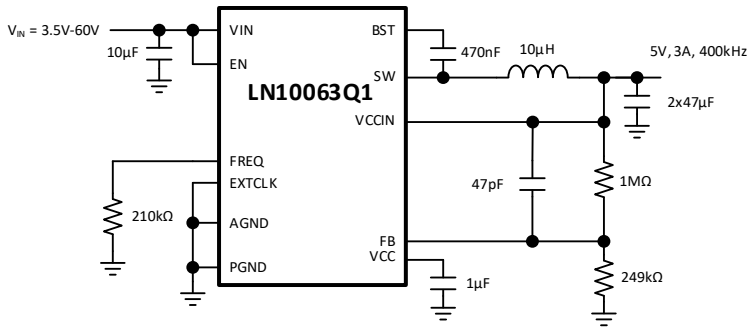

Figure 38. LN10063Q1, 400kHz, 5V, 3A Typical Application Diagram

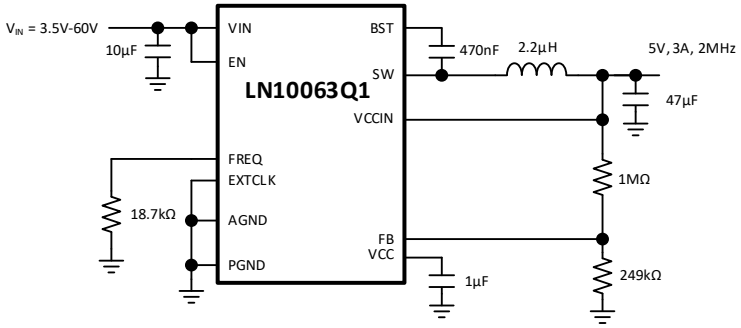

Figure 39. LN10063Q1, 2MHz, 5V, 3A Typical Application Diagram

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9.2 Typical External Components

R_{FREQ} (kΩ)	V_{OUT} (V)	V_{IN} Range (V)	C_{OUT} (µF)	L (µH)	R_{FBT} (kΩ)	R_{FBB}(kΩ)	C_{LEAD} (pF) (3)
F_s = 2.0 MHz							
18.7 kΩ	3.3	3.5 – 13(1)	47	2.2	1000	432	47
	5	5 – 20(1)	47	2.2	1000	249	47
	12	12 – 60(2)	22	8.2	1000	90.9	NA
	24	24 – 60(2)	22	15	1000	43.2	NA
F_s = 1 MHz							
64.9 kΩ	1	3.5 – 9(1)	100	2.2	Short	Open	Short
	3.3	3.5 – 29(1)	100	6.8	1000	432	47
	5	5 – 60	100	8.2	1000	249	47
	12	12 – 60	22	18	1000	90.9	NA
	24	24 – 60	22	27	1000	43.2	NA
F_s = 400 kHz							
210kΩ	1	3.5 – 21(1)	200	4.7	Short	Open	Short
	3.3	3.5 – 60	100	10	1000	432	47
	5	5 – 60	100	10	1000	249	47
	12	12 – 60	22	22	1000	90.9	47
	24	24 – 60	22	47	1000	43.2	NA

1) The maximum output voltage is limited by T_{ON-MIN}.
2) At high switching frequency, the maximum output current may not be guaranteed due to over temperature protection.
3) With large ESR capacitor, the lead compensation may not be needed.

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10 LAYOUT

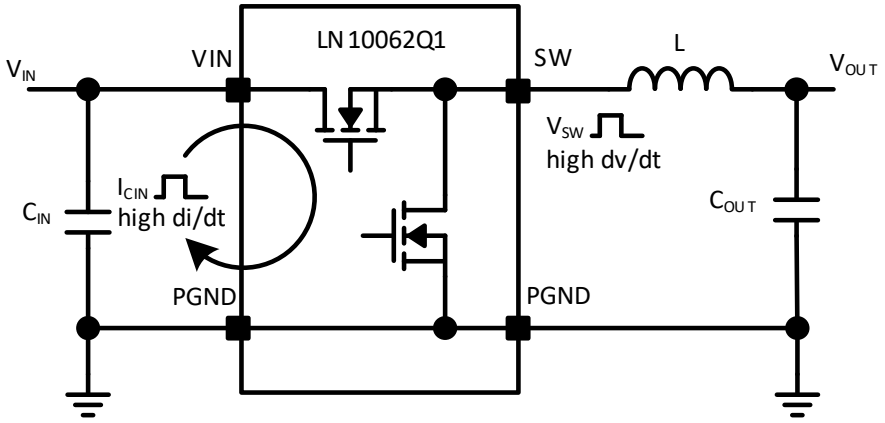
The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The LN10X62/3Q1 is designed to meet the optimization requirements of PCB layout in the pin assignment. For example, VIN and PGND pins are adjacent to each other, which is convenient for placing VIN bypass capacitors.

10.1 Layout Guidelines

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current; the more electromagnetic emission is generated. As shown in the figure below, this part of the current flows from the VIN side of the input capacitors to high side switch, to the low side switch, and then returns to the ground of the input capacitors.

The key to minimize radiated EMI is to minimize the area of this pulsing current path, thus, placing high frequency ceramic bypass capacitor(s) as close as possible to the VIN and PGND pins is necessary.

In addition, high dv/dt occurs on SW node during switching, so the trace between SW pin and inductor should be as short as possible, and just wide enough to carry the load current without excessive heating. Short and thick traces are highly recommended to minimize parasitic resistance. Besides, sensitive signal lines should be kept away from SW traces.



The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place high frequency ceramic bypass CIN as close as possible to the LN10X62/3Q1 VIN and PGND pins; a ceramic capacitor in small package (such as 0603) is still needed even if multiple input capacitors are implemented;

2. The high-current loop consisting of VIN, SW, VOUT and GND should be as compact as possible;

3. The bypass capacitors of VCCIN and VCC should be arranged close to the pins, and return to the PGND pin with the shortest connection;

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4. It is recommended to use a four-layer board with a top and bottom layer of 2oz copper, and a complete ground plane on middle layer. Use a minimum 3 by 4 arrays of 10 mil thermal vias to connect the thermal pad of LN10X62/3Q1 to the system ground plane for heat sinking;

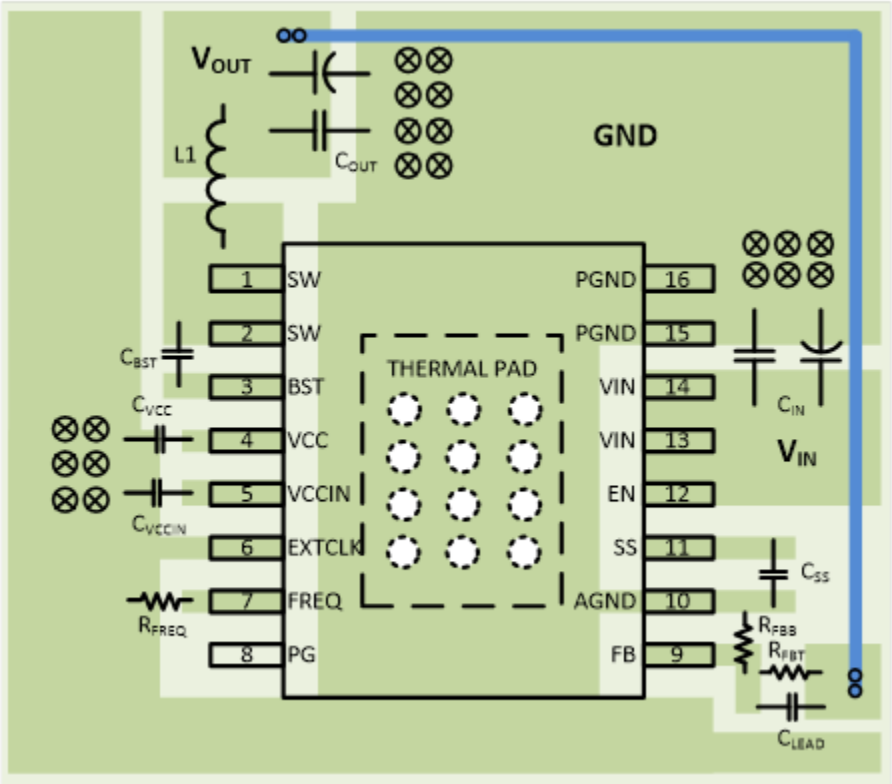
5. The SW and BST nodes contains a lot of high-frequency noise, so the connection of the pins should be as short as possible, meanwhile, there should be sufficient width to conduct the current;

6. Sensitive analog signals, such as FB, SS and FREQ, need to be far away from the noisy nodes, ground plane can be used as a shielding layer while routing these sensitive signals;

7. The feedback resistance of the FB connection must be located as close to the pin as possible, If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load;

8. For the peripheral components connected to FB, FREQ, SS and EN pins, a single point ground connection to the plane is recommended.

10.2 Layout Example



LN10X62/3Q1 Layout

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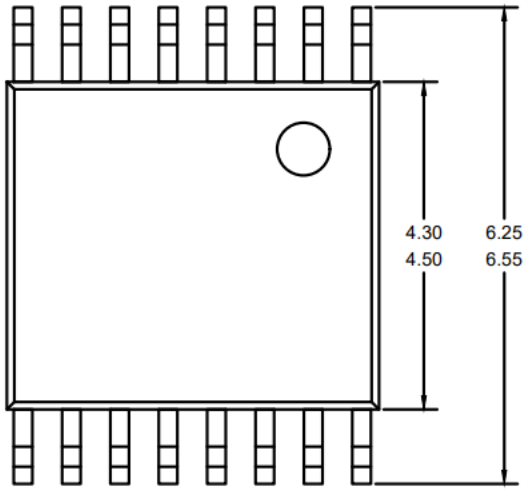
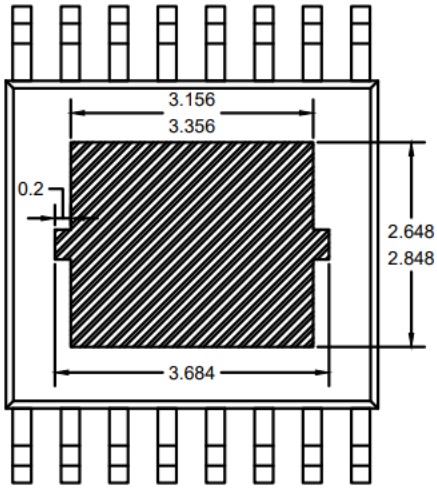
11 PACKAGE INFORMATION

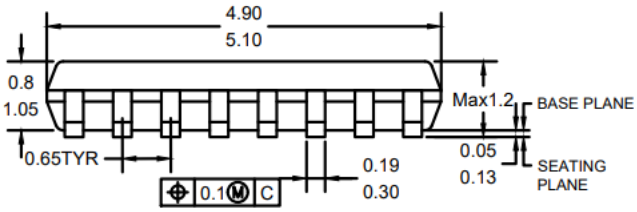
11.1 Package Outline

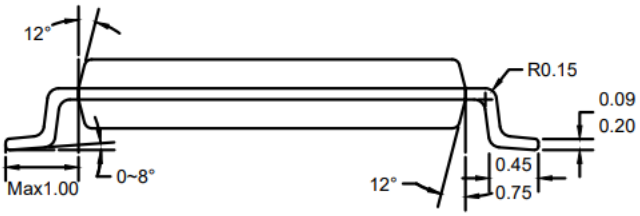


TOP VIEW



BOTTOM VIEW





Notes:

1. Both package length and width do not include mold flash.
2. Controlling dimension: mm

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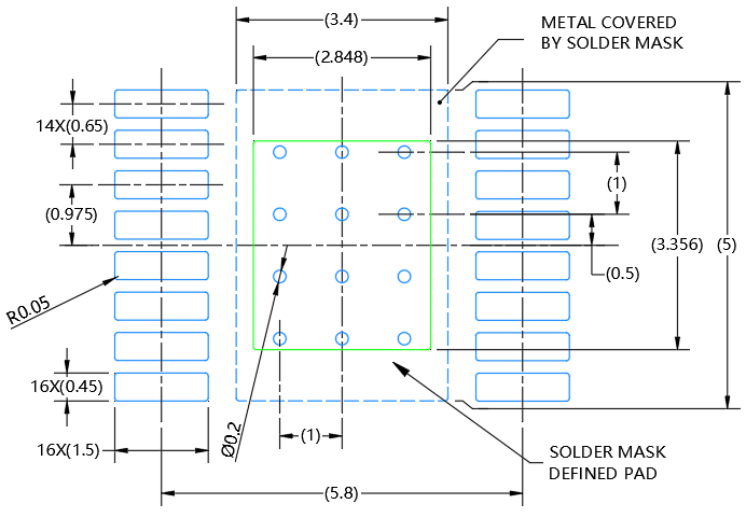
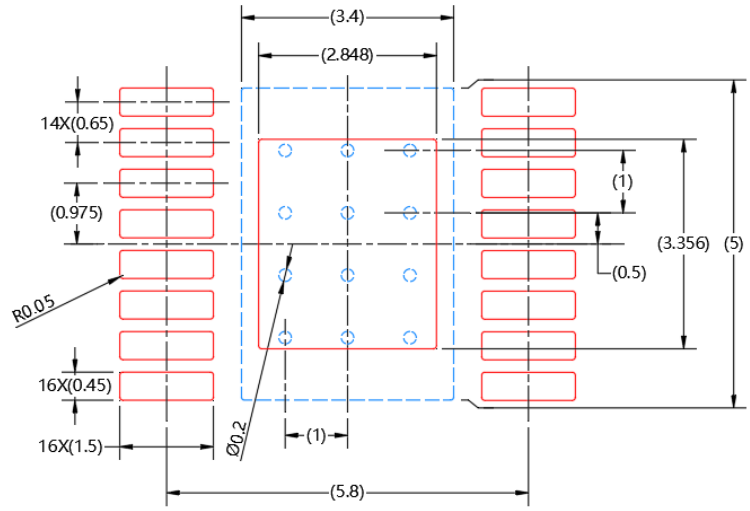
11.2 Footprint Example

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL



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