5-Channel Capacitive Touch and Proximity Controller

FEATURES

- 5-channel capacitive sensing
  - Self-capacitive sensing technology
  - Capacitance resolution down to 1aF
  - Maximum offset capacitance up to 220pF
  - Auto-Offset-Tuning (AOT)
  - Each Channel configurable independently
- 400kHz I²C interface
  - Default address: 0x12
  - Address configurable via pin CS2
- External interrupt pin INTN, open-drain output
  - Support multi-level distance interrupt
- Built-in brown-out reset (BOR)
- Low power consumption
  - Active mode: 32μA
  - Doze mode: 8.7μA
  - Sleep mode: 7.5μA
  - Deep Sleep mode: 3.3μA
- 1.7V~3.6V power supply
- Operation temperature range: -40°C~85°C
- DFN 2.1mm×1.8mm×0.55mm-10L package

APPLICATIONS

Mobile phones
Wearable devices, TWS
Tablets, Notebooks

GENERAL DESCRIPTION

AW96105ADNR is a 5-channel low power consumption capacitive touch and proximity controller. Each channel can be independently configured as sensor input, shield output.

Advanced self-capacitance technology is adopted, which supports parasitic capacitance compensation for each channel up to 220pF. The device has a high resolution ADC, the minimal capacitance that can be detected is as low as 1aF.

A high performance 32bit MCU is integrated by executing the firmware-program in the ROM, it implements all AFE sampling controlling and complicated data processing algorithms including signal filtering, RF noise suppression, baseline calculation, proximity status decision, etc.

With the auxiliary of DSP algorithm, the device is able to track slow environmental variations (such as temperature, humidity, etc.) and maintain high performance operation.

TYPICAL APPLICATION CIRCUIT

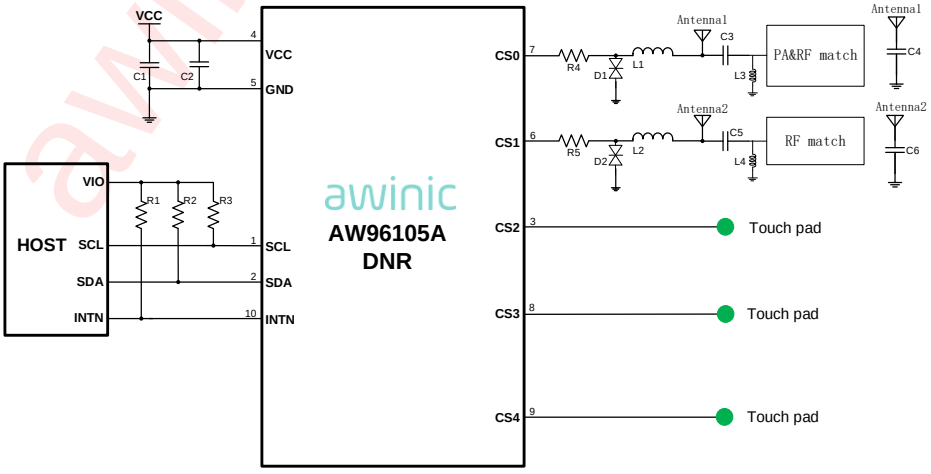
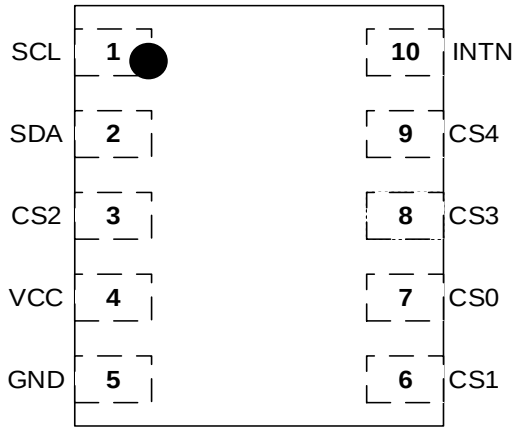


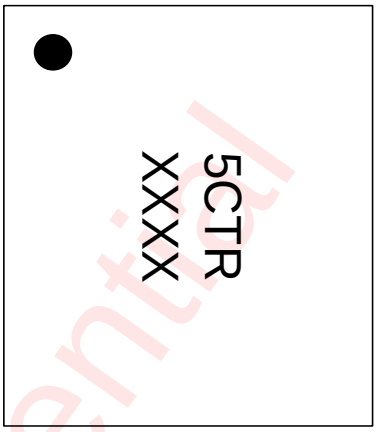
Figure 1 AW96105ADNR Typical Application Circuit

PIN CONFIGURATION AND TOP MARK

AW96105ADNR
(TOP View)



AW96105ADNR Marking
(TOP View)

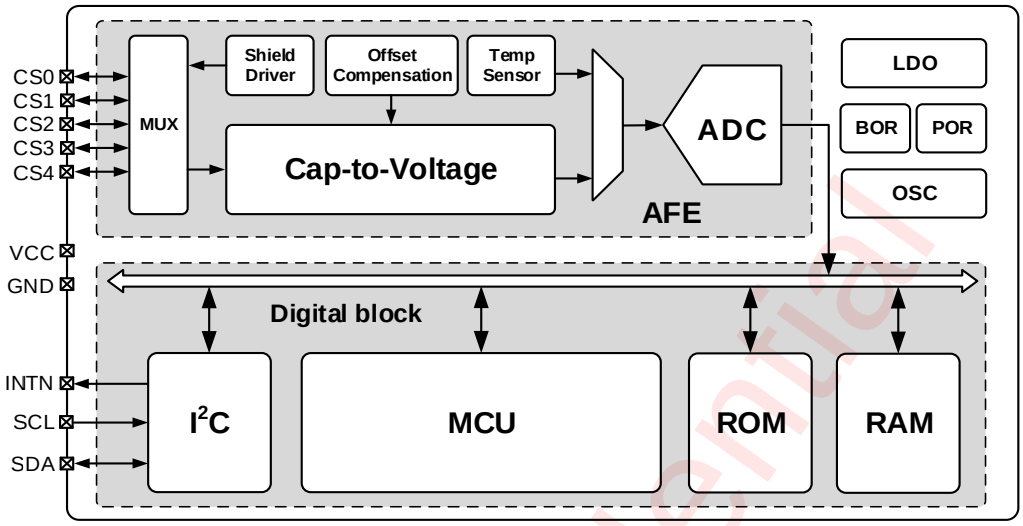


5CTR - AW96105ADNR
XXXX - Production Tracing Code

PIN DEFINITION

No.	NAME	DESCRIPTION
1	SCL	I²C clock, requires pull-up resistor
2	SDA	I²C data, requires pull-up resistor
3	CS2	Capacitive Sensor input/shield or I²C address select Input (Floating: 0x12, GND: 0x13, VCC: 0x14)
4	VCC	Power supply (1.7V~3.6V), requires decoupling capacitor
5	GND	Ground
6	CS1	Capacitive sensor input/shield
7	CS0	Capacitive sensor input/shield
8	CS3	Capacitive sensor input/shield
9	CS4	Capacitive sensor input/shield
10	INTN	Interrupt output, open drain, requires pull-up resistor

FUNCTIONAL BLOCK DIAGRAM



Notes: AFE means Analog Front-End.

Figure 2 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW96105ADNR	-40°C~85°C	DFN 2.1mm×1.8mm×0.55mm-10L	5CTR	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.5V to 4.0V
Input voltage range	CSx, SCL, SDA, INTN	-0.5V to 4.0V
Output voltage range	CSx, SCL, SDA, INTN	-0.5V to 4.0V
Junction-to-ambient thermal resistance θ_{JA}		128.6°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (Including HBM CDM)(NOTE 2)		
HBM	Pins CSx (x=0,1,2,3,4)	±8kV
	Other pins	±6kV
CDM		±1.5kV
Latch-Up		
Test condition: according to JESD78E		+IT: 350mA -IT: -350mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method: MIL-STD-883J, the CDM test method: ANSI/ESDA/JEDEC JS-002-2018.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN	MAX	UNIT
Supply voltage	V_{DD}	1.7	3.6	V
Pull-up voltage	V_{IO}	1.6	3.6	V
Ambient temperature	T_A	-40	85	°C

ELECTRICAL CHARACTERISTICS

Note: Typical values are given for T_A = +25°C, VCC= 2.8V unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CHIP CURRENTS						
$I_{DEEPSLEEP}$	Deep Sleep Mode Current	LDO on, OSC off I^2C listening		3.3	6.0	μA
I_{SLEEP}	Sleep Mode Current	LDO on, OSC on I^2C listening		7.5	10	μA
I_{DOZE}	Doze Mode Current	SCANPERIOD = 400ms FREQ = 100kHz; CDCRES = 6 CHEN = b000001 Digital filter features OFF I^2C listening. No load		8.7	16	μA
I_{ACTIVE}	Active Mode Current	SCANPERIOD = 30ms FREQ = 100kHz CDCRES = 6 CHEN = b000001 Digital filter features OFF I^2C listening. No load		32	45	μA
CAPACITANCE SENSING						
C_{RANGE}	Measurement Range		±0.55	±2.2	±9.9	pF
N_{BIT}	Measurement Resolution			21		bits
C_{RES}		CRANGE = 0001		1		aF
F_{OSC}	Nominal OSC Frequency			4		MHz
F_{Trim}	OSC Trim Accuracy	Around Nominal Value T_A = 25°C, VCC = 2.8V	-4		4	%
F_{Temp}	OSC Temp. Dependency	Around Nominal Value T_A = 25°C, VCC = 2.8V	-1		1	%
F_{VCC}	OSC VCC Dependency	Around Nominal Value T_A = 25°C, VCC = 2.8V	-0.6		0.6	%
F_S	Nominal Sampling Frequencies	Programmable with FREQ			250	kHz
C_{DCEXT}	External DC Cap. to GND per Measurement Channel	One CSx as measured input			220	pF
R_{FILTIN}	Input driving Res		0		30	kΩ
R_{INT}	Compensation Res		125		1k	Ω
TEMPERATURE SENSING						
$T_{INRANGE}$	Input Range	Ambient Temperature (T_A)	-40		85	°C
$T_{OUTRANGE}$	Output Range		0		32767	LSB
I^2C INTERFACE						
I_{OL} (SDA, INTN)	Output low current	$V_{OL} \leq 0.4V$	8			mA
V_{IH}	Input high level	SCL, SDA	1.35		3.6	V
V_{IL}	Input low level	SCL, SDA	-0.5		0.45	V

I²C INTERFACE TIMING

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency			400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
T_{LOW}	Low level width of SCL	1.3			μs
T_{HIGH}	High level width of SCL	0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6			μs
$T_{HD:DAT}$	Data hold time	0			μs
$T_{SU:DAT}$	Data setup time	0.1			μs
T_R	Rising time of SDA and SCL			0.3	μs
T_F	Falling time of SDA and SCL			0.3	μs
$T_{SU:STO}$	Stop condition setup time	0.6			μs
T_{BUF}	Time between start and stop condition	1.3			μs
T_{SP}	Input glitch suppression			50	ns

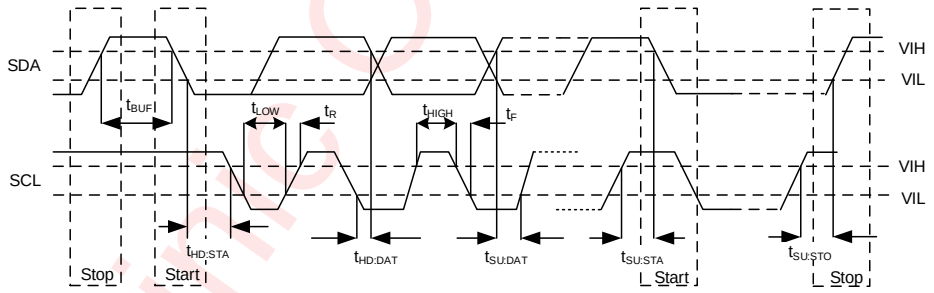


Figure 3 I²C Interface Timing

DETAILED FUNCTIONAL DESCRIPTION

OVERVIEW

AW96105ADNR is a capacitive proximity sensing controller with a built-in low-power MCU. It is comprised of high-performance self-capacitance detecting Analog-Front-End (AFE), imbedded 32bit MCU, ROM, RAM, OSC and I^2C interface, etc. The AFE drive the sensor and shield electrode, and convert the capacitance of sensor to digital data. The MCU executes the algorithm program stored in the ROM, and perform complicated data process such as signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency(RF) noise suppression, proximity decision, etc.

CAPACITIVE SENSOR INTRODUCTION

Self-capacitance sensing technology detects the capacitance change of a touch or proximity sensor caused by a target object approaching the sensor. The target object could be a human finger, face, or any conductive object. The figure below shows the basic structure and equivalent model of a capacitance sensor. The top layer is the frontpanel, and the middle green area below is a copper sensor pad. The sensor is usually surrounded by ground, resulting in a parasitic capacitance (C_{PARA}).

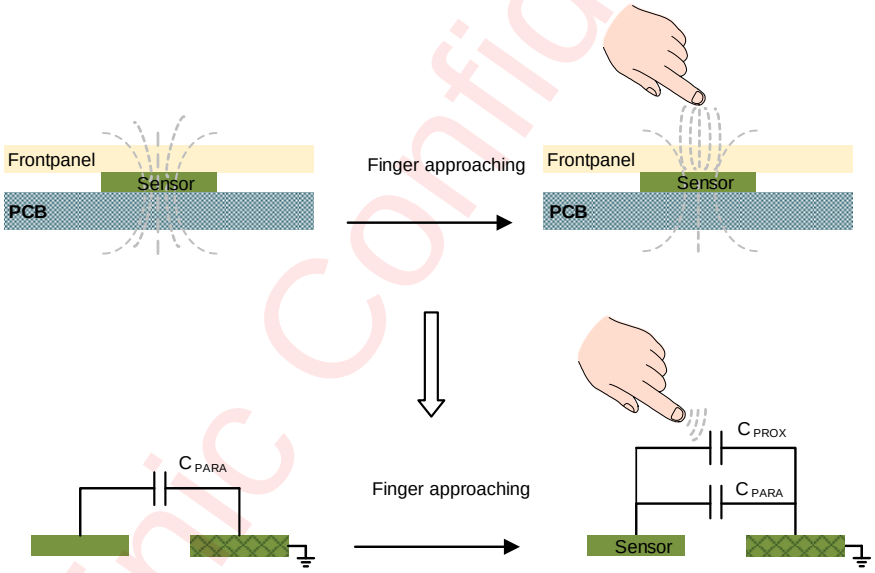


Figure 4 Capacitive sensor structure

When a voltage is forced on a sensor, an electric field is created around the sensor. As the target object approaches the electrode, some of the electric field lines couples to the target object and add a small amount of finger capacitance (C_{PROX}) to the existing C_{PARA}. This feature can be used to detect proximity or touch action.

CAPACITIVE SENSING TECHNIQUES

The proximity sensing system consists of three parts, capacitive sensor, AFE and DSP. The sensor capacitance will change when the target object is approaching or moving away. AFE drives the capacitive sensors and shield electrodes, and converts the sensor capacitance to digital data. DSP deals with the data from AFE, and transmits the sensor capacitance value (Diff) and proximity status (Status) to the host.

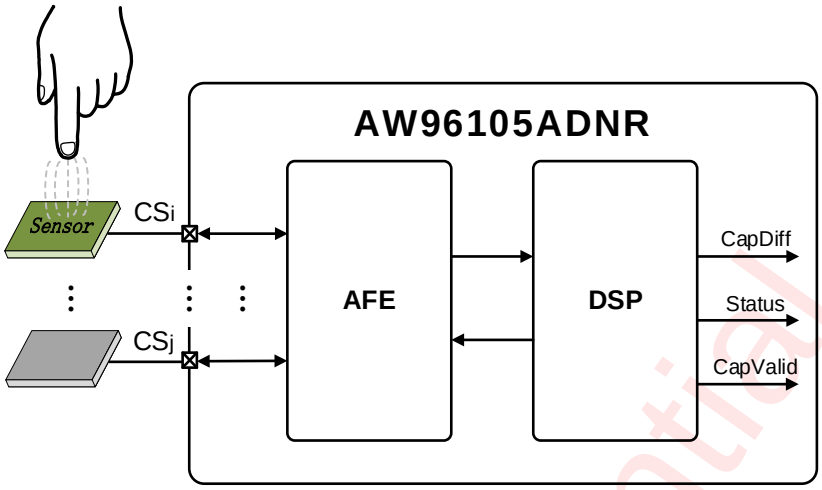


Figure 5 Proximity Sensor Operation Overview

AFE DESCRIPTION

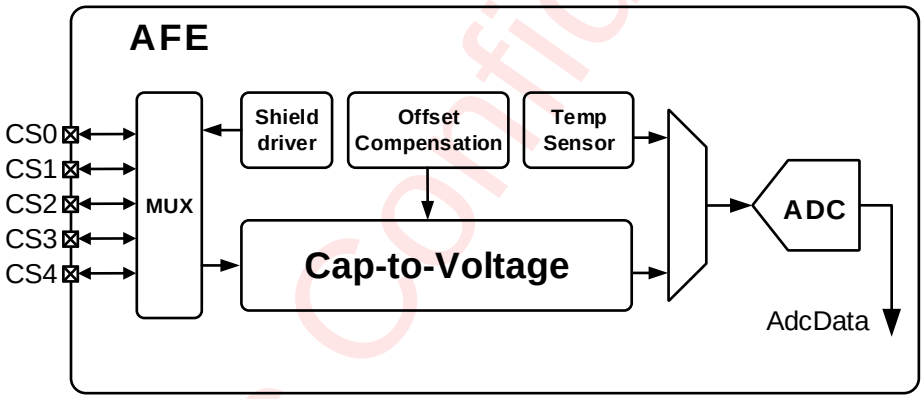


Figure 6 AFE Block Diagram

※ MUX selects CSx as capacitance measurement input or shield output

※ If CSx is used as shield electrode, it is excited by shield driver. The driven shield signal is a replica of the sensor signal. Shield electrode around can protect the sensor from noisy environment，and reduce the parasitical capacitance.

※ Cap-to-Voltage module integrates a charge amplifier, with a charge-transfer method it converts the capacitance of senor into voltage signal, as the input of ADC.

※ Offset Compensation module is used to eliminate parasitic capacitance(C_{PARA}) and ensure that the compensated capacitance is within the measurable range of C/V convertor.

※ Temp Sensor measures the internal temperature of the chip, and its output is converted by ADC into a digital data. The data can be used to correct the result of capacitance measurement.

※ ADC converts voltage signals obtained by Cap-to-Voltage or Temp Sensor into AdcData.

DSP DESCRIPTION

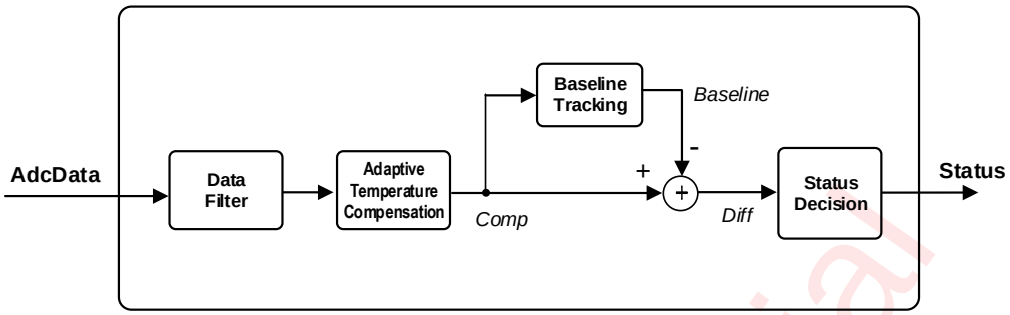


Figure 7 Digital signal processing diagram

※ DSP processes the AdcData from the AFE, and finally outputs a series of reliable proximity status.

※ Data Filter effectively filters the high-frequency noise and interference, which greatly improves the signal-to-noise ratio.

※ The adaptive temperature compensation module can automatically compensate for environmental drift in real time, especially temperature drift. Thereby it can be ensured that the final proximity status will not be misjudged due to temperature drift.

※ The role of the baseline is to further track the slow changes caused by the residual temperature compensation or other slow environmental drift.

※ Finally, the Status Decision module output a certain and reliable proximity status based on the Diff data and the proximity threshold etc.

SCAN PERIOD

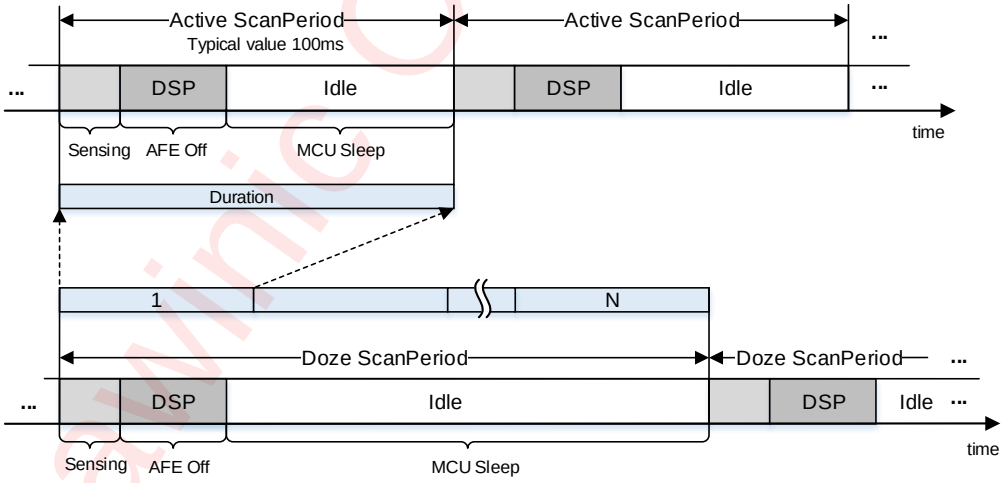


Figure 8 Active mode and Doze mode scan period

Each period is divided into 3 segments. Firstly the AFE scan the sensor channels to get the AdcData. And then AFE is off and DSP starts processing the AdcData. After all data processing are completed, the chip enters idle state both AFE and MCU don't work for low-power consumption.

The figure above also shows the scanning period of active mode and doze mode. The scan period of active mode can be configured by register SCANCTRL1 (Address: 0x0004) and AFECFG3_CHx. The doze period can be configured independently for each channel by register AFECFG4_CHx. Generally, doze mode consumes much lower power than active mode.

CLOCK

The chip uses a built-in 4MHz OSC clock.

RESET

POWER ON RESET (POR)

Reset operation is triggered during power up. When nRST (internal signal) released, the initialization process starts to perform and it will last for about 20ms. After initialization being completed, pin INTN will be pull down to low, then I²C interface can communicate normally.

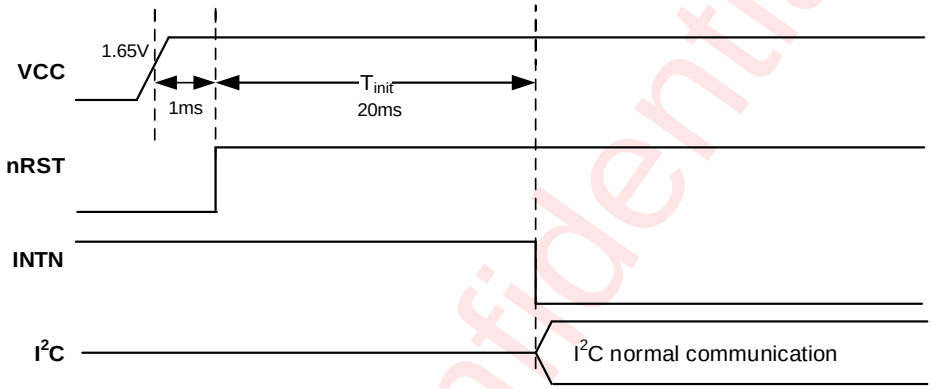


Figure 9 Power On Timing

BROWN OUT RESET (BOR)

Reset operation is triggered when VCC drop below the threshold of BOR. After the reset operation, all the registers will be reset to the default value. The chip returns to normal operation mode until the power supply rises to a normal value.

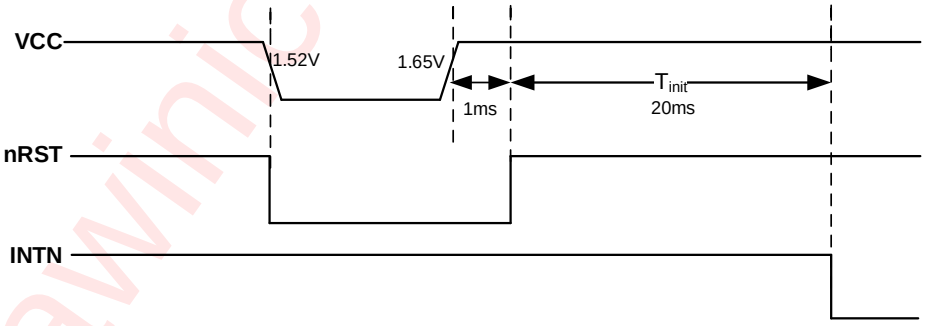


Figure 10 Brown Out Timing

SOFT RESET

Write “0” to register RESET (Address: 0xFF0C) to reset the whole chip. After the reset, all the registers will be reset to the default value.

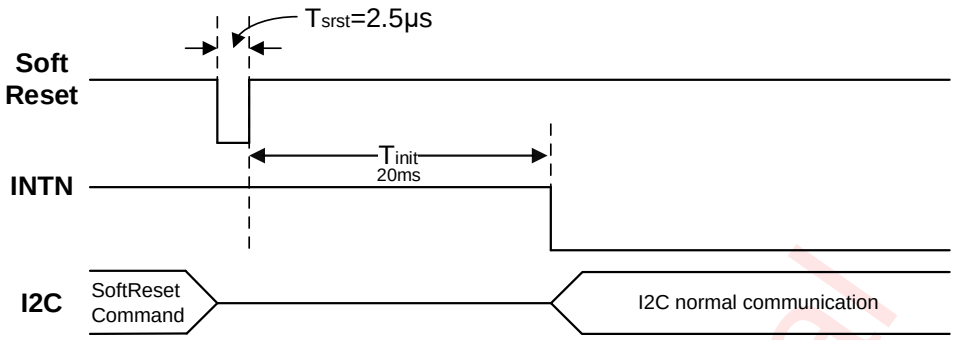


Figure 11 Soft Reset Timing

INITIALIZATION

After power on, OSC works normally, and MCU starts to execute the initialization program. It performs the following operations.

- Read information from NVM
- Set I²C device address according to the status of pin CS2
- Issue an interrupt after initialization and then enters into sleep mode.

OPERATION MODE

There are four operation modes in the chip: Deep Sleep, Sleep, Active and Doze.

DEEPSLEEP

The device consumes the lowest power. OSC and AFE are off, CPU is sleeping, only I²C interface is active.

SLEEP

The device is in a low power state. OSC is on, AFE is off, and MCU is sleeping, waiting for interrupt to wake up.

ACTIVE

The device works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When no touch or proximity has been detected for some time, it will automatically switch to Doze mode. In this mode the external HOST can send SLEEP command to switch the device to sleep mode.

DOZE

The scan period is long, MCU and AFE work intermittently. During the large part of period, most modules are in idle state. So the average power consumption is lower.

Once a proximity is detected in doze mode, it will automatically return to active mode. The external HOST can also send SLEEP command to switch the device to sleep mode.

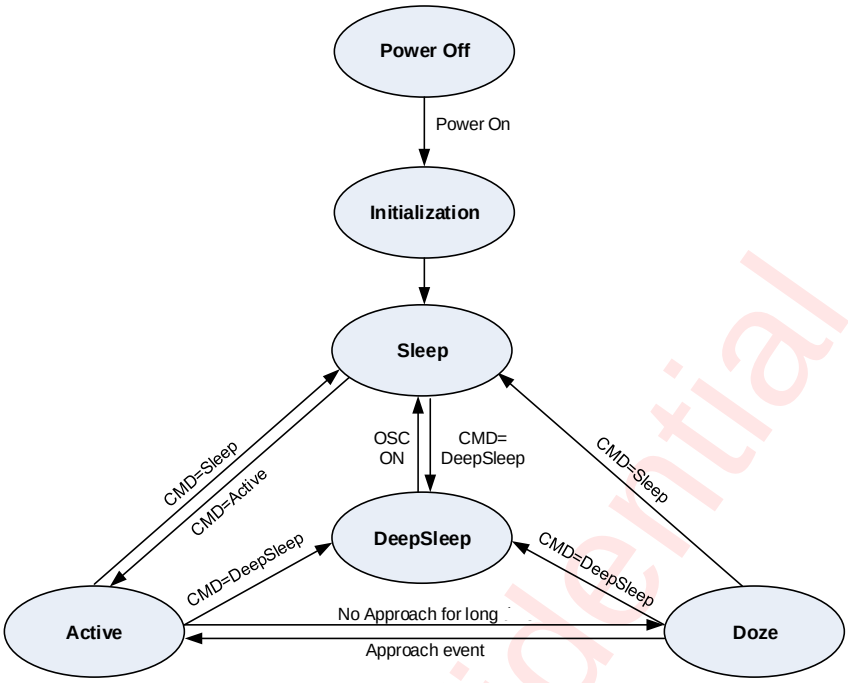


Figure 12 Operation Mode Switching

INTERRUPT

The chip reports the interrupt signal to the host through the pin INTN. Register IRQSRC (Address: 0xF080) stores interrupt information, including scan interruption, calibration completion interruption, human body approach interruption, etc. Register IRQSRC is cleared after reading. Each specified interrupt triggered or not can be configured by register IRQEN (Address: 0xF084).

I²C INTERFACE

AW96105ADNR supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW96105ADNR can support different high level of the I²C interface. Additionally, the I²C device supports continuous read and write operations. The register address is 16 bits, the register data is 32 bits, and the data transmission is in big-endian mode.

DEVICE ADDRESS

I²C device address configuration

CS2 Connection	Device Address
Floating	0x12
GND	0x13
VCC	0x14

The I²C device address (7-bit, followed by the R/W bit (Read=1/Write=0)) of AW96105ADNR depends on the pin CS2 status. The default value of I²C device address is 0x12, connecting pin CS2 to GND or VCC will change the device address as showed in table above. Note that when pin CS2 is connected to GND or VCC,

it can't be used as sensor pad.

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

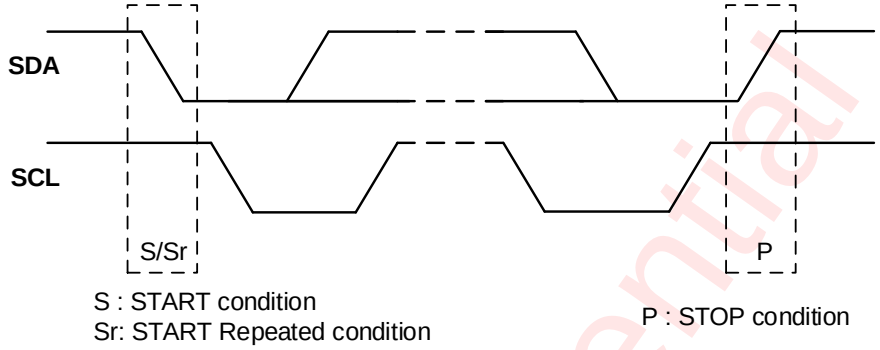


Figure 13 I²C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

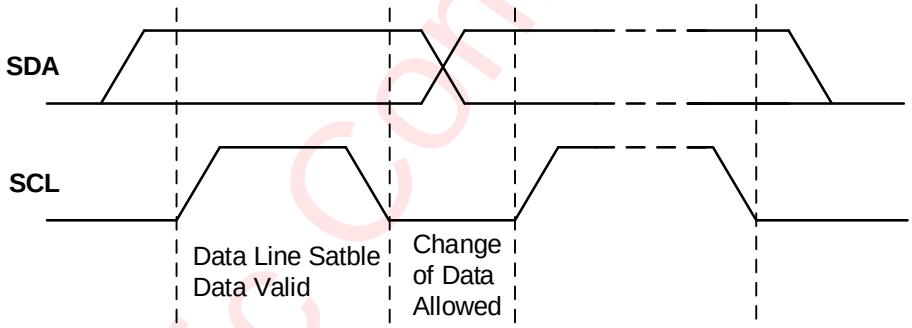


Figure 14 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

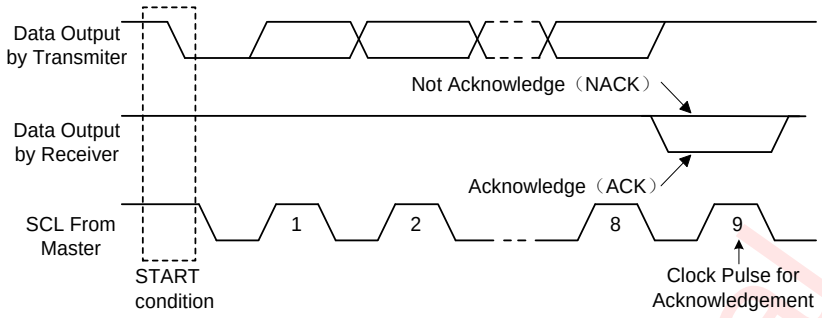


Figure 15 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 16-bit and register data is 32-bit. Note that I²C also support 8-bit data transfer. Writing process of I²C is showed as below picture.

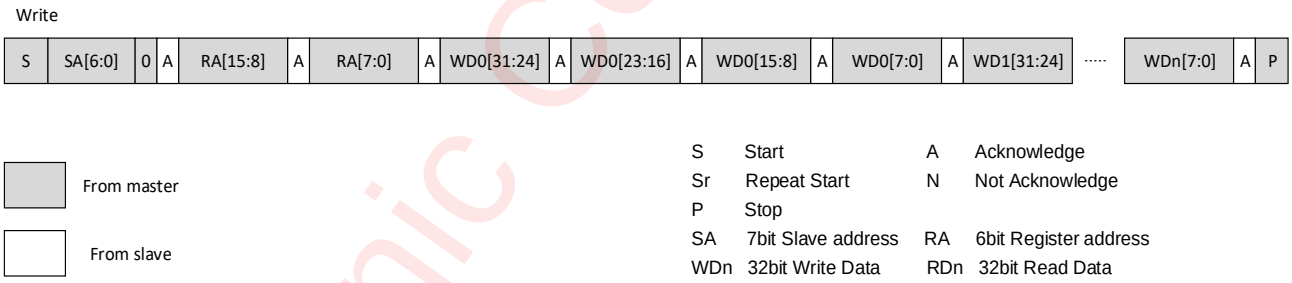


Figure 16 I²C Write Byte Cycle

READ CYCLE

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is showed as below picture.

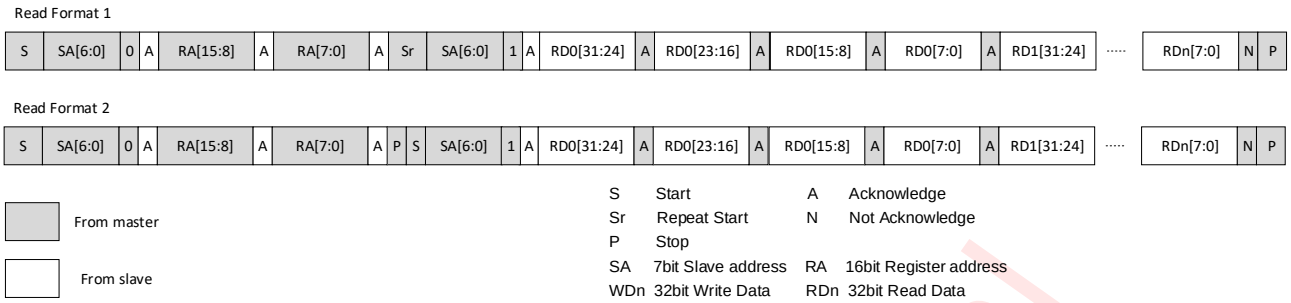


Figure 17 I²C Read Byte Cycle

REGISTER CONFIGURATION

Register List

ADDR	NAME	R/W	Description	Default
0x0000	SCANCTRL0	RW	Scan Control Register 0	0x00000000
0x0004	SCANCTRL1	RW	Scan Control Register 1	0x03F00032
0x0010	AFECFG0_CH0	RW	AFE Configure Register 0 for CH0	0x00050000
0x0014	AFECFG1_CH0	RW	AFE Configure Register 1 for CH0	0x00000009
0x001C	AFECFG3_CH0	RW	AFE Configure Register 3 for CH0	0xFF000000
0x0020	AFECFG4_CH0	RW	AFE Configure Register 4 for CH0	0x00000000
0x0024	AFECFG0_CH1	RW	AFE Configure Register 0 for CH1	0x00050000
0x0028	AFECFG1_CH1	RW	AFE Configure Register 1 for CH1	0x00000009
0x0030	AFECFG3_CH1	RW	AFE Configure Register 3 for CH1	0xFF000000
0x0034	AFECFG4_CH1	RW	AFE Configure Register 4 for CH1	0x00000000
0x0038	AFECFG0_CH2	RW	AFE Configure Register 0 for CH2	0x00050000
0x003C	AFECFG1_CH2	RW	AFE Configure Register 1 for CH2	0x00000009
0x0044	AFECFG3_CH2	RW	AFE Configure Register 3 for CH2	0xFF000000
0x0048	AFECFG4_CH2	RW	AFE Configure Register 4 for CH2	0x00000000
0x004C	AFECFG0_CH3	RW	AFE Configure Register 0 for CH3	0x00050000
0x0050	AFECFG1_CH3	RW	AFE Configure Register 1 for CH3	0x00000009
0x0058	AFECFG3_CH3	RW	AFE Configure Register 3 for CH3	0xFF000000
0x005C	AFECFG4_CH3	RW	AFE Configure Register 4 for CH3	0x00000000
0x0060	AFECFG0_CH4	RW	AFE Configure Register 0 for CH4	0x00050000
0x0064	AFECFG1_CH4	RW	AFE Configure Register 1 for CH4	0x00000009
0x006C	AFECFG3_CH4	RW	AFE Configure Register 3 for CH4	0xFF000000
0x0070	AFECFG4_CH4	RW	AFE Configure Register 4 for CH4	0x00000000
0x0074	AFECFG0_CH5	RW	AFE Configure Register 0 for CH5	0x00050000
0x0078	AFECFG1_CH5	RW	AFE Configure Register 1 for CH5	0x00000009
0x0080	AFECFG3_CH5	RW	AFE Configure Register 3 for CH5	0xFF000000
0x0084	AFECFG4_CH5	RW	AFE Configure Register 4 for CH5	0x00000000
0x008C	WST	RO	Work Status Register	0x00000003
0x0090	STAT0	RO	Status Register 0	0x00000000
0x0094	STAT1	RO	Status Register 1	0x00000000
0x0098	STAT2	RO	Status Register 2	0x00000000
0x009C	CHINTEN	RW	Interrupt Enable Register for Each Channel	0x3F3F3F3F
0x00A0	DSPCFG0_CH0	RW	DSP Configure Register 0 for CH0	0xE0400000
0x00A4	DSPCFG1_CH0	RW	DSP Configure Register 1 for CH0	0x00000000
0x00A8	BLFILT_CH0	RW	Baseline Filter Configure Register for CH0	0x000008D2
0x00B0	PROXCTRL_CH0	RW	Proximity Register for CH0	0x00000000
0x00B4	BLRSTRNG_CH0	RW	Baseline Reset Control Register for CH0	0x0000003F

ADDR	NAME	R/W	Description	Default
0x00B8	PROXTH0_CH0	RW	Proximity Threshold 0 Register for CH0	0x00000000
0x00BC	PROXTH1_CH0	RW	Proximity Threshold 1 Register for CH0	0x00000000
0x00C0	PROXTH2_CH0	RW	Proximity Threshold 2 Register for CH0	0x00000000
0x00C4	PROXTH3_CH0	RW	Proximity Threshold 3 Register for CH0	0x00000000
0x00C8	STDDET_CH0	RW	Steady Detection Register for CH0	0x00000000
0x00CC	INITOFFCFG0_CH0	RW	Initial offset register 0 for CH0	0x00000000
0x00D0	INITOFFCFG1_CH0	RW	Initial offset register 1 for CH0	0x00000000
0x00D4	DATAOFFSET_CH0	RW	Data Offset Control Register for CH0	0x00000000
0x00D8	AOTTAR_CH0	RW	Target Data Setting for Offset Compensation for CH0	0x00000000
0x00DC	DSPCFG0_CH1	RW	DSP Configure Register 0 for CH1	0xE0400000
0x00E0	DSPCFG1_CH1	RW	DSP Configure Register 1 for CH1	0x00000000
0x00E4	BLFILT_CH1	RW	Baseline Filter Configure Register for CH1	0x000008D2
0x00EC	PROXCTRL_CH1	RW	Proximity Register for CH1	0x00000000
0x00F0	BLRSTRNG_CH1	RW	Baseline Reset Control Register for CH1	0x0000003F
0x00F4	PROXTH0_CH1	RW	Proximity Threshold 0 Register for CH1	0x00000000
0x00F8	PROXTH1_CH1	RW	Proximity Threshold 1 Register for CH1	0x00000000
0x00FC	PROXTH2_CH1	RW	Proximity Threshold 2 Register for CH1	0x00000000
0x0100	PROXTH3_CH1	RW	Proximity Threshold 3 Register for CH1	0x00000000
0x0104	STDDET_CH1	RW	Steady Detection Register for CH1	0x00000000
0x0108	INITOFFCFG0_CH1	RW	Initial offset register 0 for CH1	0x00000000
0x010C	INITOFFCFG1_CH1	RW	Initial offset register 1 for CH1	0x00000000
0x0110	DATAOFFSET_CH1	RW	Data Offset Control Register for CH1	0x00000000
0x0114	AOTTAR_CH1	RW	Target Data Setting for Offset Compensation for CH1	0x00000000
0x0118	DSPCFG0_CH2	RW	DSP Configure Register 0 for CH2	0xE0400000
0x011C	DSPCFG1_CH2	RW	DSP Configure Register 1 for CH2	0x00000000
0x0120	BLFILT_CH2	RW	Baseline Filter Configure Register for CH2	0x000008D2
0x0128	PROXCTRL_CH2	RW	Proximity Register for CH2	0x00000000
0x012C	BLRSTRNG_CH2	RW	Baseline Reset Control Register for CH2	0x0000003F
0x0130	PROXTH0_CH2	RW	Proximity Threshold 0 Register for CH2	0x00000000
0x0134	PROXTH1_CH2	RW	Proximity Threshold 1 Register for CH2	0x00000000
0x0138	PROXTH2_CH2	RW	Proximity Threshold 2 Register for CH2	0x00000000
0x013C	PROXTH3_CH2	RW	Proximity Threshold 3 Register for CH2	0x00000000
0x0140	STDDET_CH2	RW	Steady Detection Register for CH2	0x00000000
0x0144	INITOFFCFG0_CH2	RW	Initial offset register 0 for CH2	0x00000000
0x0148	INITOFFCFG1_CH2	RW	Initial offset register 1 for CH2	0x00000000
0x014C	DATAOFFSET_CH2	RW	Data Offset Control Register for CH2	0x00000000
0x0150	AOTTAR_CH2	RW	Target Data Setting for Offset Compensation for CH2	0x00000000

ADDR	NAME	R/W	Description	Default
0x0154	DSPCFG0_CH3	RW	DSP Configure Register 0 for CH3	0xE0400000
0x0158	DSPCFG1_CH3	RW	DSP Configure Register 1 for CH3	0x00000000
0x015C	BLFILT_CH3	RW	Baseline Filter Configure Register for CH3	0x000008D2
0x0164	PROXCTRL_CH3	RW	Proximity Register for CH3	0x00000000
0x0168	BLRSTRNG_CH3	RW	Baseline Reset Control Register for CH3	0x0000003F
0x016C	PROXTH0_CH3	RW	Proximity Threshold 0 Register for CH3	0x00000000
0x0170	PROXTH1_CH3	RW	Proximity Threshold 1 Register for CH3	0x00000000
0x0174	PROXTH2_CH3	RW	Proximity Threshold 2 Register for CH3	0x00000000
0x0178	PROXTH3_CH3	RW	Proximity Threshold 3 Register for CH3	0x00000000
0x017C	STDDET_CH3	RW	Steady Detection Register for CH3	0x00000000
0x0180	INITOFFCFG0_CH3	RW	Initial offset register 0 for CH3	0x00000000
0x0184	INITOFFCFG1_CH3	RW	Initial offset register 1 for CH3	0x00000000
0x0188	DATAOFFSET_CH3	RW	Data Offset Control Register for CH3	0x00000000
0x018C	AOTTAR_CH3	RW	Target Data Setting for Offset Compensation for CH3	0x00000000
0x0190	DSPCFG0_CH4	RW	DSP Configure Register 0 for CH4	0xE0400000
0x0194	DSPCFG1_CH4	RW	DSP Configure Register 1 for CH4	0x00000000
0x0198	BLFILT_CH4	RW	Baseline Filter Configure Register for CH4	0x000008D2
0x01A0	PROXCTRL_CH4	RW	Proximity Register for CH4	0x00000000
0X01A4	BLRSTRNG_CH4	RW	Baseline Reset Control Register for CH4	0x0000003F
0x01A8	PROXTH0_CH4	RW	Proximity Threshold 0 Register for CH4	0x00000000
0x01AC	PROXTH1_CH4	RW	Proximity Threshold 1 Register for CH4	0x00000000
0x01B0	PROXTH2_CH4	RW	Proximity Threshold 2 Register for CH4	0x00000000
0x01B4	PROXTH3_CH4	RW	Proximity Threshold 3 Register for CH4	0x00000000
0x01B8	STDDET_CH4	RW	Steady Detection Register for CH4	0x00000000
0x01BC	INITOFFCFG0_CH4	RW	Initial offset register 0 for CH4	0x00000000
0x01C0	INITOFFCFG1_CH4	RW	Initial offset register 1 for CH4	0x00000000
0x01C4	DATAOFFSET_CH4	RW	Data Offset Control Register for CH4	0x00000000
0x01C8	AOTTAR_CH4	RW	Target Data Setting for Offset Compensation for CH4	0x00000000
0x01CC	DSPCFG0_CH5	RW	DSP Configure Register 0 for CH5	0xE0400000
0x01D0	DSPCFG1_CH5	RW	DSP Configure Register 1 for CH5	0x00000000
0x01D4	BLFILT_CH5	RW	Baseline Filter Configure Register for CH5	0x000008D2
0x01DC	PROXCTRL_CH5	RW	Proximity Register for CH5	0x00000000
0X01E0	BLRSTRNG_CH5	RW	Baseline Reset Control Register for CH5	0x0000003F
0x01E4	PROXTH0_CH5	RW	Proximity Threshold 0 Register for CH5	0x00000000
0x01E8	PROXTH1_CH5	RW	Proximity Threshold 1 Register for CH5	0x00000000
0x01EC	PROXTH2_CH5	RW	Proximity Threshold 2 Register for CH5	0x00000000
0x01F0	PROXTH3_CH5	RW	Proximity Threshold 3 Register for CH5	0x00000000
0x01F4	STDDET_CH5	RW	Steady Detection Register for CH5	0x00000000

ADDR	NAME	R/W	Description	Default
0x01F8	INITOFFCFG0_CH5	RW	Initial offset register 0 for CH5	0x00000000
0x01FC	INITOFFCFG1_CH5	RW	Initial offset register 1 for CH5	0x00000000
0x0200	DATAOFFSET_CH5	RW	Data Offset Control Register for CH5	0x00000000
0x0204	AOTTAR_CH5	RW	Target Data Setting for Offset Compensation for CH5	0x00000000
0x0208	ATCCR0	RW	Adaptive Temperature Compensation Control Register 0	0x00000005
0x020C	ATCCR1	RW	Adaptive Temperature Compensation Control Register 1	0x00000005
0x0210	COMP_CH0	RO	Comp Data Register of CH0	0x00000000
0x0214	COMP_CH1	RO	Comp Data Register of CH1	0x00000000
0x0218	COMP_CH2	RO	Comp Data Register of CH2	0x00000000
0x021C	COMP_CH3	RO	Comp Data Register of CH3	0x00000000
0x0220	COMP_CH4	RO	Comp Data Register of CH4	0x00000000
0x0224	COMP_CH5	RO	Comp 0Data Register of CH5	0x00000000
0x0228	BASELINE_CH0	RO	Baseline Data Register of CH0	0x00000000
0x022C	BASELINE_CH1	RO	Baseline Data Register of CH1	0x00000000
0x0230	BASELINE_CH2	RO	Baseline Data Register of CH2	0x00000000
0x0234	BASELINE_CH3	RO	Baseline Data Register of CH3	0x00000000
0x0238	BASELINE_CH4	RO	Baseline Data Register of CH4	0x00000000
0x023C	BASELINE_CH5	RO	Baseline Data Register of CH5	0x00000000
0x0240	DIFF_CH0	RO	Difference Data Register of CH0	0x00000000
0x0244	DIFF_CH1	RO	Difference Data Register of CH1	0x00000000
0x0248	DIFF_CH2	RO	Difference Data Register of CH2	0x00000000
0x024C	DIFF_CH3	RO	Difference Data Register of CH3	0x00000000
0x0250	DIFF_CH4	RO	Difference Data Register of CH4	0x00000000
0x0254	DIFF_CH5	RO	Difference Data Register of CH5	0x00000000
0x0410	FWVER2	RO	Firmware Version 2	0x03000B00
0xF008	CMD	WO	Command Register	0x00000000
0xF080	IRQSRC	RC	Interrupt Source Register	0x00000000
0xF084	IRQEN	RW	Interrupt Enable Register	0x00000FFF
0xF0F0	I2CADDR	RO	I²C Device Address Register	0x00000012
0xFF00	OSCEN	RW	Host Control Register	0x00000301
0xFF0C	RESET	WO	Software Reset Register	0x01000000
0xFF10	CHIPID	RO	CHIP ID Register	0xA9610B00

Register Detailed Description

SCANCTRL0: Scan Control Register 0 (Address 0000h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:14	Reserved	RO	Reserved	h00000
13:8	AOTEN	WC	Defines which channels need auto offset tuning (AOT). And after the offset tuning, the corresponding bit will be cleared to “0”. b0: Disable b1: Enable Bit[13:8] = [CH5, CH4, CH3, CH2, CH1, CH0]	b000000
7:6	Reserved	RO	Reserved	b00
5:0	CHEN	RW	Enable the measurement channel. b0: Disable b1: Enable Bit[5:0] = [CH5, CH4, CH3, CH2, CH1, CH0]	b000000

SCANCTRL1: Scan Control Register 1 (Address 0004h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:26	Reserved	RO	Reserved	b000000
25:20	DOZEEN	RW	Doze mode enable. b0: Disable b1: Enable Bit[25:20] = [CH5, CH4, CH3, CH2, CH1, CH0]	b111111
19:16	Reserved	RO	Reserved	b0000
15:11	DOZEDEB	RW	Debounce times for entering into doze mode.	b00000
10:0	SCANPERIOD	RW	Basic scan period for active mode:	h032

AFECFG0_CH0: AFE Configure Register 0 for CH0 (Address 0010h)
AFECFG0_CH1: AFE Configure Register 0 for CH1 (Address 0024h)
AFECFG0_CH2: AFE Configure Register 0 for CH2 (Address 0038h)
AFECFG0_CH3: AFE Configure Register 0 for CH3 (Address 004Ch)
AFECFG0_CH4: AFE Configure Register 0 for CH4 (Address 0060h)
AFECFG0_CH5: AFE Configure Register 0 for CH5 (Address 0074h)

Bit	**Symbol**	**R/W**	**Description**	**Default**
31:30	MEASMOD_CHx	RW	Measurement mode selection of CHx (x = 0, 1, …, 5). b00: Capacitance b10: Temperature other: Reserved	b00
29:26	RDRV_CHx	RW	Driving resistance of sensing electrode for CHx.	b0000
25:22	Reserved	RO	Reserved	b0000

21:20	ROFF_CHx	RW	Driving resistance of offset capacitance for CHx. b00: 125 Ω b01: 250 Ω b10: 500 Ω b11: 1 kΩ	b00
19:16	CDCRES_CHx	RW	Capacitance-Digital-Conversion resolution setting for CHx. Higher resolution achieves higher SNR, but takes longer measurement time.	b0101
15:12	CRANGE_CHx	RW	Capacitance measurement range of CHx. b0000: 1.1 pF b0001: 2.2 pF b0010: 3.3 pF b0011: 4.4 pF b0100: 6.6 pF b0101: 7.7 pF b0110: 8.8 pF b0111: 9.9 pF b1000: 11 pF b1001: 12.1 pF b1010: 13.2 pF b1011: 14.3 pF b1100: 16.5 pF b1101: 17.6 pF b1110: 18.7 pF b1111: 19.8 pF	b0000
11:10	Reserved	RO	Reserved	b00
9:8	CS4SEL_CHx	RW	Same as CS0SEL_CHx for pin CS4.	b00
7:6	CS3SEL_CHx	RW	Same as CS0SEL_CHx for pin CS3.	b00
5:4	CS2SEL_CHx	RW	Same as CS0SEL_CHx for pin CS2.	b00
3:2	CS1SEL_CHx	RW	Same as CS0SEL_CHx for pin CS1.	b00
1:0	CS0SEL_CHx	RW	CS0 connection for CHx. b00: HZ b01: Measured input b10: Shield b11: GND	b00

AFECFG1_CH0: AFE Configure Register 1 for CH0 (Address 0014h)
AFECFG1_CH1: AFE Configure Register 1 for CH1 (Address 0028h)
AFECFG1_CH2: AFE Configure Register 1 for CH2 (Address 003Ch)
AFECFG1_CH3: AFE Configure Register 1 for CH3 (Address 0050h)
AFECFG1_CH4: AFE Configure Register 1 for CH4 (Address 0064h)
AFECFG1_CH5: AFE Configure Register 1 for CH5 (Address 0078h)

Bit	Symbol	R/W	Description	Default
31:16	COFF_CHx	RW	Offset capacitance for CHx (x = 0, 1, …, 5).	h0000
15:8	Reserved	RO	Reserved	h00
7:0	FREQ_CHx	RW	Driving frequency for CHx.	h09

AFECFG3_CH0: AFE Configure Register 3 for CH0 (Address 001Ch)
AFECFG3_CH1: AFE Configure Register 3 for CH1 (Address 0030h)

AFECFG3_CH2: AFE Configure Register 3 for CH2 (Address 0044h) AFECFG3_CH3: AFE Configure Register 3 for CH3 (Address 0058h) AFECFG3_CH4: AFE Configure Register 3 for CH4 (Address 006Ch) AFECFG3_CH5: AFE Configure Register 3 for CH5 (Address 0080h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	Reserved	RO	Reserved	h00
23:16	ACTPERIOD_CHx	RW	Scan period in active mode for CHx.	h00
15:0	Reserved	RO	Reserved	h0000

AFECFG4_CH0: AFE Configure Register 4 for CH0 (Address 0020h) AFECFG4_CH1: AFE Configure Register 4 for CH1 (Address 0034h) AFECFG4_CH2: AFE Configure Register 4 for CH2 (Address 0048h) AFECFG4_CH3: AFE Configure Register 4 for CH3 (Address 005Ch) AFECFG4_CH4: AFE Configure Register 4 for CH4 (Address 0070h) AFECFG4_CH5: AFE Configure Register 4 for CH5 (Address 0084h)				
31:25	DOZEPERIOD_CHx	RW	Scan period in dozen mode for CHx.	h00
24:0	Reserved	RO	Reserved	h000000

WST: Work Status Register (Address 008Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	WST	RO	Current work status. h00: Active mode h01: Doze mode Other: Reserved	h00
23:0	Reserved	RO	Reserved	h000003

STAT0: Status Register 0 (Address 0090h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:30	Reserved	RO	Reserved	b00
29:24	PROX0ST	RO	Proximity status 0 for corresponding channel. When DIFF > PROXTH0 and more than INDEB_CHx times, the corresponding bit will be set. Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
23:22	Reserved	RO	Reserved	b00
21:16	PROX1ST	RO	Proximity status 1 for corresponding channel. When DIFF > PROXTH1 and more than INDEB_CHx times, the corresponding bit will be set. Bit[21:16]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
15:14	Reserved	RO	Reserved	b00
13:8	PROX2ST	RO	Proximity status 2 for corresponding channel. When DIFF > PROXTH2 and more than INDEB_CHx times, the corresponding bit will be set. Bit[13:8]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
7:6	Reserved	RO	Reserved	b00

5:0	PROX3ST	RO	Proximity status 3 for corresponding channel. When DIFF > PROXTH3 and more than INDEB_CHx times, the corresponding bit will be set. Bit[5:0]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000

STAT1: Status Register 1 (Address 0094h)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	b00
29:24	STDST	RO	Steady status indication. Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
23:14	Reserved	RO	Reserved	h000
13:8	AOTST	RO	Indicates whether AOT is being performed. Bit[13:8]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
7:6	Reserved	RO	Reserved	b00
5:0	SATST	RO	data saturation status indication. Bit[5:0]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000

STAT2: Status Register 2 (Address 0098h)

Bit	Symbol	R/W	Description	Default
31:22	Reserved	RO	Reserved	h000
21:16	INITPROXST	RO	Indicates if proximity has being detected when performing start-up offset compensation. Bit[21:16] = [CH5, CH4, CH3, CH2, CH1, CH0]	b000000
15:5	Reserved	RO	Reserved	h000
4	CONVST	RO	Indicates if any channel is being measured or processed. b0: Idle b1: Data is being measured or processed	b0
3	INITPROXSTANY	RO	Indicates if any INITPROXST is set to 1.	b0
2	Reserved	RO	Reserved	b0
1	STDSTALL	RO	Indicates if all STDST bits are set to 1.	b0
0	PROXSTANY	RO	Indicates if any PROXST is set to 1.	b0

CHINTEN : Interrupt Enable for Each channel (Address 009Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	b00
29:24	PROXSTINTEN	RW	Proximity status interrupt enable for each channel: b0: Disable b1: Enable Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	b111111
23	EXITSATANYEN	RW	Exit saturation judgment enable for any channel: b0: Disable b1: Enable	b0

22	ENTERSATANYEN	RW	Enter saturation judgment enable for any channel: b0: Disable b1: Enable	b0
21:16	PROXANYINTEN	RW	Proximity interrupt enable for each channel: b0: Disable b1: Enable Bit[21:16]=[CH5, CH4, CH3, CH2, CH1, CH0]	b111111
15	EXITSTDANYEN	RW	Exit steady state judgment enable for any channel: b0: Disable b1: Enable	b0
14	ENTERSTDANYEN	RW	Enter steady state judgment enable for any channel: b0: Disable b1: Enable	b0
13:8	FARANYINTEN	RW	Far interrupt enable for each channel: b0: Disable b1: Enable Bit[13:8]=[CH5, CH4, CH3, CH2, CH1, CH0]	b111111
7	EXITTOUCHANYEN	RW	Exit touch state judgment enable for any channel: b0: Disable b1: Enable	b0
6	ENTERTOUCHANYEN	RW	Enter touch state judgment enable for any channel: b0: Disable b1: Enable	b0
5:0	CONVDONEINTEN	RW	Scan over interrupt for each channel: b0: Disable b1: Enable Bit[5:0]=[CH5, CH4, CH3, CH2, CH1, CH0]	b111111

DSPCFG0_CH0: DSP Configure Register 0 for CH0 (Address 00A0h)
DSPCFG0_CH1: DSP Configure Register 0 for CH1 (Address 00DCh)
DSPCFG0_CH2: DSP Configure Register 0 for CH2 (Address 0118h)
DSPCFG0_CH3: DSP Configure Register 0 for CH3 (Address 0154h)
DSPCFG0_CH4: DSP Configure Register 0 for CH4 (Address 0190h)
DSPCFG0_CH5: DSP Configure Register 0 for CH5 (Address 01CCh)

Bit	Symbol	R/W	Description	Default
31:27	Reserved	RO	Reserved	b11100
26:25	SMPLNUM_CHx	RW	The number of sample for CHx.	b00
24:22	LPFCOEF_CHx	RW	Coefficient of the low pass filter for CHx.	b001
21:20	Reserved	RO	Reserved	h0
19:0	ATCCFG0_CHx	RW	Auto temperature configure register0 for CHx.	h00000

DSPCFG1_CH0: DSP Configure Register 1 for CH0 (Address 00A4h)
DSPCFG1_CH1: DSP Configure Register 1 for CH1 (Address 00E0h)

DSPCFG1_CH2: DSP Configure Register 1 for CH2 (Address 011Ch)
DSPCFG1_CH3: DSP Configure Register 1 for CH3 (Address 0158h)
DSPCFG1_CH4: DSP Configure Register 1 for CH4 (Address 0194h)
DSPCFG1_CH5: DSP Configure Register 1 for CH5 (Address 01D0h)

Bit	Symbol	R/W	Description	Default
31:16	ATCCFG1_CHx	RW	Auto temperature configure register1 for CHx.	h0000
15:8	PROXRLSCNT_CHx	RW	Counter for long time proximity release of CHx.	h00
7:4	BASERSTCNT_CHx	RW	Defines the times of DIFF < -PROXTH0 before reset baseline.	b0000
3:2	NEGSATEN_CHx	RW	Negative saturation judgment and process method for CHx (x=0, 1, …, 5). b00: Disable for CompData. b01: Only judge saturation status b10: Enable the saturation judgment, and when saturation detected, capacitance offset compensation will be performed automatically. b11: Reserved	b00
1:0	NEGSATTH_CHx	RW	Negative saturation threshold. b00：- 0x09A000 b01：- 0x0BA000 b10：- 0x0DA000 b11：- 0x0EF000	b00

BLFILT_CH0: Baseline Filter Configure Register for CH0 (Address 00A8h)
BLFILT_CH1: Baseline Filter Configure Register for CH1 (Address 00E4h)
BLFILT_CH2: Baseline Filter Configure Register for CH2 (Address 0120h)
BLFILT_CH3: Baseline Filter Configure Register for CH3 (Address 015Ch)
BLFILT_CH4: Baseline Filter Configure Register for CH4 (Address 0198h)
BLFILT_CH5: Baseline Filter Configure Register for CH5 (Address 01D4h)

Bit	Symbol	R/W	Description	Default
31:30	POSSATEN_CHx	RW	Positive saturation judgment and process method for CHx (x=0, 1, …, 5). b00: Disable saturation judgment for CompData b01: Only judge saturation status b10: Enable the saturation judgment, and when saturation detected, capacitance offset compensation will be performed automatically. b11: Reserved	b00
29:28	POSSATTH_CHx	RW	Positive saturation threshold of CHx. b00：0x09A000 b01：0x0BA000 b10：0x0DA000 b11：0x0EF000	b00
27:26	SATDEB_CHx	RW	The debouncer applied to set the saturation status for CHx.	b00
25	Reserved	RO	Reserved	b0

24:19	BLMAX_CHx	RW	Defines the max threshold of baseline that will trig offset compensation for CHx.	b000000
18:13	BLMIN_CHx	RW	Defines the min threshold of baseline that will trig offset compensation for CHx.	b000000
12:11	BLERRDEB_CHx	RW	The debouncer applied to baseline error judgment.	b01
10:9	BLTSDOZE_CHx	RW	Baseline tracing speed factor in doze mode for CHx.	b00
8:5	BLFUPCOEF_CHx	RW	Coefficient of baseline upward tracing for CHx.	b0110
4:2	BLFDOWNCOEF_CHx	RW	Coefficient of baseline downward tracing for CHx.	b100
1:0	Reserved	RO	Reserved	b10

PROXCTRL_CH0: Proximity Register for CH0 (Address 00B0h)
PROXCTRL_CH1: Proximity Register for CH1 (Address 00ECh)
PROXCTRL_CH2: Proximity Register for CH2 (Address 0128h)
PROXCTRL_CH3: Proximity Register for CH3 (Address 0164h)
PROXCTRL_CH4: Proximity Register for CH4 (Address 01A0h)
PROXCTRL_CH5: Proximity Register for CH5 (Address 01DCh)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	h00000
13:12	THHYST_CHx	RW	Defines the hysteresis of PROXTH0/PROXTH1/PROXTH2/PROXTH3 for CHx. b00: Hyst = 0 b01: Hyst = Th/16 b10: Hyst = Th/8 b11: Hyst = Th/4	b00
11:10	INDEB_CHx	RW	The debouncer applied to enter into proximity status for CHx.	b00
9:8	OUTDEB_CHx	RW	The debouncer applied to exit proximity status for CHx.	b00
7:0	Reserved	RO	Reserved	h00

BLRSTRNG_CH0: Baseline Reset Control Register for CH0 (Address 00B4h)
BLRSTRNG_CH1: Baseline Reset Control Register for CH1 (Address 00F0h)
BLRSTRNG_CH2: Baseline Reset Control Register for CH2 (Address 012Ch)
BLRSTRNG_CH3: Baseline Reset Control Register for CH3 (Address 0168h)
BLRSTRNG_CH4: Baseline Reset Control Register for CH4 (Address 01A4h)
BLRSTRNG_CH5: Baseline Reset Control Register for CH5 (Address 01E0h)

Bit	Symbol	R/W	Description	Default
31:6	Reserved	RO	Reserved	h000000
5:0	BLRSTRNG_CHx	RW	Select which channels to calibrate when the baseline is abnormal b0: Disable	b111111

			b1: Enable Bit[5:0] = [CH5, CH4, CH3, CH2, CH1, CH0]	

PROXTH0_CH0: Proximity Threshold 0 Register for CH0 (Address 00B8h)
PROXTH0_CH1: Proximity Threshold 0 Register for CH1 (Address 00F4h)
PROXTH0_CH2: Proximity Threshold 0 Register for CH2 (Address 0130h)
PROXTH0_CH3: Proximity Threshold 0 Register for CH3 (Address 016Ch)
PROXTH0_CH4: Proximity Threshold 0 Register for CH4 (Address 01A8h)
PROXTH0_CH5: Proximity Threshold 0 Register for CH5 (Address 01E4h)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h000
20:0	PROXTH0_CHx	RW	Defines the proximity threshold 0 of CHx:	h000000

PROXTH1_CH0: Proximity Threshold 1 Register for CH0 (Address 00BCh)
PROXTH1_CH1: Proximity Threshold 1 Register for CH1 (Address 00F8h)
PROXTH1_CH2: Proximity Threshold 1 Register for CH2 (Address 0134h)
PROXTH1_CH3: Proximity Threshold 1 Register for CH3 (Address 0170h)
PROXTH1_CH4: Proximity Threshold 1 Register for CH4 (Address 01ACh)
PROXTH1_CH5: Proximity Threshold 1 Register for CH5 (Address 01E8h)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h000
20:0	PROXTH1_CHx	RW	Defines the proximity threshold 1 of CHx:	h000000

PROXTH2_CH0: Proximity Threshold 2 Register for CH0 (Address 00C0h)
PROXTH2_CH1: Proximity Threshold 2 Register for CH1 (Address 00FCh)
PROXTH2_CH2: Proximity Threshold 2 Register for CH2 (Address 0138h)
PROXTH2_CH3: Proximity Threshold 2 Register for CH3 (Address 0174h)
PROXTH2_CH4: Proximity Threshold 2 Register for CH4 (Address 01B0h)
PROXTH2_CH5: Proximity Threshold 2 Register for CH5 (Address 01ECh)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h000
20:0	PROXTH2_CHx	RW	Defines the proximity threshold 2 of CHx:	h000000

PROXTH3_CH0: Proximity Threshold 3 Register for CH0 (Address 00C4h)
PROXTH3_CH1: Proximity Threshold 3 Register for CH1 (Address 0100h)
PROXTH3_CH2: Proximity Threshold 3 Register for CH2 (Address 013Ch)
PROXTH3_CH3: Proximity Threshold 3 Register for CH3 (Address 0178h)
PROXTH3_CH4: Proximity Threshold 3 Register for CH4 (Address 01B4h)
PROXTH3_CH5: Proximity Threshold 3 Register for CH5 (Address 01F0h)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h000
20:0	PROXTH3_CHx	RW	Defines the proximity threshold 3 of CHx:	h000000

STDDET_CH0: Steady Detection Register for CH0 (Address 00C8h)
STDDET_CH1: Steady Detection Register for CH1 (Address 0104h)
STDDET_CH2: Steady Detection Register for CH2 (Address 0140h)

STDDET_CH3: Steady Detection Register for CH3 (Address 017Ch)
STDDET_CH4: Steady Detection Register for CH4 (Address 01B8h)
STDDET_CH5: Steady Detection Register for CH5 (Address 01F4h)

Bit	Symbol	R/W	Description	Default
31:16	STDTH_CHx	RW	The steady threshold for CHx.	h0000
15:14	STDTHMUL_CHx	RW	Steady threshold multiply factor:	b00
13:11	STDSMPLNUM_CHx	RW	The number of data to be compared with steady threshold for CHx.	b000
10:9	STDJUDGEEN_CHx	RW	Data selection and steady check for CHx. b00: Disable data steady judge b01: Reserved b10: Use CompData as judgment data b11: Use DIFF as judgment data Note: Judge data steady or not only when proximity is detected.	b00
8:2	STDINDEB_CHx	RW	The debouncer applied to enter steady status for CHx.	h00
1:0	STDOUTDEB_CHx	RW	The debouncer applied to exit steady status for CHx.	b00

INITOFFCFG0_CH0: Initial offset register 0 for CH0 (Address 00CCh)
INITOFFCFG0_CH1: Initial offset register 0 for CH1 (Address 0108h)
INITOFFCFG0_CH2: Initial offset register 0 for CH2 (Address 0144h)
INITOFFCFG0_CH3: Initial offset register 0 for CH3 (Address 0180h)
INITOFFCFG0_CH4: Initial offset register 0 for CH4 (Address 01BCh)
INITOFFCFG0_CH5: Initial offset register 0 for CH5 (Address 01F8h)

Bit	Symbol	R/W	Description	Default
31:16	INITCOMPTH_CHx	RW	The initial Comp Data threshold for CHx.	h0000
15:0	INITCOFF_CHx	RW	The default value of offset compensation for CHx.	h0000

INITOFFCFG1_CH0: Initial offset register 1 for CH0 (Address 00D0h)
INITOFFCFG1_CH1: Initial offset register 1 for CH1 (Address 010Ch)
INITOFFCFG1_CH2: Initial offset register 1 for CH2 (Address 0148h)
INITOFFCFG1_CH3: Initial offset register 1 for CH3 (Address 0184h)
INITOFFCFG1_CH4: Initial offset register 1 for CH4 (Address 01C0h)
INITOFFCFG1_CH5: Initial offset register 1 for CH5 (Address 01FCh)

Bit	Symbol	R/W	Description	Default
31	INITPROXEN_CHx	RW	Enable for proximity detection during start up. b0: Disable b1: Enable	b0
30:0	Reserved	RO	Reserved	h00000000

DATAOFFSET_CH0: Data Offset Control Register for CH0 (Address 00D4h)
DATAOFFSET_CH1: Data Offset Control Register for CH1 (Address 0110h)
DATAOFFSET_CH2: Data Offset Control Register for CH2 (Address 014Ch)
DATAOFFSET_CH3: Data Offset Control Register for CH3 (Address 0188h)

DATAOFFSET_CH4: Data Offset Control Register for CH4 (Address 01C4h)
DATAOFFSET_CH5: Data Offset Control Register for CH5 (Address 0200h)

Bit	Symbol	R/W	Description	Default
31:22	Reserved	RO	Reserved	h000
21:0	DATAOFFSET_CHx	RW	Offset value for Data.	h000000

AOTTAR_CH0: Target Data Setting for Offset Compensation for CH0 (Address 00D8h)
AOTTAR_CH1: Target Data Setting for Offset Compensation for CH1 (Address 0114h)
AOTTAR_CH2: Target Data Setting for Offset Compensation for CH2 (Address 0150h)
AOTTAR_CH3: Target Data Setting for Offset Compensation for CH3 (Address 018Ch)
AOTTAR_CH4: Target Data Setting for Offset Compensation for CH4 (Address 01C8h)
AOTTAR_CH5: Target Data Setting for Offset Compensation for CH5 (Address 0204h)

Bit	Symbol	R/W	Description	Default
31:22	Reserved	RO	Reserved	h000
21:0	AOTTAR_CHx	RW	Defines target value when performing auto offset tuning.	h000000

ATCCR0: Adaptive Temperature Compensation Control Register 0 (Address 0208h)

Bit	Symbol	R/W	Description	Default
31:27	Reserved	RO	Reserved	b00000
26:0	ATCCR0	RW	Adaptive Temperature Compensation Control Register 0.	h0000005

ATCCR1: Adaptive Temperature Compensation Control Register 1 (Address 020Ch)

Bit	Symbol	R/W	Description	Default
31:27	Reserved	RW	Reserved	b00000
26:0	ATCCR1	RW	Adaptive Temperature Compensation Control Register 1.	h0000005

COMP_CH0: Comp Data Register of CH0 (Address 0210h)
COMP_CH1: Comp Data Register of CH1 (Address 0214h)
COMP_CH2: Comp Data Register of CH2 (Address 0218h)
COMP_CH3: Comp Data Register of CH3 (Address 021Ch)
COMP_CH4: Comp Data Register of CH4 (Address 0220h)
COMP_CH5: Comp Data Register of CH5 (Address 0224h)

Bit	Symbol	R/W	Description	Default
31:0	COMP_CHx	RO	Current value (COMP) of CHx.	h00000000

BASELINE_CH0: Baseline Data Register of CH0 (Address 0228h)
BASELINE_CH1: Baseline Data Register of CH1 (Address 022Ch)
BASELINE_CH2: Baseline Data Register of CH2 (Address 0230h)
BASELINE_CH3: Baseline Data Register of CH3 (Address 0234h)
BASELINE_CH4: Baseline Data Register of CH4 (Address 0238h)
BASELINE_CH5: Baseline Data Register of CH5 (Address 023Ch)

Bit	Symbol	R/W	Description	Default

31:0	BASELINE_CHx	RO	Current baseline value (BASELINE) of CHx.	h00000000

DIFF_CH0: Difference Data Register of CH0 (Address 0240h)
DIFF_CH1: Difference Data Register of CH1 (Address 0244h)
DIFF_CH2: Difference Data Register of CH2 (Address 0248h)
DIFF_CH3: Difference Data Register of CH3 (Address 024Ch)
DIFF_CH4: Difference Data Register of CH4 (Address 0250h)
DIFF_CH5: Difference Data Register of CH5 (Address 0254h)

Bit	Symbol	R/W	Description	Default
31:0	DIFF_CHx	RO	Current different Data (DIFF) of CHx.	h00000000

FWVER2: Firmware Version 2 Resister (Address 0410h)

Bit	Symbol	R/W	Description	Default
31:0	FWVER2	RO	Firmware Version 2	h03000B00

CMD: Command Register (Address F008h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	h000000
7:0	CMD	WO	Commands: h00: Reserved h01: IC will enter active mode h02: IC will enter normal sleep mode h03: IC will enter deep sleep mode Other: IC will enter sleep mode after current scan period finish.	h00

IRQSRC: Interrupt Source Register (Address F080h)

Bit	Symbol	R/W	Description	Default
31:15	Reserved	RO	Reserved	h00000
14	EXITSTDANYIRQ	RC	Exit steady state interrupt source status b0: No channels exit steady state b1: Any STDST falling edge	b0
13	ENTERSTDANYIRQ	RC	Enter steady state interrupt source status b0: No channels enter steady state b1: Any STDST rising edge	b0
12	EXITTOUCHANYIRQ	RC	Exit touch state interrupt source status b0: No channels exit touch state b1: Any PROX1/2/3ST falling edge	b0
11	INITPROXIRQ	RC	Initial proximity interrupt source status b0: No channels detect initial proximity b1: Any INITPROXST falling edge	b0
10:9	Reserved	RC	Reserved	b00
8	EXITSATANYIRQ	RC	Exit saturation interrupt source status b0: No channels exit saturation state b1: Any SATST falling edge	b0

7	ENTERSATANYIRQ	RC	Enter saturation interrupt source status b0: No channels enter saturation state b1: Any SATST rising edge	b0
6	PROXSTATANYIRQ	RC	Proximity status interrupt source status b0: No channels in proximity state b1: Any PROX0ST is set	b0
5	TOUCHANYIRQ	RC	Touch interrupt source status b0: No channels enter touch state b1: Any PROX1/2/3ST rising edge	b0
4	CONVDONEIRQ	RC	Indicates if the AFE sampling conversion is done. b0: Not done b1: Done	b0
3	AOTDONEIRQ	RC	Auto offset tuning done interrupt source status b0: Invalid b1: AOT Done	b0
2	FARANYIRQ	RC	Exit proximity state interrupt source status b0: No channels exit proximity state b1: Any PROX0ST falling edge	b0
1	PROXANYIRQ	RC	Enter proximity state interrupt source status b0: No channels enter proximity state b1: Any PROX0ST rising edge	b0
0	INITOVERIRQ	RC	Chip initial over interrupt source status b0: Invalid b1: Initial over	b0

IRQEN: Interrupt Enable Register (Address F084h)

Bit	Symbol	R/W	Description	Default
31:15	Reserved	RO	Reserved	h00000
14	EXITSTDANYIRQEN	RW	Enable exit steady state interrupt (any). b0: Disable b1: Enable Note: If need to enable the interrupt, the bit EXITSTDANYEN (address 009Ch) should be set to 1.	b0
13	ENTERSTDANYIRQEN	RW	Enable enter steady state interrupt (any). b0: Disable b1: Enable Note: If need to enable the interrupt, the bit ENTERSTDANYEN (address 009Ch) should be set to 1.	b0
12	EXITTOUCHANYIRQEN	RW	Enable the interrupt when any channel exits touch state (PROX1/2/3ST from 1 to 0, any). b0: Disable b1: Enable Note: If need to enable the interrupt, the bit EXITTOUCHANYEN (address 009Ch) should be set to 1.	b0
11	INITPROXIRQEN	RW	Start-up proximity interrupt Enable (any). b0: Disable b1: Enable	b1

10:9	Reserved	RW	Reserved	b11
8	EXITSATANYIRQEN	RW	Enable the interrupt when any channel exits saturated state (any). b0: Disable b1: Enable Note: If need to enable the interrupt, the bit EXITSATANYEN (address 009Ch) should be set to 1.	b1
7	ENTERSATANYIRQEN	RW	Enable enter saturated state interrupt (any). b0: Disable b1: Enable Note: If need to enable the interrupt, the bit ENTERSATANYEN (address 009Ch) should be set to 1.	b1
6	PROXSTANYIRQEN	RW	Enable proximity interrupt (any). b0: Disable b1: Enable Note: If need to enable the interrupt, the bits PROXINTEN (address 009Ch) should be configured first.	b1
5	TOUCHANYIRQEN	RW	Enable the interrupt when any channel from far to touch (PROX1/2/3ST from 0 to 1, any). b0: Disable b1: Enable Note: If need to enable the interrupt, the bit ENTERTOUCHANYEN (address 009Ch) should be set to 1.	b1
4	CONVDONEIRQEN	RW	Enable data conversion done interrupt. b0: Disable b1: Enable Note: If need to enable the interrupt, the bits CONVDONEINTEN (address 009Ch) should be configured first.	b1
3	AOTDONEIRQEN	RW	Enable auto offset tuning done interrupt. b0: Disable b1: Enable	b1
2	FARANYIRQEN	RW	Enable the interrupt when any channel from close to far. b0: Disable b1: Enable Note: If need to enable the interrupt, the bits FARANYINTEN (address 009Ch) should be configured first.	b1
1	PROXANYIRQEN	RW	Enable the interrupt when any channel from far to proximity (PROX0ST from 0 to 1). b0: Disable b1: Enable Note: If need to enable the interrupt, the bits PROXANYINTEN (address 009Ch) should be configured first.	b1

0	INITOVERIRQEN	RW	Enable chip initial over interrupt. b0: Disable b1: Enable	b1

I2CADDR: I²C Address Register (Address F0F0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:7	Reserved	RO	Reserved	h0000000
6:0	I2CADDR	RO	I²C device address.	h12

OSCEN: Clock Control Register (Address FF00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:10	Reserved	RO	Reserved	h000000
9	CPUST	RO	Internal CPU core status indication. b0:CPU is in a working state b1:CPU is in sleep state	b1
8	OSCST	RO	OSC status indication. b0: The OSC is turned off b1: The OSC is turned on	b1
7:1	Reserved	RO	Reserved	h00
0	OSCEN	RW	OSC enable. b0: Disable b1: Enable	b1

RESET: Software Reset Register (Address FF0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	RESET	WO	Write “0” to reset the whole chip.	h00
23:0	Reserved	RO	Reserved	h000000

CHIPID: CHIP ID Register (Address FF10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	CHIPID	RO	CHIP ID Register.	hA9610B00

APPLICATION INFORMATION

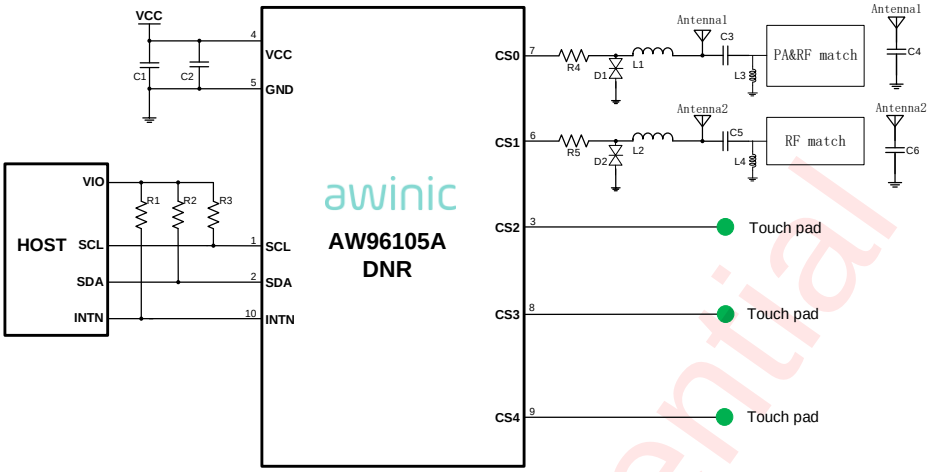


Figure 18 AW96105ADNR Typical Application Circuit

Inductor Selection

The recommended values of the Inductance L1~L2, which were applied in pins CS0,CS1, respectively, are all 200nH.

The recommended values of the Inductance L3~L4, are from 8nH to 100nH, typically 68nH.

Capacitors Selection

The recommended value of the capacitance C1 is 1μF and C2 is 0.1μF.

The recommended value of the capacitance C3-C6 are 22pF. It is suggested to use temperature insensitive capacitors to adjust the sensitivity, such as NP0 capacitors.

Resistor Selection

The recommended values of the resistor R1~R3 , which were applied in pins SCL,SDA and INTN, are 4.7kΩ.

The recommended values of the resistor R4~R5 , which were applied in pins CS0,CS1, are 390Ω.

RECOMMENDED COMPONENTS LIST

Component	Name	DESCRIPTION	TYP	UNIT
L	L1,L2	-	200	nH
	L3,L4	-	68	nH
C	C1	-	1	μF
	C2	-	0.1	μF
	C3,C4,C5,C6	5% resolution Low temperature coefficient	22	pF
R	R1,R2,R3	5% resolution	4.7	kΩ
	R4,R5	5% resolution	390	Ω

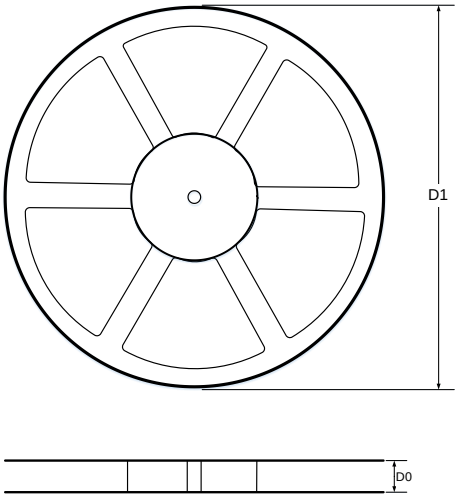
PCB LAYOUT CONSIDERATION

AW96105ADNR is a 5-channel capacitive touch and proximity controller, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

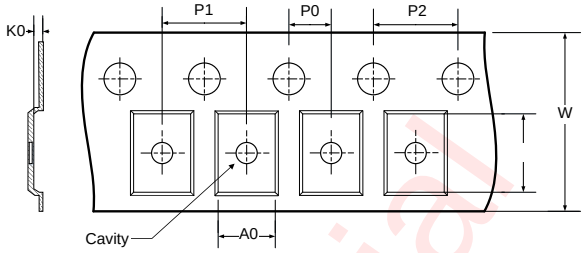
1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC. Avoid connecting peripheral devices and chip pins with two different layers of copper, use the same layer of copper instead.
2. Place the chip close to capacitive sensor and make trace as short as possible.
3. Make sure the sensor and traces be away from mic and earphone line, because capacitive sensor will disturb audio line.
4. Place reference channel along with sensor channel to get better performance.
5. Use low noise power supply for SAR sensor.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

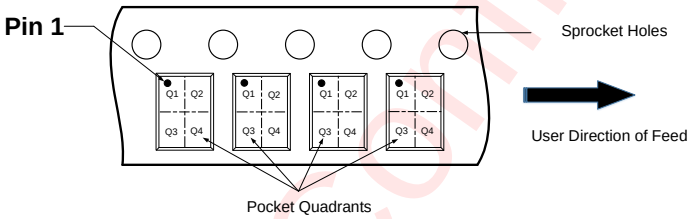


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



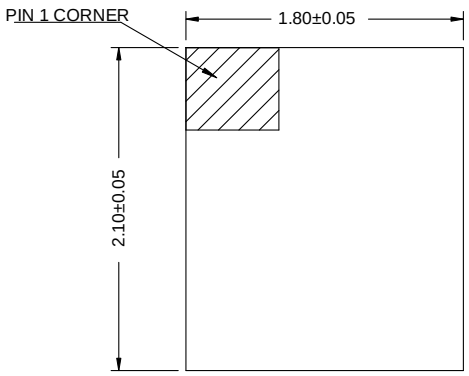
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

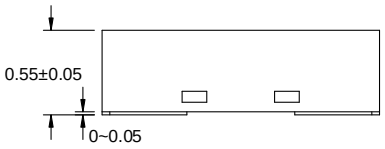
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2	2.3	0.75	2	4	4	8	Q1

All dimensions are nominal

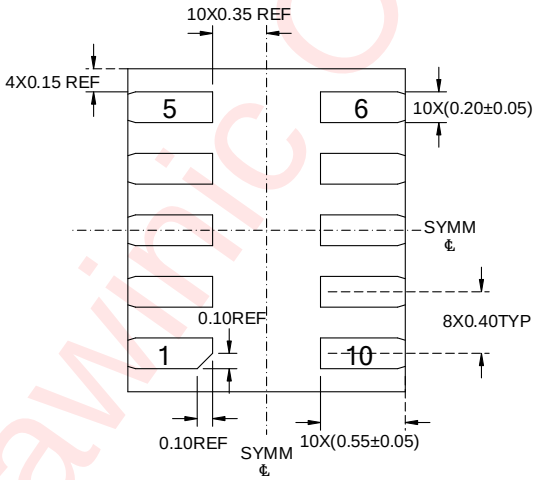
PACKAGE DESCRIPTION



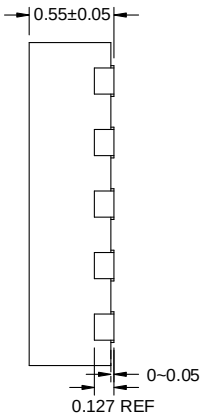
TOP VIEW



SIDE VIEW



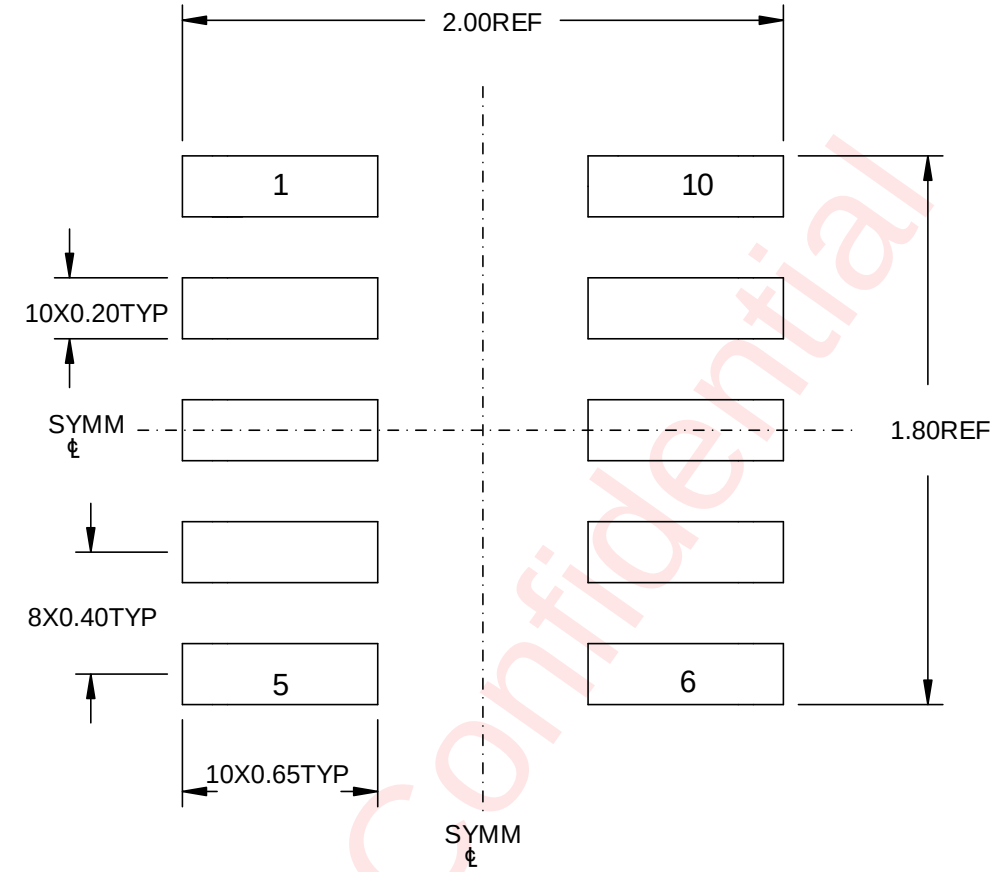
BOTTOM VIEW

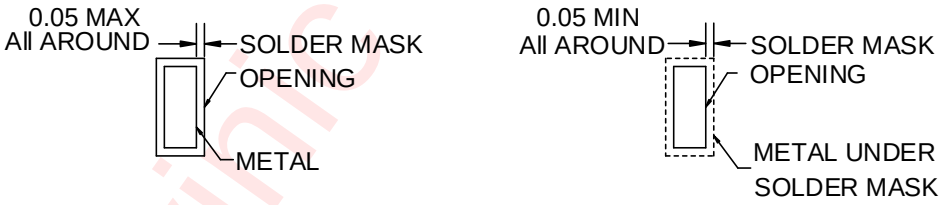


SIDE VIEW

Unit：mm

LAND PATTERN DATA





NON SOLDER MASK DEFINED **SOLDER MASK DEFINED**

Unit：mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Dec.2020	Officially released.
V1.1	Mar.2021	Add Support multi-level distance interrupt.
V1.2	Mar.2021	Update the Register List.
V1.3	Nov.2021	Update application block diagram parameters.
V1.4	Mar.2022	Updated the self-capacity principle.
V1.5	Sept.2022	Improve CMD register description.
V1.6	Dec.2022	Improve AOTTAR_CHx register description. (P29)

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