4-Channel LDO PMIC For Camera Applications

Features

- VIN1 input voltage range: 0.6V to 2V
- DVDD1/2 output voltage range: 0.6V~1.8V
- DVDD1/2 dropout voltage: 100mV@0.8A
- DVDD1/2 output drive capability: 1A Min.
- The max of DVDD1/2 output drive capability can be set to 1.3A by config I2C
- VIN2 quiescent current: typical: 65μA
- VIN2 shutdown current: typical: 0.25μA
- VIN2 input voltage range: 3V to 5.5V
- VIN2 UVLO voltage value: 2V
- AVDD1/2 output voltage range: 1.2V~4.3V
- AVDD1/2 output typical 98mV dropout voltage at 300mA load, V_{OUT}=2.8V
- AVDD1/2 output drive capability: 300mA Min.
- The max of AVDD1/2 output drive capability can be set to 600mA by config I2C
- AVDD1/2 power supply rejection ratio: typical 92dB (I_{OUT}=30mA, freq=1KHz)
- AVDD1/2 noise: typical 10μVrms (I_{OUT}=30mA, BW=10Hz to 100KHz)
- DFN 2mmX2mmX0.75mm-10L package

Applications

Digital camera

Smart phone

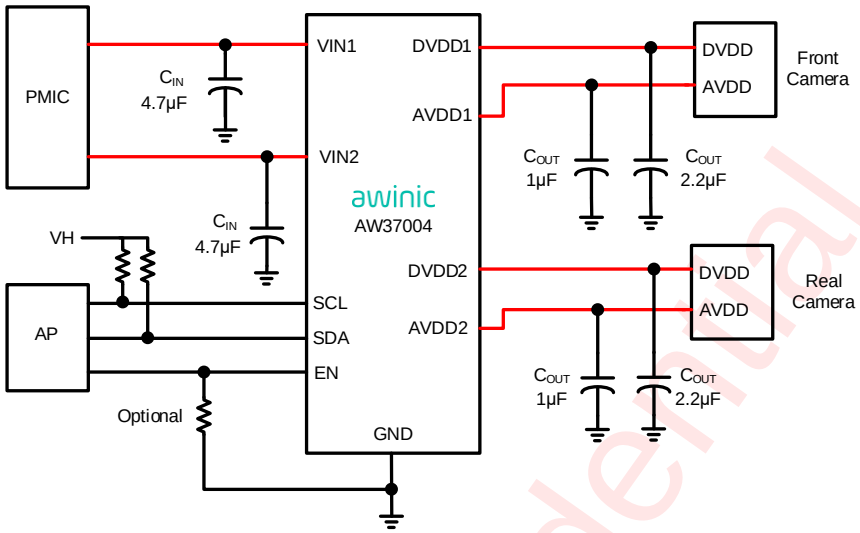
Camera module

General Description

AW37004DNR is a 4-ch integrated LDO PMIC for camera applications include 2-ch DVDD, 2-ch AVDD, with 400KHz high speed I2C interface, the function setting is flexible such as power sequence, output discharge. The chip enable control support EN pin control and I2C control.

Due to high load current and lower working voltage of DVDD, AW37004DNR used N-MOSFET LDO architecture without charge pump for 2-ch DVDD LDO. DVDD LDO input source is VIN1 and VIN2 is the bias voltage. Ultra low dropout voltage of DVDD LDOs is designed for high efficiency and lower power dissipation purpose. For the AVDD, AW37004DNR used P-MOSFET LDO architecture. The input source is VIN2. Due to high performance requirement of AVDD, AW37004DNR's AVDD used special circuit design and optimized pin assignment which is easy for system PCB layout.

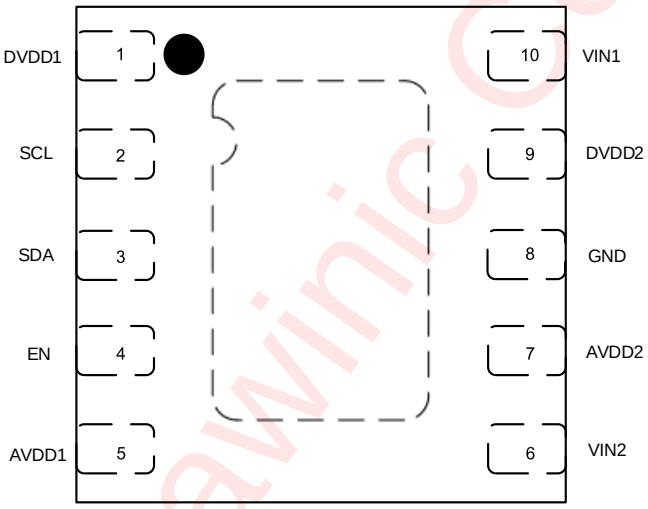
Typical Application Circuit



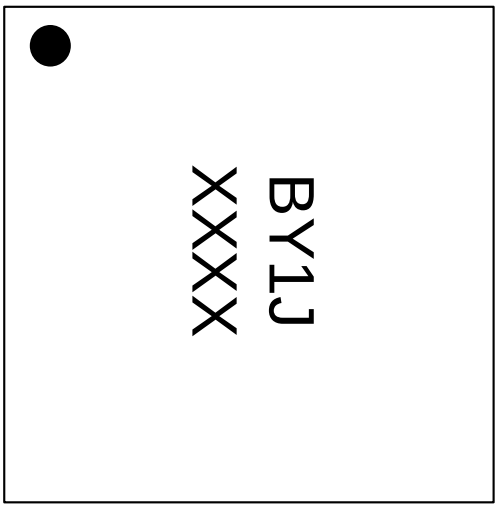
Camera Application

Pin Configuration And Top Mark

AW37004DNR
(Top View)



AW37004DNR Marking
(Top View)



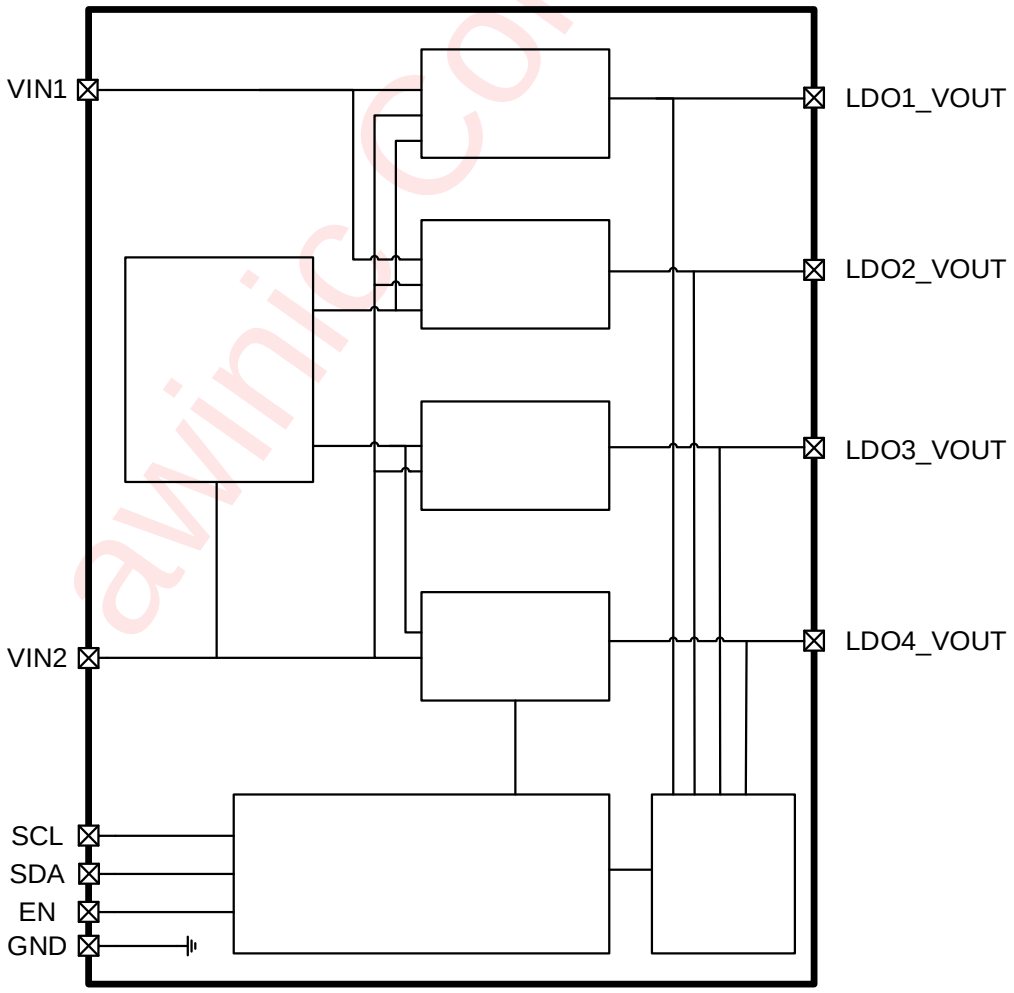
BY1J – AW37004DNR
XXXX – Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	DVDD1	LDO1 output channel. Connecting a 2.2μF or more ceramic capacitor at the output pin.
2	SCL	I2C data and clock interface.

3	SDA	
4	EN	Enable control pin, tie high to enable the chip, tie low if I2C control used.
5	AVDD1	LDO3 output channel. Connecting a 1μF or more ceramic capacitor at the output pin.
6	VIN2	LDO1 and LDO2 VBIAS input pin, LDO3 and LDO4 power supply input pin. Connecting a 4.7μF or more ceramic capacitor at the input pin.
7	AVDD2	LDO4 output channel. Connecting a 1μF or more ceramic capacitor at the output pin.
8	GND	Ground pin.
9	DVDD2	LDO2 output channel. Connecting a 2.2μF or more ceramic capacitor at the output pin.
10	VIN1	LDO1 and LDO2 power supply input pin. Connecting a 4.7μF or more ceramic capacitor at the input pin.

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37004DNR	-40℃ ~ 85℃	DFN 2mmX2mm -10L	BY1J	MSL1	ROHS+HF	3000 units/ Tape and Reel

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN1}	Input voltage	0.6		2	V
V_{IN2}	Input voltage	3		5.5	V
T_J	Operating free-air temperature range	-40	27	85	°C

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Input voltage range VIN1 and VIN2	-0.3V to 6.5V
Enable control voltage range	-0.3V to 6.5V
Output voltage range	-0.3V to VIN+0.3V, max. 6.5V
Junction-to-ambient thermal resistance θ_{JA}（NOTE2）	88°C/W
Junction-to-board thermal resistance θ_{JB}（NOTE2）	8°C/W
Junction-to-case thermal resistance θ_{JC}（NOTE2）	120°C/W
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model)(NOTE3)	±2kV
CDM(Charged device model) (NOTE4)	±1.5kV
Latch-Up	
Latch-Up(NOTE5)	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE5: Test Condition: JESD78E.

Electrical Characteristics

V_{IN1}=1.35V, V_{IN2}=3.3V, V_{EN}>1.1V, I_{OUT}=1mA, C_{IN}=4.7μF, C_{OUT_AVDD}=1μF, C_{OUT_DVDD}=2.2μF, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Whole device						
I_{SD}	Shutdown Current	V_{CE}<0.4V or shutdown by I2C		0.25	1	μA
I_Q	Quiescent Current	I_{OUT}=0mA, V_{EN}>1.1V or all channels enabled by I2C		65	100	μA
V_{ENH}	EN Input Voltage "H"	-40°C≤T_A≤85°C	1.1			V
V_{ENL}	EN Input Voltage "L"	-40°C≤T_A≤85°C			0.4	V
R_{EN}	EN Pull Down Resistance	V_{EN}=0V to 5.5V		2.2		MΩ
R_{DISC}	Auto Discharge Resistance	V_{EN}<0.4V, I_{OUT}=0mA,for AVDD		430		Ω
		V_{EN}<0.4V, I_{OUT}=0mA,for DVDD		540		Ω
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising		140		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling		110		°C
V_{UVLO}	Under Voltage Lock-out	VIN1 Falling		N.A		V
		VIN2 Falling		2		V
V_{UVLO_HYS}	UVLO Hysteresis	VIN2 Rising		0.1		V

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
DVDD1 and DVDD2							
V_{IN1_RANGE}	Input Supply Range			0.6		2.0	V
V_{OUT_ACC}	Output Voltage Accuracy			-2		2	%
V_{OUT_RANGE}	Output Voltage Range			0.6		1.8	V
$V_{OUT\_DEFAULT}$	Default Output Voltage				1.2		V
$LOAD_{Reg}$	Load Regulation	1mA≤I_{OUT}≤1A			1		mV
$LINE_{Reg}$	Line Regulation	V_{IN2}=3.3V, 1.25V≤V_{IN1} ≤2V, I_{OUT}=1mA			0.1		mV
		V_{IN1}=1.3V, 3V≤V_{IN2} ≤4V, I_{OUT}=1mA			0.5		mV
$V_{dropout}$	Dropout Voltage(1)	I_{OUT}=800mA, $V_{OUT(SET)}$=1.2V V_{IN2}=3.3V			100		mV
		I_{OUT}=800mA, $V_{OUT(SET)}$=1.2V V_{IN2}=4.4V			110		mV
PSRR	Power Supply Ripple Rejection	I_{OUT}=10mA, f=1kHz V_{IN1}=1.7V+0.2V_{PP} V_{IN2}=4.4V, $V_{OUT(SET)}$=1.2V			71		dB
		I_{OUT}=10mA, f=1kHz V_{IN2}=4.4V+0.2V_{PP} V_{IN1}=1.35V, $V_{OUT(SET)}$=1.2V			47		dB
V_N	Output Voltage Noise	I_{OUT}=30mA, BW=10Hz to 100kHz			90		μVrms
I_{CL}	Output Current Limit	DVDD1	DVDD2				
		REG0X01[1]=0 REG0X01[0]=0 (default)	REG0X01[3]=0 REG0X01[2]=0 (default)	1000	1300		mA
		REG0X01[1]=0 REG0X01[0]=1	REG0X01[3]=0 REG0X01[2]=1	1100	1440		mA
		REG0X01[1]=1 REG0X01[0]=0	REG0X01[3]=1 REG0X01[2]=0	1200	1580		mA
		REG0X01[1]=1 REG0X01[0]=1	REG0X01[3]=1 REG0X01[2]=1	1300	1720		mA
I_{SC}	Short Current Limit	V_{OUT}=0V			380		mA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
VTC	Output Voltage Temperature Coefficient	-40°C≤T_A≤85°C		±50		ppm/°C

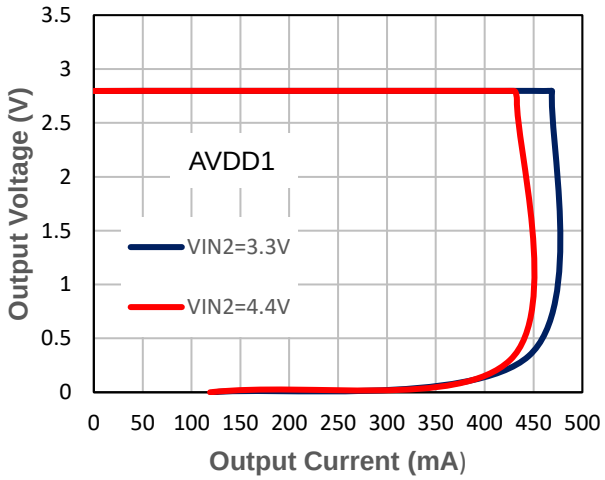
PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
AVDD1 and AVDD2							
V_{IN2_RANGE}	Input Supply Range			3		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy			-2		2	%
V_{OUT_RANGE}	Output Voltage Range			1.2		4.3	V
$V_{OUT\_DEFAULT}$	Default Output Voltage				2.8		V
$LOAD_{Reg}$	Load Regulation	1mA≤I_{OUT}≤300mA, $V_{OUT(SET)}$=2.8V V_{IN1}=1.35V, V_{IN2}=3.3V			2		mV
$LINE_{Reg}$	Line Regulation	V_{IN1}=1.35V, $V_{OUT(SET)}$=2.8V, 3.0V≤V_{IN2}≤4.0V, I_{OUT}=1mA			0.1		mV
$V_{dropout}$	Dropout Voltage(1)	I_{OUT}=300mA, $V_{OUT(SET)}$=2.8V			98		mV
PSRR	Power Supply Ripple Rejection	I_{OUT}=50mA, f=1kHz V_{IN2}=4.4V+0.2V_{PP} V_{IN1}=1.35V, $V_{OUT(SET)}$=2.8V			92		dB
		I_{OUT}=50mA, f=1MHz V_{IN2}=4.4V+0.2V_{PP} V_{IN1}=1.35V, $V_{OUT(SET)}$=2.8V			38		dB
V_N	Output Voltage Noise	I_{OUT}=30mA, BW=10Hz to 100kHz			10		μVrms
I_{CL}	Output Current Limit	AVDD1	AVDD2				
		REG0X01[5]=0 REG0X01[4]=0 (default)	REG0X01[7]=0 REG0X01[6]=0 (default)	300	480		mA
		REG0X01[5]=0 REG0X01[4]=1	REG0X01[7]=0 REG0X01[6]=1	400	620		mA
		REG0X01[5]=1 REG0X01[4]=0	REG0X01[7]=1 REG0X01[6]=0	500	760		mA
		REG0X01[5]=1 REG0X01[4]=1	REG0X01[7]=1 REG0X01[6]=1	600	900		mA
I_{SC}	Short Current Limit	V_{OUT}=0V			120		mA
VTC	Output Voltage Temperature Coefficient	-40°C≤T_A≤85°C			±50		ppm/°C

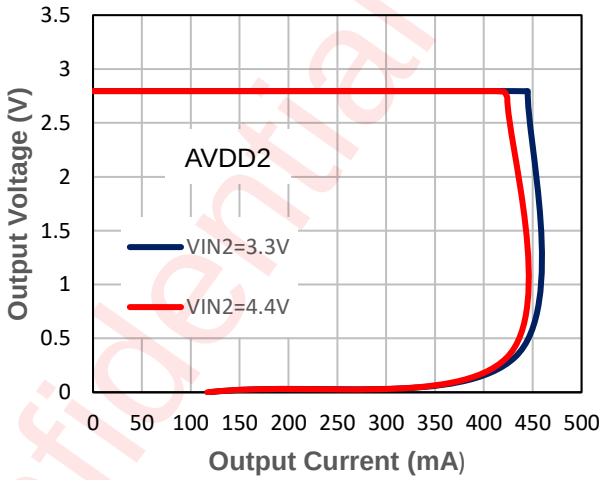
(1) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 98% of its nominal value.

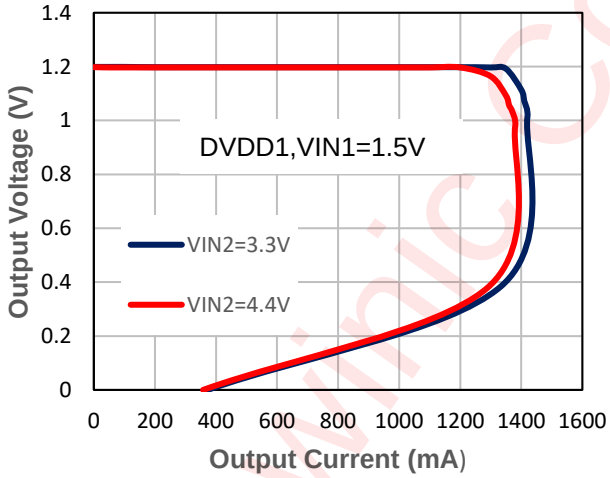
Typical Characteristics

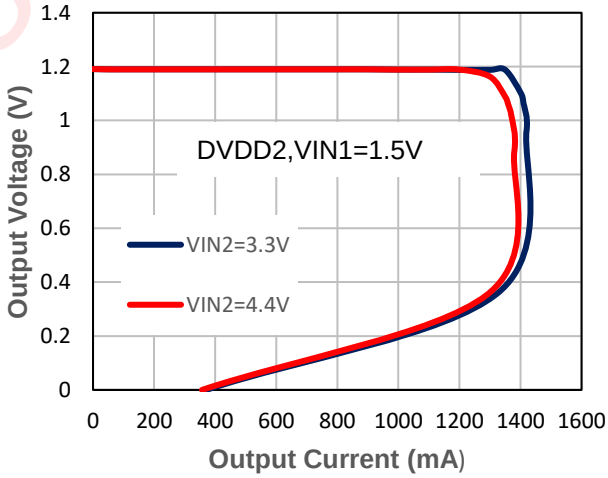
V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=4.7μF, C_{OUT_AVDD}=1μF, C_{OUT_DVDD}=2.2μF, T_A=25°C, In Typical Application Circuit, unless otherwise noted.

1) Ouput Voltage vs. Output Current

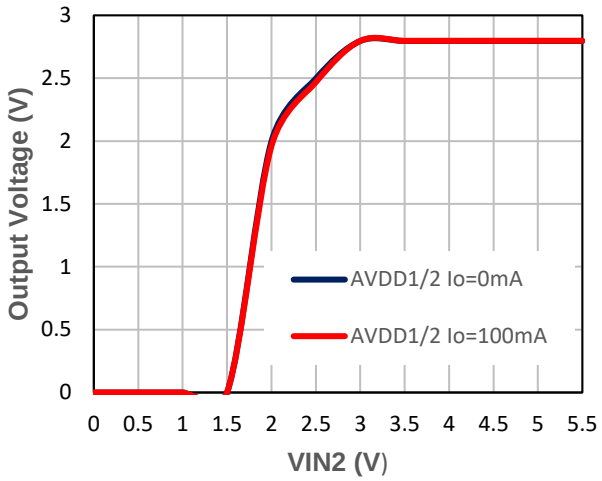


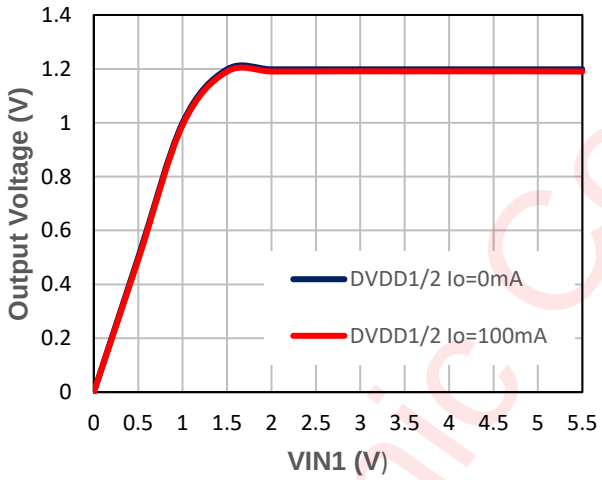


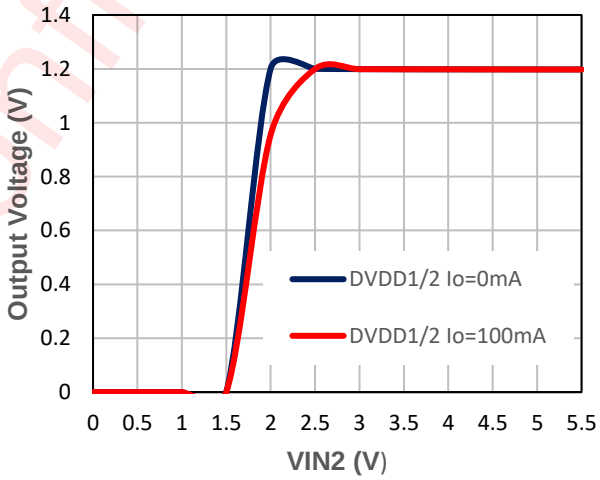




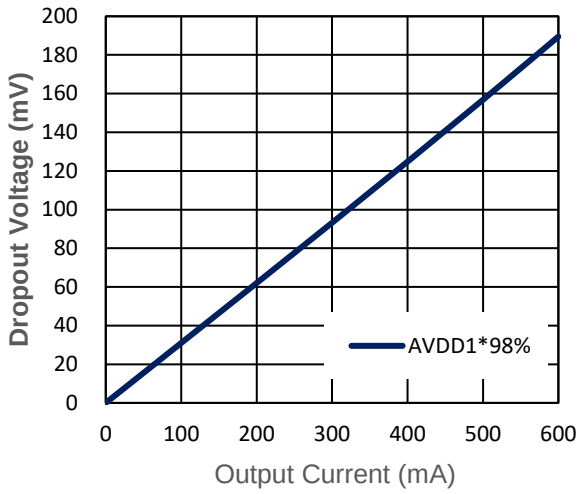
2) Ouput Voltage vs. Input Voltage

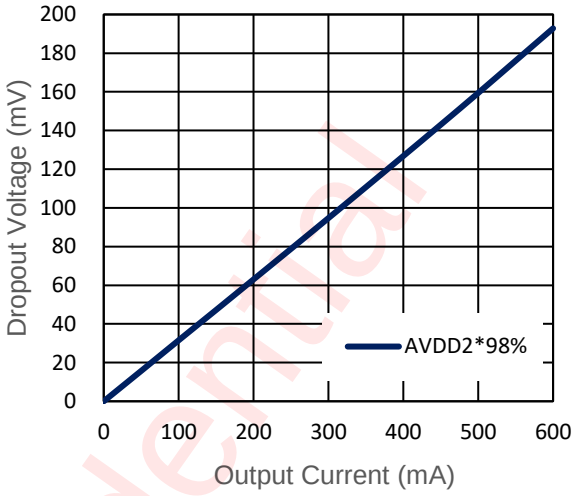


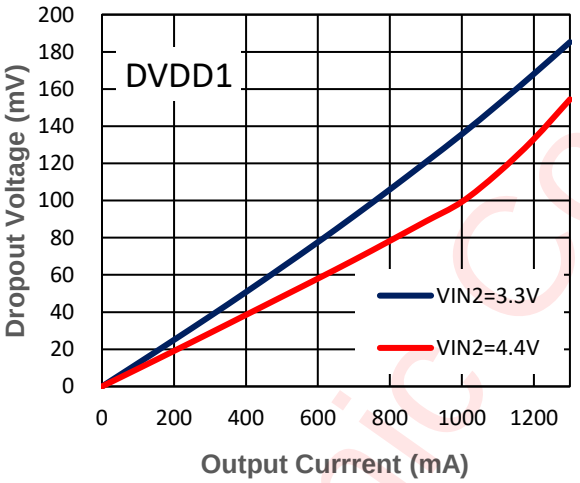


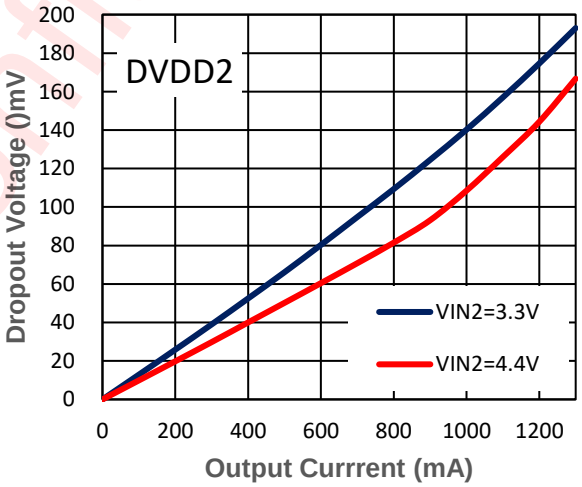


3) Droput Voltage vs. Output Current(Set the Current Limit Control Register of AVDD、DVDD to 0X11)

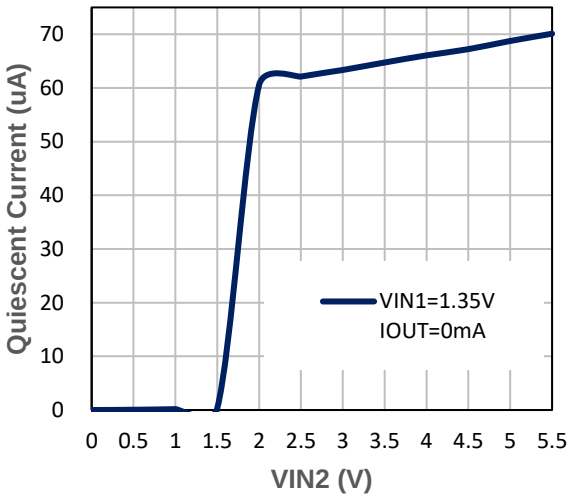




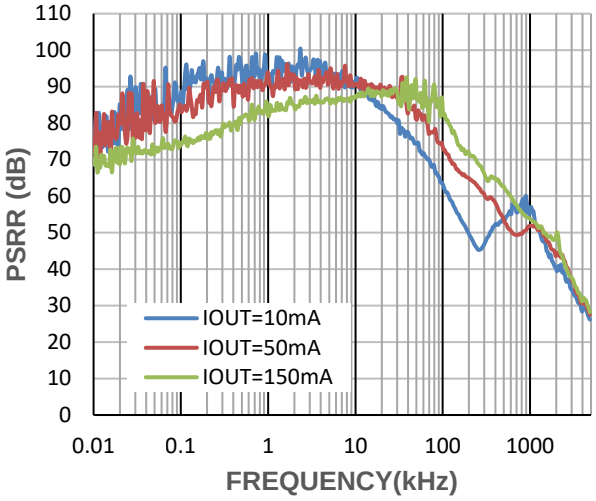




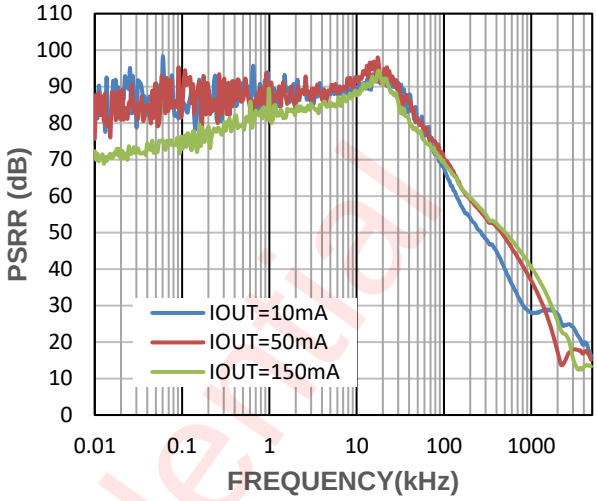
4) Ground Current vs. Input Voltage



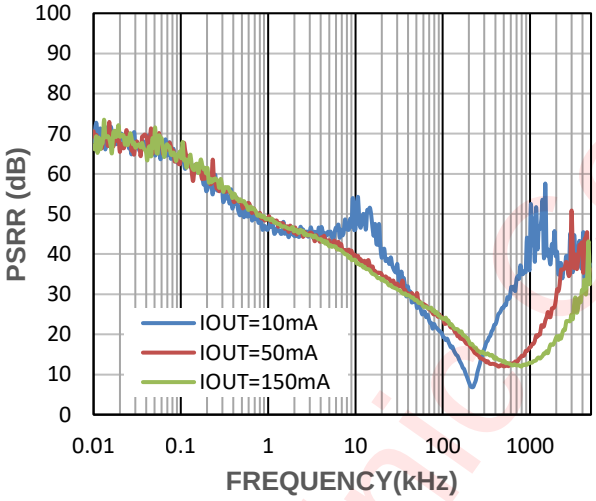
5) Ripple Rejection vs. Frequency (C_{IN}=1μF)



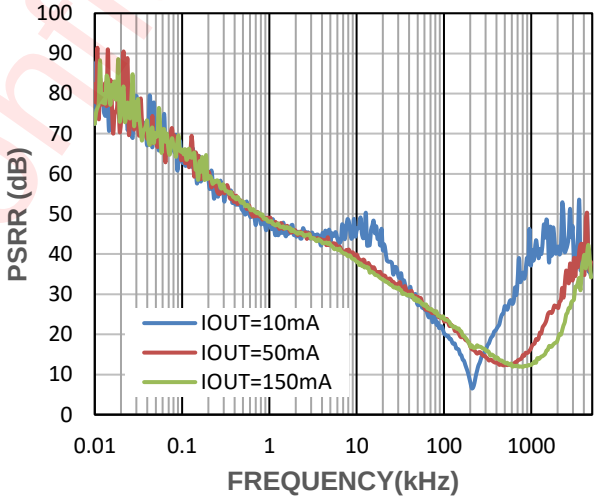
AVDD1,VIN1=1.35V,VIN2=4.4VDC+0.2VPP



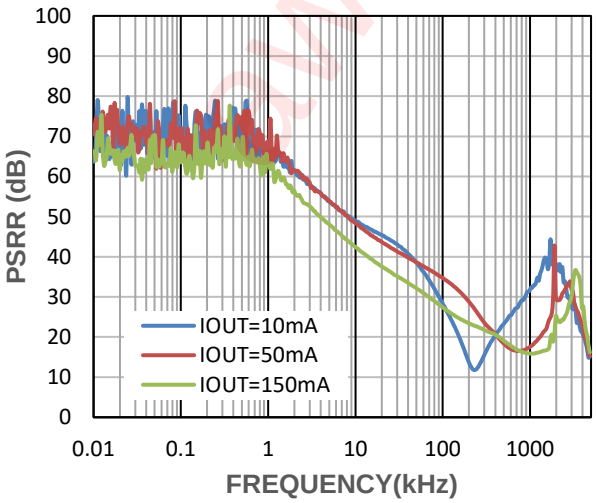
AVDD2,VIN1=1.35V,VIN2=4.4VDC+0.2VPP



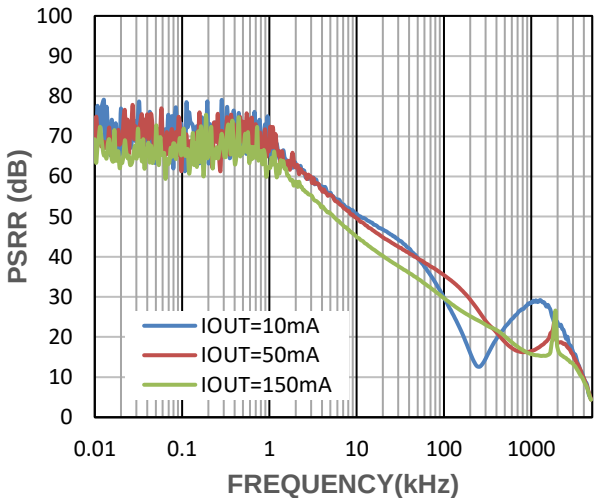
DVDD1,VIN1=1.35V,VIN2=4.4VDC+0.2VPP



DVDD2,VIN1=1.35V,VIN2=4.4VDC+0.2VPP

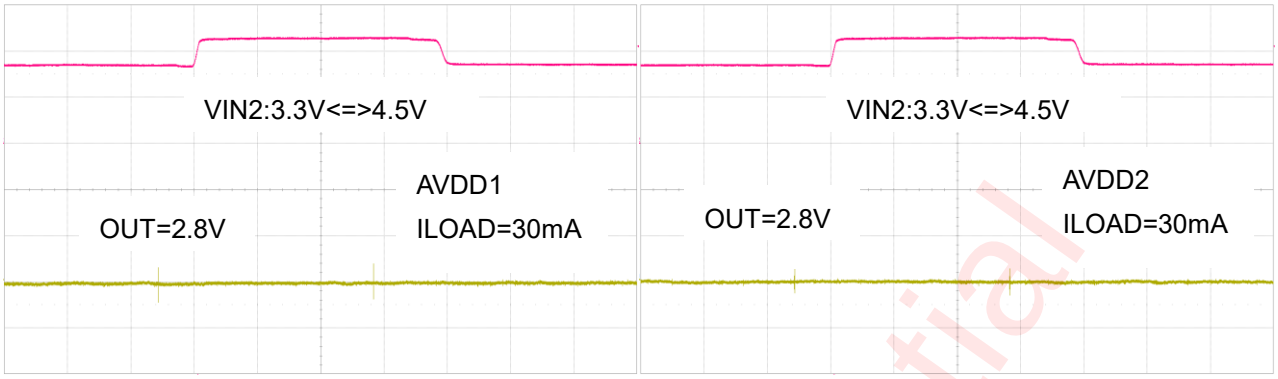


DVDD1,VIN1=1.35VDC+0.1VPP,VIN2=4.4V

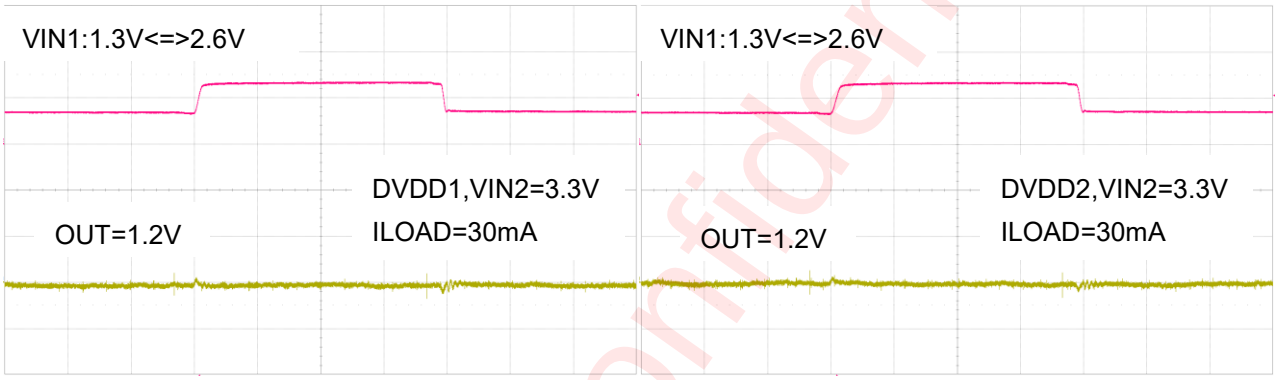


DVDD2,VIN1=1.35VDC+0.1VPP,VIN2=4.4V

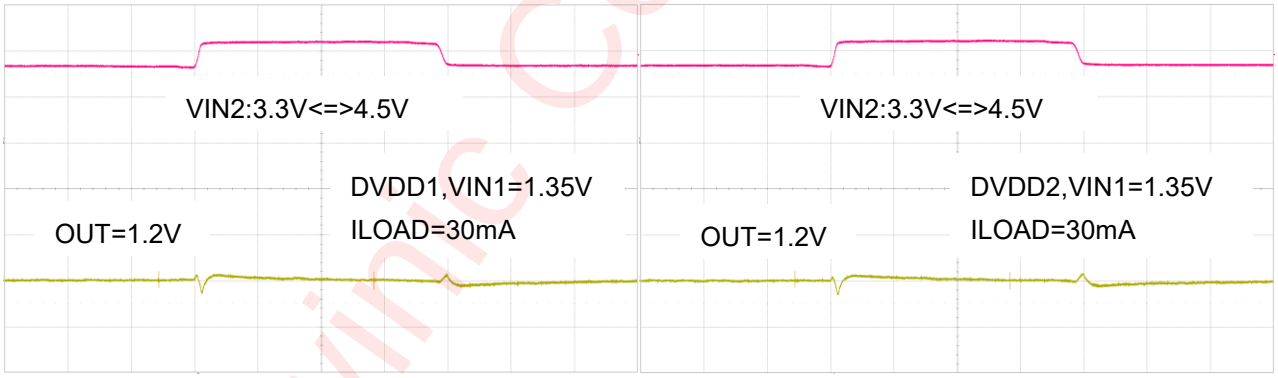
6) Line Transient (tr = tf =10μs)



C1: 20.0mV/div C2: 2V/div C1: 20.0mV/div C2: 2V/div

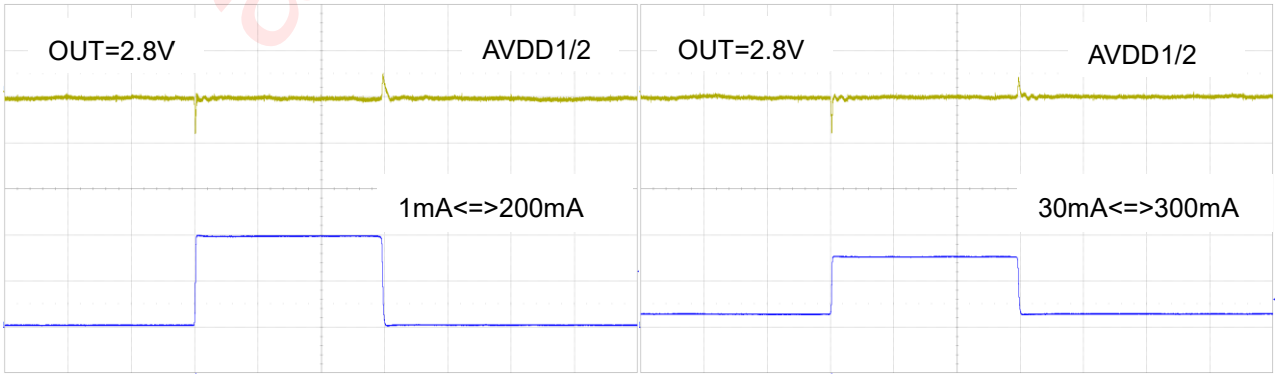


C1: 20.0mV/div C2: 2V/div C1: 20.0mV/div C2: 2V/div

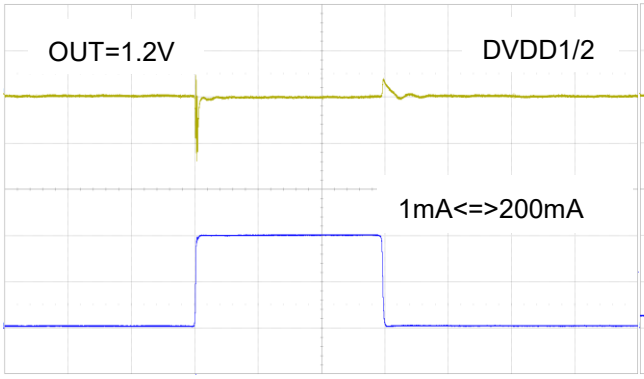


C1: 50.0mV/div C2: 2V/div C1: 50.0mV/div C2: 2V/div

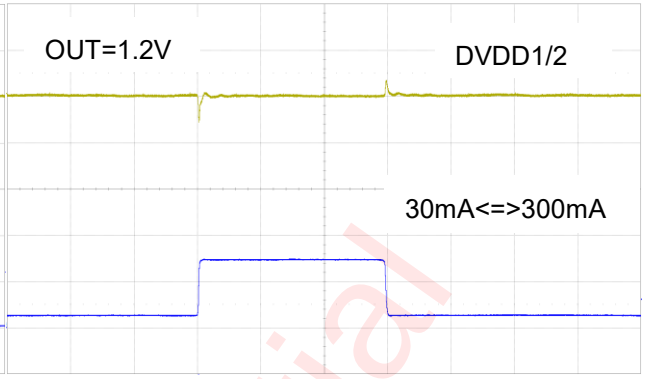
7) Load Transient (tr=tf=1μs)



C1: 20mV/div C3: 100.0mA/div C1: 20mV/div C3: 200.0mA/div

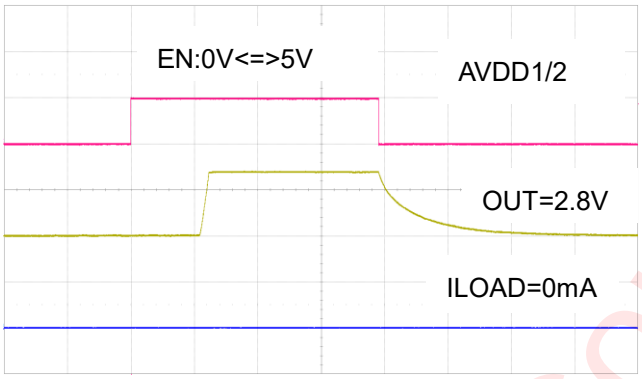


C1: 50mV/div C3: 100.0mA/div

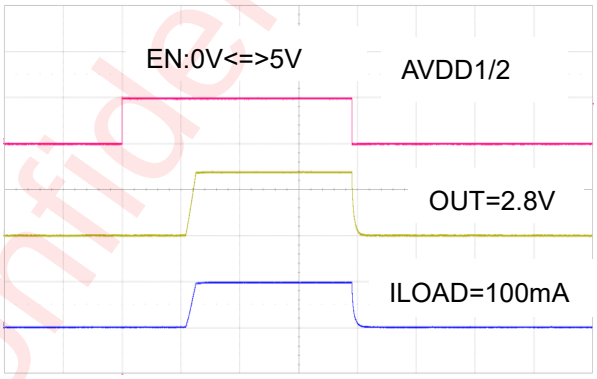


C1: 50mV/div C3: 200.0mA/div

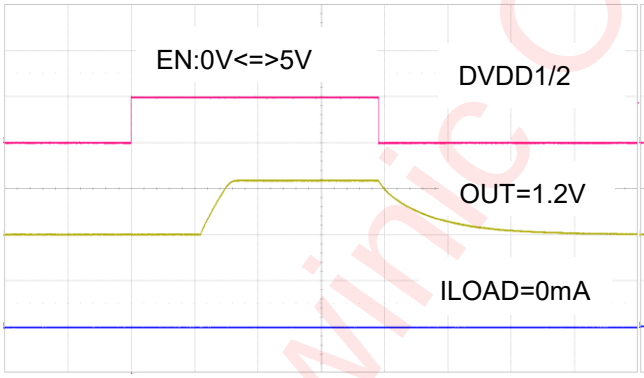
8) Turn-on/off Waveform by EN Pin signal (VIN1=1.35V VIN2=3.3V)



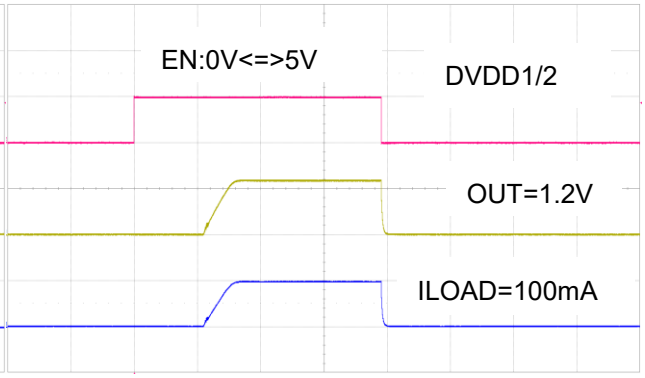
C1: 2V/div C2: 5V/div C3: 100.0mA/div



C1: 2V/div C2: 5V/div C3: 100.0mA/div



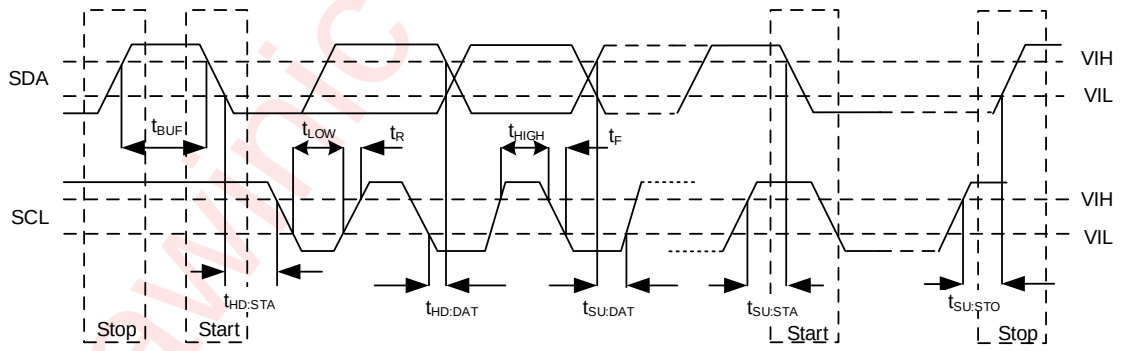
C1: 1V/div C2: 5V/div C3: 100.0mA/div



C1: 1V/div C2: 5V/div C3: 100.0mA/div

I²C Interface Timing

PARAMETER		FAST MODE			FAST MODE PLUS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
F_{SCL}	Interface clock frequency	-		400	-		1000	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	0.26		-	μs
T_{LOW}	Low level width of SCL	1.3		-	0.5		-	μs
T_{HIGH}	High level width of SCL	0.6		-	0.26		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	0.26		-	μs
$T_{HD:DAT}$	Data hold time	0		-	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	0.05		-	μs
T_R	Rising time of SDA and SCL	-		0.3	-		0.12	μs
T_F	Falling time of SDA and SCL	-		0.3	-		0.12	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	0.26		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	0.5		-	μs



Detailed Functional Description

WORK MODE

AW37004DNR has 4 LDO regulators. Power up/down of each regulator can be controlled by the followling three ways. It can be set at the registers DVDDx_SEQ[3:0] & AVDDx_SEQ[3:0] (x=1~2) respectively.

A. External EN pin toggles from low to high, it will force DVDDx & AVDDx regulators powered up.

B. Individual on/off control.

C. Automatic power up/down sequence control.

CHIP ENABLE CONTROL

External EN pin toggles from low to high, it will force DVDDx & AVDDx regulators powered up, output voltage of each LDO is default voltage, and the detailed description is in register DVDDx_VOUT & AVDDx_VOUT.

When external EN pin is low, LDO output can be controlled by an I2C register.

INDIVIDUAL ON/OFF CONTROL

Power-up and shut down of each regulator can be controlled by I2C register. DVDDx_EN & AVDDx_EN are internal signals to enable one regulators. If DVDDx_SEQ[3:0] & AVDDx_SEQ[3:0] set to 4'b0000, that DVDDx & AVDDx channels can be controlled directly by a bit specified in register DVDDx_EN & AVDDx_EN. DVDDx_VOUT[7:0] & AVDDx_VOUT[7:0] can set output voltage of each channel.

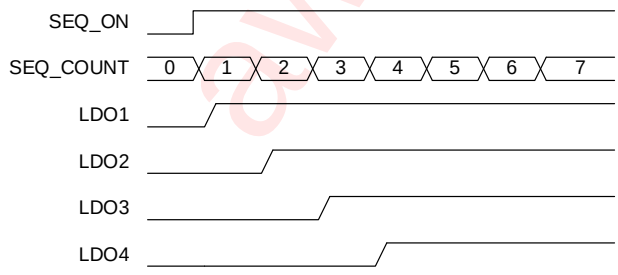
AUTOMATIC POWER UP/DOWN SEQUENCE CONTROL

AW37004DNR has 7 SLOTs to which each regulator can be assigned.

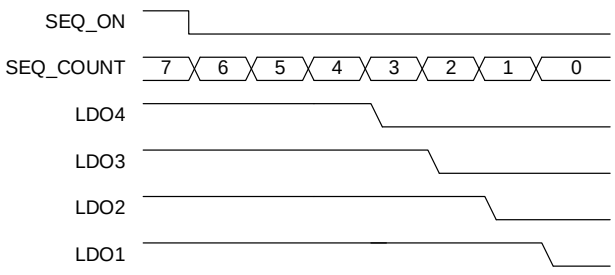
SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7

They are started by SEQ_ON signal. When SEQ_ON is high. Internal counter SEQ_COUNT[2:0] starts increment from 0 (3'b000) to 7 (3'b111). When SEQ_ON is low, SEQ_COUNT[2:0] decrements from 7 (3'b111) to 0 (3'b000). Regulators assigned to one of SLOTs starts power-up or power-down when SEQ_COUNT[2:0] matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I2C, writing 1'b0 to SEQ_CTRL will set SEQ_ON to '0', while writing 1'b1 to SEQ_CTRL will set SEQ_ON to '1'.



Example of Power-up in the case of DVDDx & AVDDx are assigned to SLOT1 ~ SLOT4 respectively.



Example of Shut-down in the case of DVDDx & AVDDx are assigned to SLOT1 ~ SLOT4 respectively.

OUTPUT DISCHARGE SETTING

Set related bits to select output discharge function for Discharge Resistor (DISCR, Address 0x02), 1'b1:

Disable, 1'b0: Enable. AW37004DNR support 2 modes for Discharge, which controlled by DISCHG_MD (bit 7 of DISCR register). It will force enable each LDO Discharge function when DISCHG_MD=0. AVDDx & DVDDx Discharge function is controlled by bit 3 ~ bit 0 of DISCR register when DISCHG_MD=1.

I²C INTERFACE

AW37004DNR supports the I²C protocol. The maximum frequency supported by the I²C is 1MHz. The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C, 1kΩ is recommended for 1MHz I²C. The voltage from 1.8V to 3.3V is allowed for the I²C interface. Additionally, the I²C device supports continuous reading and writing operations.

DEVICE ADDRESS

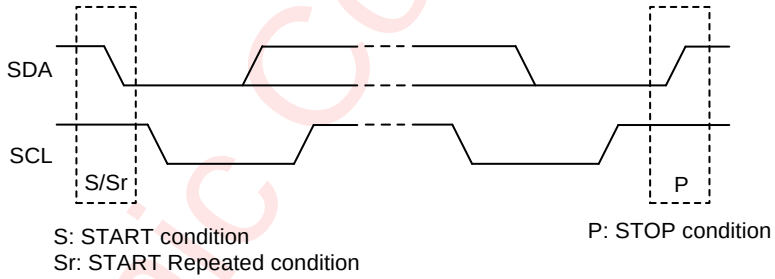
The I²C device address is 7-bit (A7~A1), followed by the R/W bit A0 (Read=1/Write=0). Set A0 to "0" for writing and "1" for reading.

A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	W/R

I²C START/STOP

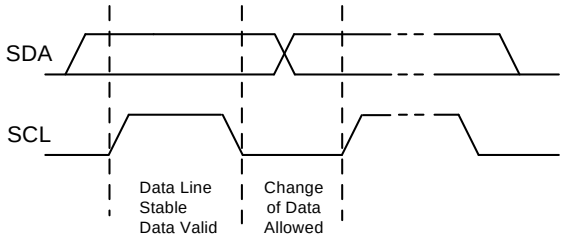
I²C START: SDA changes from high level to low level when SCL is high level.

I²C STOP: SDA changes from low level to high level when SCL is high level.



DATA VALIDATION

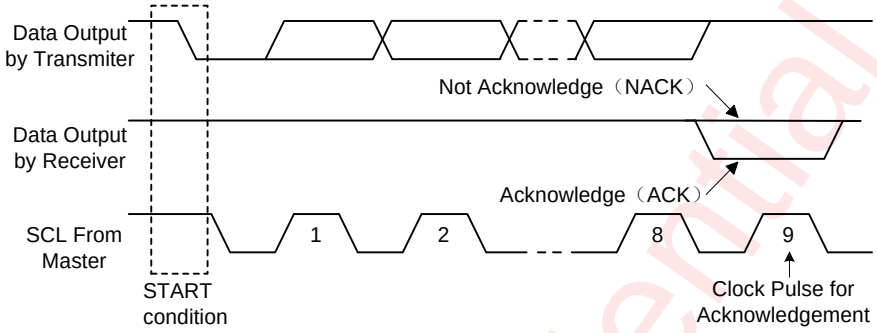
When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.



ACK (ACKNOWLEDGEMENT)

ACK means the successful transition of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C STOP is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.



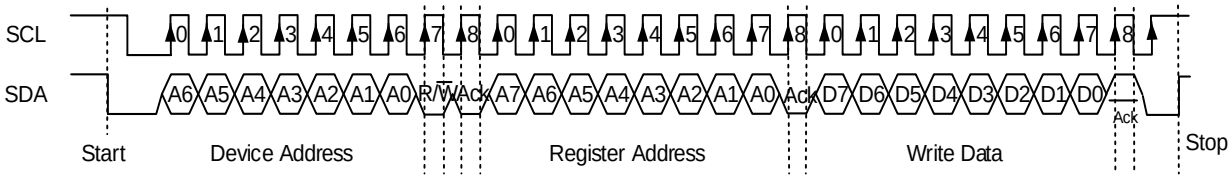
WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

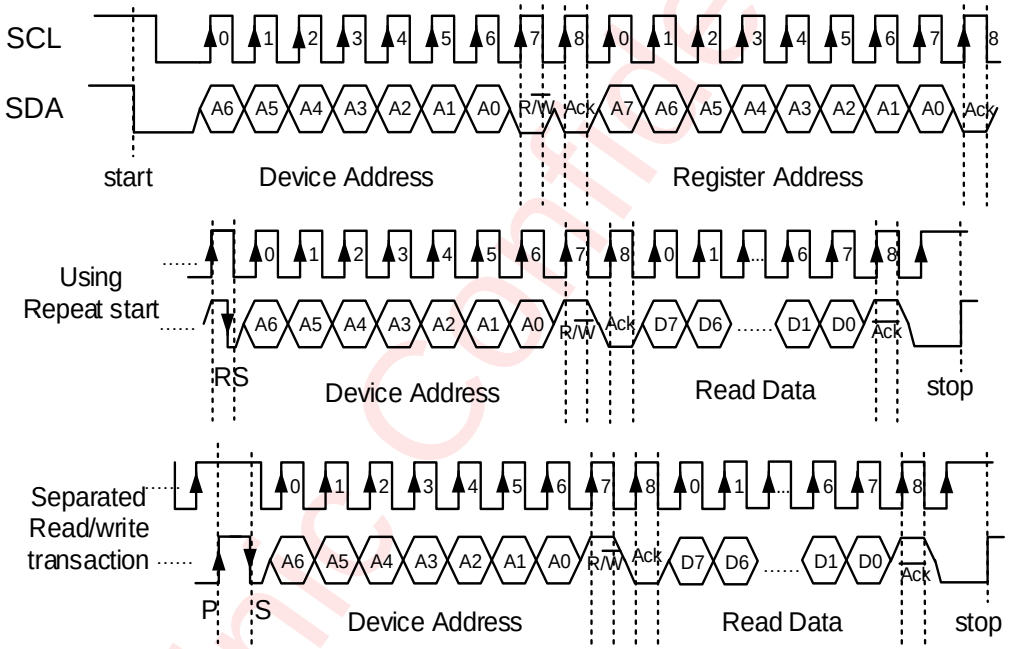
a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master sends data byte to be written to the addressed register.
g) Slave sends acknowledge signal.
h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g).
i) Master generates STOP condition to indicate write cycle end.



READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master generates STOP condition followed with START condition or REPEAT START condition.
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
k) If the master device generates STOP condition, the read cycle ends.



REGISTER DESCRIPTION

Ad.	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Init
0x00	CHIP_ID	R	CHIP_ID								0x00
0x19	CHIP_ID2	R	CHIP_ID2								0x04
0x01	CLMTCR	R/W	AVDD2_CLMT		AVDD1_CLMT		DVDD2_CLMT		DVDD1_CLMT		0x00
0x02	DISCR	R/W	DISCHG_MD				AVDD2_DISCHG	AVDD1_DISCHG	DVDD2_DISCHG	DVDD1_DISCHG	0x00
0x03	DVDD1_VOUT	R/W	DVDD1_VOUT								0x64
0x04	DVDD2_VOUT	R/W	DVDD2_VOUT								0x64
0x05	AVDD1_VOUT	R/W	AVDD1_VOUT								0x80
0x06	AVDD2_VOUT	R/W	AVDD2_VOUT								0x80
0x0A	DVDD_SEQ	R/W	DVDD2_SEQ				DVDD1_SEQ				0x00
0x0B	AVDD_SEQ	R/W	AVDD2_SEQ				AVDD1_SEQ				0x00
0x0E	ENCR	R/W					AVDD2_EN	AVDD1_EN	DVDD2_EN	DVDD1_EN	0x00
0x0F	SEQCR	R/W	SEQ_SPEED			SEQ_CTRL	SEQ_ON	SEQ_COUNT			0x00

REGISTER DETAILED DESCRIPTION

CHIP_ID: Chip ID (Address 0x00)

Bit	Symbol	R/W	Description	Init
7:0	CHIP ID	R	Indicates the device ID	0x00

CHIP_ID2: Chip ID (Address 0x19)

Bit	Symbol	R/W	Description	Init
7:0	CHIP ID2	R	Indicates the device ID	0x04

CLMTCR: Current Limit Control Register (Address 0x01)

Bit	Symbol	R/W	Description	Init
7:6	AVDD2_CLMT	R/W	AVDD2 current limit control 2'b00: ILIMIT_TYP mA; 2'b01: ILIMIT_TYP +140 mA; 2'b10: ILIMIT_TYP +280 mA; 2'b11: ILIMIT_TYP +420 mA;	00

Bit	Symbol	R/W	Description	Init
5:4	AVDD1_CLMT	R/W	AVDD1 current limit control 2'b00: ILIMIT_TYP mA; 2'b01: ILIMIT_TYP +140 mA; 2'b10: ILIMIT_TYP +280 mA; 2'b11: ILIMIT_TYP +420 mA;	00
3:2	DVDD2_CLMT	R/W	DVDD2 current limit control 2'b00: ILIMIT_TYP mA; 2'b01: ILIMIT_TYP +140 mA; 2'b10: ILIMIT_TYP +280 mA; 2'b11: ILIMIT_TYP +420 mA;	00
1:0	DVDD1_CLMT	R/W	DVDD1 current limit control 2'b00: ILIMIT_TYP mA; 2'b01: ILIMIT_TYP +140 mA; 2'b10: ILIMIT_TYP +280 mA; 2'b11: ILIMIT_TYP +420 mA;	00

DISCR: Discharge Control Register (Address 0x02)

Bit	Symbol	R/W	Description	Init
7	DISCHG_MD	R/W	Discharge mode control 0: Auto mode, all LDOs discharge Function is enabled; 1: Manuel mode, discharge function controlled by DVDDx_DISCHG & AVDDx_DISCHG;	0
6:4	RESERVED	R	Reserved	000
3	AVDD2_DISCHG	R/W	Discharge function enable of AVDD2 0: Disable; 1: Enable;	0
2	AVDD1_DISCHG	R/W	Discharge function enable of AVDD1 0: Disable; 1: Enable;	0
1	DVDD2_DISCHG	R/W	Discharge function enable of DVDD2 0: Disable; 1: Enable;	0
0	DVDD1_DISCHG	R/W	Discharge function enable of DVDD1 0: Disable; 1: Enable;	0

DVDD1_VOUT: DVDD1 Output Voltage Control Register (Address 0x03)

Bit	Symbol	R/W	Description	Init
7:0	DVDD1_VOUT	R/W	DVDD1 output voltage control VOUT1 = 0.6V + DVDD1_VOUT[7:0]*0.006V 0x00: 0.600V 0x01: 0.606V 0x02: 0.612V	0x64

Bit	Symbol	R/W	Description	Init
			… 0x63: 1.194V **0x64: 1.200V** 0x65: 1.206V … 0xFF: 2.130V	

DVDD2_VOUT: DVDD2 Output Voltage Control Register (Address 0x04)

Bit	Symbol	R/W	Description	Init
7:0	DVDD2_VOUT	R/W	DVDD2 output voltage control VOUT2 = 0.6V + DVDD2_VOUT[7:0]*0.006V 0x00: 0.600V 0x01: 0.606V 0x02: 0.612V … 0x63: 1.194V **0x64: 1.200V** 0x65: 1.206V … 0xFF: 2.130V	0x64

AVDD1_VOUT: AVDD1 Output Voltage Control Register (Address 0x05)

Bit	Symbol	R/W	Description	Init
7:0	AVDD1_VOUT	R/W	AVDD1 output voltage control VOUT1 = 1.2V + AVDD1_VOUT[7:0]*0.0125V 0x00: 1.2000V 0x01: 1.2125V 0x02: 1.2250V … 0x7F: 2.7875V **0x80: 2.8000V** 0x81: 2.8125V … 0xFF: 4.3875V	0x80

AVDD2_VOUT: AVDD2 Output Voltage Control Register (Address 0x06)

Bit	Symbol	R/W	Description	Init
7:0	AVDD2_VOUT	R/W	AVDD2 output voltage control VOUT2 = 1.2V + AVDD2_VOUT[7:0]*0.0125V 0x00: 1.2000V 0x01: 1.2125V 0x02: 1.2250V … 0x7F: 2.7875V **0x80: 2.8000V** 0x81: 2.8125V … 0xFF: 4.3875V	0x80

DVDD_SEQ: DVDDx Sequence Control Register (Address 0x0A)

Bit	Symbol	R/W	Description	Init
7:4	DVDD2_SEQ	R/W	DVDD2 sequence slot set 4'b0000: disable sequence mode; 4'bx001: set sequence slot is 1; 4'bx010: set sequence slot is 2; 4'bx011: set sequence slot is 3; 4'bx100: set sequence slot is 4; 4'bx101: set sequence slot is 5; 4'bx110: set sequence slot is 6; 4'bx111: set sequence slot is 7;	0000
3:0	DVDD1_SEQ	R/W	DVDD1 sequence slot set 4'b0000: disable sequence mode; 4'bx001: set sequence slot is 1; 4'bx010: set sequence slot is 2; 4'bx011: set sequence slot is 3; 4'bx100: set sequence slot is 4; 4'bx101: set sequence slot is 5; 4'bx110: set sequence slot is 6; 4'bx111: set sequence slot is 7;	0000

AVDD_SEQ: AVDDx Sequence Control Register (Address 0x0B)

Bit	Symbol	R/W	Description	Init
7:4	AVDD2_SEQ	R/W	AVDD2 sequence slot set 4'b0000: disable sequence mode; 4'bx001: set sequence slot is 1; 4'bx010: set sequence slot is 2; 4'bx011: set sequence slot is 3; 4'bx100: set sequence slot is 4; 4'bx101: set sequence slot is 5; 4'bx110: set sequence slot is 6; 4'bx111: set sequence slot is 7;	0000

Bit	Symbol	R/W	Description	Init
3:0	AVDD1_SEQ	R/W	AVDD1 sequence slot set 4'b0000: disable sequence mode; 4'bx001: set sequence slot is 1; 4'bx010: set sequence slot is 2; 4'bx011: set sequence slot is 3; 4'bx100: set sequence slot is 4; 4'bx101: set sequence slot is 5; 4'bx110: set sequence slot is 6; 4'bx111: set sequence slot is 7;	0000

ENCR: Individual Enable Control Register (Address 0x0E)

Bit	Symbol	R/W	Description	Init
7:4	RESERVED	R	Reserved	0000
3	AVDD2_EN	R/W	AVDD2 enable control 0: Disable; 1: Enable;	0
2	AVDD1_EN	R/W	AVDD1 enable control 0: Disable; 1: Enable;	0
1	DVDD2_EN	R/W	DVDD2 enable control 0: Disable; 1: Enable;	0
0	DVDD1_EN	R/W	DVDD1 enable control 0: Disable; 1: Enable;	0

SEQCR: Sequence Control Register (Address 0x0F)

Bit	Symbol	R/W	Description	Init
7:6	SEQ_SPEED	R/W	The seq_count increment period in sequence mode 2'b00: 2.00 ms; 2'b01: 1.00 ms; 2'b10: 0.50 ms; 2'b11: 0.25 ms;	00
5	RESERVED	R	Reserved	0
4	SEQ_CTRL	R/W	Sequence control when AVDDx/DVDDx slot isn't 0 1'b0: Shutdown; 1'b1: Power up;	0
3	SEQ_ON	R	The indication of sequence activation 0: Shutdown; 1: Power up;	0

2:0	SEQ_COUNT	R	The indication of the SEQ slot number at moment 3'b000: No LDO slots active; 3'b001: slot 1 active; 3'b010: slot 2 active; 3'b011: slot 3 active; 3'b100: slot 4 active; 3'b101: slot 5 active; 3'b110: slot 6 active; 3'b111: slot 7 active, and stop counting;	000

Application Information

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37004DNR advises to use a 4.7μF or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AW37004DNR advises to use a 1μF or more X5R or X7R ceramic capacitor at AVDD pin as shown in Typical Application Circuit;

AW37004DNR advises to use a 2.2μF or more X5R or X7R ceramic capacitor at DVDD pin as shown in Typical Application Circuit.

Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	4.7	μF
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
	GRM153R60J225ME95	6.3V, X5R, 0402	MURATA	2.2	μF
	GRM153R60J475ME15	6.3V, X5R, 0402	MURATA	4.7	μF

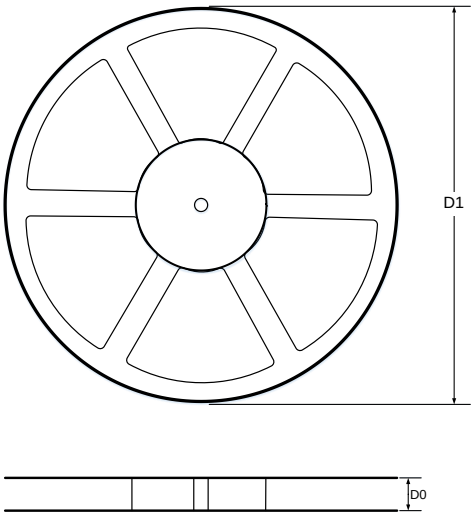
PCB Layout Consideration

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37004DNR should be obeyed:

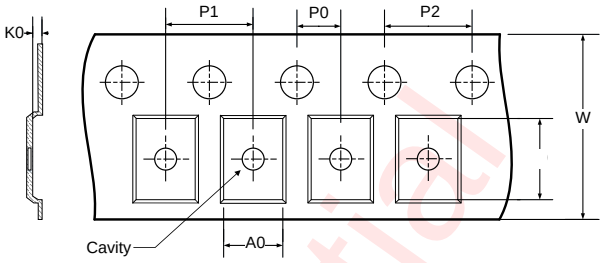
1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information

REEL DIMENSIONS

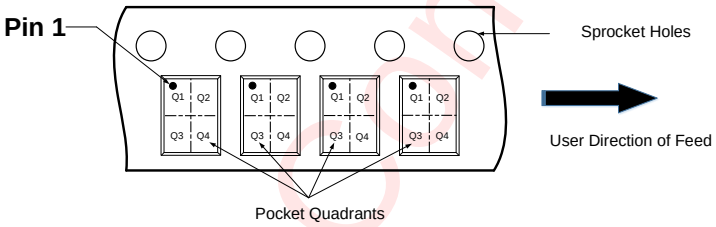


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



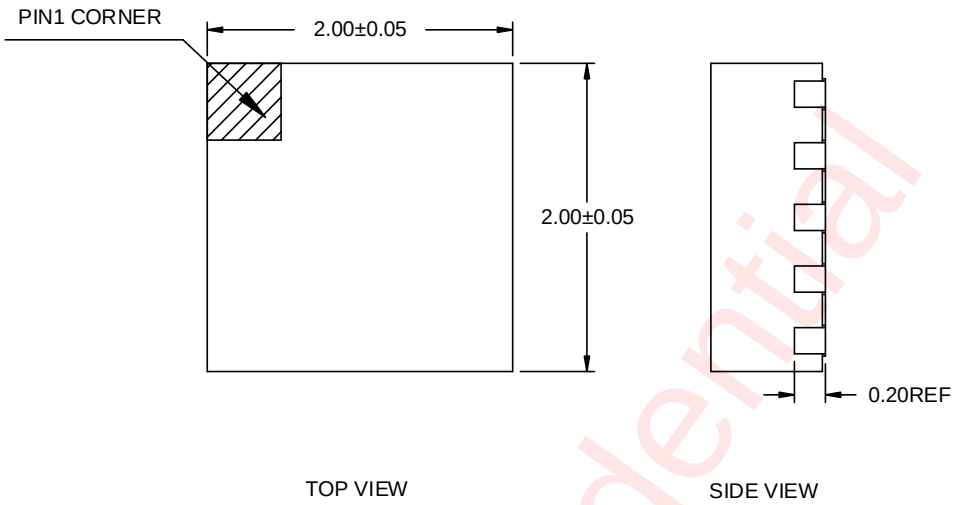
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

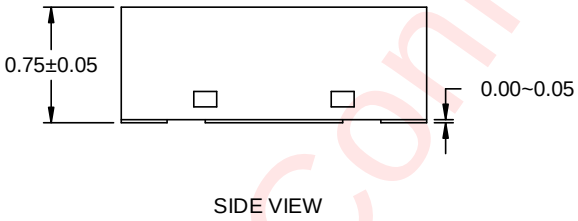
DIMENSIONS AND PIN1 ORIENTATION

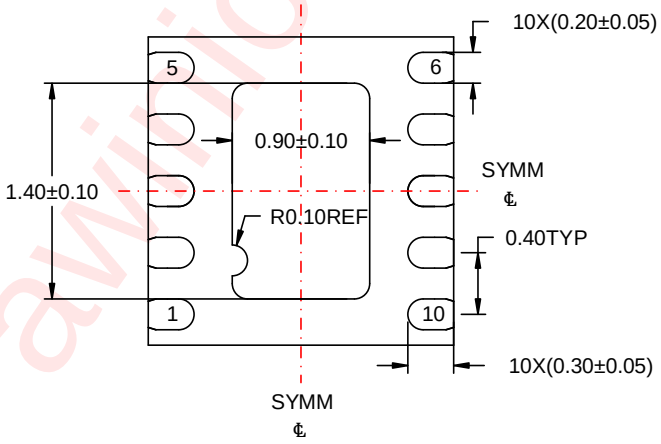
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1	2	4	4	8	Q1

All dimensions are nominal

Package Description

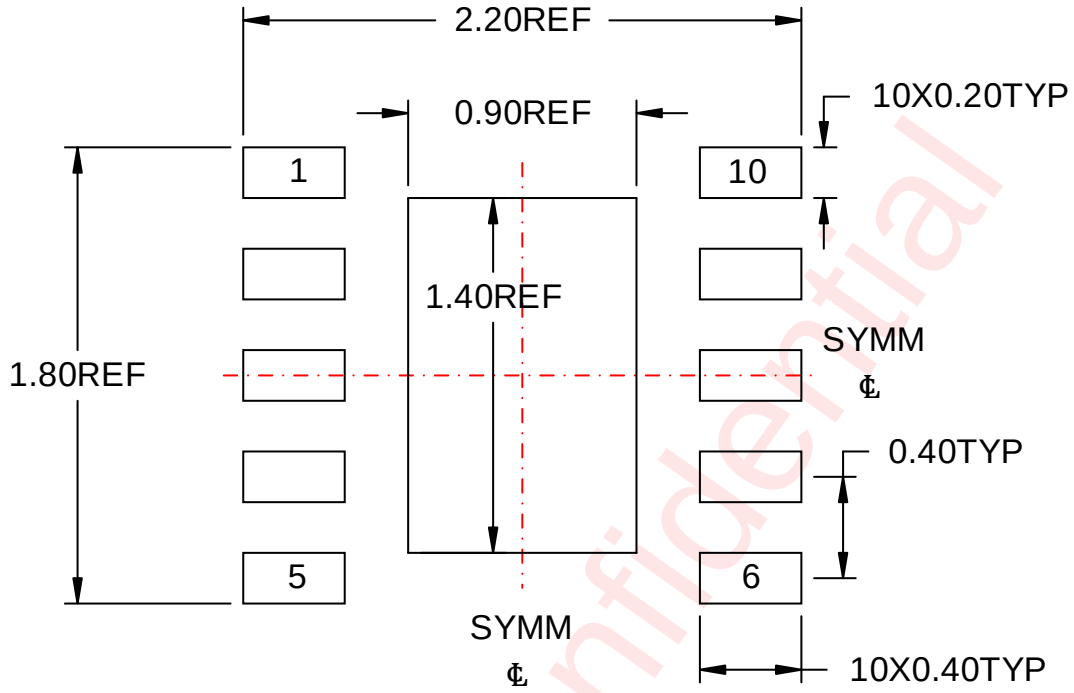


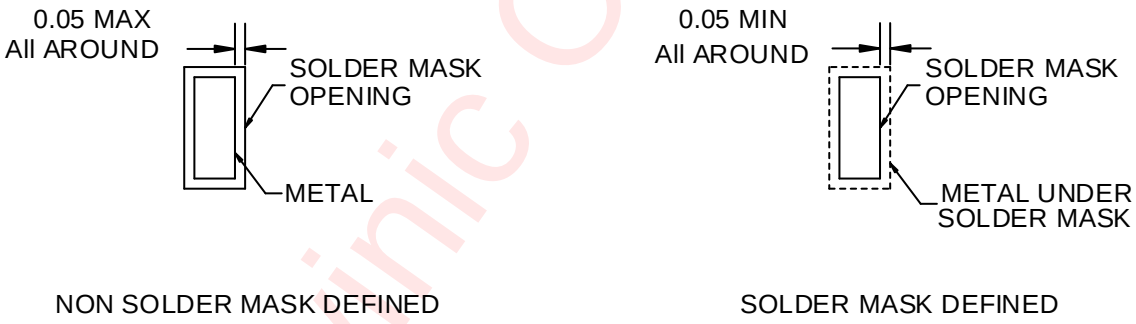




Unit：mm

Land Pattern Data





Unit：mm

Revision History

Version	Date	Change record
V1.0	Jul. 2022	Officially released
V1.1	Jul. 2022	Revised the typical characteristics test condition; Add recommended operating conditions section;
V1.2	Aug. 2022	Revised the description of the address from 0x03 to 0x06;
V1.3	Dec. 2022	Revised output current limit corresponding to the address of 0X01.
V1.4	Mar. 2023	Revised the recommended output capacitance of DVDD to 2.2μF.
V1.5	Jul. 2023	Revised the Dropout of DVDD in Typical Characteristics(P12); Add min of I_{CL}(P7 P9).
V1.6	Aug. 2023	Revised the drive capability of DVDD1/2 in Features(P1); Revised the Dropout of DVDD in Typical Characteristics(P12); Revised the description of Current Limit Control Register(P22 P23).
V1.7	Sep. 2023	Revised the Dropout of AVDD in Typical Characteristics(P12); Revised the min of I_{CL}(P7 P9). Add Chip ID2(P22).

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