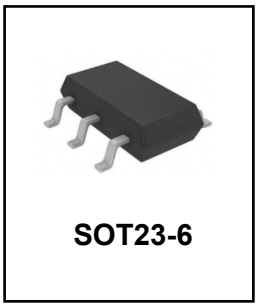
4.5V~100V, 450kHz, Asynchronous, Step-Down Converter

LA1821

Overview



The LA1821 is an easy -to-use, non-sync buck converter, which is integrated with 900mΩ low R_{DS_ON} high-side power MOSFET.

The LA1821 can provide up to 1A continues output current with advanced COT control for fast response and ease loop compensation.

The switching frequency of LA1821 is typically 450kHz, which will help to minimize the solution size and reduce BOM cost.

The LA1821 has 4.5V to 100V input voltage range, which accommodates a variety of step-down applications.

The LA1821 has built-in full protection features, cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation.

The LA1821 is available in a cost-effective SOT23-6 package.

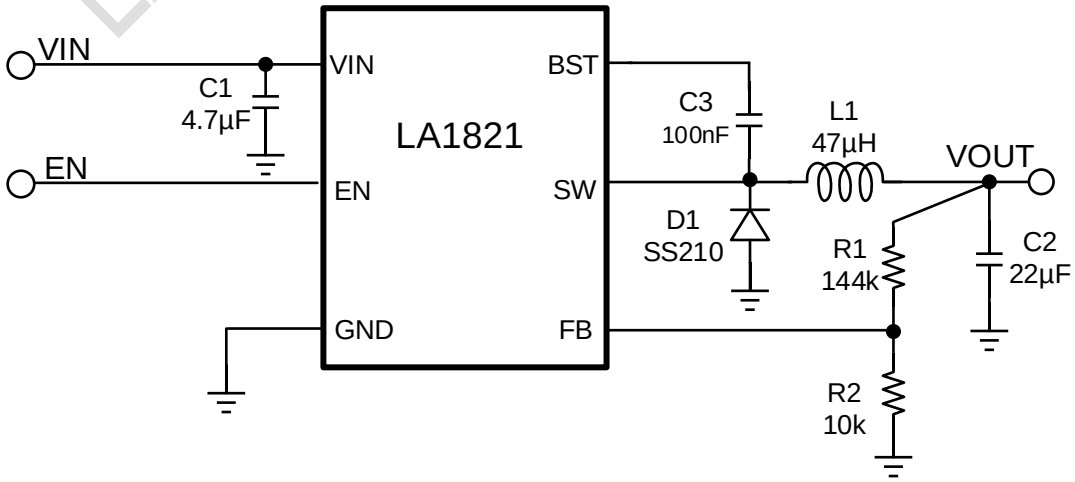
Features

- 4.5V to 100V Wide Input Range
- Integrated 900mΩ low resistance high side power MOS
- Constant On Time Control for Fast Loop Response
- 180uA low Quiescent Current
- 450kHz Switching Frequency
- Special Valley Current Limit for non-sync Buck Short Protection
- 3μA Low Current at Off-state
- Float EN pin for automatically start-up
- Low Drop Out Mode Support 97% Duty Cycle
- Reference Voltage 0.78V
- Available in SOT23-6 package
- Short Circuit Protection with Hiccup Mode
- Over Temperature Protection

Typical Application

- Battery powered tools
- E-bike powers, E-motors
- Industry applications

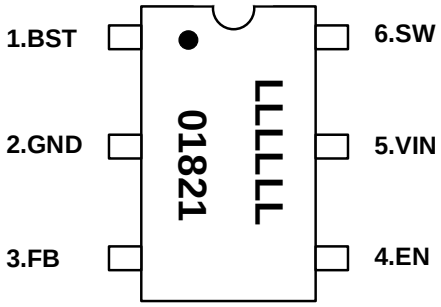
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1821	SOT23-6	-40 to 125°C	T/R 3000pcs/roll	sales@latticeart.com

Pin Diagram

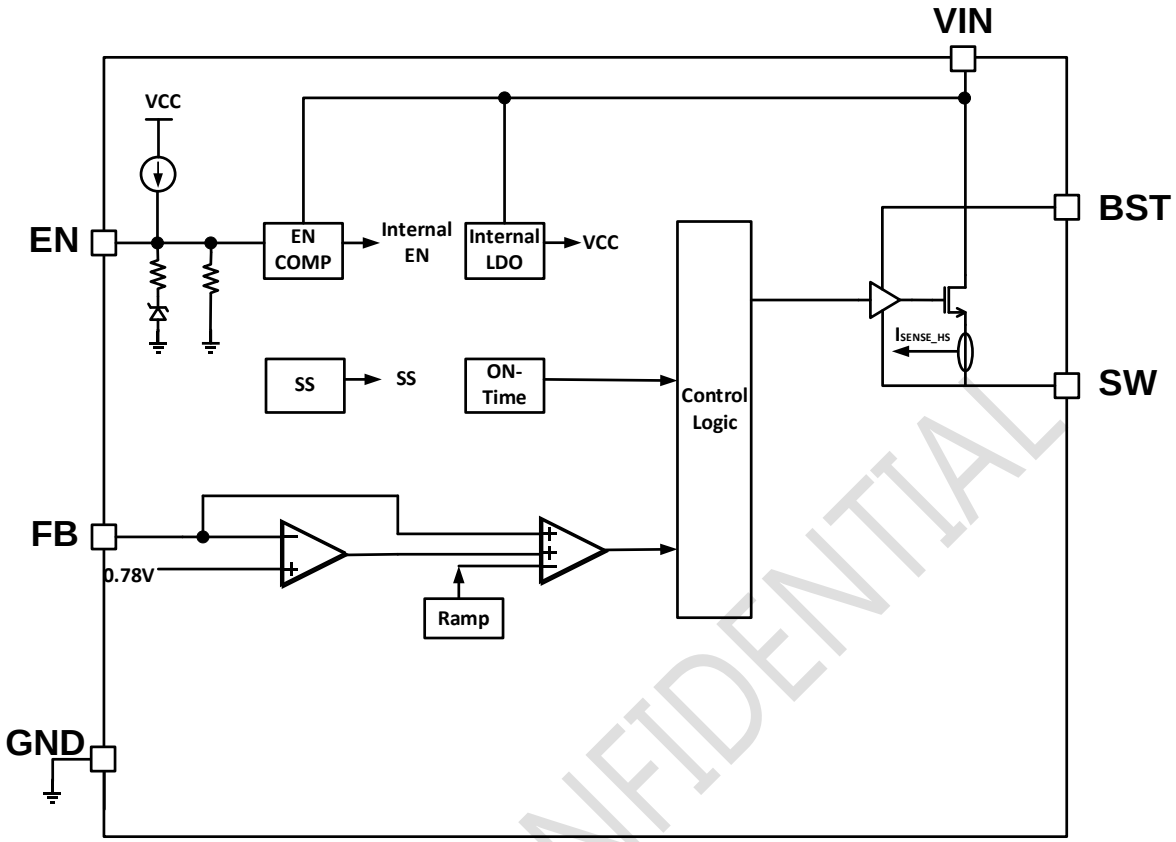


LLLLLL: Lot number
01821: Product code

Pin Description

Pin No.	Symbol	Pin Description
1	BST	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	GND	Ground pin of the IC, connect to the ground of the system
3	FB	Feedback input to the convertor. Connect a resistor divider to set the output voltage.
4	EN	Enable of the part. float this pin for automatically start-up, pull down this pin to shut down the part.
5	VIN	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
6	SW	Switching node of power stage. Connect to power inductor.

Block Diagram



Absolute Maximum Ratings (1)

T_j=25°C, unless otherwise specified.

Symbol	Definition	Absolute max Ratings	Unit
V_{IN}	Power supply	-0.3~105	V
V_{SW}	Switching node of power stage	-0.3~105	V
V_{BST}-V_{SW}	Bootstrap pin for high side power MOS driving.	5.5	V
I_{EN}	Max Input current to EN pin	100(2)	μA
All other pins	Pin to GND	-0.3~5.5	V
T_{STG}	Storage temperature	-55 to150	°C
T_j	Junction temperature	-40 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Note 2: For details on EN's ABS max rating, please refer to the Enable Control section.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
V_{IN}	Power supply pin	4.5 to 100	V
V_{OUT}	Output voltage	0.78~VIN*D_{MAX}(3) or VOUT<24V	V
I_{OUT}	Output current	0~1	A

Note 3: $D_{MAX} = T_{ON\_MAX}/(T_{ON\_MAX} + T_{OFF\_MIN})$. Typical value is 97%.

Thermal Resistance (4)

Symbol	Definition	Ratings	Unit
$R_{\theta JC}$	Junction to case thermal resistance	21	°C/W
$R_{\theta JA}$	Junction to ambient thermal resistance	40	°C/W

Note 4: Measured on DEM1821-H-00B 2-Layer PCB.

Electrical Characteristics

V_{IN}=60V and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIN_{UVLO_RISING}	VIN UVLO rising voltage			4.3		V
$VIN_{UVLO\_FALLING}$	VIN UVLO falling voltage			4		V
V_{HYS_UVLO}	Hysteresis voltage of VIN UVLO			0.3		V
I_{SHUT_DOWN}	VIN current at shut down	V_{EN}=0V		3		μA
I_Q	Quiescent current at no switch state	V_{FB}=0.85V		180		μA
V_{EN_RISING}	Enable rising threshold			1.2		V
$V_{EN\_FALLING}$	Enable falling threshold			1		V
I_{ENPULL_UP}	EN pull-up current	V_{EN}=L		1		μA
		V_{EN}=H		4		
$V_{ENCLAMP}$	EN clamp voltage	EN voltage at 100uA current		5.7		V
V_{FB}	Feedback voltage		0.768	0.78	0.792	V
V_{FB_UV}	Feedback voltage			0.1		V
R_{HSON}	High Side power MOS ON resistance	V_{BST}-V_{SW}=5V		900		mΩ
$I_{LIMITHS}$	High side current limit threshold			1.7		A
T_{SS}	Soft-start time	V_{FB} from 10% to 90%		1.8		ms
F_{SW}	Switching Frequency			450		kHz
T_{ONMIN}(5)	Min On pulse			150		ns
T_{ONMAX}	Max On pulse			10		μs
T_{OFFMIN}(5)	Min Off time			350		ns
T_{VALLEY_MAX}(5)	Max valley off time			100		μs
T_{OTPR}(6)	Thermal shutdown			160		°C
T_{OTPF}(6)	Thermal shutdown hysteresis			140		°C

Note 5: Not tested in production and derived from bench characterization.

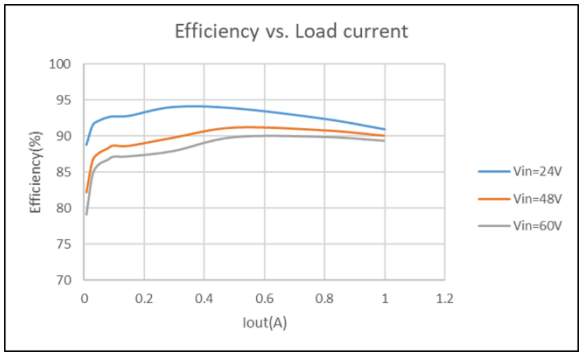
Note 6: Guaranteed by design.

Typical Performance Characteristic

V_{IN} = 48V, V_{OUT} = 12V, C1 = 10μF, C2 = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.

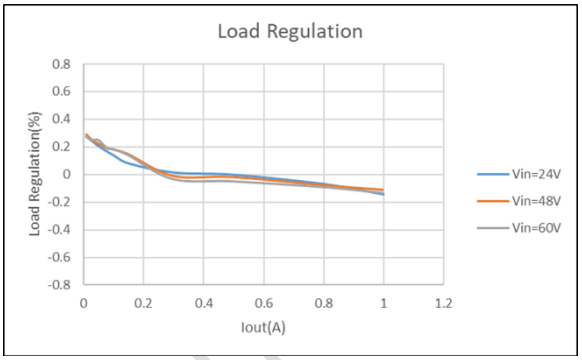
Efficiency vs. Load Current

VOUT=12V



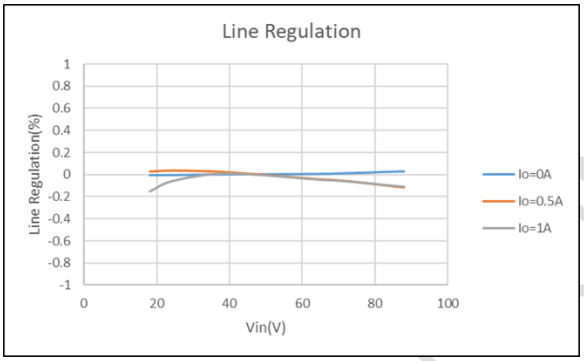
Load Regulation

IOUT=1A



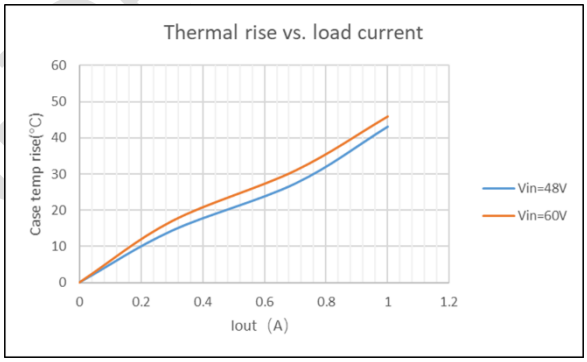
Line Regulation

IOUT=0A



Thermal Rise

VOUT=12V, no air flow

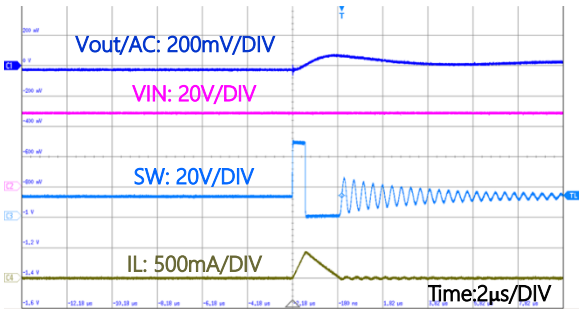


Typical Performance Characteristic*(continued)*

V_{IN} = 48V, V_{OUT} = 12V, C1 = 10μF, C2 = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.

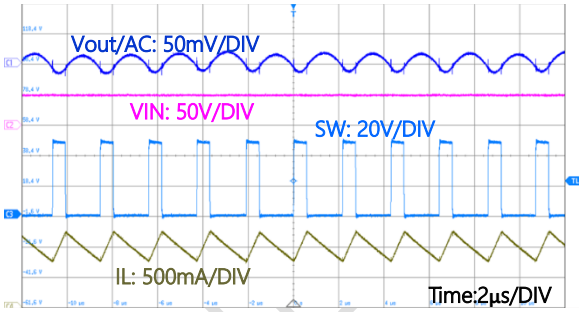
Output Voltage Ripple

IOUT=0A



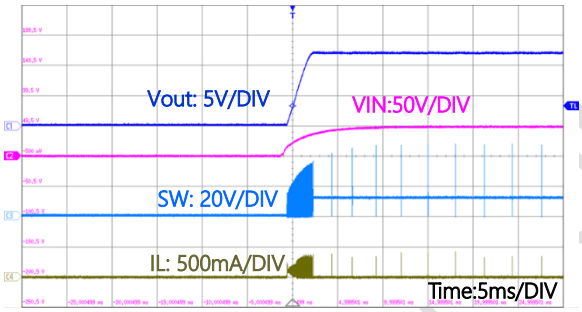
Output Voltage Ripple

IOUT=1A



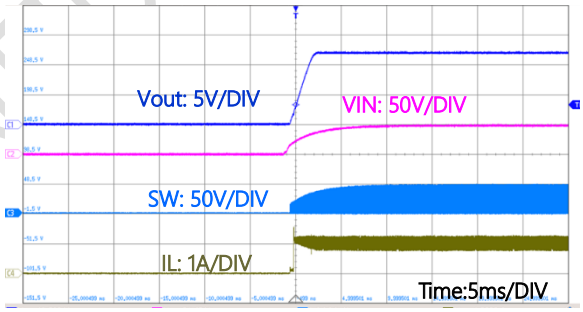
Start-Up through V_{IN}

IOUT=0A



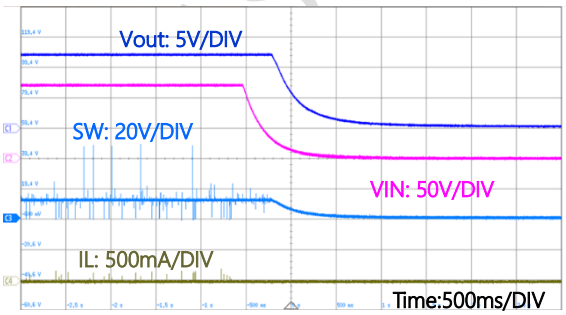
Start-Up through V_{IN}

IOUT=1A



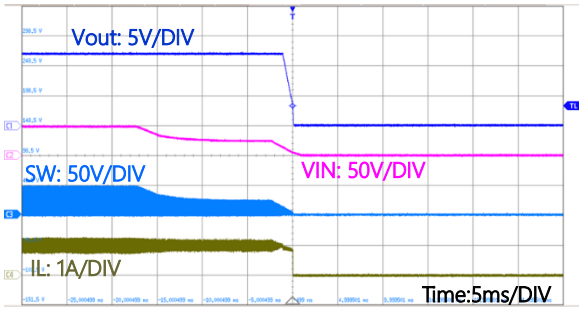
Shut-Down through V_{IN}

IOUT=0A



Shut-Down through V_{IN}

IOUT=1A

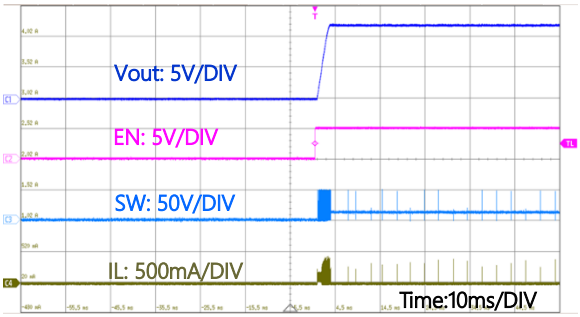


Typical Performance Characteristic *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, C1 = 10μF, C2 = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.

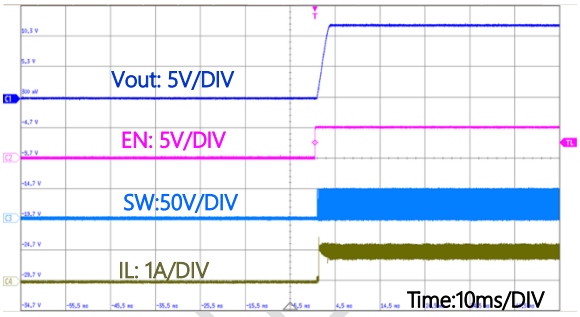
Start-Up through EN

IOUT=0A



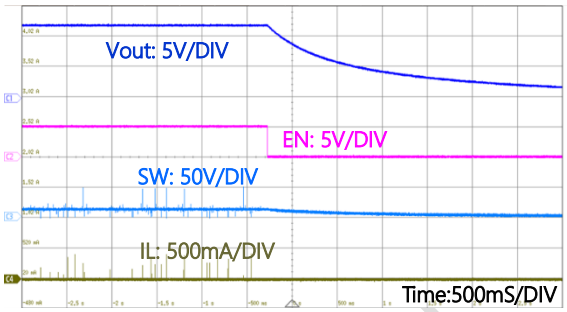
Start-Up through EN

IOUT=1A



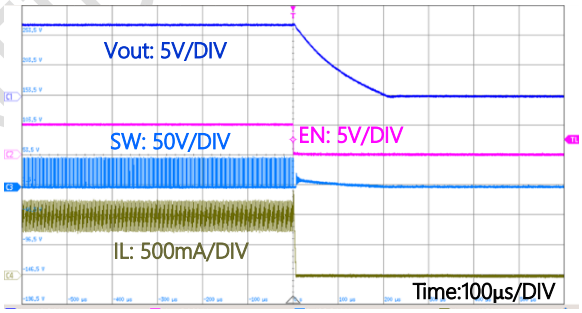
Shut-Down through EN

IOUT=0A



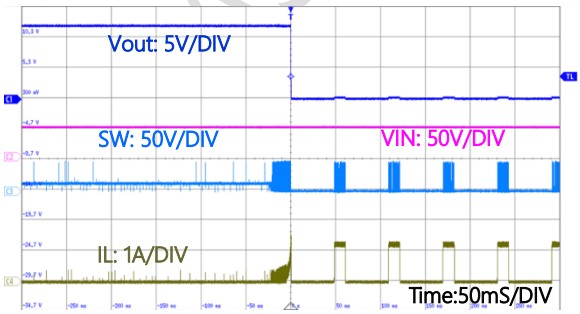
Shut-Down through EN

IOUT=1A



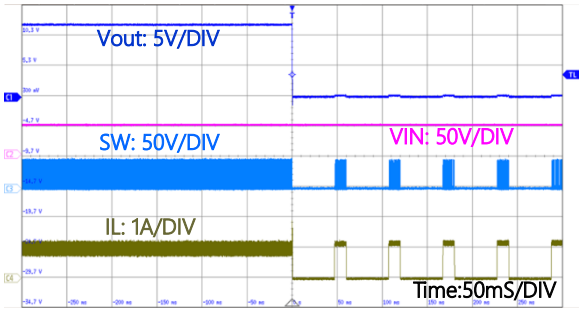
Short-Circuit Entry

IOUT=0A



Short-Circuit Entry

IOUT=1A

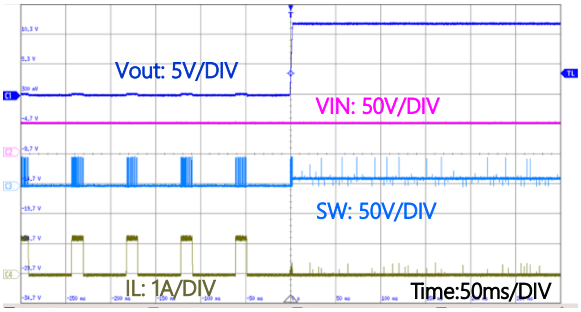


Typical Performance Characteristic *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, C1 = 10µF, C2 = 22µF, L1 = 47µH, and T_A = +25°C, unless otherwise noted.

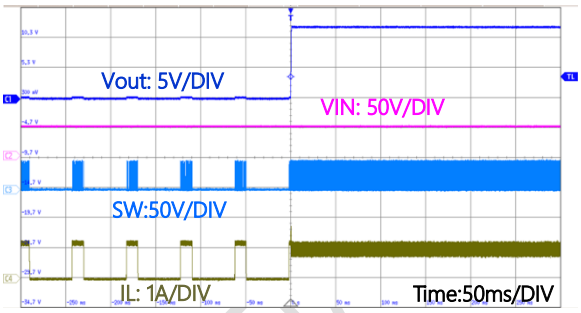
Short-Circuit Recovery

IOUT=0A

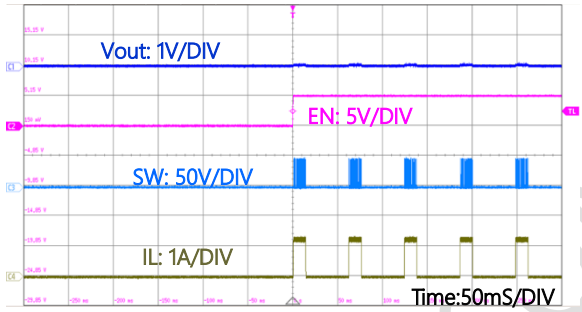


Short-Circuit Recovery

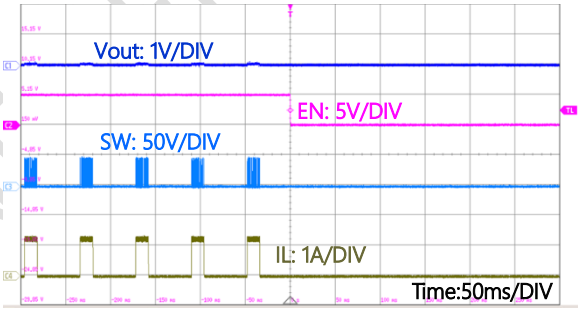
IOUT=1A



Short-circuit EN power on

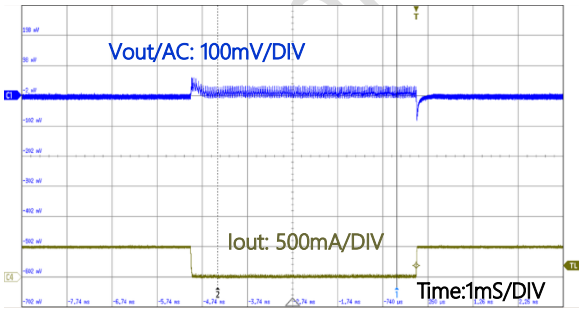


Short-circuit EN power off



Load Transient

VOUT=5V, L=33µH, IOUT = 0.01A to 0.5A, 2.5A/us slew rate



Function Descriptions

Pulse-Width Modulation (PWM) Operation

The LA1821 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the On-period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 1). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the external free-wheeling diode will handle the current.

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

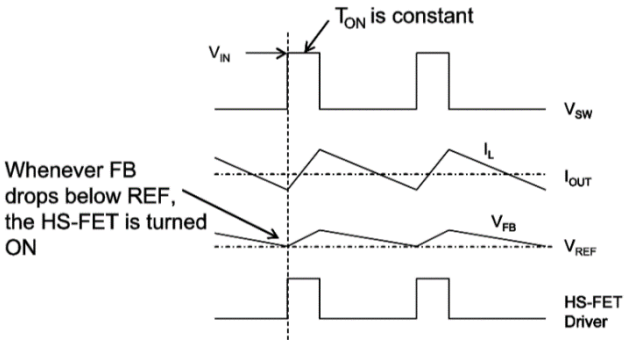


Figure 1: Heavy-Load Operation

Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 2. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on- timer. When the HS-FET is turned off, the free-wheeling diode is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The free-

wheeling diode will shut down the negative current and IC goes into tri-state. The output capacitors discharge to GND through the feedback resistor slowly. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the LA1821 reduces the switching frequency naturally. High efficiency is achieved at light load.

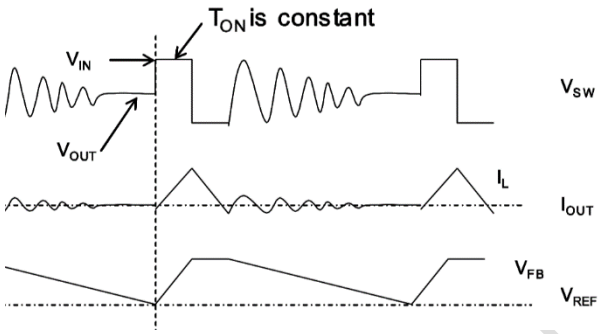


Figure 2: Light-Load Operation

As the output current increases from the light-load condition, the HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT\_critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{sw} \times V_{IN}}$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The LA1821's UVLO comparator will monitor the input voltage. its UVLO rising threshold is 4.3V, while its falling threshold is consistently 4V.

Enable (EN) Control

The LA1821 has a dedicated enable control pin with positive logic. Drive EN pin voltage higher than 1.2V(typical) to turn on the regulator, and drive EN pin voltage lower than 1V(typical) to turn it off.

The EN pin has an internal 4μA pullup current source, thus the LA1821 can automatically startup under EN pin floating conditions.

More than 4μA pulldown current is required to shut down the regulator via EN pin, after EN pin is pulled low, its internal pullup current will be decreased to 1μA to reduce the shutdown current.

By using the two external resistor dividers, it is easy to optimize the start and stop voltage of the system via EN pin:

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4\mu A \times R_{ENUP}$$

Stop voltage setting:

$$V_{STOP} = 1 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4\mu A \times R_{ENUP}$$

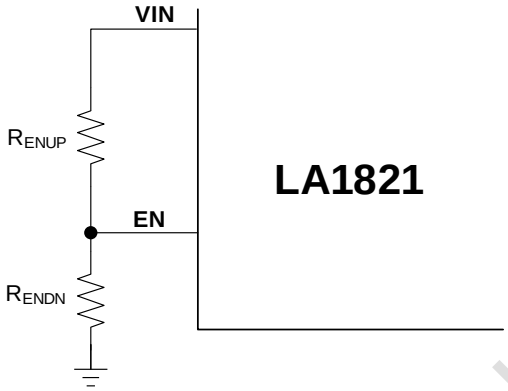


Figure 3: EN divider for adjustable UVLO

Internal Soft Start (SS)

Soft start (SS) prevents the output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set to 1.8ms internally.

High Duty Mode Operation

The LA1821 will automatically extend the on time to support the application when V_{IN} is close to V_{OUT}. The on time extend circuit will be triggered when T_{OFFMIN} time is reached. The LA1821 can support up to 97% maximum duty cycle.

Current Limit and Short Protection

The LA1821 has a peak current limit and a special valley current. During HS-FET on, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after blanking time, the HS-FET would be turn off. Due to the peak current limit's blanking time, the inductor current might runaway when output shorts to ground for a non-sync buck. The special valley current limit in LA1821 can prevent this happen. When HS-FET is off and the inductor current is larger than the valley current limit, the HS-FET keeps off until the output current drops below the valley current limit threshold.
When the output is short to ground, LA1821 will fold back the switching frequency automatically to prevent the current from runaway. It will make the system more reliable.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 140°C), the chip is enabled again.

Application Information

Setting the Output Voltage

The LA1821 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.78V. The feedback network is shown below Figure.

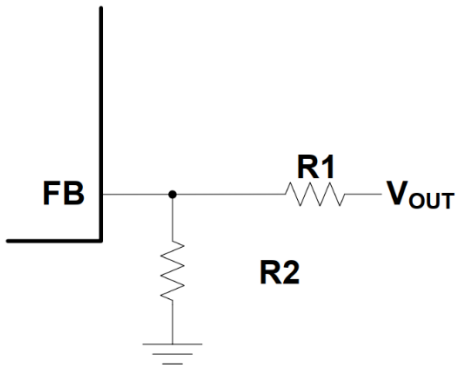


Figure 4: Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2}$$

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from Equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{sw}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (7)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff}(pF)	L (μH)	C_{OUT}(uF)
12	144	10	10	47	22
5	54	10	47	33	22

Note 7: For a detailed design circuit, please refer to the Typical Application Circuits.

Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{sw} \times C_{OUT}})$$

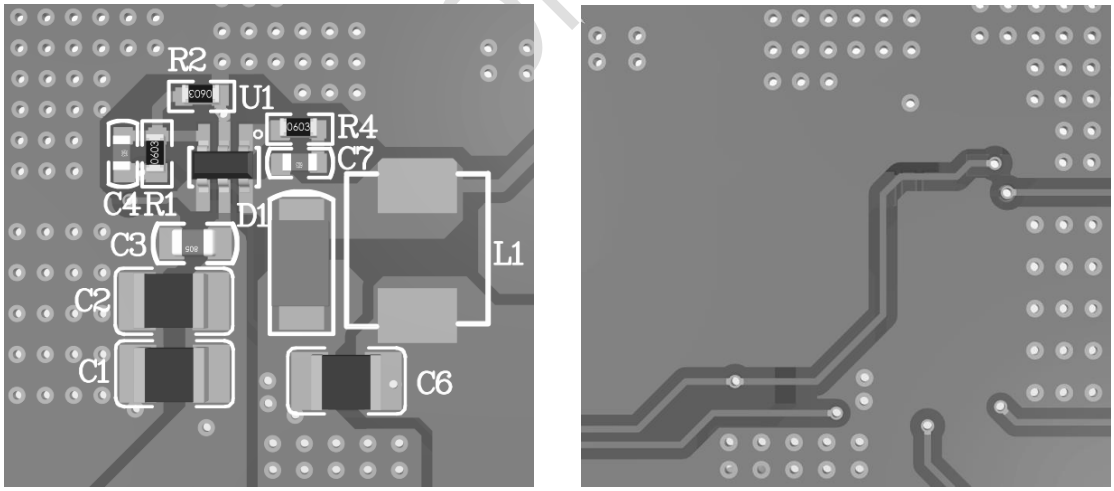
Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The LA1821 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.



Top Layer **Bottom Layer**

Figure 5: Recommend PCB Layout

Typical Application Circuits

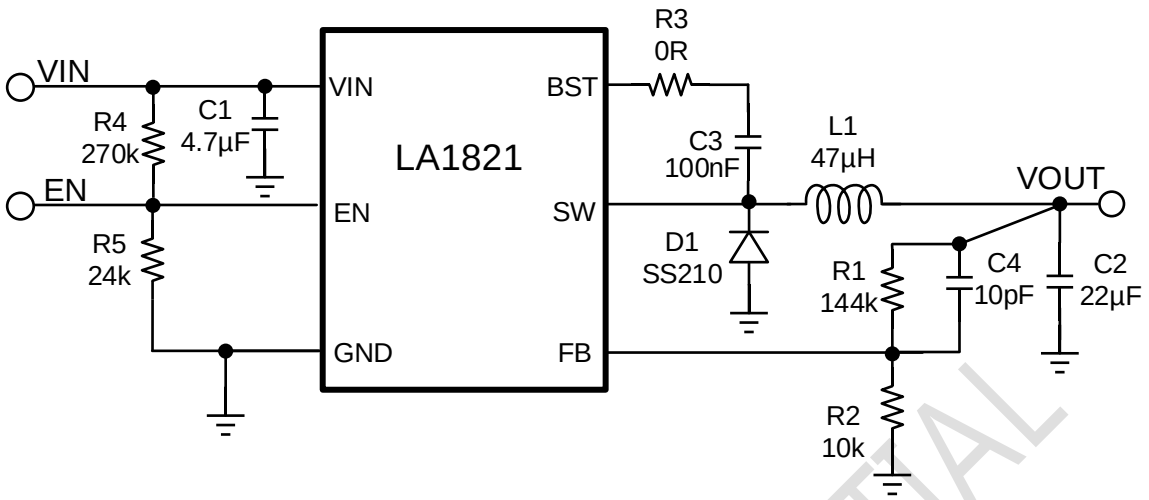


Figure 6: V_{IN}=48V, V_{OUT}=12V/1A

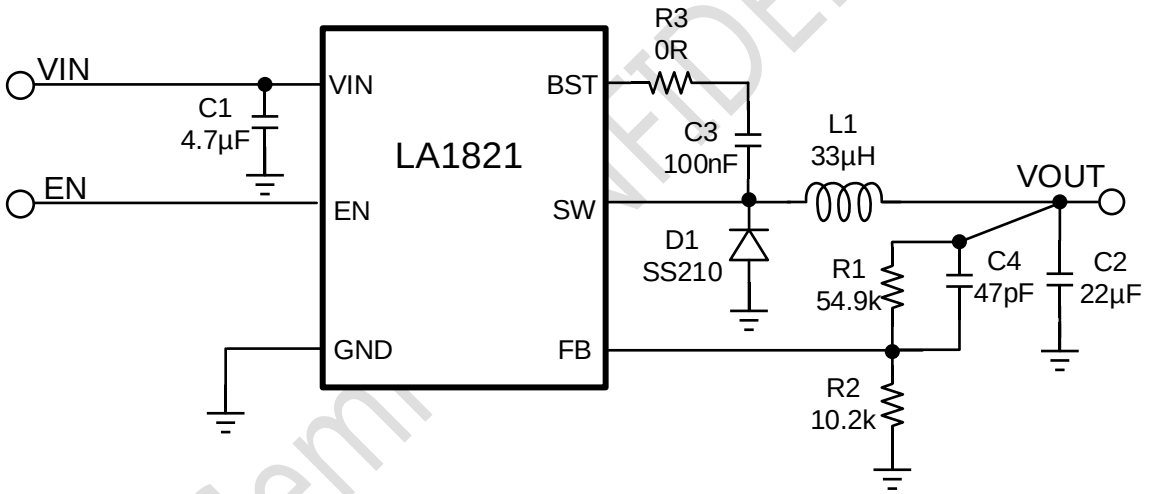
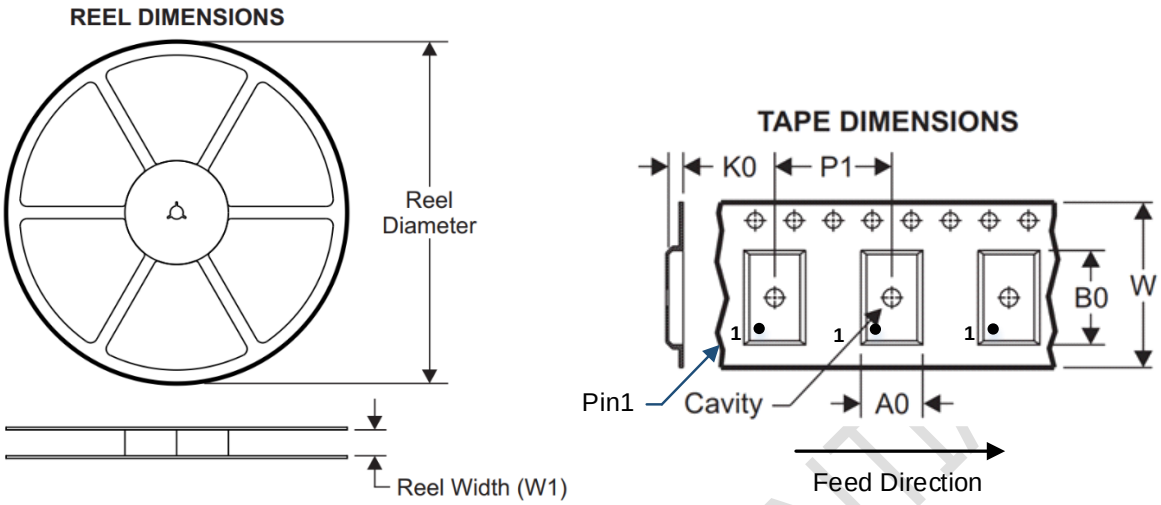


Figure 7: V_{IN}=48V, V_{OUT}=5V/1A

Tape and Reel Information



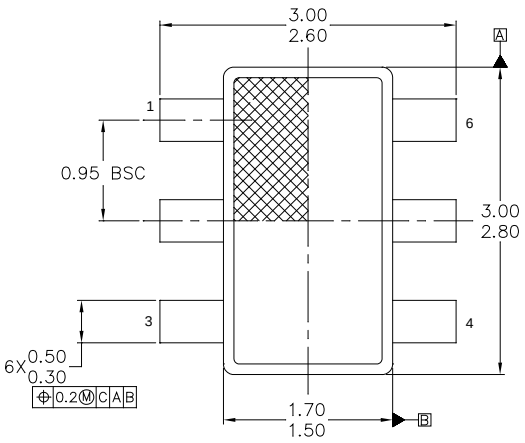
Information[8]

Device	Package Type	Pins	SPQ	Real Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
LA1821	SOT23-6	6	3000	178	9	3.25	3.3	1.38	4	8

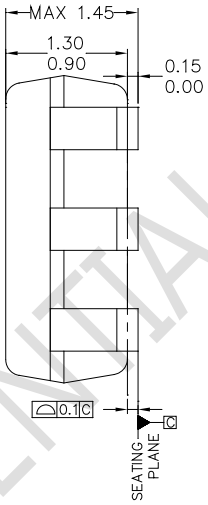
Note 8: Drawing is not to scale

Detail Package Outline Drawing

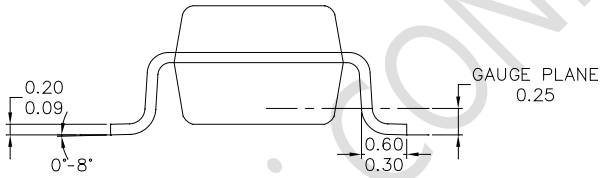
PACKAGE TYPE: SOT23-6



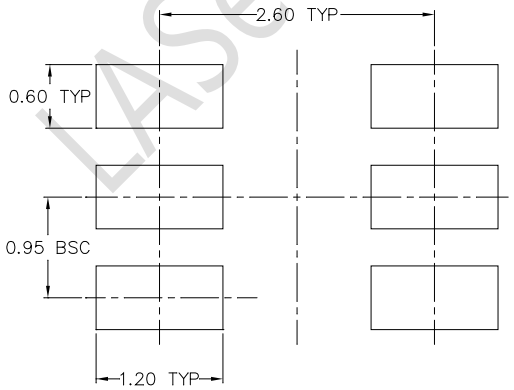
TOP VIEW



SIDE VIEW



FRONT VIEW



RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

N028029006A-A-22/03

单击下面可查看定价，库存，交付和生命周期等信息

>>Lattice Art