STK37660

RGB Sensor and Proximity Sensor with I2C interface

Datasheet

Version – 1.41

Hazardous Substance Free
RoHS / REACH Compliant

Sensortek Technology Corporation

1. OVERVIEW

Description

The STK37660 is an integrated color(RGB) and infrared light to digital converter with I²C interface. This device provides not only color(RGB)/ambient light sensing to allow robust backlight/display brightness control but also infrared sensing to allow proximity estimation featured with interrupt function.

For color(RGB)/ambient light sensing, the STK37660 incorporates Red, Green, Blue coating photodiode array and a reference Clear photodiode array, timing controller and ADC in a single chip to accurately measure the ambient light illumination and the environment CCT (correlated color temperature)

For proximity sensing, the STK37660 also incorporates a photodiode, timing controller and ADC in the same chip. The spectral response of STK37660 is optimized for wavelength 940nm infrared light. The STK37660 provides programmable current setting to drive IR LED and employs a noise cancellation scheme to highly reject unwanted ambient IR noise.

The STK37660 has excellent temperature compensation, robust on-chip refresh rate setting without external components. Software shutdown mode control is provided for power saving application. The STK37660 operating voltage range is 1.7V to 2.0V.

Feature

- Integrated ambient light sensor, proximity sensor in one package.

Proximity Sensor

- 16 bits resolution for proximity detection
- Built-in LED driver with flexible setting
  - LED turn-on time : 32 steps IT
  - LED current : 3.125 / 6.25 / 12.5 / 18.75 / 25 ..... / 193.75 / 200 mA
- Flexible interrupt setting
  - Several interrupt modes meet application requirements
  - Flag modes are included
  - Persistence : 1/2/4/8/16 times
- Low noise design
- High ambient light suppression

Color Sensor

- Convert ambient light intensity to 16-bit digital data format
- RGB sensor which closes to ideal human-eye response and suppress IR portion to enhance the accuracy of color temperature calculation
- Flexible digital settings
  - Long integration time : 8 steps IT
    - 3.125 / 6.25 / 12.5 /... / 200 / 400 ms
  - Short integration time : 20 steps IT
    - 192 / 288 / ... / 2112 us
- Flexible interrupt setting
  - Interrupt while out-of- window
  - Persistence : 1/2/4/8 times
- Clear channel for different light source identification
- FIFO buffer size is 2048 byte
  - FIFO mode
  - Stream mode

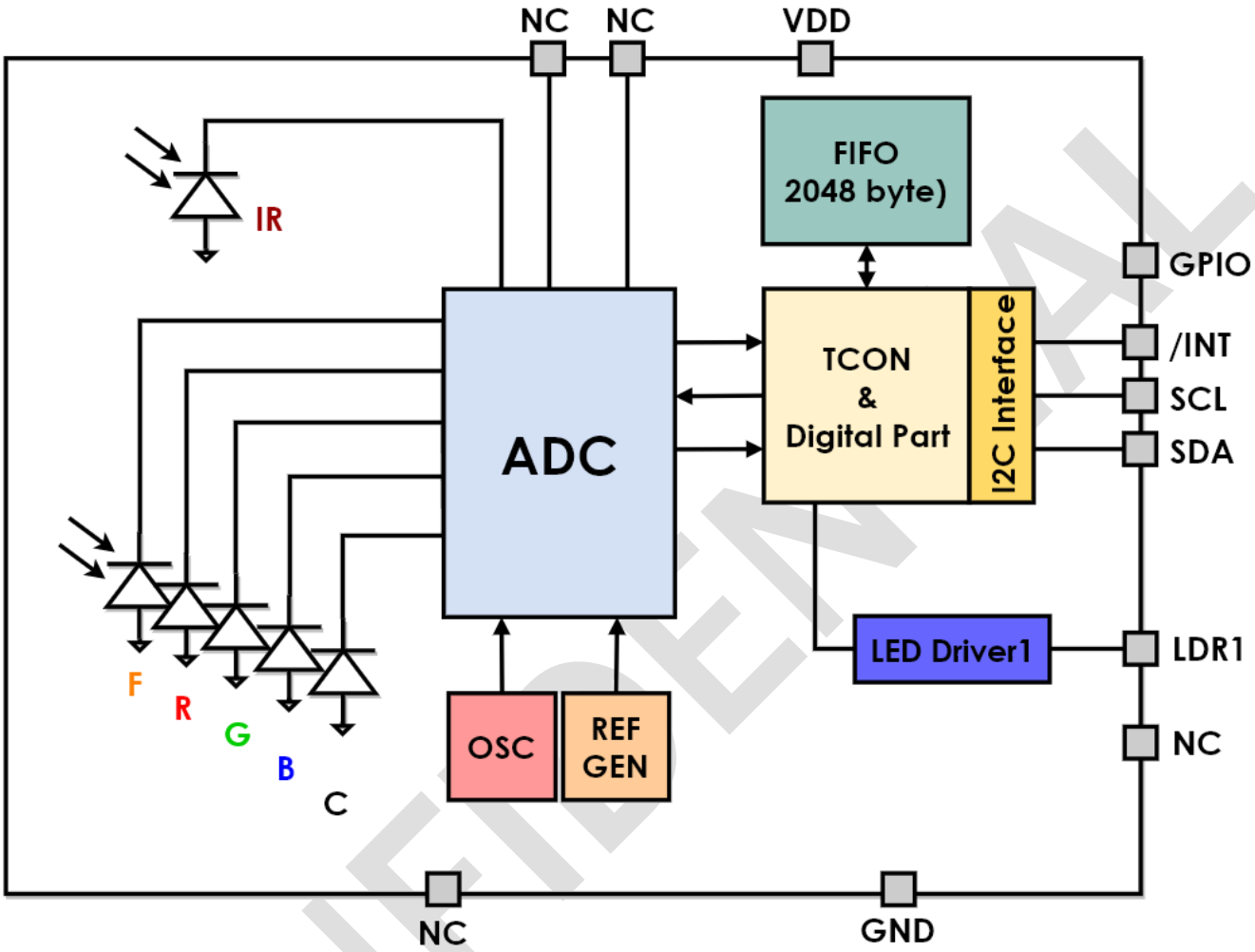
General

- Fully digital control with I²C interface
  - 1.7 ~ 3.6V I²C interface
- Low power design
  - Standby mode
  - Wait mode
- V_{DD} wide operation voltage : 1.7~2.0V
- Excellent temperature compensation: -40 to 85°C
- Available package options: OPLGA
  - STK37660 : 2.5 x 2.0 x 0.5 (mm)
- Lead-free package (RoHS compliant)
- Moisture Sensitivity Level 3

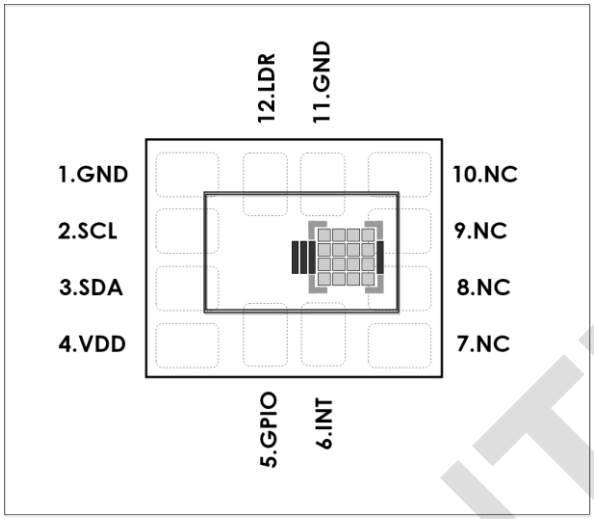
Applications

- Mobile Phone, Smart-phone, PDA

2. FUNCTION BLOCK



3. PINOUT DIAGRAM



Top View

4. PIN DESCRIPTION

Pin No.	Pin Name	Dir.	Pin Function
1	GND	GND	Ground. The thermal pad is also connected to the GND pin.
2	SCL	I	I²C serial clock line.
3	SDA	B	I²C serial data line. (Open Drain)
4	VDD	PWR	Power supply: 1.7V to 2.0V.
5	GPIO	I	Ext. Trigger (Open Drain)
6	/INT	O	Interrupt pin, LO for interrupt alarming. (Open Drain)
7	NC	-	No connect
8	NC	-	No connect
9	NC	-	No connect
10	NC	-	No connect
11	GND	GND	Ground. The thermal pad is also connected to the GND pin.
12	LDR	I	IR LED driver pin connecting to the cathode of the external IR LED. The sink current of the IR LED driver can be programmed through I²C or the external resistor. external resistor.

Direction denotation:

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connect

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	-0.3	2.0	V
V_{LDR}	Voltage of LDR		3.6	V
Ta	Operation temperature	-40	85	°C

NOTE: All voltages are measured with respect to GND

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	1.7	2.0	V
f_{I2C}	Clock frequency of I²C	—	400	KHz
Ta	Operation temperature	-40	85	°C

NOTE: All voltages are measured with respect to GND

Symbol	Parameter	Max.	Unit
ESD	Electrostatic discharge protection	2 (HBM)	kV
		200 (MM)	V
		100 (Latch Up)	mA

NOTE: All voltages are measured with respect to GND

5.1 Electrical and Optical Characteristics

V_{DD} = 1.8V & V_{LED} = 2.8V, under room temperature 25°C (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Characteristics						
I_{ALS}	ALS only supply current	Note1,2	290	360	394	μA
I_{PS}	PS only supply current	Note1,2	261	300	353	μA
I_{SD}	Shutdown current	Note1,2	0	3	7	μA
V_{IH}	Logic high, I²C	Note6	1.3		V_{DD}	V
V_{IL}	Logic low, I²C	Note7	0		0.4	V
ALS Characteristics						
λp_1	Peak sensitivity wavelength for ALS			550		nm
ALS_{FSCNT}	Full scale ALS counts				65535	counts
ALS_{DARK}	ALS dark offset	Note2,3,4		3		counts
ALS_{SENSE}	ALS sensing tolerance	Note2,3	-12.5		+12.5	%
	Red/F channel ratio	White LED,5000K	12.0	17.0	22.0	%
	Green/F channel ratio		25.0	37.5	50.0	
	Blue/F channel ratio		7.0	10.0	13.0	
Proximity Characteristics						
λp_2	High sensitivity wavelength range for PS		800	940	1000	nm
PS_{FSCNT}	Full scale PS counts				65535	counts
$ILED_{SINK}$	LED sink current	IRDR_LED[4:0] Note5				
		00000		03.125		mA
		00001		06.250		mA
		00010		12.500		mA
		00011		18.750		mA
		00100		25.000		mA
		...		...		mA
		01111		193.750		mA
		10000		200.000		mA

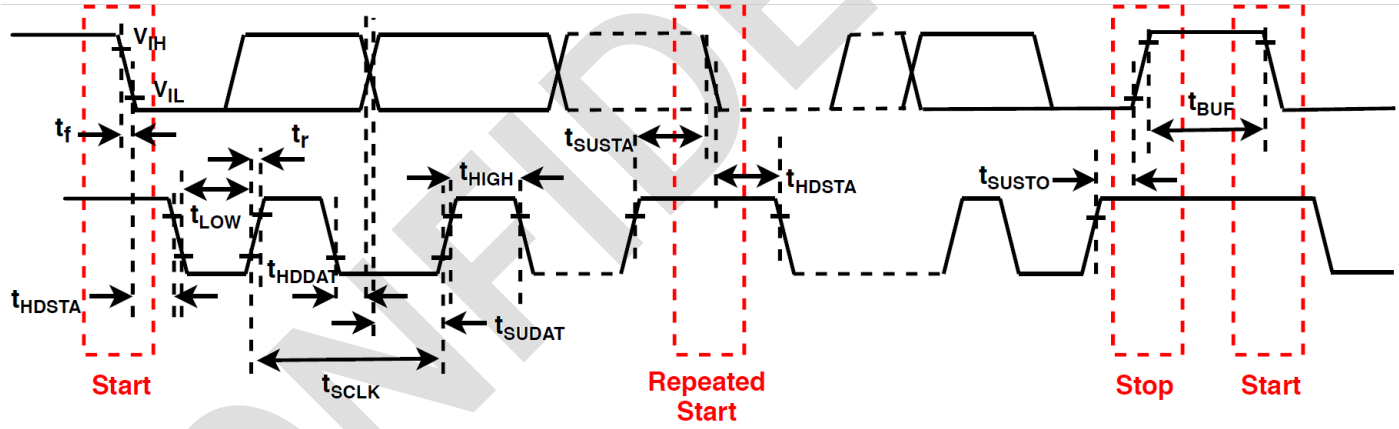
Note 1 : Operation without IR-LED.
Note 2 :
ALS : GAIN_ALS_C2_DX128[0] = 1'b1,GAIN_C1_DX128[0] = 1'b1,IT_ALS[3:0] = 4'b0101
PS : GAIN_PS_DX16[0] = 1'b1, IT_PS[3:0] = 4'b0100.
Note 3 : White LED parallel light source.
Note 4 : $E_{ambient}$ = 0 Lux.
Note 5 : The voltage of LDR pin is fixed at 1.2V.
Note 6 : I²C logical high voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical high level is different when different supply voltage is applied.
Note 7 : I²C logical low voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical low level is different when different supply voltage is applied.
Note 8 : Sunlight environment.

5.2 Timing Chart

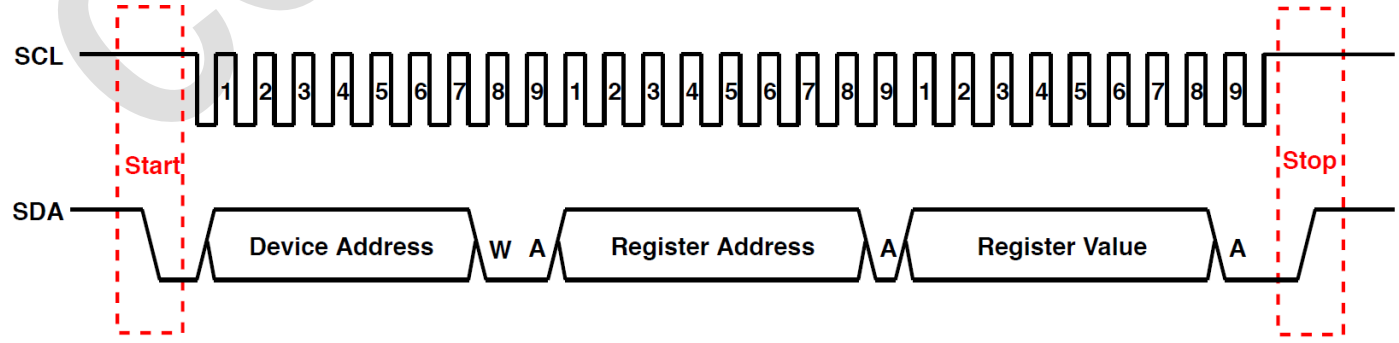
Characteristics of the SDA and SCL I/O

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	KHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	μs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs

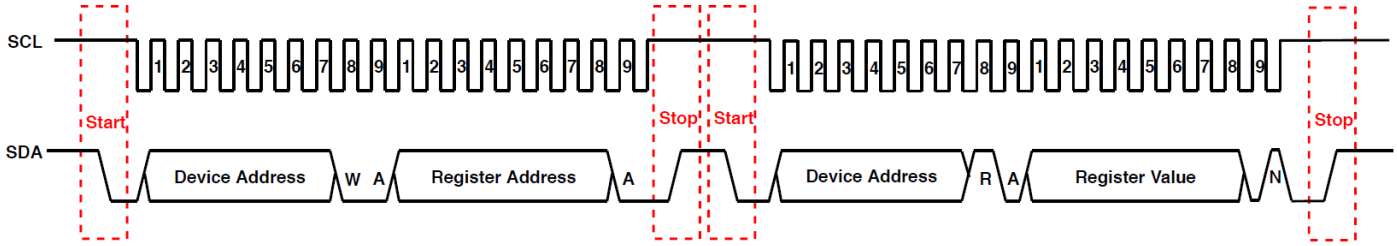
Note 1: f_{SCLK} is the $(t_{SCLK})^{-1}$.



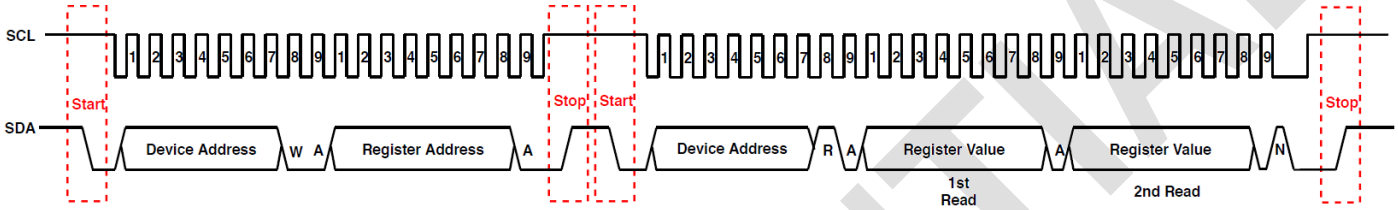
Timing Chart of the SDA and SCL



Write Command



Read Data



Sequential Read Data

6. FUNCTION DESCRIPTION

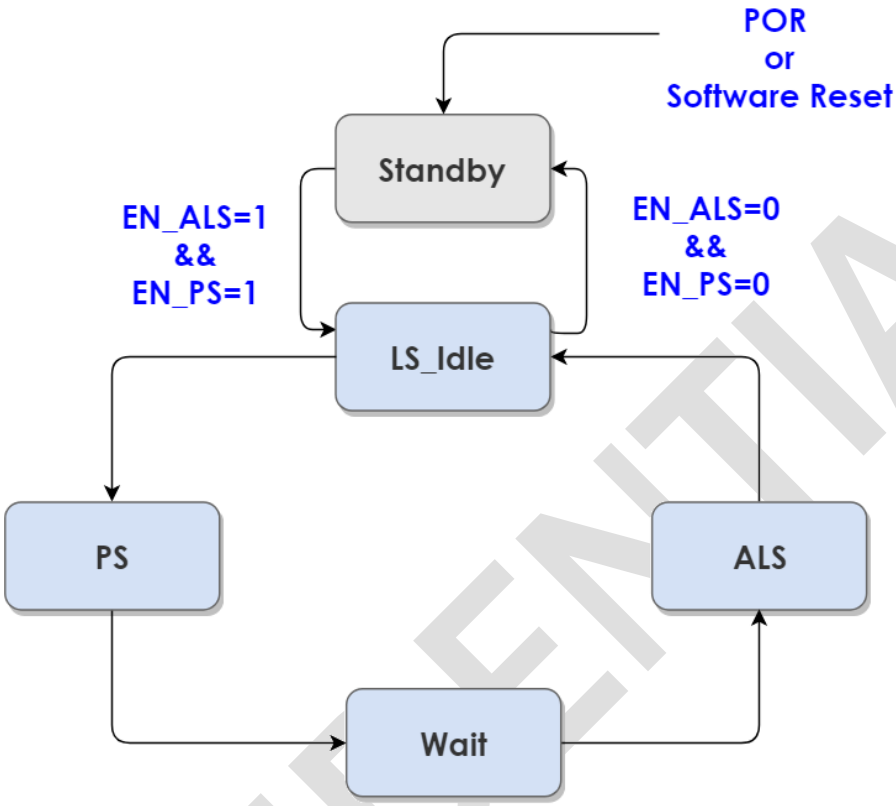
6.1 Digital Interface

STK37660 contains eight-bit registers accessed via the I²C bus. All operations can be controlled by the command register. The simple command structure makes user easy to program the operation setting and latch the output data from STK37660. Section 5.2 Timing chart displays the STK37660 I²C command format for reading and writing operation between host and STK37660.

STK37660 provides fixed I²C slave address of 0x48 using 7 bit addressing protocol.

Slave Address	R/W Command Bit	OPERATION
0x48 (followed by the R/W bit)	0	Write Command to STK37660
	1	Read Data from STK37660

6.2 System Operation



6.3 ALS Operation

6.3.1 ALS General Operation

The related ALS control bits are summarized below.

ALS Control Bits

General Control	
EN_ALS	Enable ALS sensing function
IT_ALS_SEL	Select ALS integration time
IT_ALS[3:0]	ALS long integration time
IT2_ALS[4:0]	ALS short integration time
GAIN_RGB[1:0]	ALS gain control
GAIN_RGB_DX128	ALS gain control specially for 128x
PRST_ALS[1:0]	ALS persistence number
GAIN_F_C[1:0]	Clear channel gain control
GAIN_F_C_DX128	Clear gain control specially for 128x
ALS Interrupt Control	
EN_ALS_INT	Enable ALS function interrupt
EN_ALS_DR_INT	Enable ALS data ready interrupt

THDH_ALS[15:0]	ALS out-of-windows high threshold
THDL_ALS[15:0]	ALS out-of-windows low threshold

ALS Data/Status Bits

Data	
DATA_F[15:0]	16-bits Flicker channel raw data
DATA_R[15:0]	16-bits Red channel raw data
DATA_G[15:0]	16-bits Green channel raw data
DATA_B[15:0]	16-bits Blue channel raw data
DATA_C[15:0]	16-bits Clear channel raw data
Status	
FLG_ALS_DR	Indicate the ALS data ready event
FLG_ALS_INT	Indicate the Green channel out-of-windows event

STK37660 uses the coated photodiode array to measure the Lux of the incoming light and also an un-filtered clear photodiode array to improve the ALS sensing accuracy.

The ALS sensing function is enabled by the EN_ALS bit and the gain control bit GAIN_RGB[1:0], GAIN_RGB_DX128, GAIN_F_C[1:0], GAIN_F_C_DX128 and IT period IT_ALS[3:0] shall be set before the EN_ALS.

The FLG_ALS_DR bit shall be asserted every ADC conversion cycle complete and shall be cleared automatically after one of the DATA_F[15:0]/DATA_C[15:0] is be read out through I²C.

The F/R/G/B/C data are 16-bit output and are stored in two bytes register. Higher byte register must be read first than lower byte. Data reading word protection is implemented to make sure the conversion data within the same conversion cycle could be read correctly. When the higher byte register is read, the lower 8-bit data will be stored into a shadow register which is read by the following sequential read or another single read to the lower byte register.

6.3.2 ALS Interrupt Description

ALS Out-of-Windows Interrupt

STK37660 provides the ALS data out-of-windows interrupt. Once the EN_ALS_INT is set to 1, then the STK37660 shall issue an ALS interrupt and assert the FLG_ALS_INT bit if the ALS data DATA_G[15:0] are outside the user's programmed window defined by THDH_ALS[15:0] and THDL_ALS[15:0]. The FLG_ALS_INT shall be cleared by write the bit 0 and shall be reset to 0 if POR/SWRst or EN_ALS = 0. Clear the EN_ALS_INT will also clear the FLG_ALS_INT bit to 0.

ALS persistence numbers PRST_ALS[1:0] is used to avoid the false alarm of ALS out-of-windows event due to environment noise. If ALS persistence is set larger than 1, then the ALS out-of-windows interrupt will not be issued until continuous persistence numbers of ADC conversion results outside the defined windows.

ALS Data Ready Interrupt

STK37660 also provides the ALS data ready interrupt. Once the EN_ALS_DR_INT is set to 1, then the STK37660 shall issue an ALS data ready interrupt every ADC conversion cycle and assert the FLG_ALS_DR bit. The FLG_ALS_DR shall be cleared automatically after any one of the DATA_R/G/B/C[15:0] is be read out through I²C and shall be reset to 0 if POR/SWRst or EN_ALS = 0. Clear the EN_ALS_DR_INT will not influence the FLG_ALS_DR status.

6.4 PS Operation

6.4.1 PS General Operation

The related PS control bits are summarized below.

PS Control Bits

General Control	
EN_PS	Enable PS function
IT_PS[3:0]	PS integration time
GAIN_PS[1:0]	PS gain control
GAIN_PS_DX16	PS gain control specially for 16x
PRST_PS[1:0]	PS persistence number
DATA_PS_OFFSET[15:0]	PS digital offset cancellation
LED Control	
IRDR_LED[3:0]	Select LED driving current
PS Interrupt Control	
EN_PS _INT	Enable PS function interrupt
EN_PS_DR_INT	Enable PS data ready interrupt
PS_INT_MODE	Choose PS interrupt triggered mode.
PS_NF_MODE	Choose FLG_NF observed mode
THDH_PS[15:0]	PS near-far detect high threshold
THDL_PS[15:0]	PS near-far detect low threshold

PS Data/Status Bits

Data	
DATA_PS[15:0]	16-bits PS raw data
Status	
FLG_NF	Indicate the current object near/far state
FLG_PS_INT	Indicate the object near/far state changed event
FLG_PS_DR	Indicate the PS data ready event
FLG_INVALID_PS_INT	Indicate the PS data is invalid

The proximity function is used for object detection by IR-sensitivity photodiode detection of reflected IR energy emitted by the built-in IR LED.

The DATA_PS[15:0] will be the ADC output subtract offset data defined in DATA_PS_OFFSET[15:0]. The PS data are 16-bit output and are stored in two bytes register. Higher byte register must be read first than lower byte. Data reading word protection is implemented to make sure the conversion data within the same conversion cycle could be read correctly. When the higher byte register is read, the lower 8-bit data will be stored into a shadow register which is read by the following sequential read or another single read to the lower byte register.

The FLG_NF is used to indicate the current object is in near or far state and persistence is also applied to this flag if PRST_PS > 1.

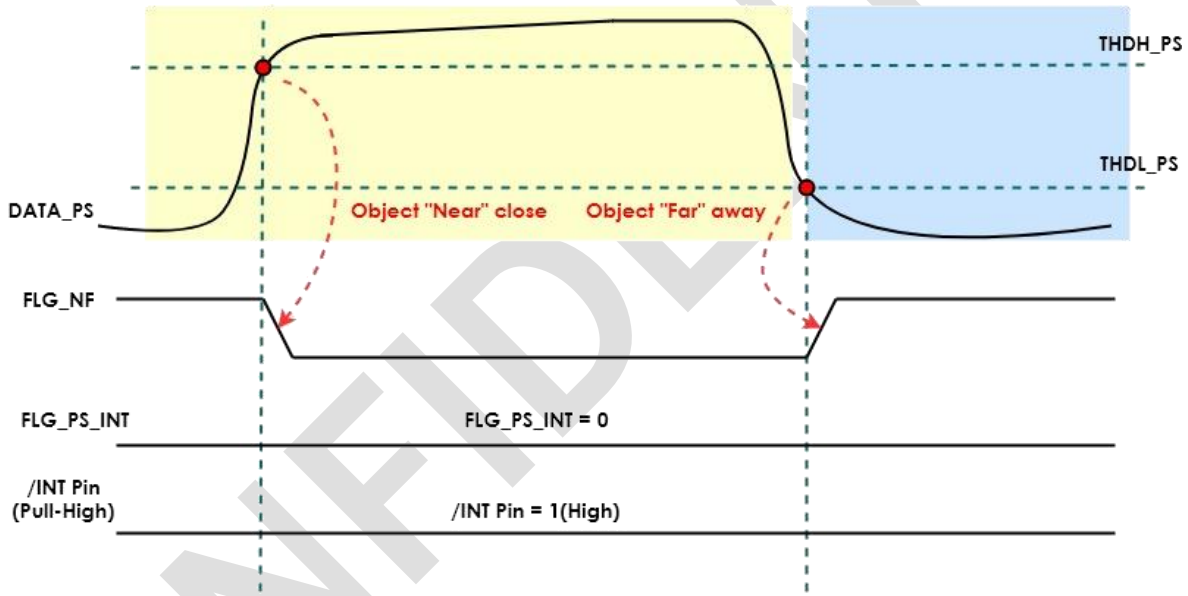
The FLG_PS_DR bit shall be asserted every ADC conversion cycle complete and shall be cleared automatically after the DATA_PS[15:0] is be read out through I^2C.

IRDR_LED[3:0] is used to choose different LED constant driving current. STK37660 has 11 different LED current levels 3.125/6.25/12.5/25/50/75/100/125/150/175/200 mA

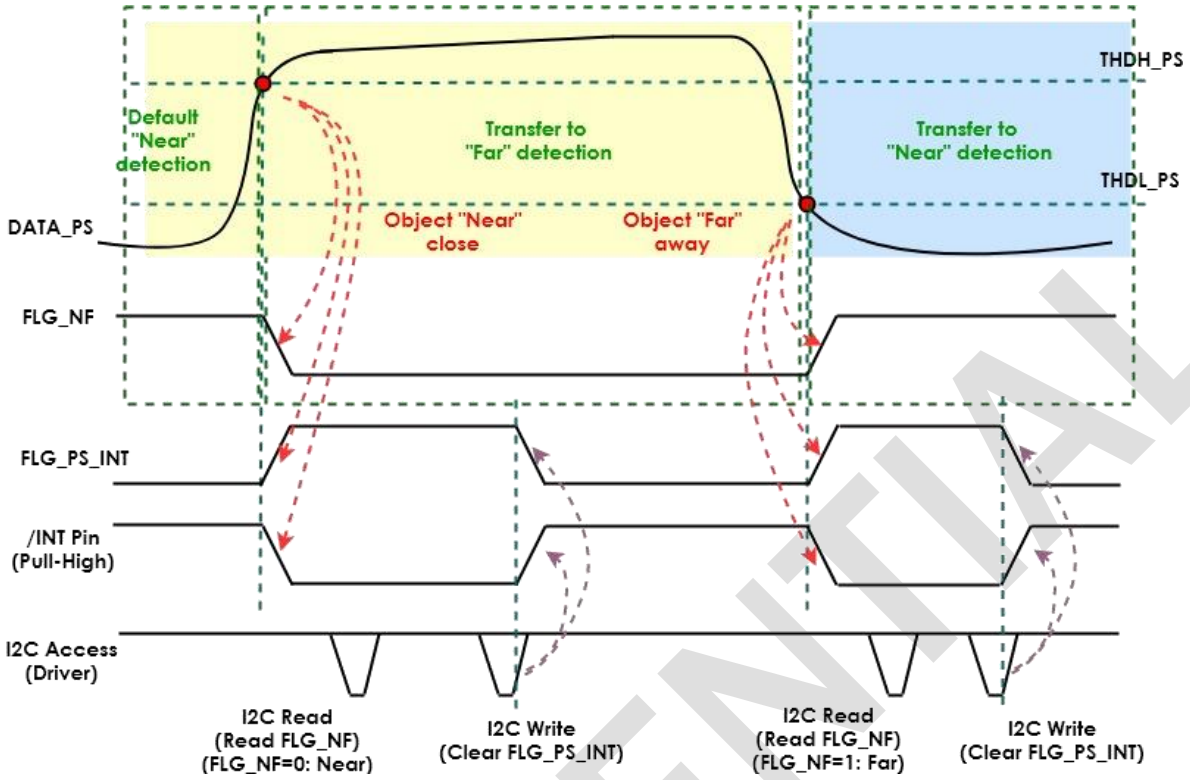
6.4.2 PS Interrupt Description

The EN_PS_INT[0] register is used to control PS interrupt function for enable or disable
The PS_NF_MODE[1] register is used to select how STK37660 reports the object near/far state to application.
The PS_INT_MODE[2] register is PS interrupt modes for near/far state change are described as below.

PS INT Function (EN_PS_INT[0] = 1'b0) & PS Near/Far Flag Mode (PS_NF_Mode[1] = 1'b0)
If EN_PS_INT[0] is set to 1'b0, then the polling mode is used and the INT pin is non-active when near/far event detected. In this mode, the INT output level is fixed to pull-high and the FLG_PS_INT will never be asserted. The application simply polls the FLG_NF to check the object in near or far state.



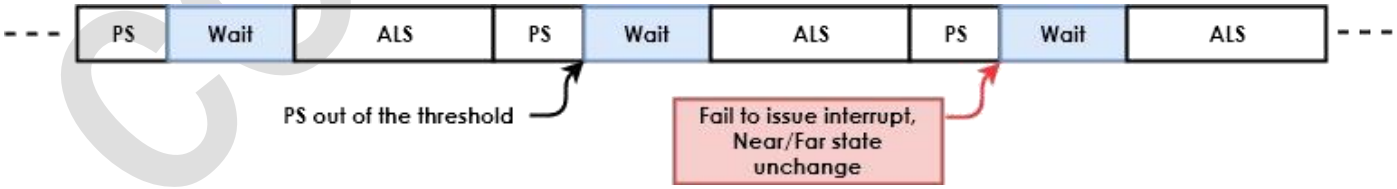
PS INT Function (EN_PS_INT[0] = 1'b1) & PS Near/Far Flag Mode (PS_NF_Mode[1] = 1'b0)
The INT pin is treated as interrupt signal. The FLG_NF is used to indicate whether the object is in near or far state. The STK37660 is default in object far state and the FLG_NF = 1. Once the object moving close to the STK37660 and PS code exceed the high threshold THDH_PS, STK37660 will switch to object near state and the FLG_NF is cleared to 0. STK37660 will issue a PS interrupt to inform the object near/far state changed and also set the FLG_PS_INT to 1. If the object move far away from the STK37660 and PS code lower than the low threshold THDL_PS, STK37660 will switch to object far state and the FLG_NF is set to 1. STK37660 will also issue a PS interrupt to inform and set FLG_PS_INT. The FLG_PS_INT shall be cleared by write the bit 0 and shall be reset to 0 if POR/SWRst or EN_PS = 0. The FLG_NF shall be reset to 1 if POR/SWRst or EN_PS = 0. Change the PS_MODE will also clear the FLG_PS_INT to 0, but keep the current PS code and FLG_NF state.



PS persistence numbers PRST_PS[1:0] is used to avoid the false alarm of PS interrupt event due to environment noise. If PS persistence is set larger than 1, then the PS interrupt will not be issued until continuous persistence numbers of ADC conversion results meet the interrupt condition describe above.

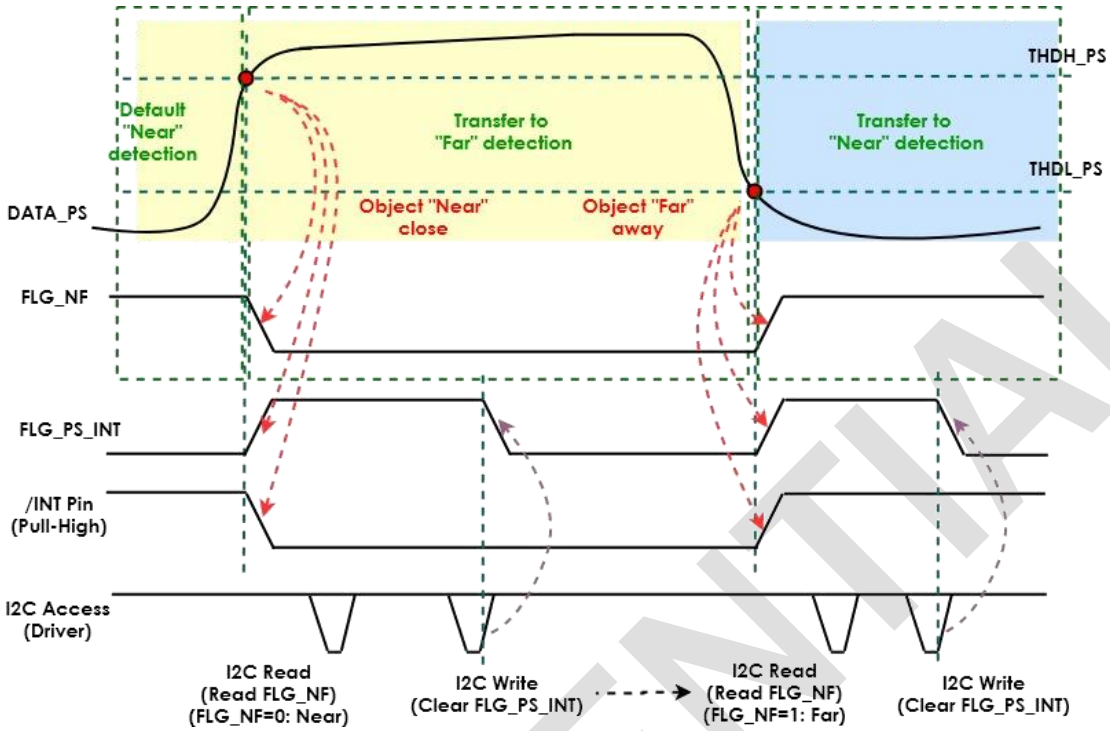
For example:
(1) PRST_PS[1:0] = 2'b01 (x2), EN_ALS = 1, EN_PS = 1, EN_WAIT = 1

(2) PRST_PS[1:0] = 2'b01 (x2), EN_ALS = 1, EN_PS = 1, EN_WAIT = 1, and fail to issue interrupt event (no continue persistence numbers of PS ADC conversion results is out of threshold),



PS INT Function (EN_PS_INT[0] = 1'b1) & PS Near/Far Flag Mode (PS_NF_Mode[1] = 1'b1)

If PS_NF_MODE[1] = 1'b1, then the polling mode is used and the INT pin is treated as a near/far flag signal, not an interrupt signal. In this mode, the INT output level is same with the FLG_NF signal level and the FLG_PS_INT will never be asserted. The application simply polls the INT level (high or low) to check the object in near or far state. INT Pin is only from PS FLG_NF, and the ALS interrupt, Invalid PS interrupt is ignored.



PS Data Ready Interrupt

STK37660 provides the PS data ready interrupt. Once the EN_PS_DR_INT is set to 1, then the STK37660 shall issue a PS data ready interrupt every ADC conversion cycle and assert the FLG_PS_DR bit. The FLG_PS_DR shall be cleared automatically after the DATA_PS[15:0] is be read out through I²C and shall be reset to 0 if POR/SWRst or EN_PS = 0. Clear the EN_PS_DR_INT will not influence the FLG_PS_DR status.

6.5 Wait State Operation

6.5.1 Wait State General Operation

The related Wait control bits are summarized below.

Wait Control Bits

General Control	
EN_WAIT	Enable Wait state
WAIT[7:0]	Wait period

Wait state is used for power saving

7. CONTROL REGISTER MAP

ADDR	REG NAME	BIT								Default
		7	6	5	4	3	2	1	0	
0x00	STATE						EN_WAIT	EN_ALS	EN_PS	0x00
0x01	PSCTRL	PRST_PS[1:0]		GAIN_PS[1:0]		IT_PS[3:0]				0x02
0x02	ALSCTRL1	PRST_ALS[1:0]		GAIN_RGB[1:0]		IT_ALS[3:0]				0x05
0x03	LEDCTRL	IRDR[5:0]								0x40
0x04	INTCTRL1	INT_CTRL		EN_INVALID_PS_INT		EN_ALS_INT	PS_INT_MODE	PS_NF_MODE	EN_PS_INT	0x00
0x05	WAIT	WAIT[7:0]								0x00
0x06	THDH1_PS	THDH_PS[15:8]								0xFF
0x07	THDH2_PS	THDH_PS[7:0]								0xFF
0x08	THDL1_PS	THDL_PS[15:8]								0x00
0x09	THDL2_PS	THDL_PS[7:0]								0x00
0x0A	THDH1_ALS	THDH_ALS[15:8]								0xFF
0x0B	THDH2_ALS	THDH_ALS[7:0]								0xFF
0x0C	THDL1_ALS	THDL_ ALS[15:8]								0x00
0x0D	THDL2_ALS	THDL_ ALS[7:0]								0x00
0x10	FLAG	FLG_ALS_DR	FLG_PS_DR	FLG_ALS_INT	FLG_PS_INT		FLG_ALS_SAT	FLG_INVALID_PS_INT	FLG_NF	0x01
0x11	DATA1_PS	DATA_PS[15:8]								0x00
0x12	DATA2_PS	DATA_PS[7:0]								0x00
0x13	DATA1_F	DATA_F[15:8]								0x00
0x14	DATA2_F	DATA_F[7:0]								0x00
0x15	DATA1_R	DATA_R[15:8]								0x00
0x16	DATA2_R	DATA_R[7:0]								0x00
0x17	DATA1_G	DATA_G[15:8]								0x00
0x18	DATA2_G	DATA_G[7:0]								0x00
0x19	DATA1_B	DATA_B[15:8]								0x00
0x1A	DATA2_B	DATA_B[7:0]								0x00
0x1B	DATA1_C	DATA_C[15:8]								0x00
0x1C	DATA2_C	DATA_C[7:0]								0x00
0x1D	DATA1_PS_OFFSET	DATA_PS_OFFSET[15:8]								0x00
0x1E	DATA2_PS_OFFSET	DATA_PS_OFFSET[7:0]								0x00
0x3E	PDT_ID	PDT_ID[7:0]								0x25
0x3F	Reserved	Reserved								
0x4E	GAINCTRL			GAIN_F_C[1:0]			GAIN_F_C_DX128	GAIN_RGB_DX128	GAIN_PS_DX16	0x00
0x60	FIFOCTRL1			FIFO_MODE[1:0]			FIFO_DATA_SEL[2:0]			0x00
0x61	THD1_FIFO_FCNT						THD_FIFO_FCNT[10:8]			0x00
0x62	THD2_FIFO_FCNT	THD_FIFO_FCNT[7:0]								0x00
0x63	FIFOCTRL2						FIFO_OVR_EN	FIFO_THD_EN	FIFO_FULL_EN	0x00
0x64	FIFO_FCNT1						FIFO_FCNT[10:8]			0x00
0x65	FIFO_FCNT2	FIFO_FCNT[7:0]								0x00
0x66	FIFO_OUT	FIFO_OUT[7:0]								0x00
0x67	FIFO_FLAG	FLG_FIFO_OVR			FLG_FIFO_THD				FLG_FIFO_FULL	0x00

0x6F	ALSCTRL2	IT_ALS_SEL			IT2_ALS[4:0]					**0x00**
0x80	SOFT_RESET	Write any to soft reset								**0x00**
0xA1	PDCTRL1				ALS_SEL[4:0]					**0x1F**
0xA2	PDCTRL2					PS_SEL[3:0]				**0x0F**
0xA5	INTCTRL2							EN_ALS_DR_INT	EN_PS_DR_INT	**0x00**
0xDB	AGCTRL			F_C_CI[1:0]		RGB_CI[1:0]		PS_CI[1:0]		**0x00**

STATE Register (0x00)

Bit	7	6	5	4	3	2	1	0
ITEM						EN_WAIT	EN_ALS	EN_PS
Access						R/W	R/W	R/W
Default						0	0	0

Bit	ITEM	Description
0	EN_PS	Enable the PS function. 0 : Disable 1 : Enable
1	EN_ALS	Enable the ALS/C function. 0 : Disable 1 : Enable
2	EN_WAIT	Enable the Wait state. 0 : Disable 1 : Enable

PSCTRL Register (0x01)

Bit	7	6	5	4	3	2	1	0
ITEM	PRST_PS[1:0]		GAIN_PS[1:0]		IT_PS[3:0]			
Access	R/W		R/W		R/W			
Default	2'b00		2'b00		4'b0000			

Bit	ITEM	Description
3:0	IT_PS[3:0]	PS integration time. 4'b0000 — 24 us 4'b0001 — 48 us **4'b0010 — 96 us** 4'b0011 — 192 us 4'b0100 — 384 us 4'b0101 — 768 us 4'b0110 — 1.536 ms 4'b0111 — 3.072 ms 4'b1000 — 6.144 ms
5:4	GAIN_PS[1:0]	PS gain setting. **2'b00 — x 1 times** 2'b01 — x 2 times 2'b10 — x 4 times 2'b11 — x 8 times
7:6	PRST_PS[1:0]	PS persistence setting. The PS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-threshold PS occurrences before an interrupt is triggered. **2'b00 — x 1 times** 2'b01 — x 2 times 2'b10 — x 4 times 2'b11 — x 8 times

ALSCTRL1 Register (0x02)

Bit	7	6	5	4	3	2	1	0
ITEM	PRST_ALS[1:0]		GAIN_RGB[1:0]		IT_ALS[3:0]			
Access	R/W		R/W		R/W			
Default	2'b00		2'b00		4'b0101			

Bit	ITEM	Description
3:0	IT_ALS[3:0]	ALS integration time. 4'b0000 — 3.125 ms 4'b0001 — 6.25 ms 4'b0010 — 12.5 ms 4'b0011 — 25 ms 4'b0100 — 50 ms **4'b0101 — 100 ms** 4'b0110 — 200 ms 4'b0111 — 400 ms
5:4	GAIN_RGB[1:0]	RGB gain setting. GAIN_RGB[1:0] is used to control of the RGBchannels signal gain. The F/C channel is controlled by GAIN_F_C[1:0]. **2'b00 — x 1 times** 2'b01 — x 4 times 2'b10 — x 16 times 2'b11 — x 64 times
7:6	PRST_ALS[1:0]	ALS persistence setting. The ALS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-windows ALS occurrences before an interrupt is triggered. **2'b00 — x 1 times** 2'b01 — x 2 times 2'b10 — x 4 times 2'b11 — x 8 times

BIT[3:0]	REFRESH TIME	Multiple of Base Refresh Time	mLux/LSB under GAIN_F_C_DX128
0000	3.125ms	x1	7.1111
0001	6.25ms	x2	3.5555
0010	12.5ms	x4	1.7777
0011	25ms	x8	0.8888
0100	50ms	x16	0.4444
0101	100ms	x32	0.2222
0110	200ms	x64	0.1111
0111	400ms	X128	0.0555

BIT[5:4]	Gain	mLux/LSB under IT_ALS=4'b0101 (100ms)
00	x1	28.4416
01	x4	7.1104
10	x16	1.7776
11	x64	0.4444

LEDCTRL Register (0x03)

Bit	7	6	5	4	3	2	1	0
ITEM	IRDR_LED[5:0]							
Access	R/W							
Default	4'b010000							

Bit	ITEM	Description
7:2	IRDR_LED[5:0]	LED constant current setting. The STK37660 provides different sinking ability for IRLED through setting IRDR.(one step=6.25mA)

6'b000000	3.125 mA current sink
6'b000001	6.250 mA current sink
6'b000010	12.500 mA current sink
6'b000011	18.750 mA current sink
6'b000100	25.000 mA current sink
…	…
6'b010000	100.000 mA current sink
…	…
6'b011110	187.500 mA current sink
6'b011111	193.750 mA current sink
6'b1XXXXX	200.000 mA current sink

INTCTRL1 Register (0x04)

Bit	7	6	5	4	3	2	1	0
ITEM	INT_CTRL		EN_INVALID_PS_INT		EN_ALS_INT	PS_INT_MODE	PS_NF_MODE	EN_PS_INT
Access	R/W		R/W		R/W	R/W	R/W	R/W
Default	0		0		0	0	0	0

Bit	ITEM	Description
0	EN_PS_INT	Enable the PS interrupt
1	PS_NF_MODE	Choose FLG_NF observed mode. 0 : FLG_NF could be observed from FLAG[0] 1 : FLG_NF could be observed through INT
2	PS_INT_MODE	Choose PS interrupt triggered mode. 0 : PS interrupt is triggered by FLG_NF change 1 : PS interrupt is triggered by PS data out of window
3	EN_ALS_INT	Enable the ALS out-of-windows interrupt. 0 : Disable 1 : Enable
5	EN_INVALID_PS_INT	Enable the Invalid PS interrupt. 0 : Disable 1 : Enable
7	INT_CTRL	0 : Set /INT pin low if FLG_ALS_INT or FLG_ALS_DR or FLG_PS_INT or FLG_PS_DR or FLG_POCKET_MODE_INT or FLG_INVALID_PS_INT high 1 : Set /INT pin low if (FLG_ALS_INT and FLG_PS_INT) or FLG_ALS_DR or FLG_PS_DR high or FLG_POCKET_MODE_INT or FLG_INVALID_PS_INT high

WAIT Register (0x05)

Bit	7	6	5	4	3	2	1	0
ITEM	WAIT[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
7:0	WAIT[7:0]	PS/GS wait state period. wait period = (WAIT[7:0] + 1) * 1.54 ms

THDH1_PS Register (0x06)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_PS[15:8]							
Access	R/W							
Default	8'b11111111							

THDH2_PS Register (0x07)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_PS[7:0]							
Access	R/W							
Default	8'b11111111							

THDL1_PS Register (0x08)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_PS[15:8]							
Access	R/W							
Default	8'b00000000							

THDL2_PS Register (0x09)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_PS[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
15:0	THDH_PS[15:0]	PS high threshold.
15:0	THDL_PS[15:0]	PS low threshold.

THDH1_ALS Register (0x0A)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_ALS[15:8]							
Access	R/W							
Default	8'b11111111							

THDH2_ALS Register (0x0B)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_ALS[7:0]							
Access	R/W							
Default	8'b11111111							

THDL1_ALS Register (0x0C)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_ALS[15:8]							
Access	R/W							
Default	8'b00000000							

THDL2_ALS Register (0x0D)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_ALS[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
15:0	THDH_ALS[15:0]	ALS high threshold.
15:0	THDL_ALS[15:0]	ALS low threshold.

FLAG Register (0x10)

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_ALS_DR	FLG_PS_DR	FLG_ALS_INT	FLG_PS_INT		FLG_ALS_SAT	FLG_INVALID_PS_INT	FLG_NF
Access	R/W	R/W	R/W	R/W		RO	R/W	RO
Default	0	0	0	0		0	0	1

Bit	ITEM	Description
0	FLG_NF	Object near/far flag. Default FLG_NF = 1, object in far state. 0 : Object in near state 1 : Object in far state
1	FLG_INVALID_PS_INT	Indicate if interrupt event is related to INVALID_PS_INT. Write bit 0 to clear. 0 : No INVALID_PS_INT event

		1 : INVALID_PS_INT event
2	FLG_ALS_SAT	Indicate the ALS channel circuit saturation. 0 : No ALS channel circuit saturation, the data is valid. 1 : ALS channel circuit saturation, the data is not valid.
4	FLG_PS_INT	Indicate if interrupt event is related to PS_INT. Write bit 0 to clear. 0 : No PS_INT event 1 : PS_INT event
5	FLG_ALS_INT	Indicate if interrupt event is related to ALS_INT. Write bit 0 to clear. 0 : No ALS_INT event 1 : ALS_INT event
6	FLG_PS_DR	Indicate PS data conversion complete. Automatically cleared after DATA_PS[15:0] is read. 0: PS data is not ready 1: PS data is ready
7	FLG_ALS_DR	Indicate ALS data conversion complete. Automatically cleared after DATA_ALS[15:0] is read. 0: ALS data is not ready 1: ALS data is ready

DATA1_PS Register (0x11)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_PS[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_PS Register (0x12)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_PS[7:0]							
Access	RO							
Default	8'b00000000							

The STK37660 has two 8-bit read-only registers to hold the data from ADC of PS. The most significant bit (MSB) is accessed at register 0x11, and the least significant bit (LSB) is accessed at register 0x12. The registers are updated for every PS integration time (conversion cycle).

DATA1_F Register (0x13)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_F[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_F Register (0x14)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_F[7:0]							
Access	RO							
Default	8'b00000000							

DATA1_R Register (0x15)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_R[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_R Register (0x16)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_R[7:0]							
Access	RO							
Default	8'b00000000							

DATA1_G Register (0x17)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_G[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_G Register (0x18)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_G[7:0]							
Access	RO							
Default	8'b00000000							

DATA1_B Register (0x19)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_B[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_B Register (0x1A)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_B[7:0]							
Access	RO							
Default	8'b00000000							

DATA1_C Register (0x1B)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_C[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_C Register (0x1C)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_C[7:0]							
Access	RO							
Default	8'b00000000							

The STK37660 has two 8-bit read-only registers to hold each data from ADC of F/R/G/B/C. The registers are updated for every F/R/G/B/C integration time (conversion cycle).

DATA1_PS_OFFSET Register (0x1D)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_PS_OFFSET[15:8]							
Access	RW							
Default	8'b00000000							

DATA2_PS_OFFSET Register (0x1E)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_PS_OFFSET[7:0]							
Access	RW							
Default	8'b00000000							

Product ID (0x3E)

Read Only; PDT_ID = Product ID(0x25) to indicate the product information.

Reserved (0x3F)

Read Only; RSRVD = Reserved for engineering mode.

GAINCTRL Register (0x4E)

Bit	7	6	5	4	3	2	1	0
ITEM			GAIN_F_C[1:0]			GAIN_F_C_DX128	GAIN_RGB_DX128	GAIN_PS_DX16
Access			R/W			R/W	R/W	R/W
Default			2'b00			0	0	0

Bit	ITEM	Description
0	GAIN_PS_DX16	GAIN_PS_DX16 is used to control specially for PS channel 16x gain.
1	GAIN_RGB_DX128	GAIN_RGB_DX128 is used to control specially for RGBchannel 128x gain.
2	GAIN_F_C_DX128	GAIN_F_C_DX128 is used to control specially for F/C channel 128x gain.
5:4	GAIN_F_C[1:0]	F/C channel gain setting. GAIN_F_C[1:0] is used to control of the F/C channel signal gain. The RGB are controlled by GAIN_RGB[1:0]. 2'b00 x 1 times 2'b01 x 4 times 2'b10 x 16 times 2'b11 x 64 times

FIFOCTRL1 Register (0x60)

Bit	7	6	5	4	3	2	1	0
ITEM			FIFO_MODE[1:0]			FIFO_DATA_SEL[2:0]		
Access			R/W			R/W		
Default			2'b00			3'b000		

Bit	ITEM	Description
5:4	FIFO_MODE	00: Mode off 01: Bypass mode 10: FIFO mode 11: Stream mode
2:0	FIFO_DATA_SEL	000: PS only mode (maximum FIFO frame size is 1024) 001: F+G mode (maximum FIFO frame size is 512) 010: F+C mode (maximum FIFO frame size is 512) 011: R+G+B+C mode (maximum FIFO frame size is 256) 100: F+G+C+PS mode (maximum FIFO frame size is 256)

THD1_FIFO_FCNT Register (0x61)

Bit	7	6	5	4	3	2	1	0
ITEM						THD_FIFO_FCNT[10:8]		
Access						R/W		
Default						3'b000		

THD2_FIFO_FCNT Register (0x62)

Bit	7	6	5	4	3	2	1	0
ITEM	THD_FIFO_FCNT[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
10:0	THD_FIFO_FCNT	Set the FIFO_FCNT threshold.

FIFOCTRL2 Register (0x63)

Bit	7	6	5	4	3	2	1	0
ITEM						FIFO_OVR_EN	FIFO_THD_EN	FIFO_FULL_EN
Access						R/W	R/W	R/W
Default						0	0	0

Bit	ITEM	Description
0	FIFO_FULL_EN	Enable the FIFO_FULL interrupt
1	FIFO_THD_EN	Enable the FIFO_THD interrupt
2	FIFO_OVR_EN	Enable the FIFO_OVR interrupt

FIFO_FCNT1 Register (0x64)

Bit	7	6	5	4	3	2	1	0
ITEM						FIFO_FCNT[10:8]		
Access						R		
Default						3'b000		

FIFO_FCNT2 Register (0x65)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_FCNT[7:0]							
Access	R							
Default	8'b00000000							

Bit	ITEM	Description
10:0	FIFO_FCNT	Indicate FIFO frame count if FIFO is enabled.

FIFO_OUT Register (0x66)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_OUT[7:0]							
Access	R							
Default	8'b00000000							

Bit	ITEM	Description
7:0	FIFO_OUT	FIFO output data

FIFO_FLAG Register (0x67)

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_FIFO_OVR			FLG_FIFO_THD				FLG_FIFO_FULL
Access	R			R				R
Default	0			0				0

Bit	ITEM	Description
0	FLG_FIFO_FULL	Indicate if FIFO_FCNT is full in FIFO mode. Read FIFO_OUT to clear. 0 : No FLG_FIFO_FULL event 1 : FLG_FIFO_FULL event
4	FLG_FIFO_THD	Indicate if FIFO_FCNT is equal THD_FIFO_FCNT in FIFO/Stream mode. Read FIFO_OUT to clear. 0 : No FLG_FIFO_THD event 1 : FLG_FIFO_THD event
7	FLG_FIFO_OVR	Indicate if FIFO_FCNT is overflow in Stream mode. Read FIFO_OUT to clear. 0 : No FLG_FIFO_THD event 1 : FLG_FIFO_THD event

ALSCTRL2 Register (0x6F)

Bit	7	6	5	4	3	2	1	0
ITEM	IT_ALS_SEL			IT2_ALS[4:0]				
Access	R/W			R/W				
Default	0			5'b00000				

Bit	ITEM	Description
4:0	IT_ALS2[4:0]	ALS short integration time. Enable by REG_IT_ALS_SEL = 1 5'b00000 192 us 5'b00001 288 us 5'b00010 384 us 5'b0011 480 us ... ... 5'b10010 1920 us 5'b10011 2016 us 5'b10100 2112 us
7	IT_ALS_SEL	0: Use IT_ALS[3:0] to define ALS long integration time. 1: Use IT2_ALS[4:0] to define ALS short integration time.

Soft reset (0x80)

Write any data to this register will reset the chip.

PDCTRL1 Register (0xA1)

Bit	7	6	5	4	3	2	1	0
ITEM				ALS_F	ALS_B	ALS_G	ALS_R	ALS_C
Access				R/W	R/W	R/W	R/W	R/W
Default				1	1	1	1	1

Bit	ITEM	Description
0	ALS_C	Enable the Clear PD . 0 : Disable 1 : Enable
1	ALS_R	Enable the Red PD . 0 : Disable 1 : Enable
2	ALS_G	Enable the Green PD . 0 : Disable 1 : Enable
3	ALS_B	Enable the Blue PD . 0 : Disable 1 : Enable
4	ALS_F	Enable the Flicker PD . 0 : Disable 1 : Enable

PDCTRL2 Register (0xA2)

Bit	7	6	5	4	3	2	1	0
ITEM					PS_PS3	PS_PS2	PS_PS1	PS_PS0
Access					R/W	R/W	R/W	R/W
Default					1	1	1	1

Bit	ITEM	Description
0	PS_PS0	Enable the PS0 PD . 0 : Disable 1 : Enable
1	PS_PS1	Enable the PS1 PD . 0 : Disable 1 : Enable
2	PS_PS2	Enable the PS2 PD . 0 : Disable 1 : Enable
3	PS_PS3	Enable the PS3 PD . 0 : Disable 1 : Enable

INTCTRL2 Register (0xA5)

Bit	7	6	5	4	3	2	1	0
ITEM							EN_ALS_DR_INT	EN_PS_DR_INT
Access							R/W	R/W
Default							0	0

Bit	ITEM	Description
0	EN_PS_DR_INT	Enable the PS Data Ready interrupt. 0 : Disable 1 : Enable
1	EN_ALS_DR_INT	Enable the ALS Data Ready interrupt. 0 : Disable 1 : Enable

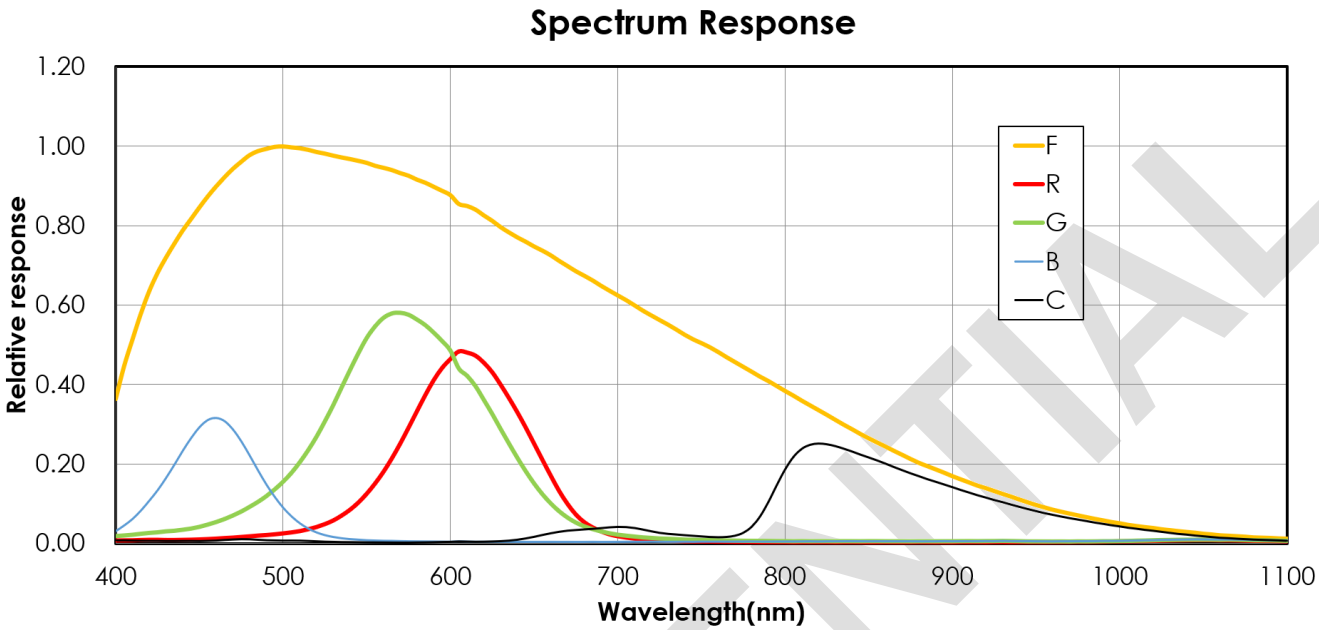
AGCTRL Register (0xDB)

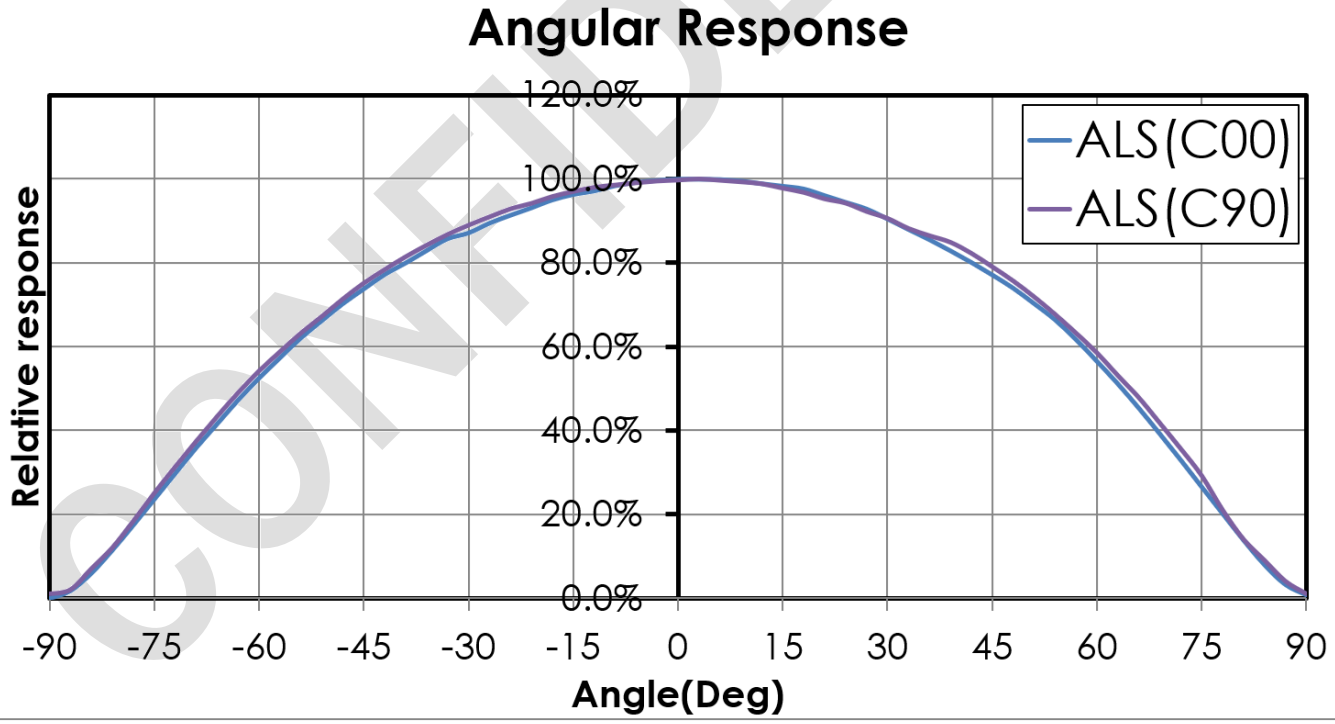
Bit	7	6	5	4	3	2	1	0
ITEM			F_C_CI[1:0]		RGB_CI[1:0]		PS_CI[1:0]	
Access			R/W		R/W		R/W	
Default			2'b00		2'b00		2'b00	

Bit	ITEM	Description
1:0	PS_CI[1:0]	PS channel analog gain setting. 2'b00 x 2 2'b01 x 1 2'b10 x 0.5

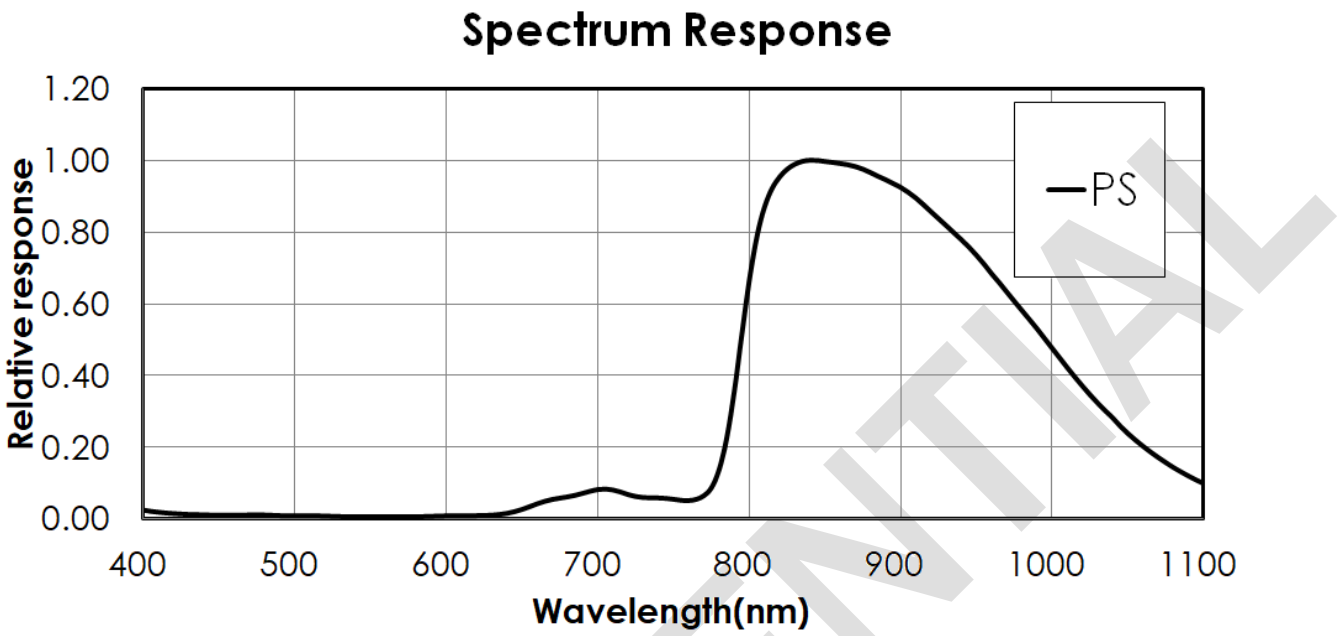
<table>
<tr><td>3:2</td><td>RGB_CI[3:2]</td><td>RGB channel analog gain setting.<table><tr><td>2'b00</td><td>x 2</td></tr><tr><td>2'b01</td><td>x 1</td></tr><tr><td>2'b10</td><td>x 0.5</td></tr></table></td></tr>
<tr><td>5:4</td><td>F_C_CI[5:4]</td><td>Flicker/CLEAR channel analog gain setting.<table><tr><td>2'b00</td><td>x 2</td></tr><tr><td>2'b01</td><td>x 1</td></tr><tr><td>2'b10</td><td>x 0.5</td></tr></table></td></tr>
</table>

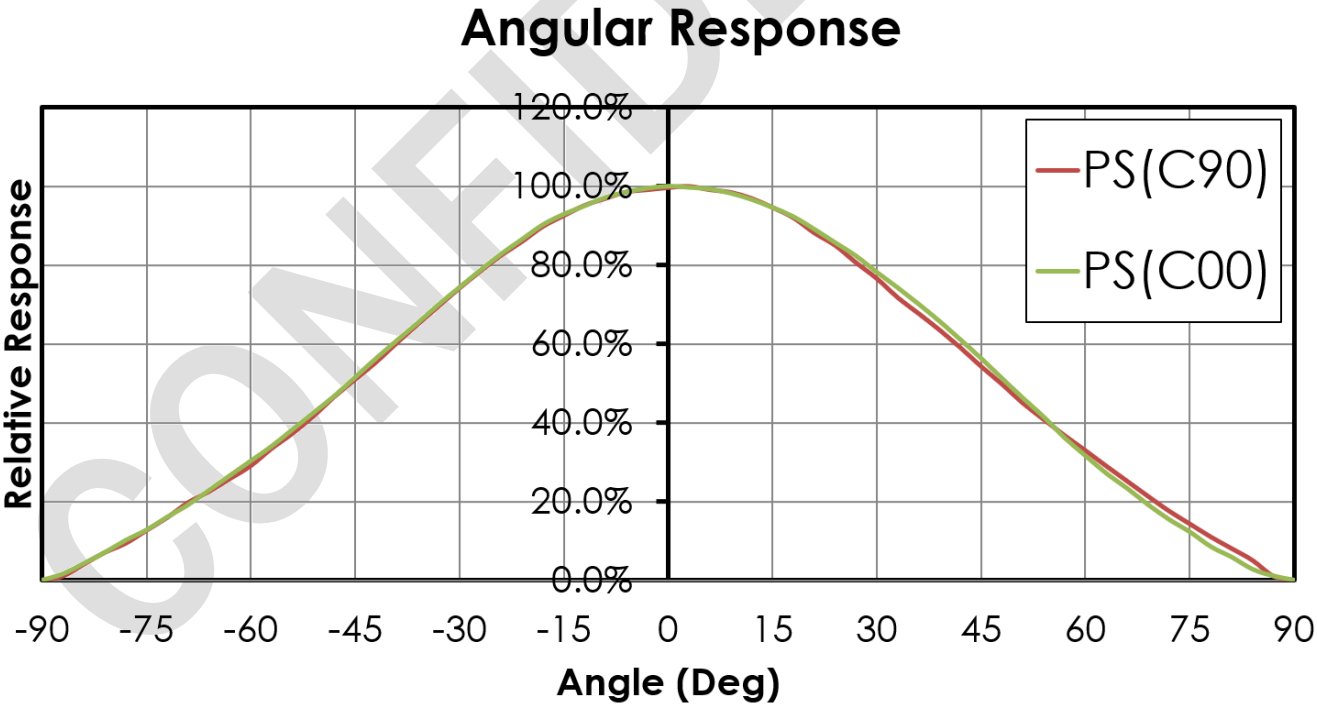
8. ALS RESPONSE CHARTS





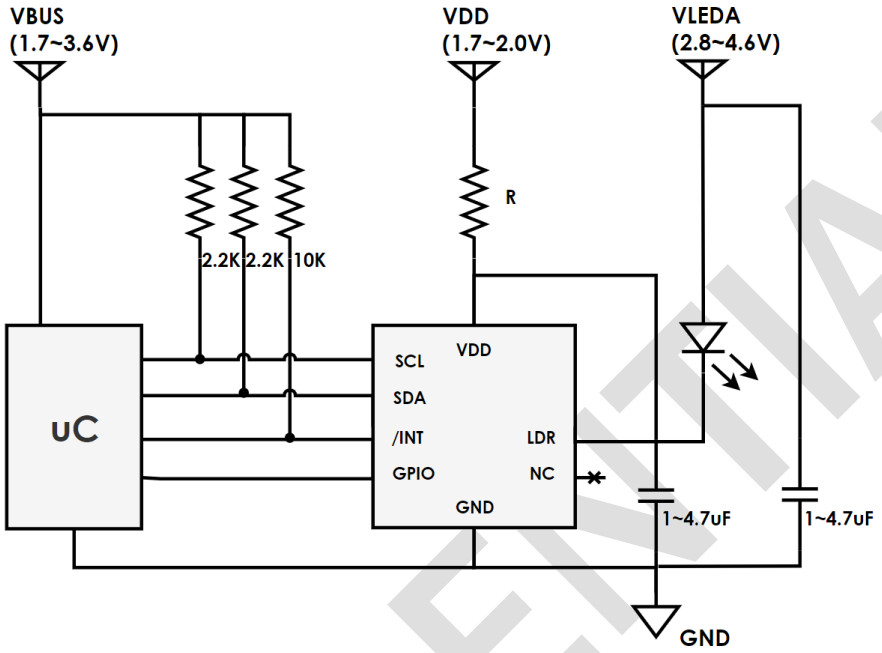
9. PROXIMITY RESPONSE CHARTS





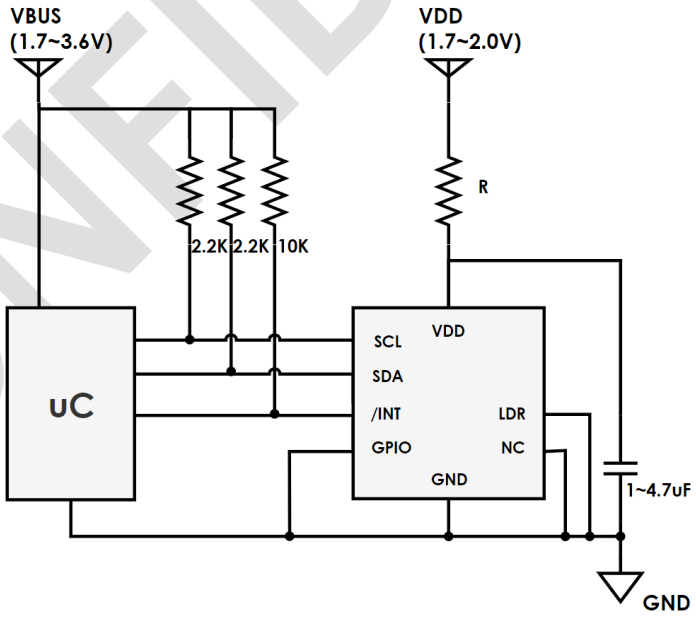
10. APPLICATION NOTE

ALS+PS



STK37660 Typical Application Circuit with Independent VDD and VLED Supply Voltage

Only ALS



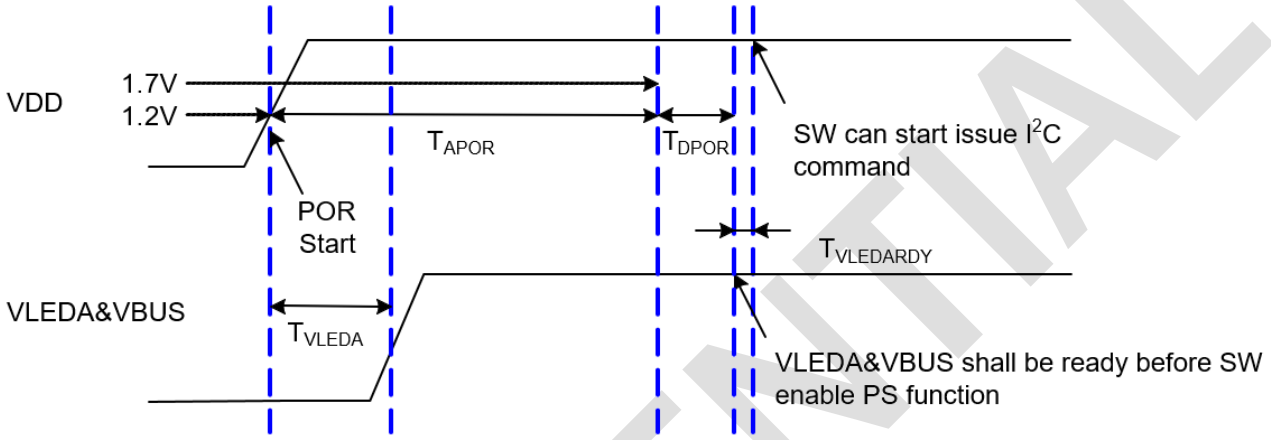
STK37660 typical application circuit2.

10.1 Power Noise Consideration

It is suggested that IC power and V_{LED} comes from individual source to get the best performance of STK37660 and an R/C low pass filter is also suggested to be added in the V_{DD} path of STK37660 to reduce the switching noise from whole system. The recommended R value is 22 Ohm.

10.2 Power ON Sequence

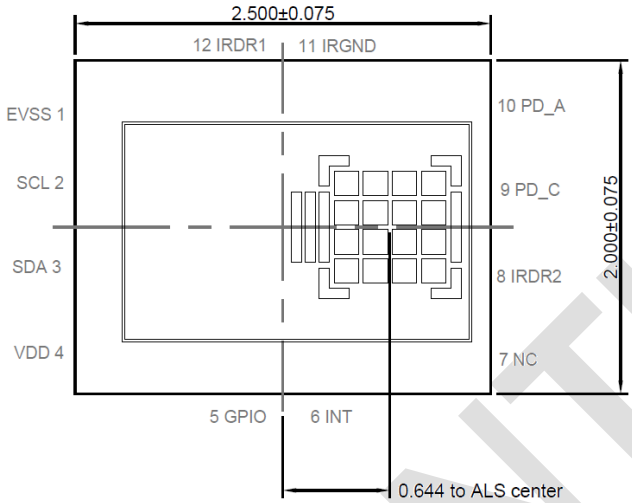
The **T_{APOR}** is must over 30ms (VDD is recommended first), and suggested that **T_{VLEDA}** ≥ 0.
VDD variation peak=100mV (+/-50mV).
VLEDA variation peak=200mV (+/-100mV).



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{APOR}	Power on reset procedure start once VDD exceed 1.2V.	30			ms
T_{VLEDA}	VLEDA & VBUS turn on time related to VDD.	≥0, and shall meet $T_{VLEDARDY}$			ms
T_{DPOR}	Logic circuit initialization timing and VDD shall exceed 1.7V.	5			ms
$T_{VLEDARDY}$	VLED & VBUS ready before SW enable PS function.	0			ms

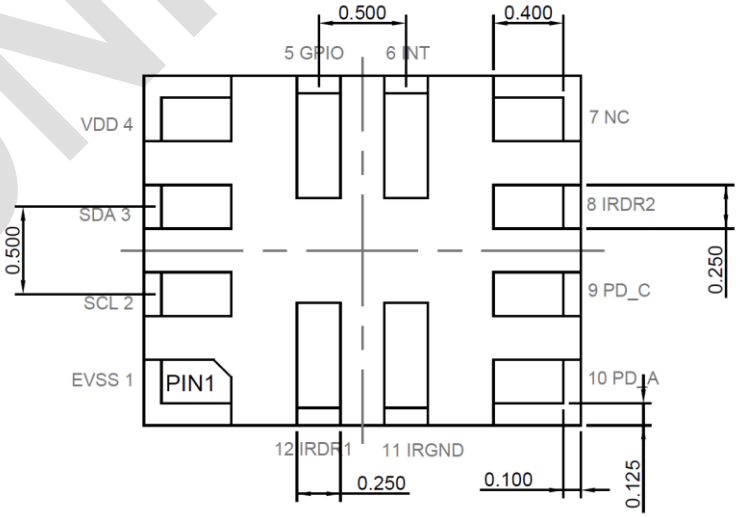
11. PACKAGE OUTLINE

Top View



Side View

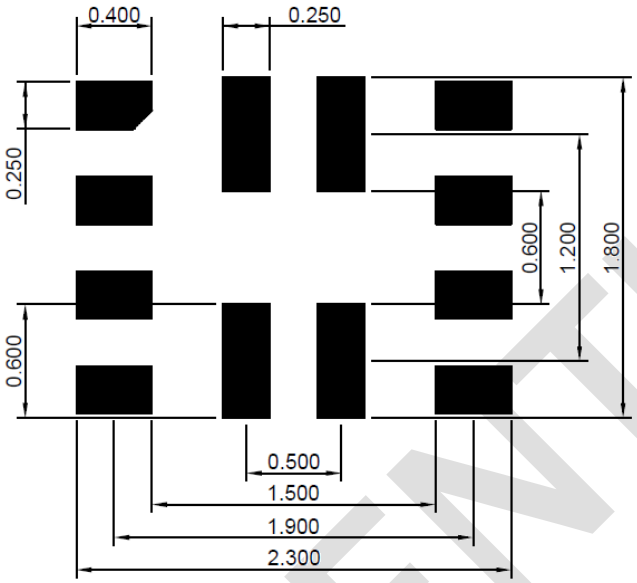
Bottom View



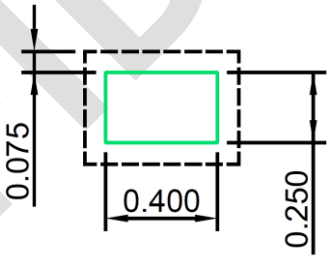
PCB Pad Layout and Solder Mask Define Recommendation

Suggested PCB pad layout guidelines are shown below.

PCB Pad Layout



Solder Mask Define

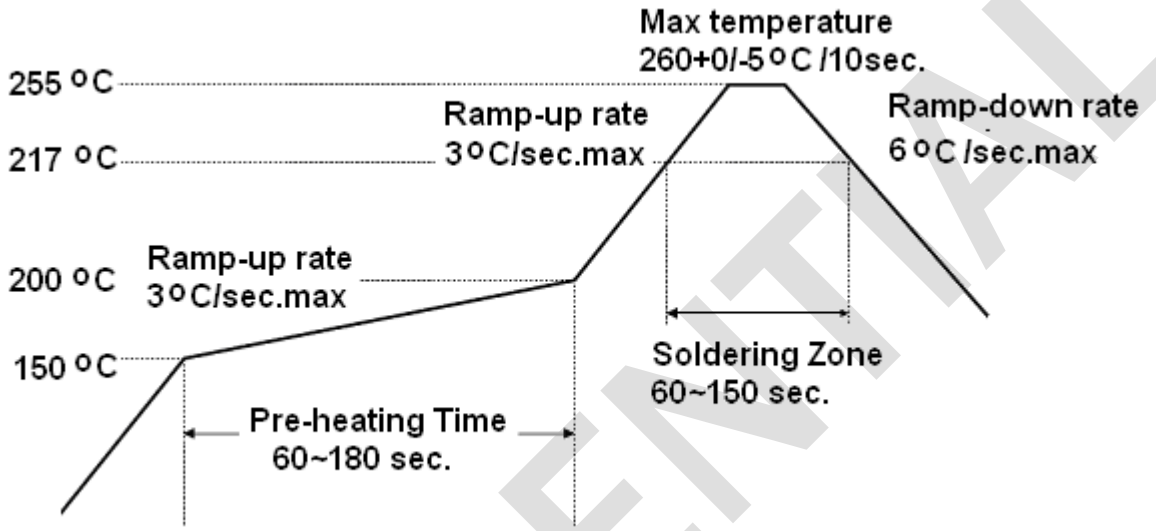


Notes: all linear dimensions are in mm.

12. SOLDERING INFORMATION

12.1 Soldering Condition

0. Pb-free solder temperature profile



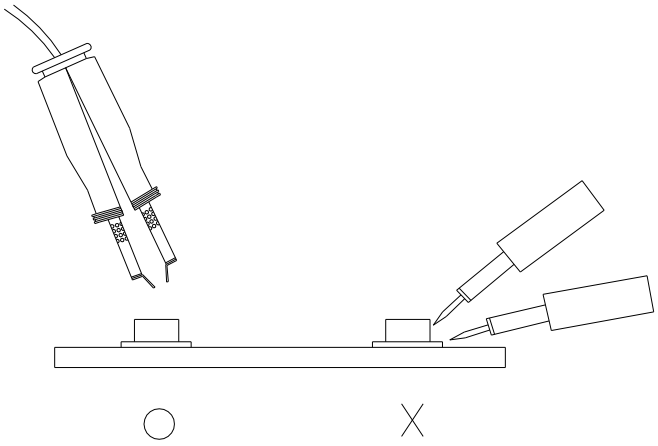
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the Ics during heating.
4. After soldering, do not warp the circuit board.

12.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350°C for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

12.3 Repairing

Repair should not be done after the Ics have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the Ics will or will not be damaged by repairing.



13. STORAGE INFORMATION

13.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

13.2 Treatment After Unsealed

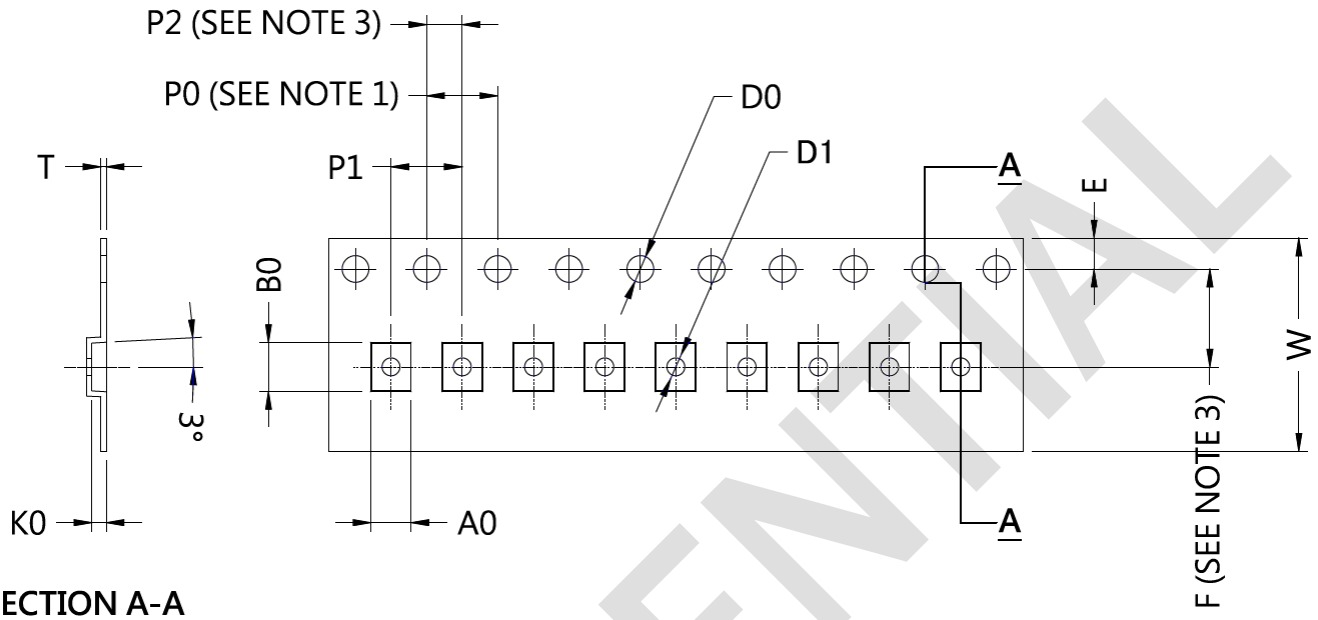
1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

14. TAPE AND REEL DIMENSION



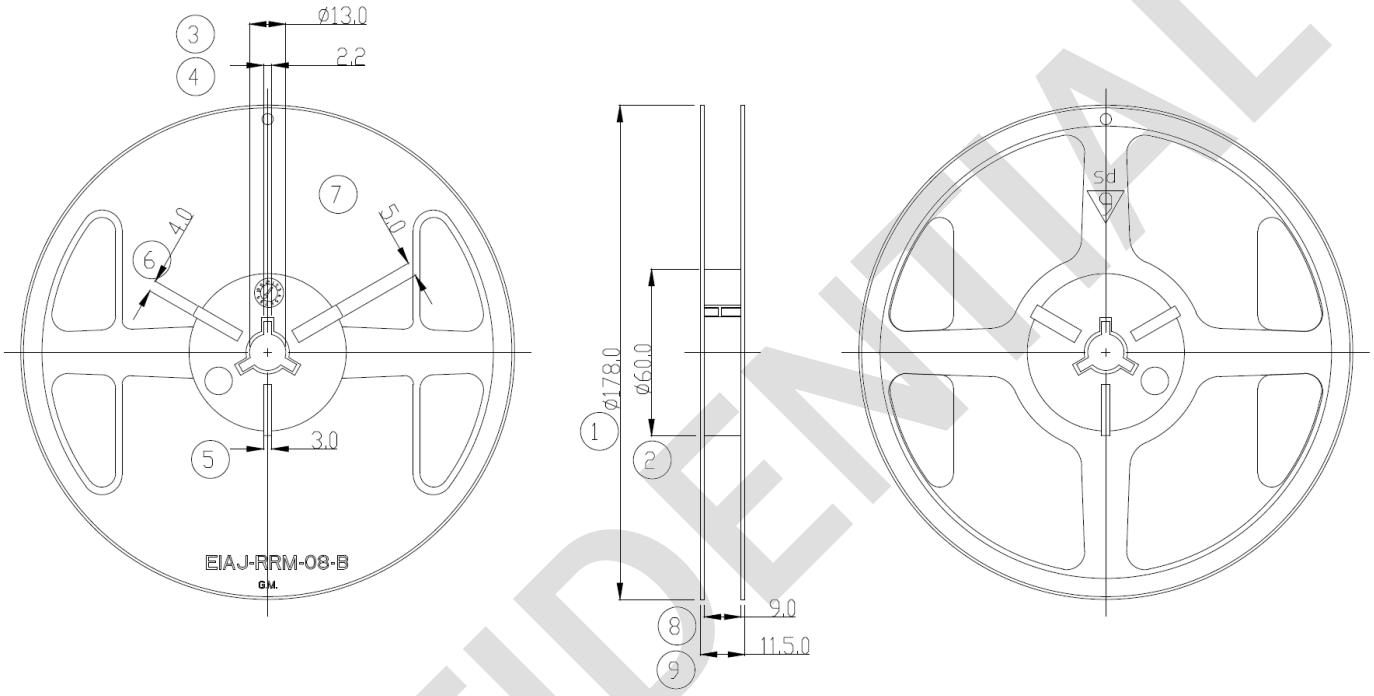
SECTION A-A

Item	Specification	Tol. (+/-)	Item	Specification	Tol. (+/-)
W	8.00	±0.30	A0	2.20	±0.05
E	1.75	±0.10	B0	2.70	±0.05
F	3.50	±0.05	K0	0.80	±0.05
D0	1.50	+0.1/-0.0	T	0.23	±0.05
D1	1.00	MIN			
P0	4.00	±0.10			
P1	4.00	±0.10			
P2	2.00	±0.05			

1.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSTION RELATIVE TO SPROCKET HOLE MEASURED AS TURE POSTION OF POCKET, NOT POCKET HOLE

Notes: all linear dimensions are in mm.

Width	1	2	3	4	5	6	7	8	9
7″	178±1	60±0.5	13±0.5	2.2±0.5	$3^{+0.5}_{-0}$	$4^{+0.5}_{-0}$	$5^{+0.5}_{-0}$	9± 0.5	11.5±0.5



Notes: all linear dimensions are in mm.

Revision History

Date	Version	Modified Items
2020/06/19	1.0	Initial release.
2020/12/07	1.1	1.Add ALS lux/code info. 2.Add ALS FOV response
2021/01/13	1.2	1.Add application circuit2
2021/02/22	1.3	1.Add optical characteristics info.
2021/07/26	1.4	1.Add Electrical and Optical Characteristics info.
2021/07/30	1.41	1.Modify Optical Characteristics info."White LED 3000K →5000K "

单击下面可查看定价，库存，交付和生命周期等信息

>>Sensortek(昇佳電子)