

**Low Consumption Current High PSRR
300mA CMOS Voltage Regulator**

S-LR6230 Series

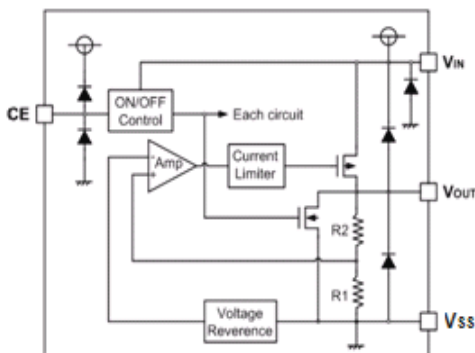
■ INTRODUCTION

The S-LR6230 series are a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection, low power consumption and low dropout voltage, which can prolong battery life in portable electronics. The S-LR6230 series work with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications. The S-LR6230 series consume less than 0.1uA in shutdown mode and have fast turn-on time less than 50us. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

■ APPLICATIONS

- Cellular and Smart Phones
- Laptop, Palmtops and PDA
- Digital Still and Video Cameras

■ BLOCK DIAGRAM



■ FEATURES

- Low Dropout Voltage: 150mV@150mA
- Low Quiescent Current: 5µA
- High Ripple Rejection: 65dB@1kHz
- Excellent Line and Load Transient Response
- Operating Voltage: 2.0V~7.0V
- Output Voltage: 1.2 ~ 5.0V
- High Accuracy: $\pm 2/\pm 1$ (Typ.)
- Built-in Current Limiter, Short-Circuit Protection
- TTL- Logic-Controlled Shutdown Input
- S-Prefix for Automotive And Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- MP3, MP4 Player
- Radio control systems
- Battery-Powered Equipment

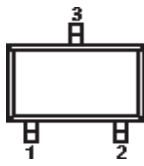
■ ORDER INFORMATION

S-LR6230①②③④⑤

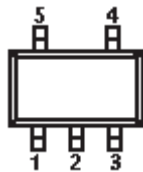
DESIGNATOR	SYMBOL	DESCRIPTION
①	A	Standard
	B	With Shutdown Function
②③	Integer	Output Voltage e.g.1.8V=②:1, ③:8
④	M/MA/MC/MY	Package:SOT-23-3/5
	P/PT	Package:SOT-89-3
	F	Package:DFN1×1-4
⑤	-	2% Accuracy
	1	1% Accuracy

■ PIN CONFIGURATION

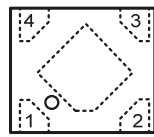
SOT-23-3



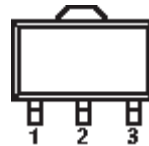
SOT-23-5



DFN1×1-4



SOT-89-3



PIN NUMBER						PIN NAME	FUNCTION
SOT-23-3			SOT-89-3				
M	MA	MC	MY	P	PT		
1	2	3	3	1	2	V _{SS}	Ground
2	1	2	1	3	1	V _{OUT}	Output
3	3	1	2	2	3	V _{IN}	Power input

SOT-23-5

PIN NUMBER	SYMBOL	FUNCTION
1	V _{IN}	Power Input Pin
2	V _{SS}	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V _{OUT}	Output Pin

DFN1×1-4

PIN NUMBER	SYMBOL	FUNCTION
F		
1	V _{OUT}	Output Pin
2	V _{SS}	Ground
3	CE	Chip Enable Pin
4	V _{IN}	Power Input Pin

■ ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNITS	
Input Voltage	V _{IN}	V _{SS} -0.3~V _{SS} +8	V	
Output Current	I _{OUT}	600	mA	
Output Voltage	V _{OUT}	V _{SS} -0.3~V _{IN} +0.3	V	
Power Dissipation	SOT-23	Pd	300	mW
	DFN1X1-4	Pd	400	mW
	SOT-89	Pd	500	mW
Operating Temperature	T _{opr}	-40~+125	°C	
Storage Temperature	T _{stg}	-40~+150	°C	
Soldering Temperature & Time	T _{solder}	260°C, 10s		
ESD rating ⁽¹⁾	Human Body Model -(HBM)	5000	V	

(1) ESD testing is performed according to the respective AEC-Q100 standard.

■ ELECTRICAL CHARACTERISTICS

S-LR6230 Series (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage ⁽²⁾	V _{OUT(E)} ⁽³⁾	I _{OUT} =1mA	V _{OUT} *0.98	V _{OUT}	V _{OUT} *1.02	V
Supply Current	I _{SS}	I _{OUT} =0		5	10	μA
Standby Current	I _{STBY}	CE = V _{SS}			0.1	μA
Output Current	I _{OUT}	—	300			mA
Dropout Voltage ⁽⁴⁾	V _{dif}	I _{OUT} =150mA V _{OUT} ≥3.0V		150		mV
Load Regulation	ΔV _{OUT}	V _{IN} = V _{OUT} +1V, 1mA≤I _{OUT} ≤100mA		10		mV
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I _{OUT} =10mA V _{OUT} +1V≤V _{IN} ≤6V		0.01	0.2	%/V
Output Voltage Temperature Characteristics	$\frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$	I _{OUT} =10mA -40≤T≤+85		100		ppm
Current Limit	I _{LIM}		500			mA
Short Current	I _{Short}	V _{OUT} =V _{SS}		50		mA
Input Voltage	V _{IN}	—	2.0		7.0	V
Power Supply Rejection Rate	1kHz	PSRR	I _{OUT} =50mA	65		dB
	10kHz			50		
CE "High" Voltage	V _{CE} "H"		1.5		V _{IN}	V
CE "Low" Voltage	V _{CE} "L"				0.3	V

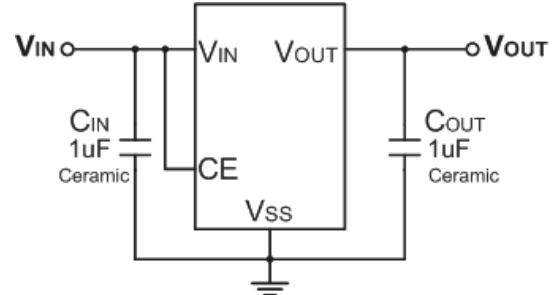
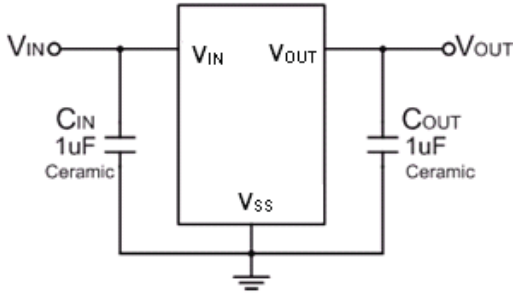
NOTE:

 (2) V_{OUT}: Specified Output Voltage.

 (3) V_{OUT(E)} : Effective Output Voltage (I.e. The Output Voltage When V_{IN} = (V_{OUT} +1.0V) And Maintain A Certain I_{OUT} Value).

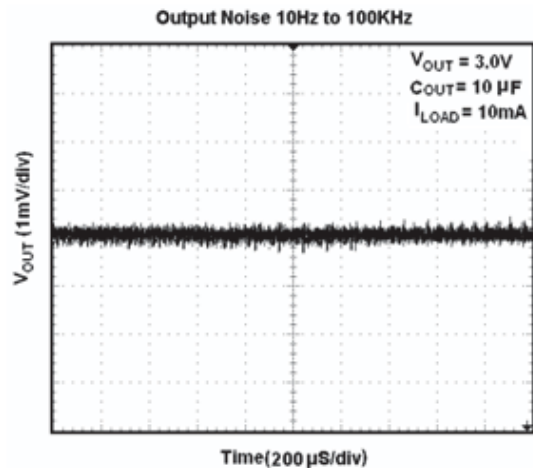
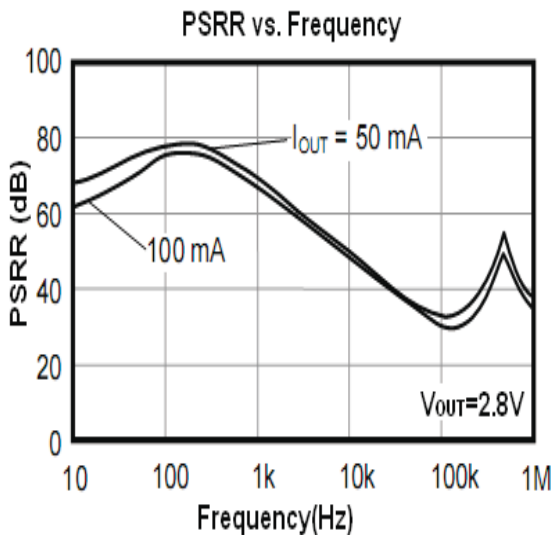
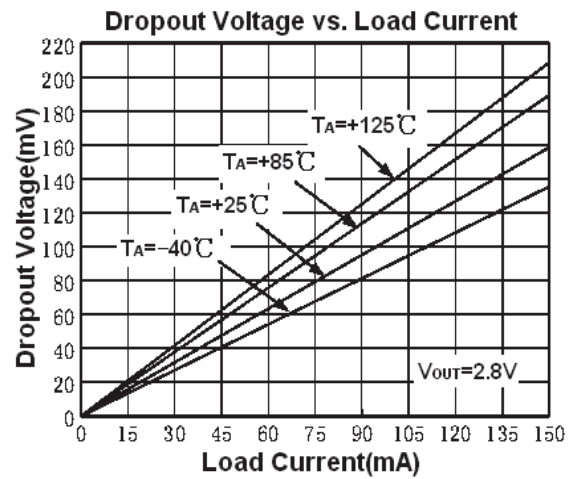
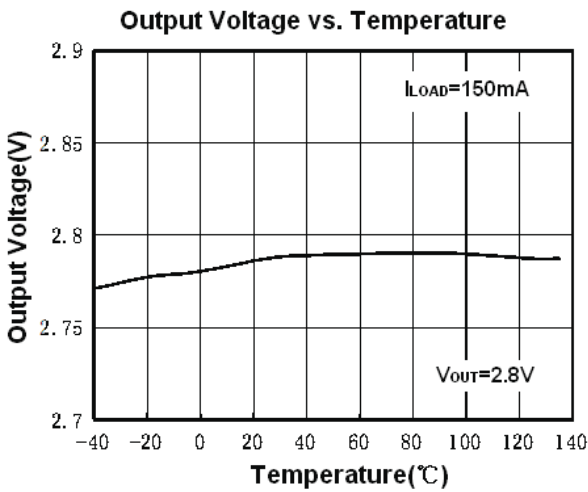
(4) V_{dif} : The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

■ TYPICAL APPLICATION



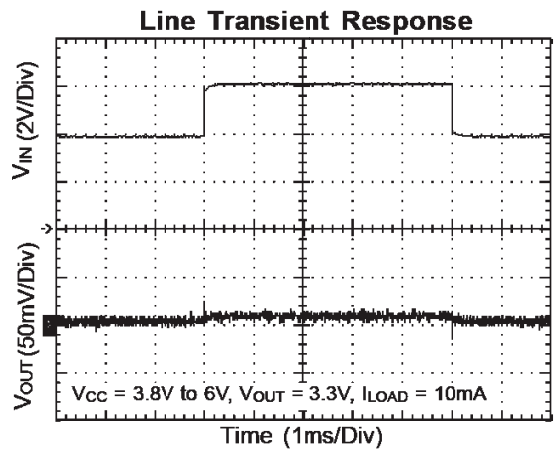
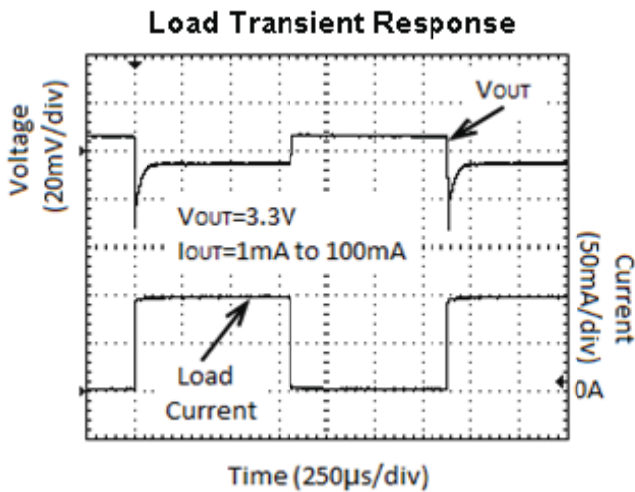
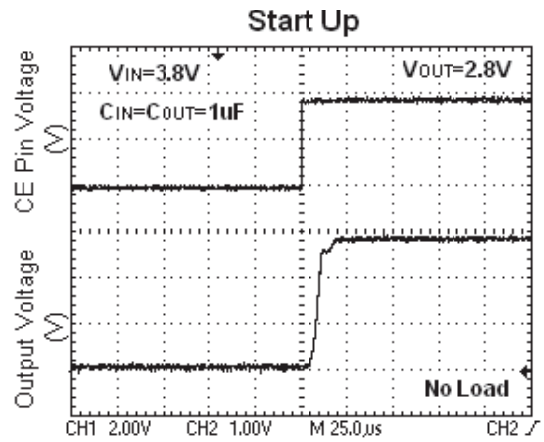
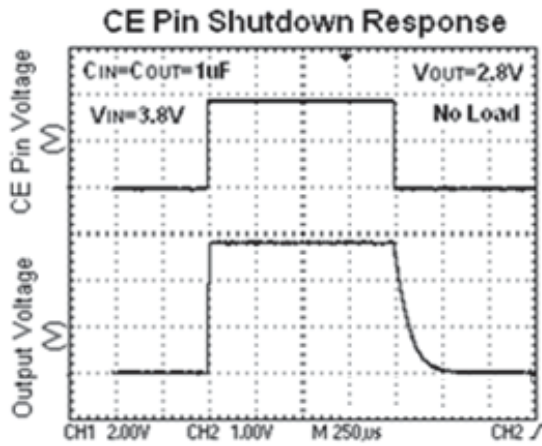
■ TYPICAL PERFORMANCE CHARACTERISTICS

($V_{CE}=V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified)



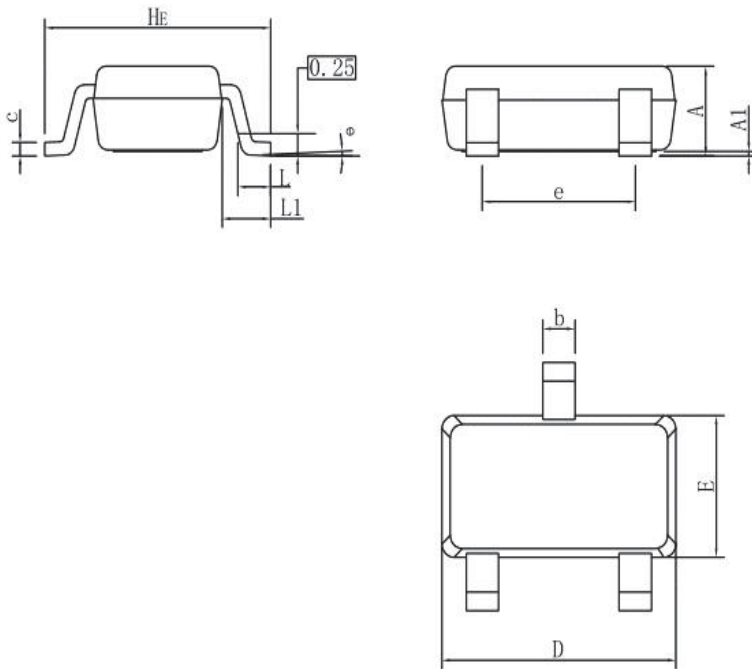
■ TYPICAL PERFORMANCE CHARACTERISTICS

($V_{CE}=V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified)



■ PACKAGING INFORMATION

● SOT-23-3 PACKAGE OUTLINE DIMENSIONS

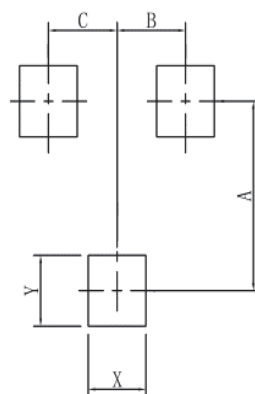


DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°
All Dimensions in mm			

GENERAL NOTES

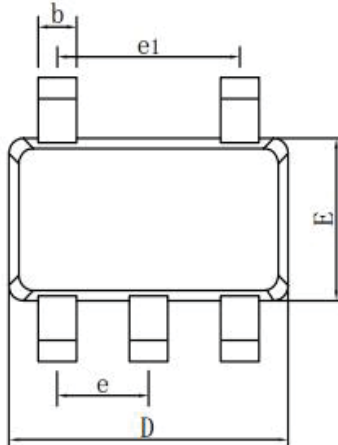
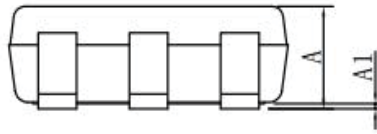
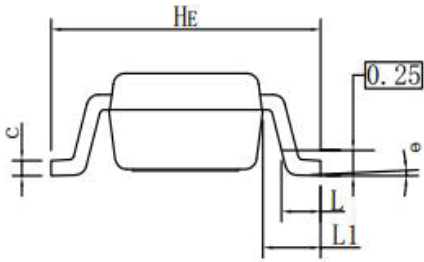
- 1.Top package surface finish Ra0.4±0.2um
- 2.Bottom package surface finish Ra0.7±0.2um
- 3.Side package surface finish Ra0.4±0.2um

SOLDERING FOOTPRINT



DIM	(mm)
X	0.80
Y	0.90
A	2.40
B	0.95
C	0.95

• SOT-23-5 PACKAGE OUTLINE DIMENSIONS

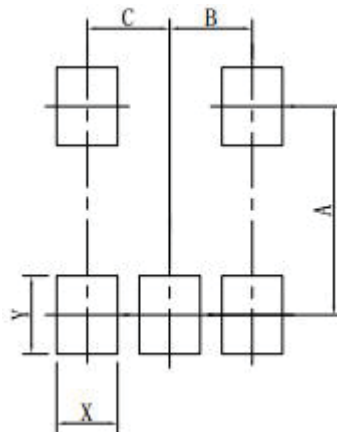


DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	0.85	0.95	1.05
e1	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°

GENERAL NOTES

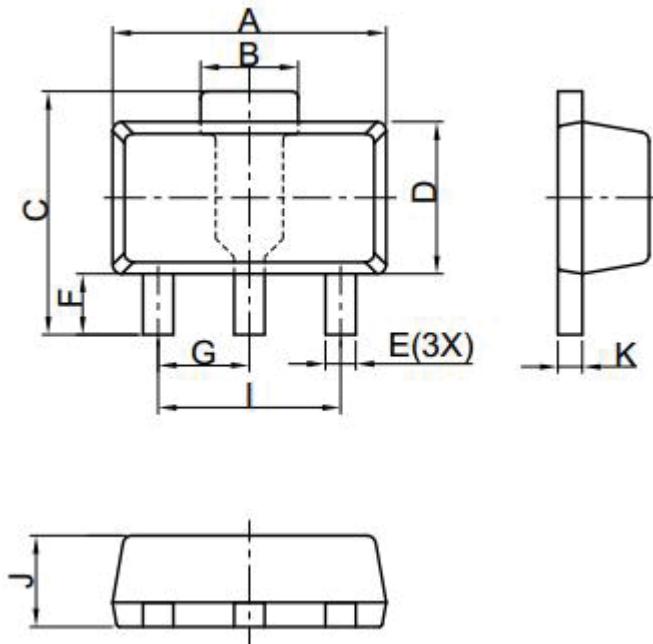
- 1.Top package surface finish Ra0.4±0.2um
- 2.Bottom package surface finish Ra0.7±0.2um
- 3.Side package surface finish Ra0.4±0.2um

SOLDERING FOOTPRINT



DIM	(mm)
X	0.70
Y	0.90
A	2.40
B	0.95
C	0.95

● SOT-89-3 PACKAGE OUTLINE DIMENSIONS

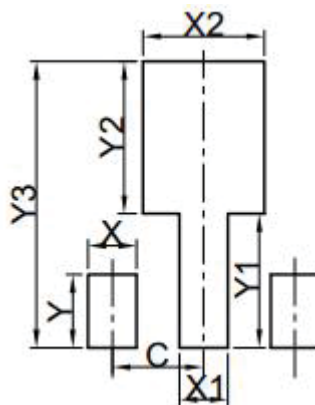


DIM	MIN	NOR	MAX
A	4.40	4.50	4.60
B	1.40	1.60	1.80
C	3.90	4.00	4.25
D	2.40	2.50	2.60
E	0.40	0.50	0.58
F	0.90	1.00	1.20
G	1.50 BSC		
I	3.00 BSC		
J	1.40	1.50	1.60
K	0.34	0.40	0.50
All Dimensions in mm			

GENERAL NOTES

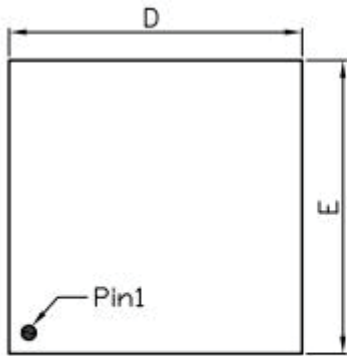
1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

SOLDERING FOOTPRINT

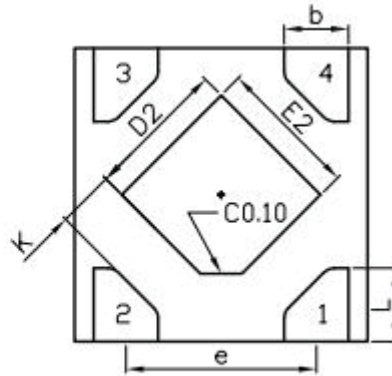


DIM	(mm)
X	0.80
Y	1.20
X1	0.80
Y1	2.20
X2	2.00
Y2	2.50
C	1.50
Y3	4.70

● DFN1×1-4 PACKAGE OUTLINE DIMENSIONS

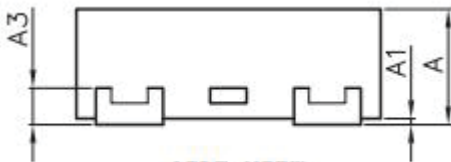


TOP VIEW



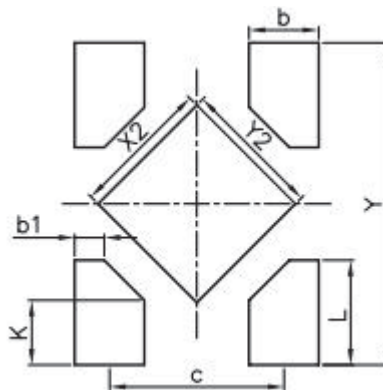
BOTTOM VIEW

DFN1010			
DIM	MIN	NOR	MAX
A	0.34	0.37	0.40
A1	0.01	0.02	0.05
b	0.17	0.22	0.25
L	0.20	0.25	0.30
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
e	0.65		
A3	0.127REF.		
K	0.15	-	-
All Dimensions in mm			



SIDE VIEW

SOLDERING FOOTPRINT



DFN1010	
DIM	(mm)
X2	0.52
Y2	0.52
L	0.39
Y	1.20
K	0.24
b	0.26
c	0.65
b1	0.11

■ DEVICE MARKING AND REEL SPECTION

Device ⁽⁵⁾	Package	Output Voltage ⁽⁶⁾	Marking ⁽⁷⁾⁽⁸⁾	Shipping
S-LR6230AxxM	SOT-23-3	1.2V~5.0V	6AX	3K/Reel
S-LR6230AxxMA	SOT-23-3	1.2V~5.0V	6MX	3K/Reel
S-LR6230AxxMC	SOT-23-3	1.2V~5.0V	6CX	3K/Reel
S-LR6230AxxMY	SOT-23-3	1.2V~5.0V	6YX	3K/Reel
S-LR6230BxxM	SOT-23-5	1.2V~5.0V	6BX	3K/Reel
S-LR6230AxxP	SOT-23-5	1.2V~5.0V	6DX	1K/Reel
S-LR6230AxxPT	SOT-23-5	1.2V~5.0V	6TX	1K/Reel
S-LR6230BxxF	DFN1x1-4	1.2V~5.0V	KX	10k/Reel

(5) : "xx" represents output voltage, eg "18" express that the output voltage is 1.8V

(6) : Output voltage varies from 1.2V to 5.0V, 0.1V an interval

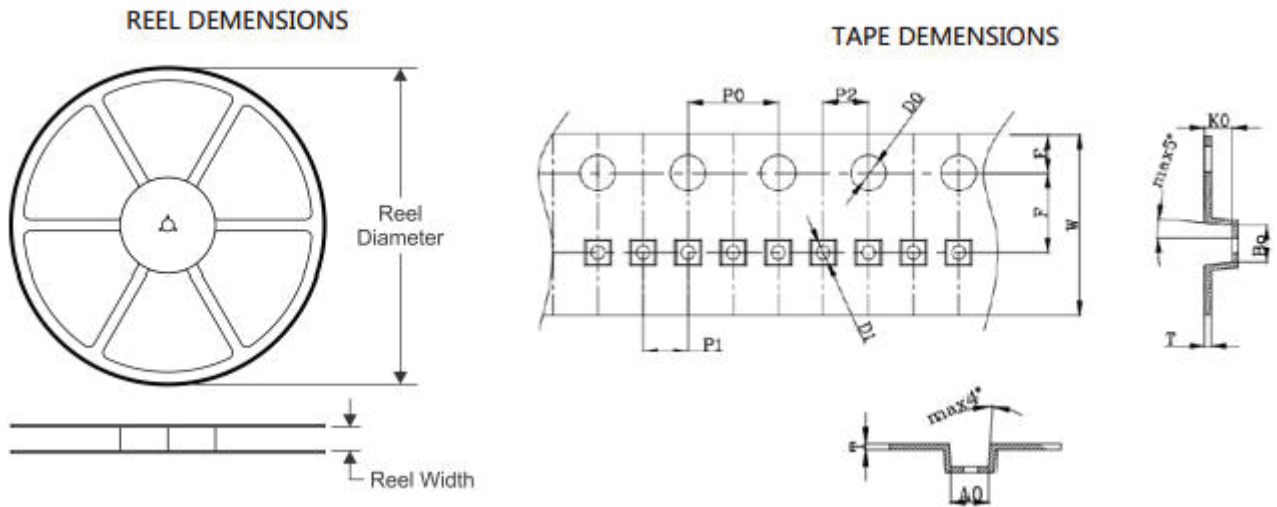
(7) : "X" : represents output voltage code, change as figure below

(8) : There are additional marking , which relates to the date code ,not list above.

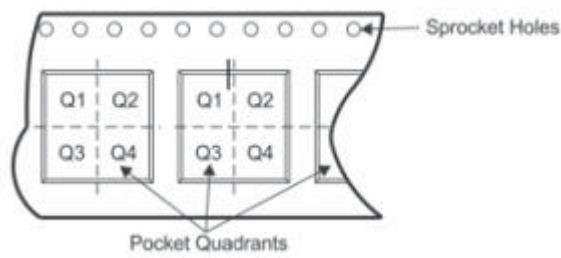
For Package DFN1x1-4,one letter(month code), for SOT-23-3, SOT-23-5, SOT-89-3,
two letters(Year and week)

Voltage	1.0	1.2	1.5	1.8	2.5	2.7	2.8	3.0	3.3	3.6	4.0	4.2	5.0
Symble	D	E	F	G	H	I	J	K	L	M	N	T	P

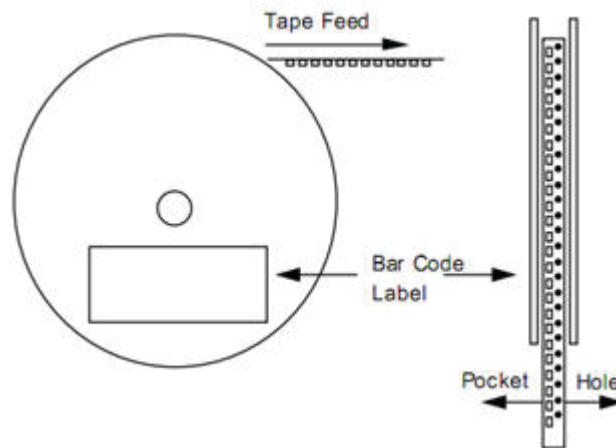
■ TAPE AND REEL INFORMATION



PIN ORIENTATION



ROLLING ORIENTATION



Device	Package	Reel Diameter (mm)	Reel width (mm)	P0 (mm)	P1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	PIN1
S-LR6230AxxM	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
S-LR6230AxxMC	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
S-LR6230AxxMY	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
S-LR6230BxxM	SOT-23-5	178±1	9.6±1.2	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	12.0 ^{+0.3} _{-0.1}	Q3
S-LR6230AxxP	SOT-89-3	178±1	13.0 ⁺¹ _{-0.5}	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	12.0 ^{+0.3} _{-0.1}	NA
S-LR6230AxxPT	SOT-89-3	178±1	13.0 ⁺¹ _{-0.5}	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	12.0 ^{+0.3} _{-0.1}	NA
S-LR6230BxxF	DFN1X1-4	178±1	9.6±1.2	4.00±0.1	2.00±0.05	1.16±0.05	1.16±0.05	0.5±0.05	8.0±0.1	Q3

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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