700V SolidGaN with Integrated Current Sense

1. Features

- 100mΩ E-Mode GaN with Integrated Gate Driver
- 700V Continuous, 800V Transient Voltage Rating
- Wide 9V to 80V VCC Range Eliminates Extra LDO
- 115uA Quiescent Current with Auto Standby Mode
- Integrated Loss-less Current Sensing
- Programmable Switch Turn-On Slew Rate
- High dv/dt Immunity up to 200V/ns
- Zero Reverse Recovery Charge
- High Frequency Operation Up to 2MHz
- Fast Propagation Delay (25ns Typical)
- Integrated 5V LDO for supplying Digital Isolator
- Built-In UVLO, OCP, OTP Protection
- QFN 6mmx8mm Package, 0.85mm Low Profile

2. Applications

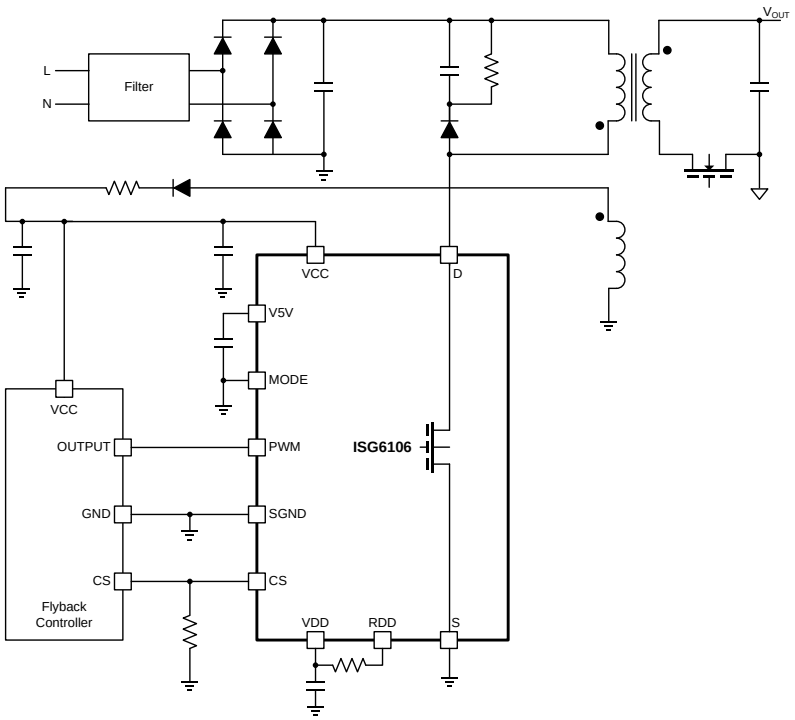
- AC-DC, DC-DC, DC-AC Power Supply
- PFC, QR Flyback, ACF, Half Bridge, Full Bridge
- PD Adaptor, LED Lighting, Solar Micro Inverter
- Server and Telecom Power Supply

3. Description

The ISG6106 SolidGaN IC integrates a 700V E-Mode GaN FET with a high-voltage linear regulator, a smart gate driver, and loss-less current sense circuitry. The high-voltage linear regulator with up to 80V input capability eliminates the need for external LDO and maintains tightly regulated 6.5V gate drive voltage. The integrated smart gate driver offers programmable 1st-stage turn-on speed for slew rate control and delayed 2nd-stage turn-on enhancement, thereby achieving high frequency, high efficiency, and low EMI performance. The loss-less current sense circuit eliminates external current sense resistor and increases system efficiency. Additional features include 5V LDO supplying external digital isolators, UVLO, OCP, and OTP protection.

The high level of integration with high current sense accuracy and low quiescent current makes the ISG6106 suitable for a simple to use, low component count, and high efficiency application solution.

4. Typical Application



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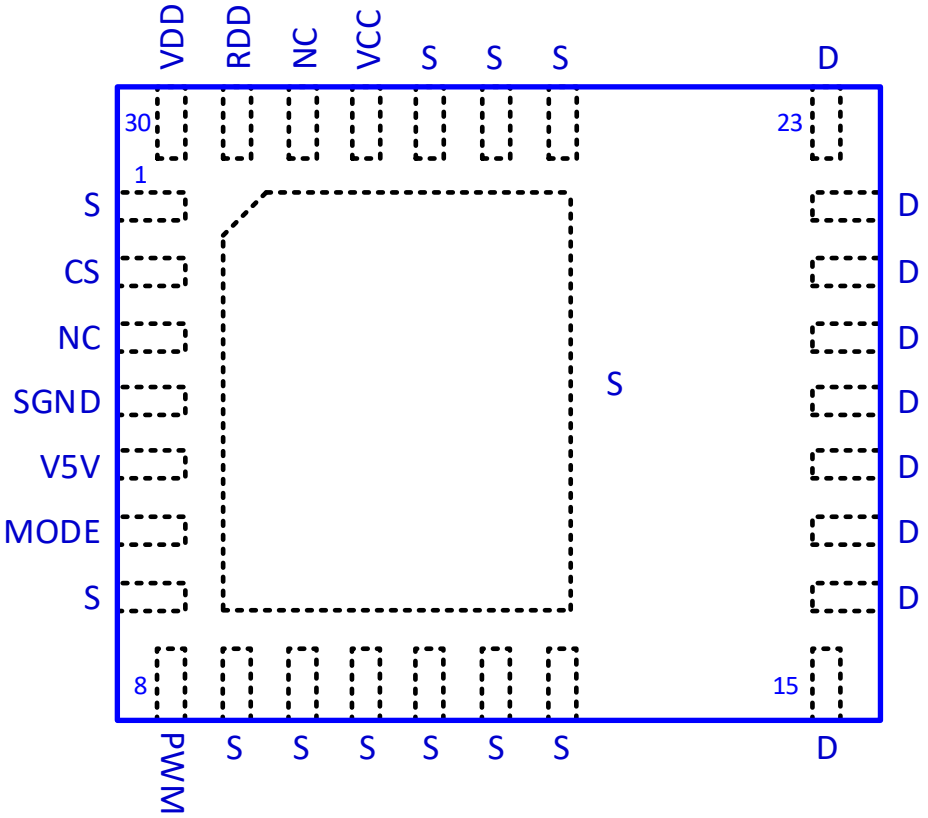
5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-03-15	Final datasheet release

6. Pin Configuration and Functions



30-Lead QFN (6mm x 8mm) Package – Top View

Pin Number	Pin Name	Description
1, 7, 9-14, 24-26, PAD	S	Source of Power GaN FET. Solder the exposed source pad directly to the ground plane.
2	CS	Power GaN FET Current Sense Output. This pin sources a current proportional to the GaN FET drain current. Connect a resistor from this pin to SGND to set current sense voltage level.
3, 28	NC	No Internal Connection.
4	SGND	Signal Ground. Must tie to the source pad directly with Kelvin connection.
5	V5V	5V LDO Output. Locally bypass this pin to SGND with a ceramic capacitor.
6	MODE	Operating Mode Selection. Tie to V5V for normal mode and SGND for auto standby mode.
8	PWM	PWM Input.
15-23	D	Drain of Power GaN FET.
27	VCC	IC Supply Input. Locally bypass this pin to SGND with a ceramic capacitor.
29	RDD	Gate Driver Turn-On Strength Setting. Connect a resistor from this pin to VDD.
30	VDD	Gate Drive Supply LDO Output. Locally bypass this pin to SGND with a ceramic capacitor.

7. Absolute Maximum Ratings

All pins are referred to S pins, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Min	Max	Unit
Drain Voltage, Continuous	-7	700	V
Drain Voltage, Transient (1)		800	V
Drain Voltage, Pulsed (2)		750	V
Drain Current, Continuous (T_C = 100°C)		12	A
Drain Current, Pulsed (T_J = 25°C)		24	A
VCC Voltage	-0.3	80	V
PWM Voltage	-0.3	20	V
VDD Voltage	-0.3	7.5	V
RDD Voltage	-0.3	7.5	V
V5V Voltage	-0.3	6	V
MODE Voltage	-0.3	6	V
CS Voltage	-0.3	6	V
Operating Junction Temperature T_J	-55	150	˚C
Storage Temperature	-55	150	˚C

(1) $V_{DS(TRAN)}$ is intended for non-repetitive events, t_{PULSE} < 200us.

(2) $V_{DS(PULS)}$ is intended for repetitive events, t_{PULSE} < 100ns.

8. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 (3)	±1000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (4)	±2000	V

(3) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(4) JEDEC document JEP155 states that 250V CDM allows safe manufacturing with a standard ESD control process.

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
VCC Voltage	9	75	V
PWM Voltage	0	15	V
MODE Voltage	0	V5V	V
V5V External Load Current		10	mA
Operating Junction Temperature T_J	-40	125	˚C

10. Thermal Information

Symbol	Parameter	ISG6106QA	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	58	˚C/W
$R_{\theta JC(TOP)}$	Thermal Resistance, Junction to Case Top	20.4	˚C/W
$R_{\theta JC(BOT)}$	Thermal Resistance, Junction to Case Bottom	1.1	˚C/W

11. Electrical Characteristics

T_J = 25°C, VCC = 15V, C_{VDD} = 10nF, C_{V5V} = 10nF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
VCC Supply						
VCC UVLO rising threshold	V_{CC_UV+}	8	8.5	9	V	
VCC UVLO falling threshold	V_{CC_UV-}		7.4		V	
VCC standby current	I_{CC_STBY}		115		uA	MODE = 0V, PWM = 0V
VCC quiescent current	I_{CC_NORM}		0.33	0.5	mA	MODE = 5V, PWM = 0V
VCC operating current	I_{CC_SW}		3.0		mA	f_{SW} = 1MHz
Linear Regulators						
VDD regulation voltage	V_{DD}	6.25	6.5	6.75	V	
VDD UVLO rising threshold	V_{DD_UV+}		5.7		V	
VDD UVLO falling threshold	V_{DD_UV-}		5.4		V	
V5V regulation voltage	V_{5V}	4.5	5	5.5	V	
PWM Input						
Input logic high threshold	V_{PWM_HI}		2.7	3.5	V	Fig. 20
Input logic low threshold	V_{PWM_LO}	0.6	1.3		V	Fig. 20
Input logic hysteresis	V_{PWM_HYS}		1.4		V	
Current Sensing						
CS pin output current	I_{CS}	1.16	1.25	1.34	mA	PWM = 5V, I_{DS} = 6A, T_J = -40°C to 125°C
CS pin output offset	I_{CS_OS}		15		uA	PWM = 5V, I_{DS} = 0A
Protection						
CS over current threshold	V_{CS_OCP}	1.6	1.9	2.2	V	
OTP shutdown rising threshold (5)	T_{OTP}		165		°C	
OTP hysteresis (5)	T_{OTP_HYS}		60		°C	
Power GaN FET						
Drain-source leakage current	I_{DSS}		0.5	25	uA	V_{DS} = 700V, PWM = 0V
Drain-source resistance	$R_{DS(ON)}$		100	140	mΩ	PWM = 5V, I_{DS} = 1A
Source-drain reverse voltage	V_{SD}		3.8		V	PWM = 0V, I_{SD} = 6A
Output charge (5)	Q_{OSS}		36.6		nC	V_{DS} = 400V, PWM = 0V
Reverse recovery charge (5)	Q_{RR}		0		nC	
Output capacitance (5)	C_{OSS}		44.1		pF	V_{DS} = 400V, PWM = 0V
Effective output capacitance, energy related (5)	$C_{O(er)}$		68		pF	V_{DS} = 400V, PWM = 0V
Effective output capacitance, time related (5)	$C_{O(tr)}$		94		pF	V_{DS} = 400V, PWM = 0V

12. Switching Characteristics

T_J = 25°C, VCC = 15V, f_{SW} = 1MHz, C_{VDD} = 10nF, C_{V5V} = 10nF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Switching frequency (5)	f_{SW}			2	MHz	
Pulse width (5)	t_{PW}	30			ns	
Turn-on propagation delay (5)	t_{PD_ON}		25		ns	Fig. 20
Turn-off propagation delay (5)	t_{PD_OFF}		35		ns	Fig. 20
Drain rise time (5)	t_R		10		ns	Fig. 20
Drain fall time (5)	t_F		10		ns	Fig. 20
2nd-stage turn-on delay	t_{PU_DLY}		180		ns	Fig. 23
Time delay to enter standby mode	t_{STBY_DLY}		120		us	Fig. 24, PWM = 0V
CS pin delay (from I_{DS} to V_{CS}, at 10% rated current) (5)	t_{CS_DLY}		30		ns	di/dt = 40A/us, R_{CS} = 400Ω, C_{CS} = 25pF

(5) Not 100% tested and guaranteed by design.

13. Typical Characteristics

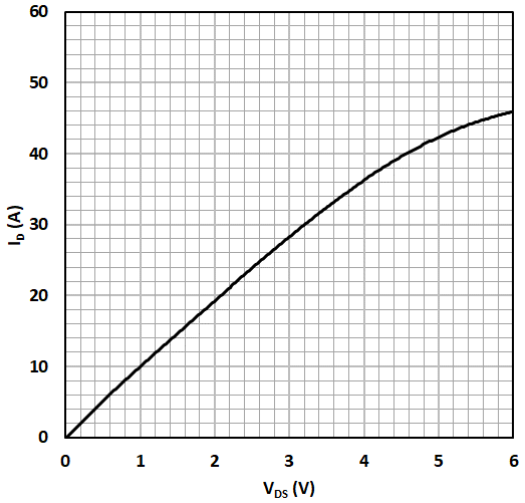


Fig. 1. Pulsed Drain Current vs. Drain Voltage, T_J = 25°C

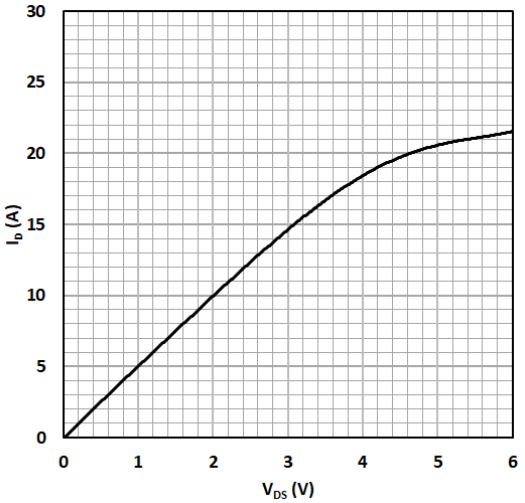


Fig. 2. Pulsed Drain Current vs Drain Voltage, T_J = 125°C

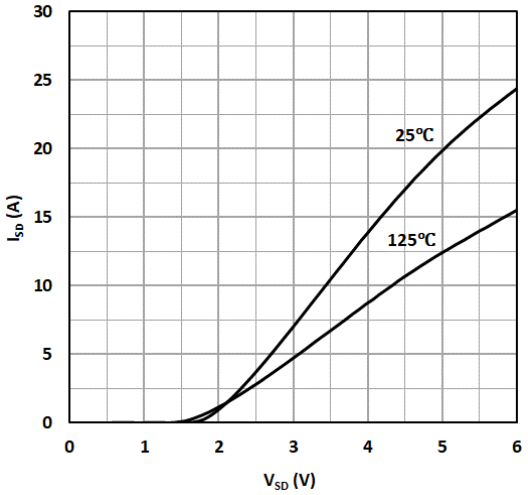


Fig. 3. Source-Drain Reverse Conduction Voltage

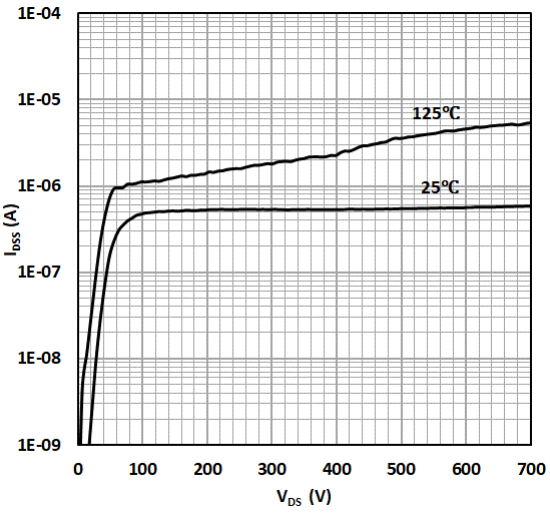


Fig. 4. Drain Leakage Current vs Drain Voltage

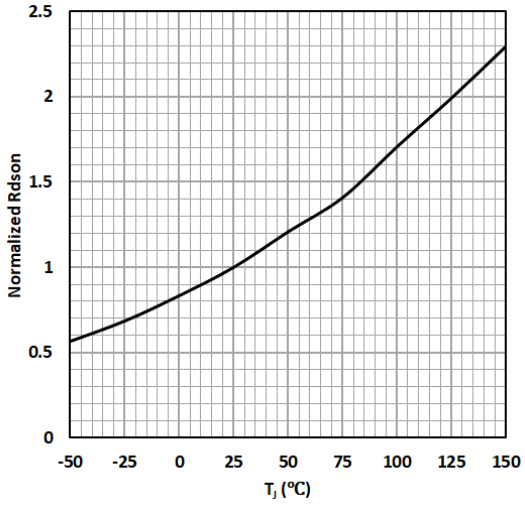


Fig. 5. Normalized $R_{DS(ON)}$ vs Temperature

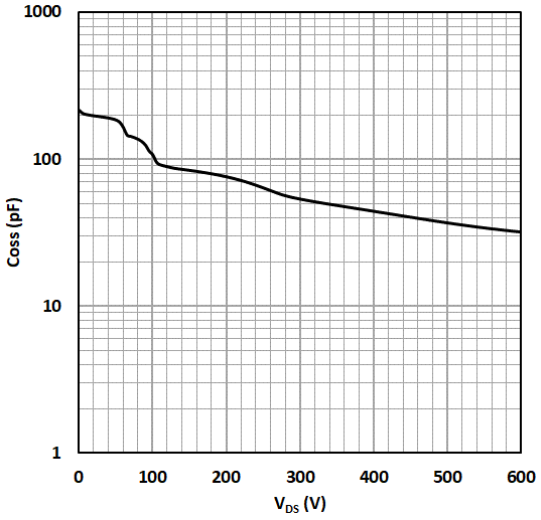


Fig. 6. Output Capacitance vs Drain Voltage

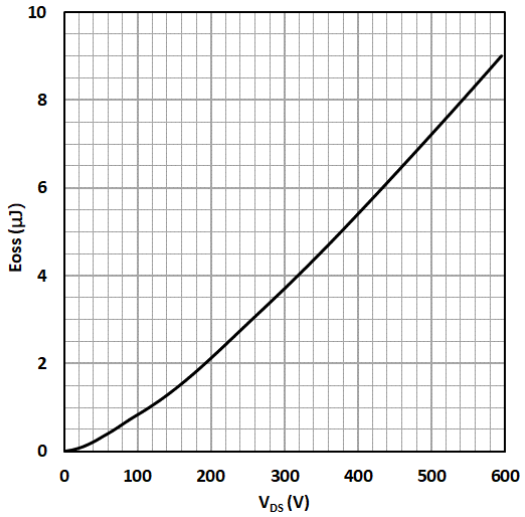


Fig. 7. Output Capacitance Stored Energy vs Drain Voltage

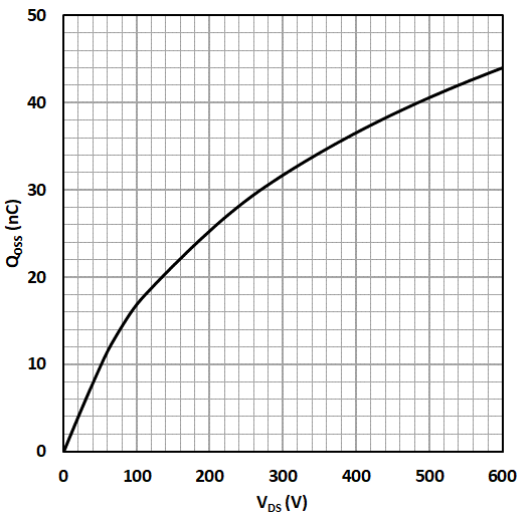


Fig. 8. Output Charge vs Drain Voltage

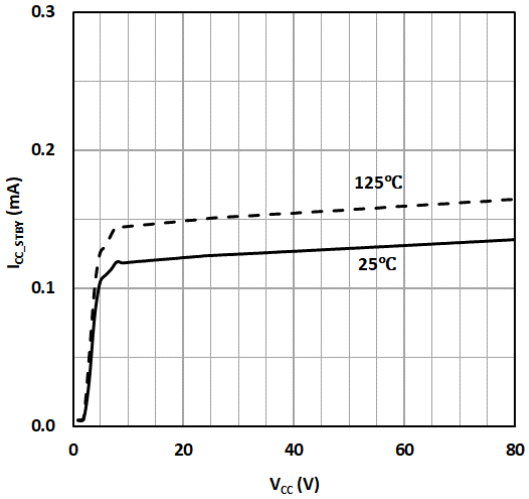


Fig. 9. VCC Standby Current vs VCC Voltage

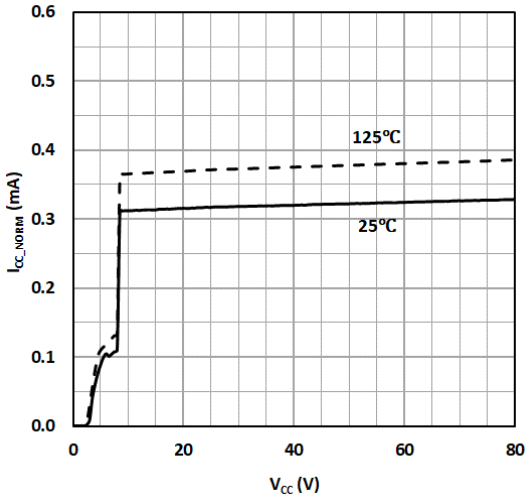


Fig. 10. VCC Quiescent Current vs VCC Voltage

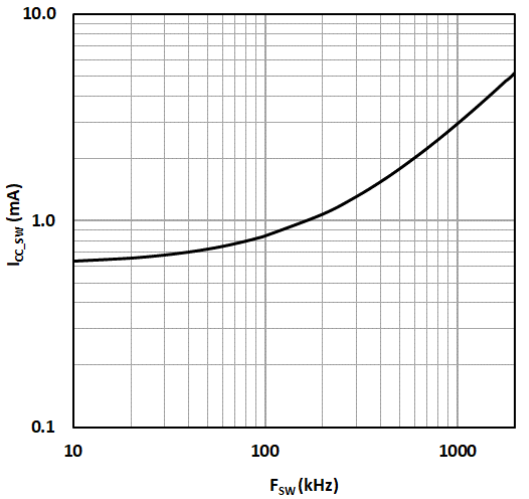


Fig. 11. VCC Operating Current vs Frequency, VCC = 15V

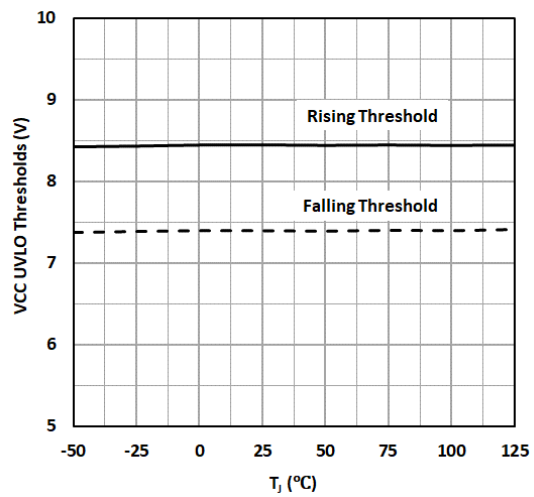


Fig. 12. VCC UVLO Thresholds vs Temperature

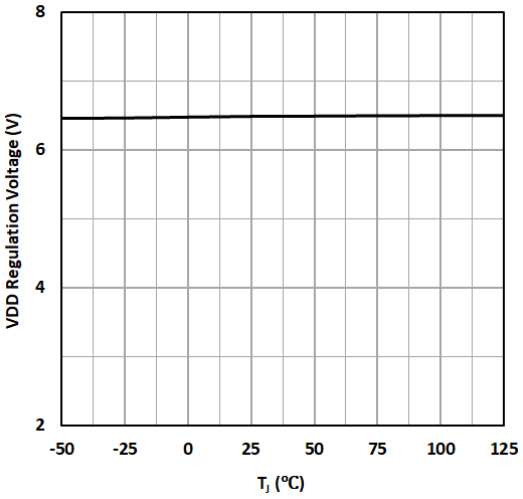


Fig. 13. VDD Regulation Voltage vs Temperature

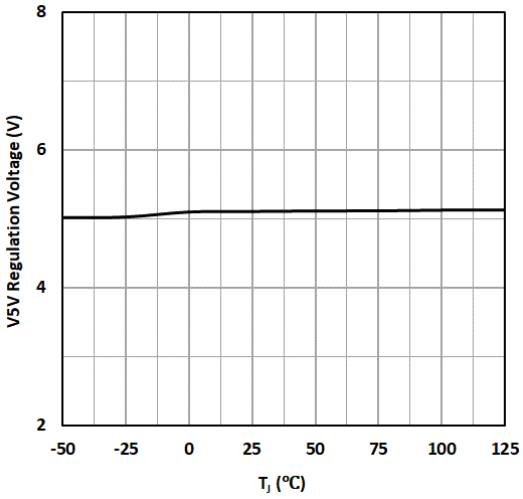


Fig. 14. V5V Regulation Voltage vs Temperature

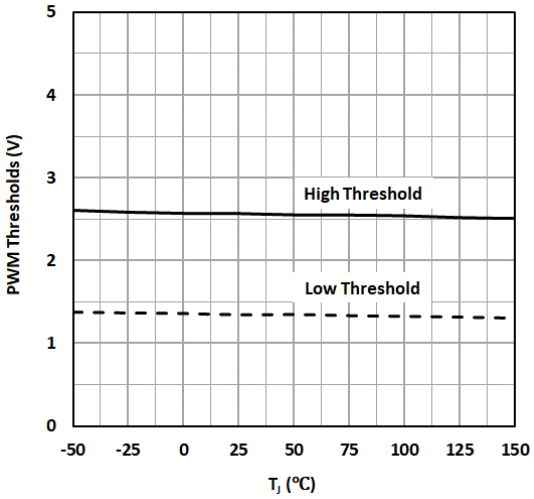


Fig. 15. PWM Input Logic Thresholds vs Temperature

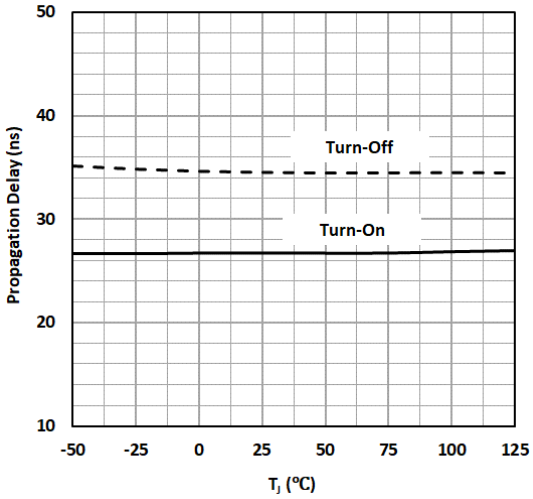


Fig. 16. Propagation Delay vs Temperature

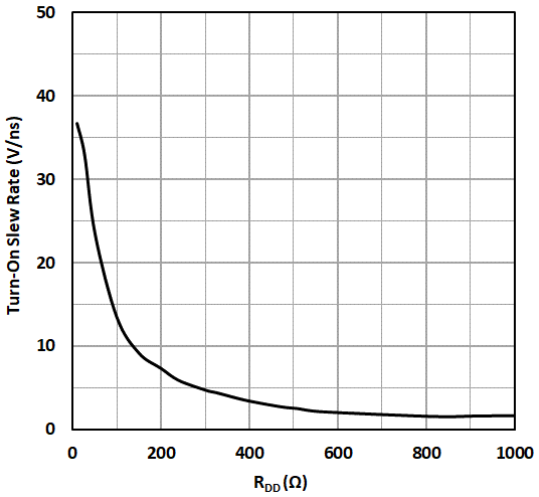


Fig. 17. Switch Slew Rate vs R_{DD} Resistor

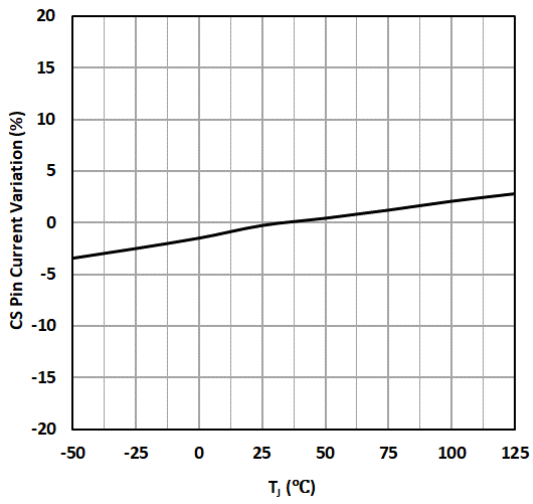


Fig. 18. CS Pin Current Variation vs Temperature

14. Block Diagram

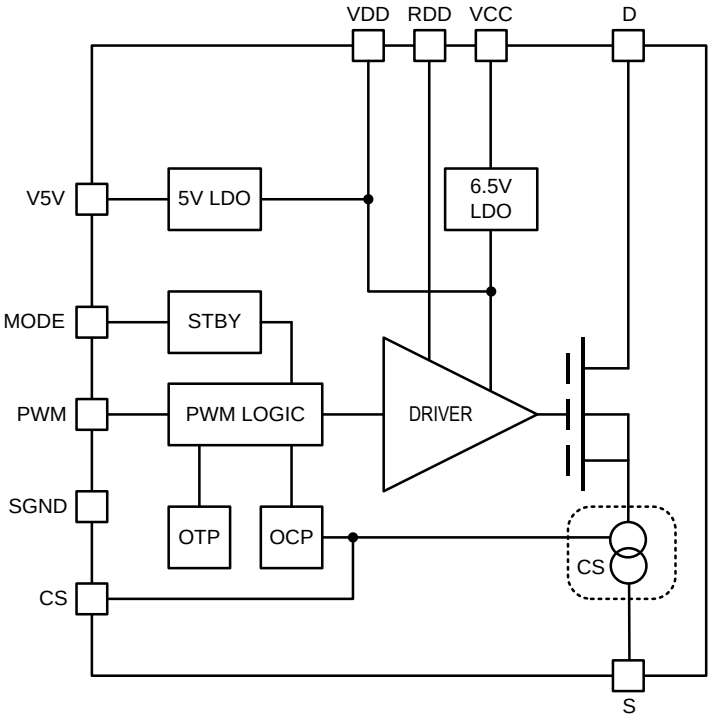


Fig. 19. Functional Block Diagram

15. Function Description

The ISG6106 is a high-performance SolidGaN IC integrating a 700V E-Mode GaN FET with a high-voltage linear regulator, a smart gate driver, and an accurate loss-less current sense circuit. The high-voltage linear regulator with up to 80V input capability eliminates the need for external voltage regulators and maintains tightly regulated 6.5V gate drive voltage for integrated GaN FET. The integrated smart gate driver provides a dual slew-rate gate driving scheme while adjusting the gate turn-on slew rate to achieve high frequency operation, high power efficiency, and low EMI performance. The loss-less current sense circuit eliminates external current sense resistors and increases system power efficiency. The ISG6106 provides an autonomous standby mode with a smooth transition and minimizes the quiescent current at no load condition. Additional features include 5V LDO supplying external digital isolators, UVLO, OCP, and OTP protection. Its operation is best understood by referring to the Functional Block Diagram, Fig. 19.

The front page shows a typical ISG6106 application circuit. The ISG6106 has output pins of drain, D, and source, S, of GaN FET and it operates based on the logic input signal of PWM pin. VDD and V5V pins which are outputs of the internal regulators must be connected to ground with a minimum of 10nF ceramic capacitor. A good local bypass is necessary to supply the high transient current required by GaN FET driving. VCC pin is connected to the external voltage source with a typical 0.1uF capacitor. To adjust the turn-on speed of GaN FET, a resistor is connected between VDD and RDD pin. CS is the output pin with the current of the current sense circuit, and a resistor needs to be connected between CS pin and SGND pin to provide a voltage signal to the controller. To use the autonomous standby mode, MODE pin is recommended to connect to SGND pin.

PWM Input and Output

The ISG6106 has a PWM input pin to control the integrated GaN FET. When the PWM input voltage is higher than the logic high threshold of 3.5V (Max), the GaN FET is turned on and the drain, D, is shorted to the source, S, with a

resistance of 100mΩ (typical). When the PWM input voltage is lower than the logic low threshold of 0.6V (Min), the GaN FET is turned off and the output of D is open. Fig. 20 illustrates the timing diagram of the input and the output.

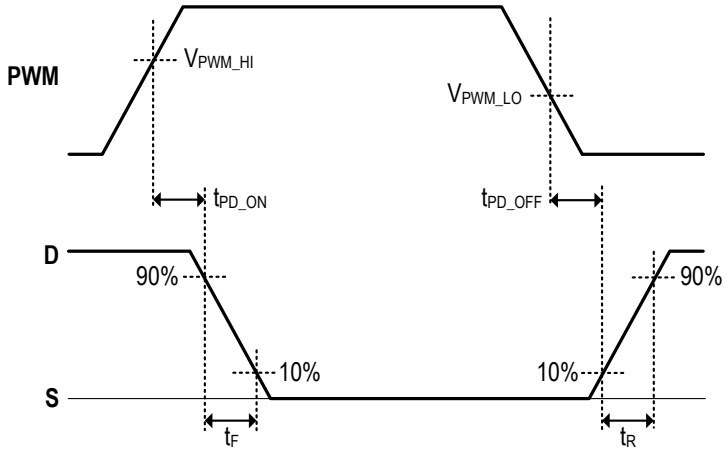


Fig. 20. Timing Diagram of Input and Output

Loss-Less Current Sensing

In many systems implemented with a peak current mode control or over current protection (OCP) functions, the current flowing through the power FET needs to be sensed. To sense the current, most solutions use a current-sense resistor in series with the FET and it increases power loss and introduces more parasitic inductance into the power loop. ISG6106 employs a current-sense circuit without any external resistor to sense the current as shown in Fig. 21. The loss-less current-sense circuit converts the current flowing through the GaN FET to the output current signal of CS pin with a conversion ratio of 4800:1 (typical). The output current of CS pin can be converted to the voltage by a resistor, R_{CS}, placed between CS pin and ground. The value of R_{CS} can be adjusted to provide the current-sense voltage with a proper voltage range for various controllers. The voltage on CS pin, V_{CS}, is determined by equation (1).

$$V_{CS}=\frac{I_D}{4800}\times R_{CS} \qquad (1)$$

where I_D is the drain current of GaN FET. Fig. 21 shows the switching timing diagram of the current sense output.

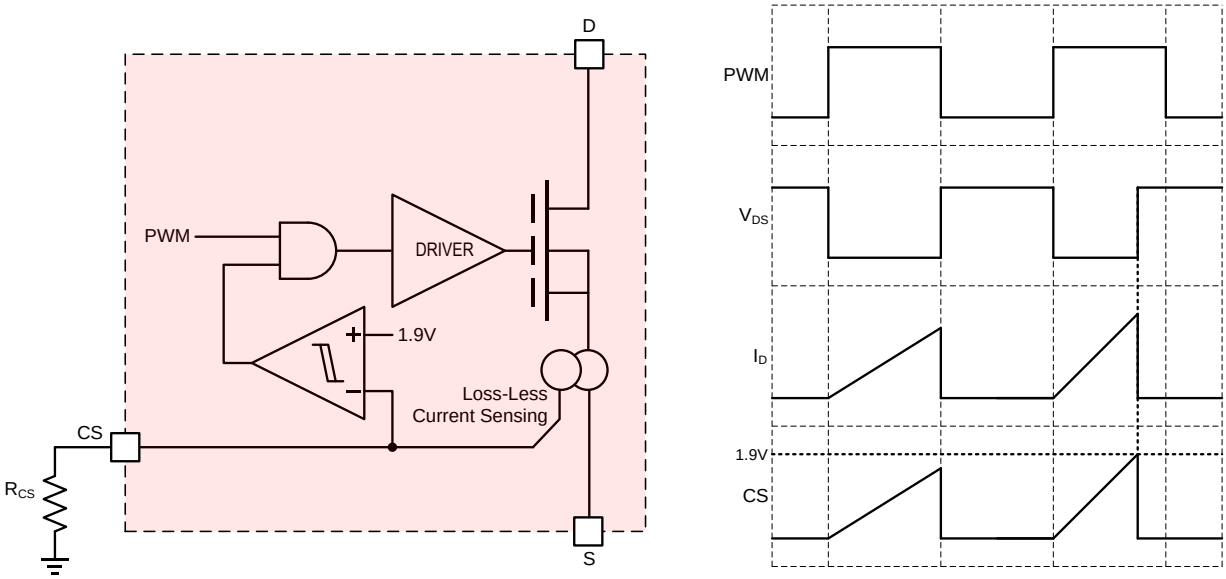


Fig. 21. Current Sense Circuit and Timing Diagram

Over Current Protection (OCP)

The ISG6106 provides a cycle-by-cycle over current protection based on the current-sense signal, V_{CS}, to protect the GaN FET. As illustrated in the timing diagram of Fig. 21, when the CS-pin voltage exceeds 1.9V (typical), the GaN FET is turned off. GaN FET will be turned on again at the next rising edge of PWM signal. The current limit by OCP can be calculated by equation (2).

$$I_{OCP}=\frac{4800\times V_{CS\_OCP}}{R_{CS}} \quad (2)$$

Programmable Gate Turn-On Slew Rate

In many applications such as QR flyback converter, it is desired to adjust the gate turn-on slew rate of power FET to meet the system requirement of both power efficiency and EMI performance. If the gate turn-on slew rate is too fast, it causes a high switching noise resulting in degradation of the EMI performance. Conversely, if the slew rate is too slow, the power efficiency is reduced. The smart gate driver in ISG6106 supports slew-rate control using an external resistor, R_{DD}, connected between VDD and RDD pin as shown in Fig. 22. R_{DD} limits the turn-on gate driving current, and as a result, the gate turn-on slew rate is controlled by the value of R_{DD}.

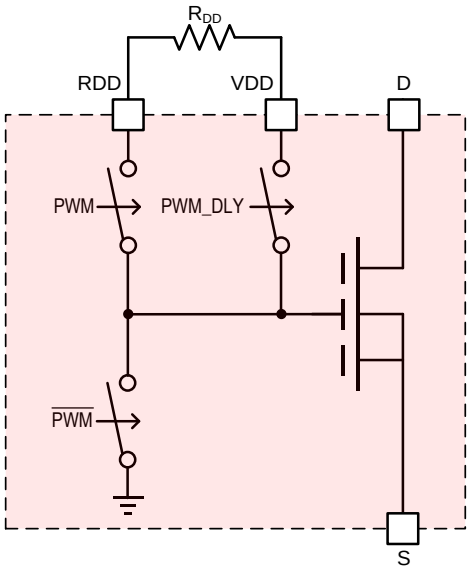


Fig. 22. Smart gate driver with a programmable dual slew-rate gate driving

Dual Slew Rate Gate Driving

The gate capacitance generally increases as the drain-to-source voltage of the power FET decreases. Specifically, the gate-to-drain capacitance increases exponentially as the drain voltage reaches the source voltage. Once the drain voltage reaches the source voltage during the turn-on period, the slow slew-rate gate driving with a large R_{DD} rarely improves the EMI performance and causes the efficiency degradation since it takes a long time to fully pull up the gate voltage. The ISG6106 employs the smart gate driver with a dual slew-rate gate driving scheme as illustrated in Fig. 22. During the turn-on period, the slow programmable slew-rate driver with R_{DD} is engaged first to reduce the switching noise as introduced in the previous section. After a typical 180ns delay time, T_{PU_DLY}, the fast slew-rate driver is engaged to increase the pull-up strength of the driver, and as a result, the GaN FET can be fully turned on quickly and the power dissipation is reduced. For maximizing both efficiency and EMI performance, R_{DD} value is recommended to be chosen considering T_{PU_DLY} for the dual slew-rate gate driving. Fig. 23 compares the two cases with different R_{DD} in QR flyback application. V_{DS} and V_{DS_SR} show the drain-to-source voltages of ISG6106 and power FET of the synchronous rectifier

(SR), respectively. Too large R_{DD} causes not only efficiency degradation, but also voltage spike in the SR resulting in damage to the power FET. It's recommended to choose R_{DD} value to turn on the fast slew-rate driver when the drain voltage reaches the source voltage.

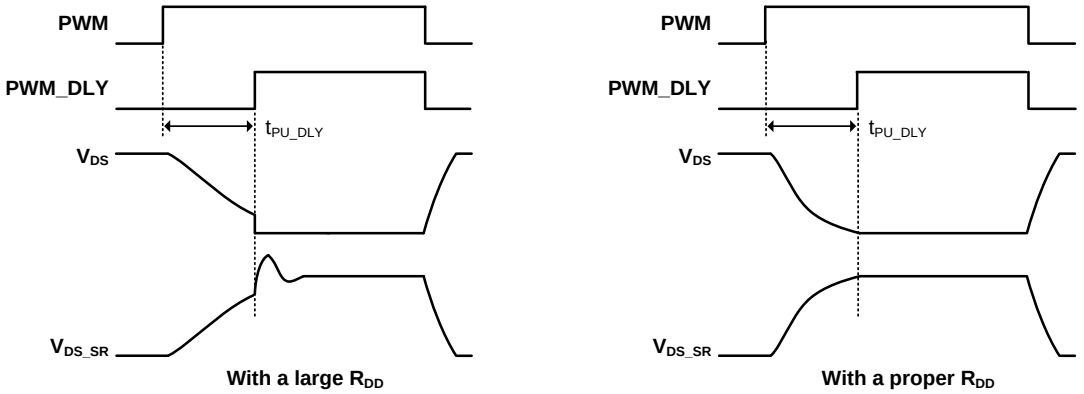


Fig. 23. Waveform comparison with different R_{DD} values in QR flyback application

Standby Mode

The ISG6106 provides an autonomous standby mode to improve system efficiency. As shown in the timing diagram of Fig. 24, if the voltage of the PWM signal stays below V_{PWM_LO} for the time duration of t_{STBY_DLY}, the ISG6106 automatically enters the standby mode. In the standby mode, most of the internal circuitry is turned off, and therefore, the VCC supply current is drastically reduced to I_{CC_STBY}, 115uA (typical). Once the PWM input voltage is applied upper V_{PWM_HI} in the standby mode, the ISG6106 wakes up at the first rising edge of the PWM input and enters normal operation mode immediately. The ISG6106 shows the smooth transition between the standby mode and the normal mode without any additional propagation delay for the recovery. MODE pin needs to be connected to SGND to enable the autonomous standby mode. If the MODE pin is connected to V5V, the ISG6106 operates in the normal mode only.

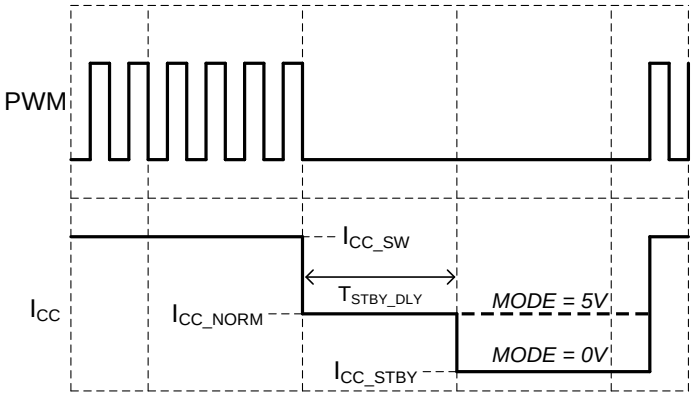


Fig. 24. Autonomous Standby Mode Timing Diagram

Internal Voltage Linear Regulators

The ISG6106 has two linear voltage regulators with output voltages of 6.5V and 5V for the gate drive of GaN FET and the internal circuitry, respectively. The high-voltage linear regulator produces 6.5V at the VDD pin from the VCC pin. The tightly regulated 6.5V output maximizes power efficiency while ensuring the reliability of the GaN FET. The low dropout voltage regulator generates 5V at the V5V pin from 6.5V at the VDD pin. Two voltage regulators must be bypassed to ground with a minimum of 10nF ceramic capacitor.

Under Voltage Lock Out (UVLO)

The ISG6106 features VCC undervoltage lockout (UVLO) protection. When VCC is below its UVLO threshold, 7.4V (typical), the ISG6106 enters UVLO mode and turns off the GaN FET and ignores the PWM input. When VCC is above the UVLO rising, 8.5V (typical), the ISG6106 will normally operate. In addition, the ISG6106 includes VDD UVLO protection with a falling threshold of 5.4V (typical) and a rising threshold of 5.7V (typical). The operation of VDD UVLO is the same as VCC UVLO.

Over Temperature Protection (OTP)

The ISG6106 employs over temperature protection (OTP). If the internal junction temperature, T_j, exceeds 165°C (typical), the PWM input is ignored and the GaN FET is turned off. When the temperature recovers to below 105°C (typical), the ISG6106 will operate normally.

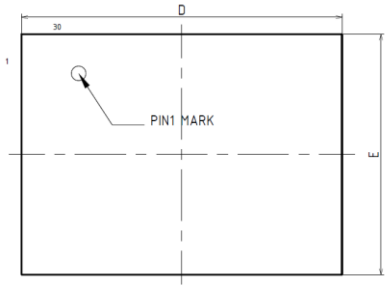
PCB Layout Checklist

A proper PCB layout is essential to support high-power and high-speed operation with GaN FETs. The PCB layout requires a dedicated ground plan layer. And it is strongly recommended to use a multilayer board to provide heat sinking. Check the following guidelines to obtain the optimum performance from ISG6106.

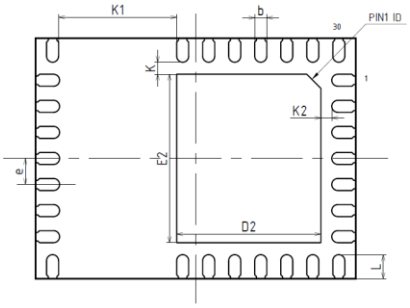
- Mount the bypass capacitors, C_{VCC}, C_{VDD}, and C_{V5V}, and the current-sense resistor, R_{CS}, as close as possible to the ISG6106 package and connect (-) terminal to SGND. Connect SGND pin directly to Source Pad underneath the IC.
- Place R_{DD} as close as possible between the (+) terminal of C_{VDD} and RDD pin.
- Use immediate vias as much as possible to connect S and the ground plane. Implement large copper area on the S and D pads.
- Flood all unused areas on all layers with copper and make thermal vias to reduce temperature rise. Connect the copper areas to ground.

16. Package Information

QFN6X8-30L Package:

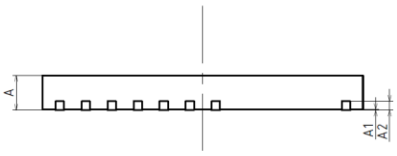


Top view



Bottom view

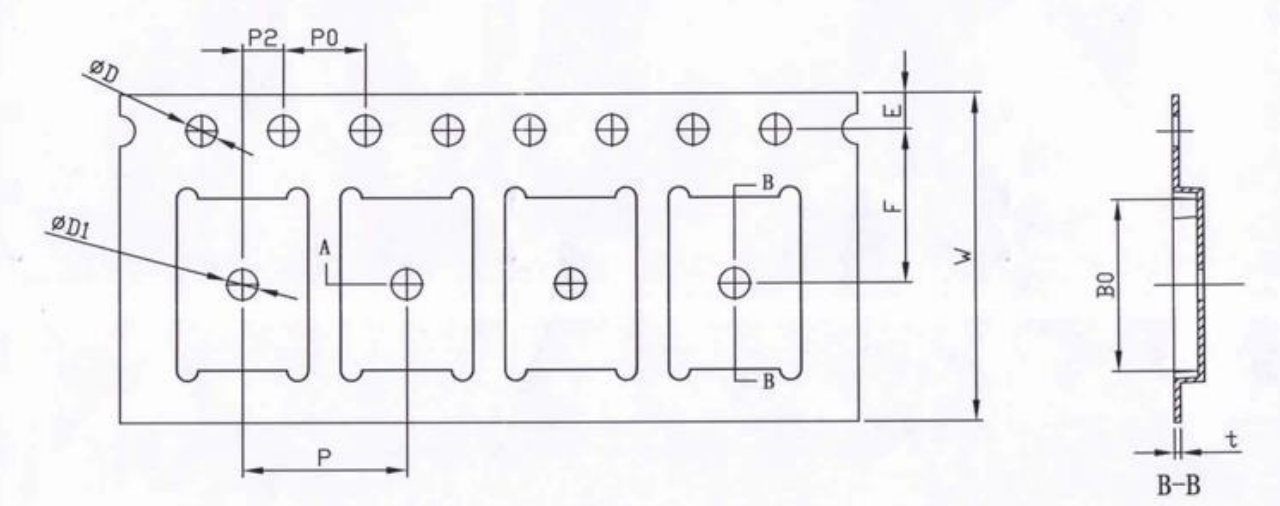
SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.25	0.30	0.35
D	7.90	8.00	8.10
D2	3.50	3.60	3.70
e		0.65BSC	
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.55	0.60	0.65
K		0.30REF	
K1	2.85	2.95	3.05
K2		0.275REF	

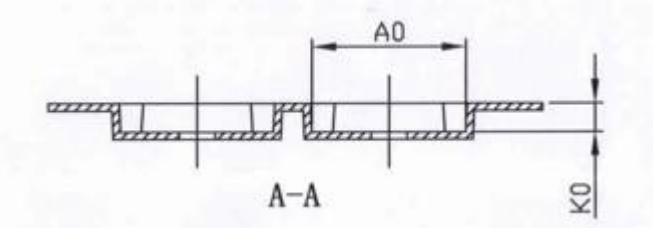


Side view

Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXXX
Row3	ASSY lot No.	XXXXXXXX
Row4	Date code	YYWW

17. Tape and Reel Information

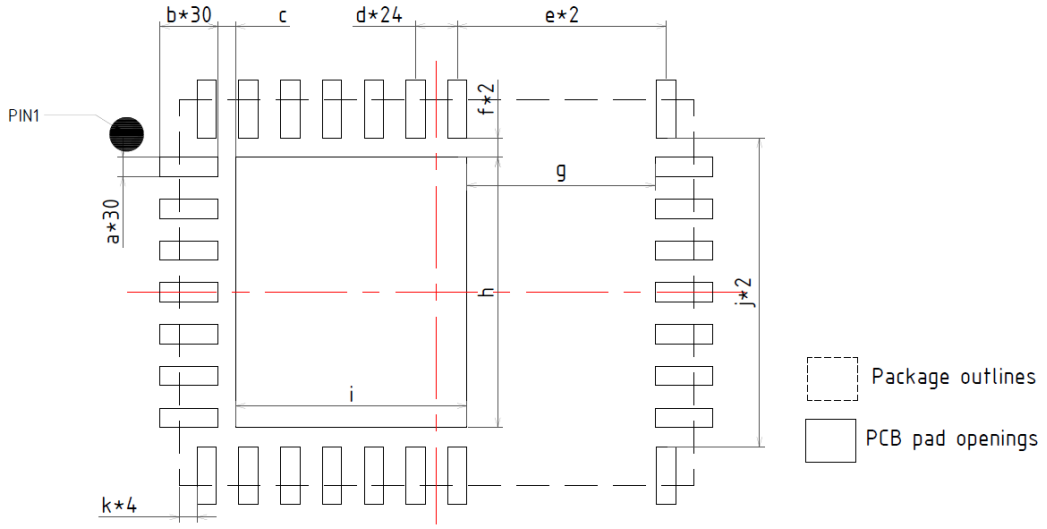




SYMBOL	DIMENSION(mm)		
	MIN	NOM	MAX
E	1.65	1.75	1.85
F	7.40	7.50	7.60
P2	1.90	2.00	2.10
D	/	1.50	1.60
D1	1.50	/	/
P0	3.90	4.00	4.10
10P0	39.8	40.0	40.2
W	15.70	16.00	16.30
P	7.90	8.00	8.10
A0	6.30	6.40	6.50
B0	8.30	8.40	8.50
K0	1.10	1.20	1.30
t	0.25	0.30	0.35

18. Recommended Land Pattern

QFN6X8-30L Package:



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	0.30	g	2.925
b	0.90	h	4.20
c	0.275	i	3.60
d	0.65	j	4.80
e	3.25	k	0.275
f	0.30		

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale.

19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
ISG6106QA	QFN6x8-30L	6106QA	MSL3	13” 2500PCS/reel

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