Single-Channel GaN Driver

1. Features

- Wide 6V to 20V Operating Voltage Range
- Dual Inverting and Non-Inverting PWM Inputs
- Independent Pullup and Pulldown Outputs for Adjustable Turn-on and Turn-off Speeds
- Strong 1.3-Ω Pullup and 0.5-Ω Pulldown Resistance
- Fast Propagation Delay with Input Deglitching
- User Programmable Gate Driver Supply Voltage
- Integrated 5V LDO for supplying Digital Isolator
- Built-In UVLO, OVP, OTP Protection

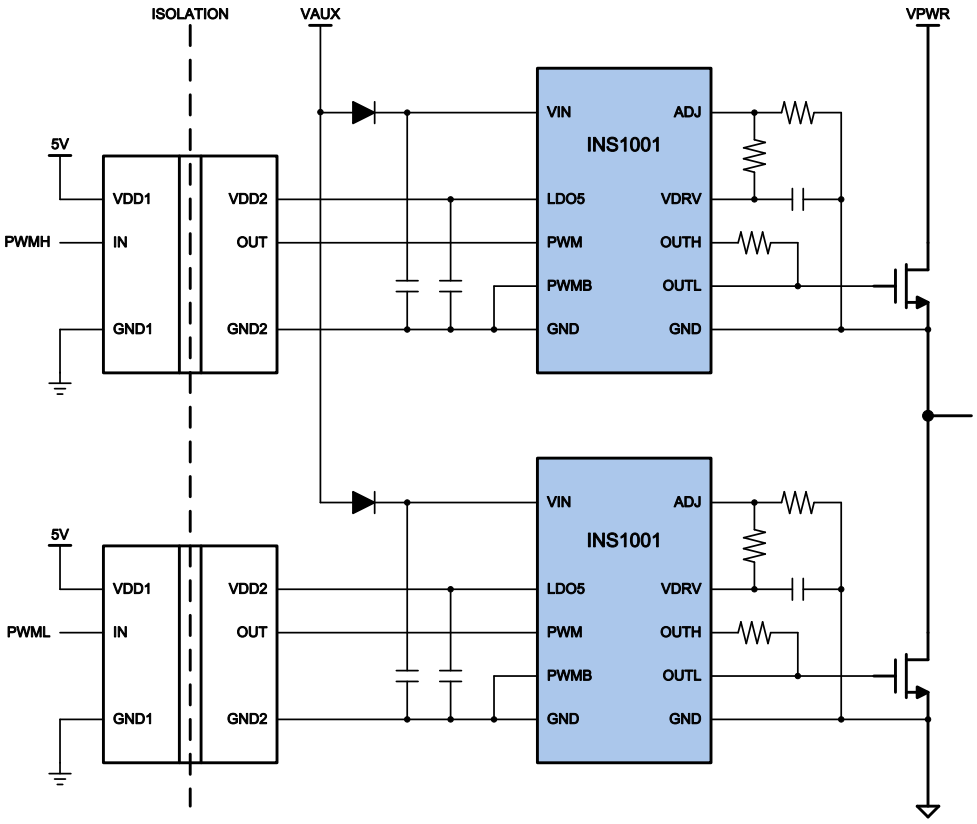
2. Applications

- Switch-Mode Power Supplies
- AC-DC, DC-DC Converters
- Boost, Flyback, and Forward Converters
- Half-Bridge and Full-Bridge Converters
- Synchronous Rectification
- Solar Inverters, Motor Control, UPS

3. Description

The INS1001 is designed to drive single-channel GaN FET(s) in either low-side, high-side, or secondary-side SR applications. It has both non-inverting and inverting PWM inputs, working with controller, opto-coupler, and digital isolator flexibly. The gate driver has two separate outputs, allowing independent adjustment of turn-on and turn-off speeds. The driver voltage can be adjusted through an external resistor divider, tailoring for different gate voltage requirements of GaN FETs. Integrated 5V LDO can supply digital isolator or other circuitry in high-side applications. The strong driving capability and fast propagation delay, along with input noise deglitching and built-in UVLO, OVP, OTP protection features, make the INS1001 extremely suitable for high power, high frequency, and robust power GaN applications. The INS1001 is available in thermally enhanced DFN3x3-10L package.

4. Typical Application



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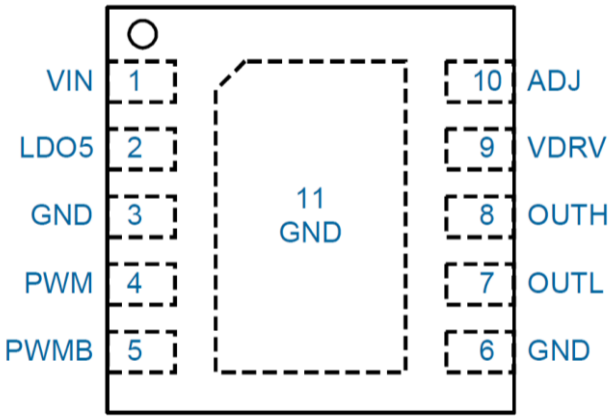
5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-01-30	Final release datasheet

6. Pin Configuration and Functions



10-Lead DFN (3mm x 3mm) Package – Top View

Pin Number	Pin Name	Description
1	VIN	Supply Voltage Input. Locally bypass this pin to GND with a ceramic capacitor.
2	LDO5	5V LDO Output. This pin provides power to internal logic circuitry and external circuitry up to 20mA. Locally bypass this pin to GND with a ceramic capacitor.
3, 6, 11	GND	Ground. Internally shorted together.
4	PWM	PWM Input. Receive PWM signal from the controller.
5	PWMB	Inverting PWM Input. Receive inverting PWM signal from the controller.
7	OUTL	Gate Driver Pulldown Output. Connect to the gate of GaN FET and use a resistor to adjust the turn-off speed.
8	OUTH	Gate Driver Pullup Output. Connect to the gate of GaN FET and use a resistor to adjust the turn-on speed.
9	VDRV	Driver Voltage Output. Regulated LDO output from VIN to supply GaN FET gate driver power. Locally bypass this pin to GND with a ceramic capacitor.
10	ADJ	Driver Voltage Adjustment. Connect a resistor divider between VDRV and GND to this pin to set the VDRV output voltage.

7. Absolute Maximum Ratings

All pins are referred to GND, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Min	Max	Unit
VIN	-0.3	22	V
VDRV	-0.3	13.2	V
OUTH, OUTL	-0.3	VDRV+0.3	V
PWM, PWMB	-0.3	6	V
LDO5, ADJ	-0.3	6	V
Operating Junction Temperature T_J	-40	150	˚C
Storage Temperature	-55	150	˚C

8. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002	±1000	V

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
VIN	6	20	V
VDRV	4	10	V
PWM, PWMB	0	5	V
Operating Junction Temperature T_J	-40	125	˚C

10. Thermal Information

Symbol	Parameter	INS1001DE	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	70.8	˚C/W
$R_{\theta JC(TOP)}$	Thermal Resistance, Junction to Case Top	67.2	˚C/W
$R_{\theta JC(BOT)}$	Thermal Resistance, Junction to Case Bottom	10.3	˚C/W

11. Electrical Characteristics

T_A = 25°C, VIN = 12V, C_{DRV} = 1uF, C_{LDO5} = 1uF, OUTH = OUTL, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Input						
VIN UVLO threshold	V_{IN_UVLO}		5.5	5.8	V	VIN rising
VIN UVLO hysteresis	V_{IN_HYS}		0.35		V	
VIN quiescent current	I_{VIN_Q}		200		uA	PMW = PWMB = 0V
PWM/PWMB Input						
Input high threshold	V_{IH}		2.6	3.2	V	
Input low threshold	V_{IL}	0.8	1.4		V	
PWM pulldown resistance	R_{PWM}		200		kΩ	To GND pin
PWMB pullup resistance	R_{PWMB}		200		kΩ	To LDO5 pin
VDRV Regulation						
ADJ regulation voltage	V_{ADJ}	0.97	1	1.03	V	
ADJ UVLO threshold	V_{ADJ_UVLO}	0.8	0.85	0.9	V	ADJ rising
ADJ UVLO hysteresis	V_{ADJ_HYS}		0.05		V	
VDRV current limit	I_{DRV}	35	55	70	mA	
VDRV dropout voltage	V_{DRV_DO}		140	250	mV	VIN = 6V, ADJ = 0V, I_{DRV} = 20mA
VDRV OVP threshold	V_{DRV_OVP}	11	11.5	12	V	VDRV rising
VDRV OVP hysteresis			0.5		V	
LDO5 Regulation						
LDO5 regulation voltage	V_{LDO5}	4.85	5	5.15	V	
LDO5 UVLO threshold	V_{LDO5_UVLO}	3.8	4	4.2	V	LDO5 rising
LDO5 UVLO hysteresis	V_{LDO5_HYS}		0.3		V	
LDO5 current limit	I_{LDO5}		38		mA	
LDO5 dropout voltage	V_{LDO5_DO}		130	250	mV	VIN = 5V, I_{LDO5} = 10mA
Gate Driver						
OUTH pull-up resistance	R_{OUTH}		1.3		Ω	VDRV = 6V, I_{OUTH} = -100mA
OUTL pull-down resistance	R_{OUTL}		0.5		Ω	I_{OUTL} = 100mA
OUTH peak source current (1)	I_{OUTH}		2		A	
OUTL peak sink current (1)	I_{OUTL}		5.5		A	
Thermal Protection						
Thermal shutdown threshold (1)	T_{SD}		160		°C	
Thermal hysteresis (1)	T_{HYS}		20		°C	

12. Switching Characteristics

T_A = 25°C, VIN = 12V, VDRV = 6V, C_{DRV} = 1uF, C_{LDO5} = 1uF, OUTH = OUTL, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum input high pulse width (1)	t_{HPW}		15		ns	
Minimum input low pulse width	t_{LPW}		15		ns	
Output rise time (1)	t_R		10		ns	Fig. 16, C_{OUT} = 1nF
Output fall time (1)	t_F		3		ns	Fig. 16, C_{OUT} = 1nF
Turn-on propagation delay (1)	t_{DLH}		35	50	ns	Fig. 16
Turn-off propagation delay (1)	t_{DHL}		35	50	ns	Fig. 16

(1) Not 100% tested and guaranteed by design.

13. Typical Characteristics

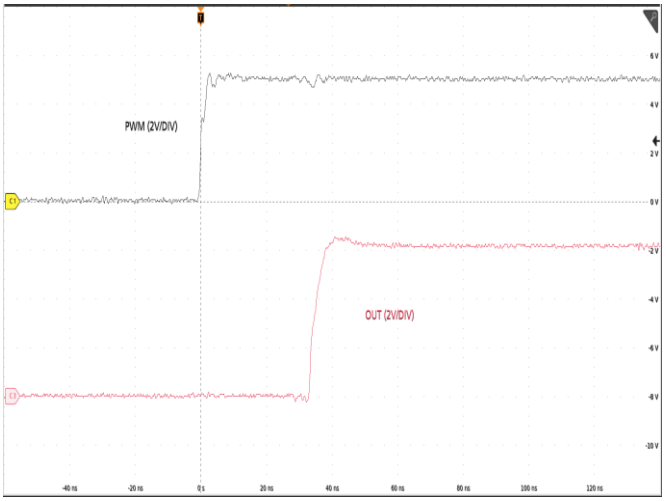


Fig. 1. Driver Turn-On Waveform, C_{OUT} = 1nF

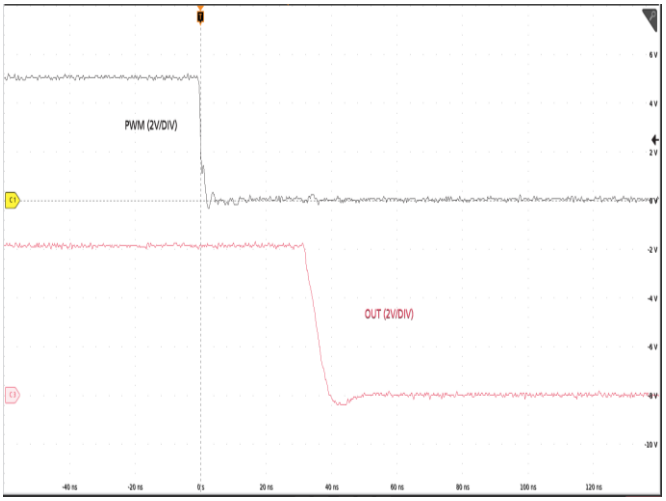


Fig. 2. Driver Turn-Off Waveform, C_{OUT} = 1nF

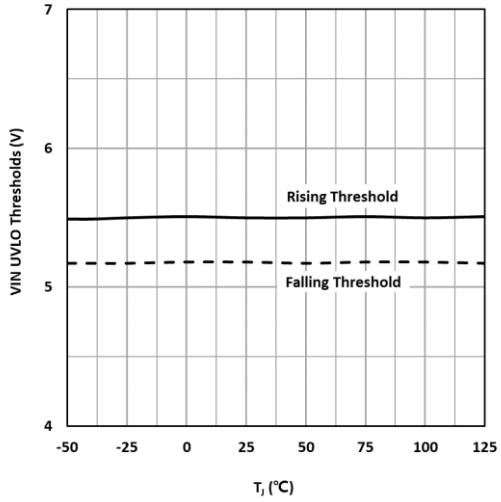


Fig. 3. VIN UVLO Thresholds vs Temperature

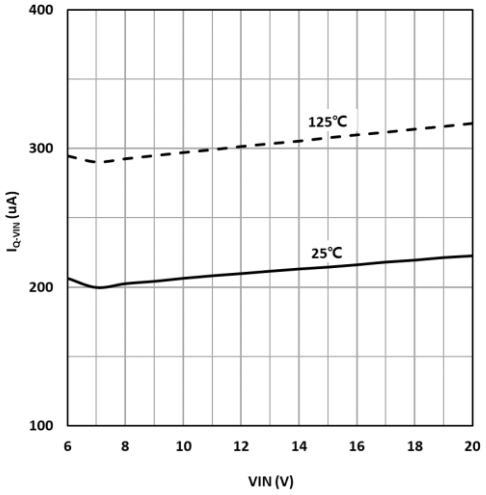


Fig. 4. VIN Quiescent Current vs VIN

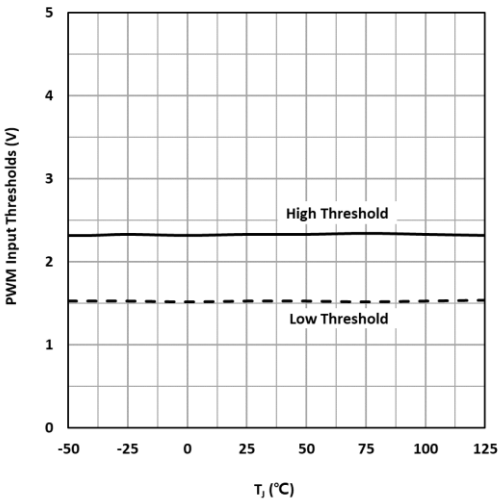


Fig. 5. PWM Input Thresholds vs Temperature

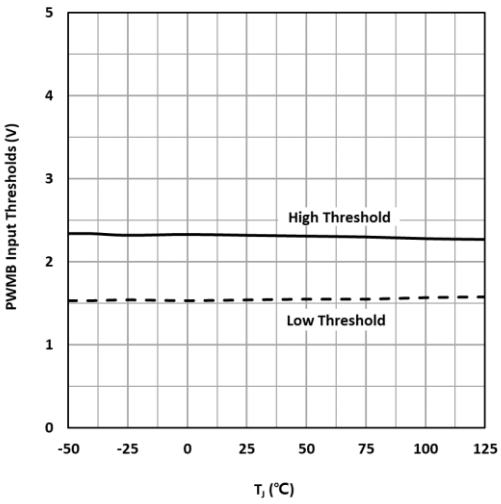


Fig. 6. PWMB Input Thresholds vs Temperature

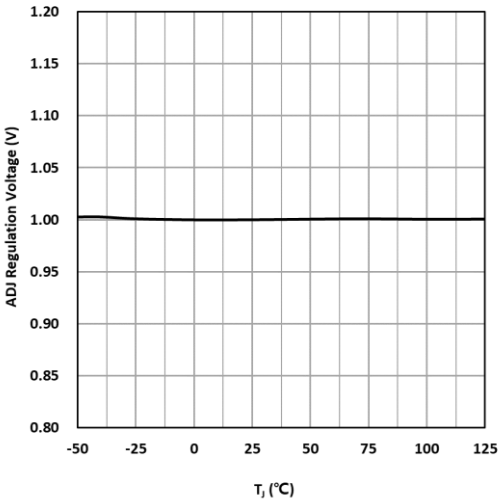


Fig. 7. ADJ Regulation Voltage vs Temperature

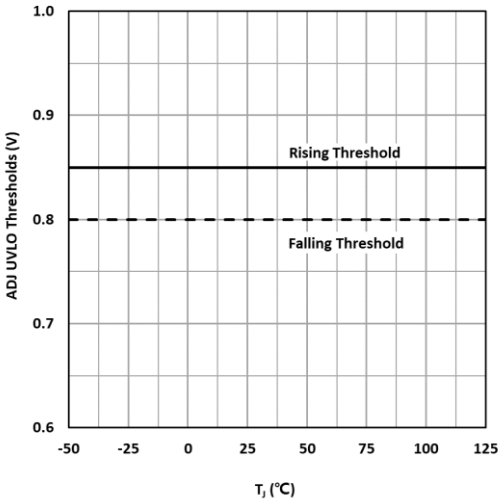


Fig. 8. ADJ UVLO Thresholds vs Temperature

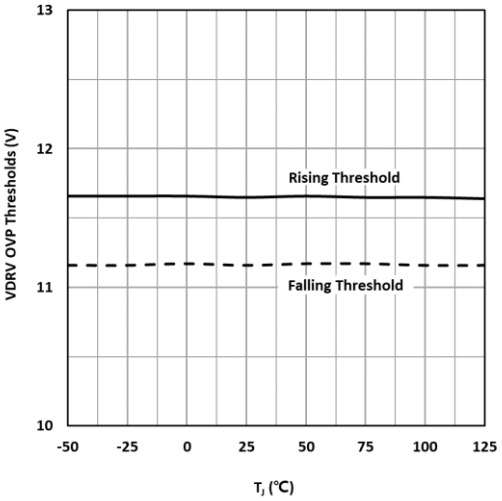


Fig. 9. VDRV OVP Thresholds vs Temperature

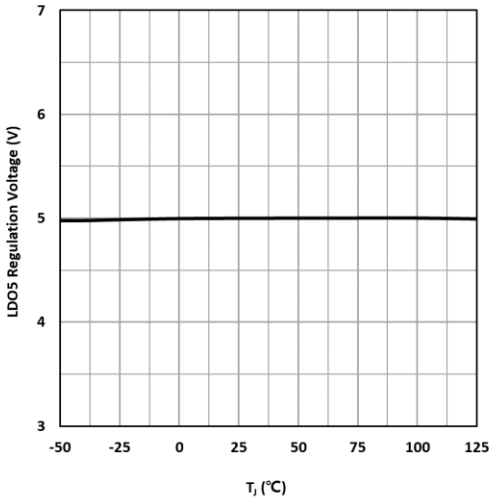


Fig. 10. LDO5 Regulation Voltage vs Temperature

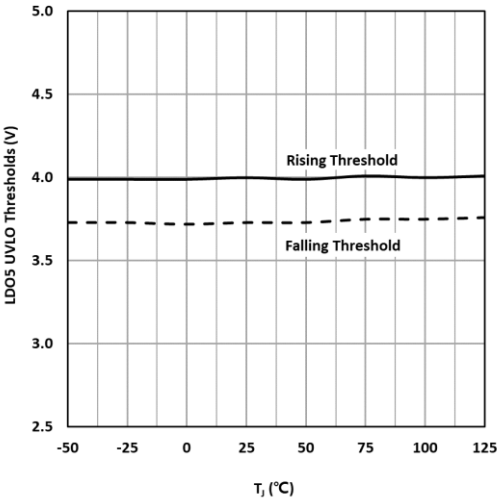


Fig. 11. LDO5 UVLO Thresholds vs Temperature

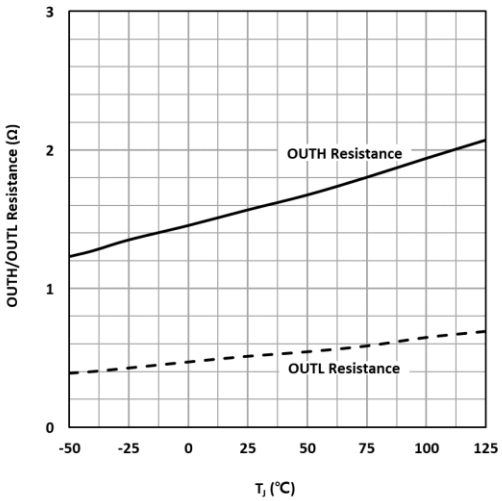


Fig. 12. OUTH/OUTL Resistance vs Temperature

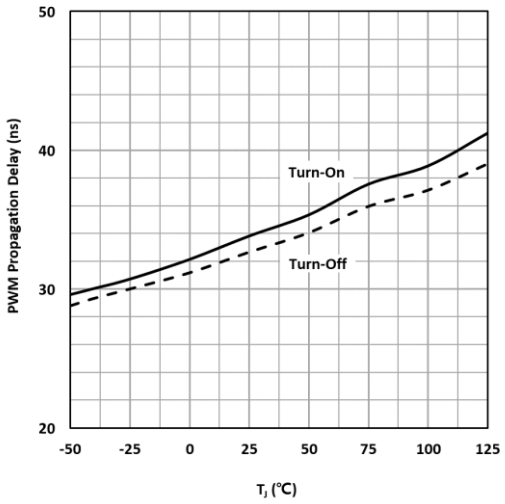


Fig. 13. PWM Propagation Delay vs Temperature

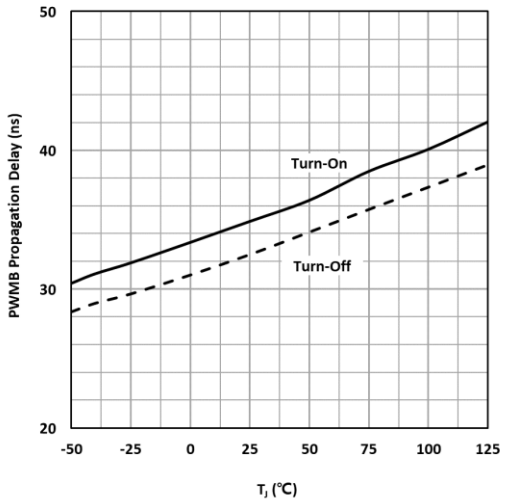


Fig. 14. PWMB Propagation Delay vs Temperature

14. Block Diagram

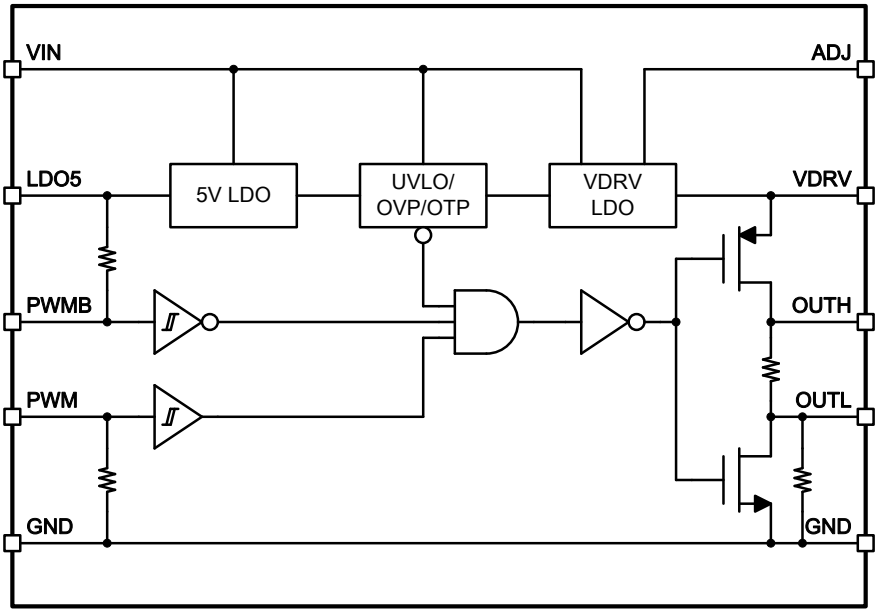


Fig. 15. Functional Block Diagram

15. Function Description

The INS1001 is a full-featured, single-channel gate driver that is fully optimized to drive a single GaN FET or multiple paralleling GaN FETs in either low-side, high-side, or secondary-side SR applications. The INS1001 solves many of the conventional challenges faced in the applications implementing GaN FETs. It features two separate non-inverting (PWM) and inverting (PWMB) inputs, working with controller, opto-coupler, and digital isolator flexibly. The split output gate driver allows independent adjustment of turn-on and turn-off speeds. The driver voltage of the INS1001 can be precisely adjusted with external resistor divider, tailoring for different gate voltage requirements of GaN FETs. Integrated 5V LDO can supply digital isolator or other circuitry in high-side applications. The strong driving capability and fast propagation delay, along with input noise deglitching and built-in UVLO, OVP, OTP protection features, make the INS1001 extremely suitable for high power, high frequency, and robust power GaN applications. Its operation is best understood by referring to the Block Diagram in Fig. 15.

PWM Input and Output

The INS1001 has two separate non-inverting (PWM) and inverting (PWMB) CMOS logic input pins to drive single-channel GaN FETs, enabling it to work with controller, opto-coupler, and digital isolator flexibly. The PWM and PWMB input states are summarized in Table 1. When the PWMB pin is low, the driver output (OUTH, OUTL) is synchronized with the PWM input logic. When the PWM pin is high, the driver output is synchronized with the PWMB pin logic.

PWM	PWMB	OUTH	OUTL
L	L	Open	Pull-Down
L	H	Open	Pull-Down
H	L	Pull-Up	Open
H	H	Open	Pull-Down

Table 1. PWM and PWMB input states

The logic input signals are independent of VIN. For example, the logic inputs are provided from a 3.3V/5V CMOS logic, while the IC is powered from 12V Supply. The CMOS logic inputs have the upper and the lower thresholds of 2.8V (Max) and 1.2V (Min) respectively with a 15ns (typical) input deglitching time to avoid any fault triggering condition such as double pulsing during transition. The PWM logic input pin has an internal 200kΩ pulldown resistor to the GND pin, and the PWMB logic input pin has an internal 200kΩ pull-up resistor to the LDO5 pin.

Split Gate Driving Outputs

It is often practiced reducing gate drive pull-up strengths in driving GaN FET switches by adding an external gate resistor, to prevent the large dv/dt induced switching spikes that deteriorates reliability and EMI. Then again, strong pull-down gate drive is always required because the fast slew rate of drain of GaN FET (SW) node may pull up the gate of the GaN FET and falsely turn it on. A traditional single gate drive can only have a single gate resistor that cannot optimize both requirements at the same time. In the INS1001, a split gate drive is provided, which allows the use of a large pull-up resistor and low pull-down resistor to achieve optimized efficiency, reliability, and EMI performance. Figure 16 illustrates the switching timing waveforms of the driver outputs.

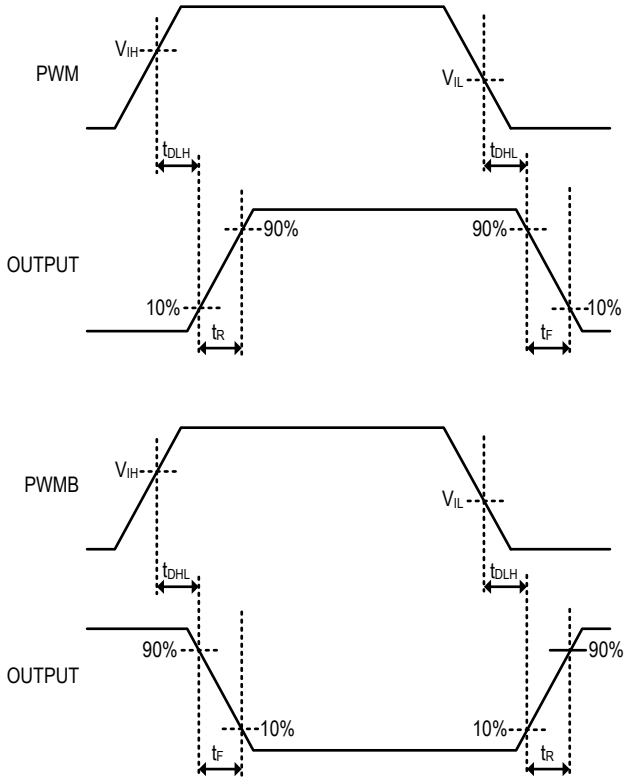


Figure 16. Circuit diagram of V_{DRV} regulation loop

LDO5 Regulator

An internal P-channel low dropout regulator produces 5V at the LDO5 pin from the V_{IN} supply pin. The LDO5 powers the internal circuitry in the INS1001 and can also supply digital isolator in high-side applications. The LDO5 regulator can supply a peak current of 38mA (typical) and must be bypassed to ground with a minimum of 1μF ceramic capacitor.

V_{IN} Undervoltage Lockout (UVLO)

The INS1001 features V_{IN} undervoltage lockout (UVLO) protection. When V_{IN} is below its UVLO threshold, 5.5V (typical), the INS1001 enters V_{IN} UVLO mode and turns off the driver.

V_{DRV} Regulator

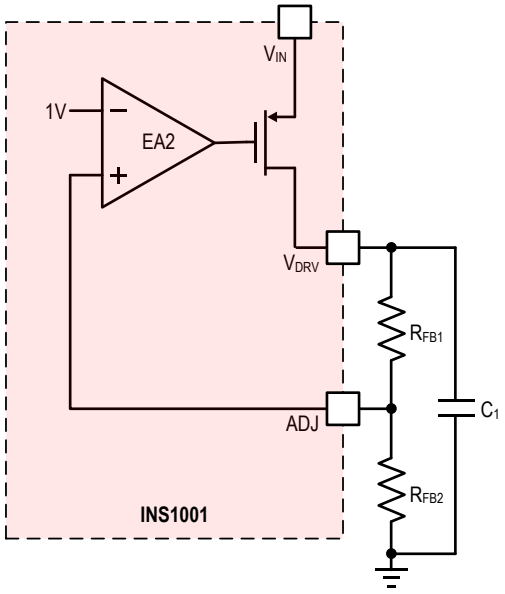


Figure 17. Circuit diagram of V_{DRV} regulation loop

The INS1001 has an integrated LDO for adjustable gate driver output voltage (V_{DRV}), which can be programmed through control of two external resistors. Figure 17 demonstrates the V_{DRV} closed loop regulation through the ADJ pin and two external resistors. The ADJ pin is the negative feedback input pin that is regulated at 1V (typical) internal reference voltage, and thus the V_{DRV} is regulated to:

$$V_{DRV}=1V \times \frac{R_{FB1}+R_{FB2}}{R_{FB2}}$$

The V_{DRV} regulator can supply a peak current of 55mA (typical) and must be bypassed to ground with a minimum of 1μF ceramic capacitor (C_1). When V_{DRV} passes its OVLO threshold, 11.5V (typical), the INS1001 enters to the V_{DRV} clamp mode and disables V_{DRV} regulator. When supplying V_{DRV} directly from V_{IN}, the recommended pin configuration is shown in Figure 18.

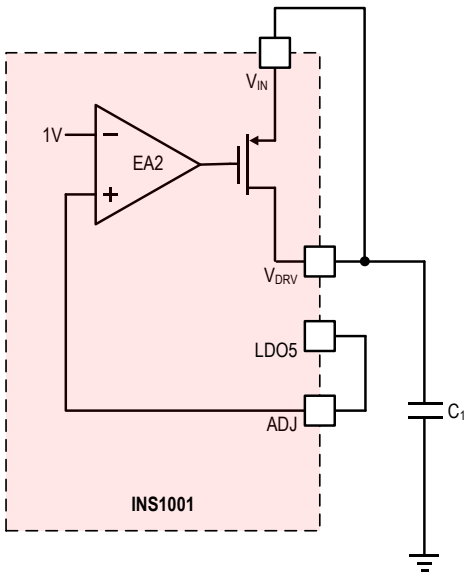


Figure 18. Configuration of V_{DRV} supplied directly from V_{IN}

Startup Power Sequence

Figure 19 shows the start-up power sequence for the INS1001. Once the V_{IN} is supplied and rises enough to wake up startup circuitry, the INS1001 generates bandgap reference and powers up the internal LDO5 LDO. The LDO5 LDO supplies the internal V_{DRV} control circuitry and now the INS1001 enters LDO5 undervoltage lockout (UVLO) mode. When the LDO5 pin is charged above its rising UVLO threshold (4V typical), the V_{IN} pin passes its rising enable threshold (5.5V typical), and the junction temperature is less than its thermal shutdown (160°C typical), the INS1001 powers up the V_{DRV} LDO and now the INS1001 enters V_{DRV} UVLO mode. From the time of entering V_{DRV} UVLO mode to the time of V_{DRV} passing its rising UVLO threshold, (85% of ADJ pin voltage typical), the INS1001 is going through a power-on-reset (POR), waking up the entire internal driver control circuitry and settling to the right initial conditions. After the POR, the INS1001 starts passing the PWM inputs to its output.

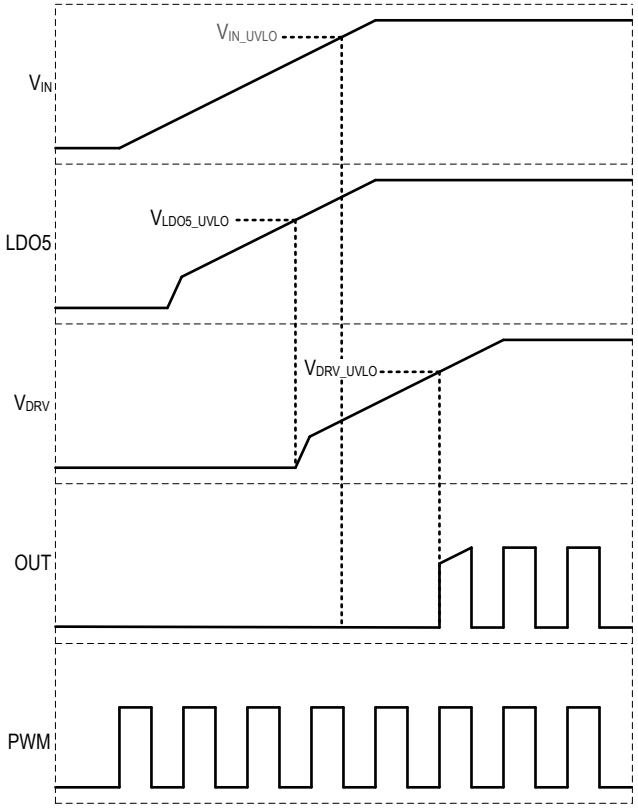
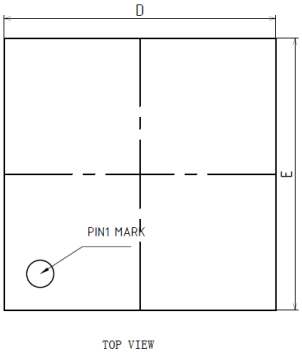
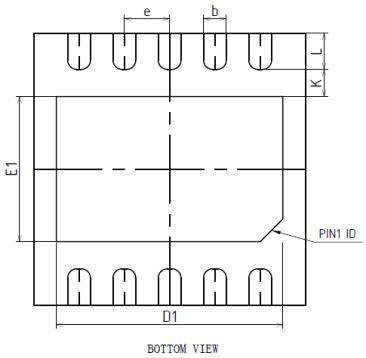


Figure 19. Waveforms of startup power sequence

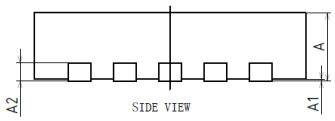
16. Package Information

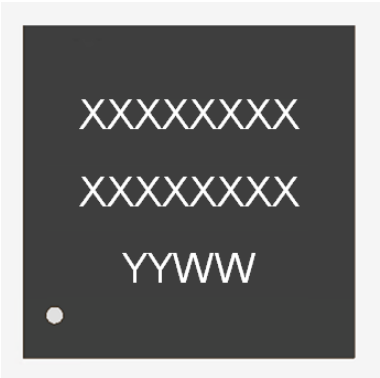
DFN3X3-10L Package:





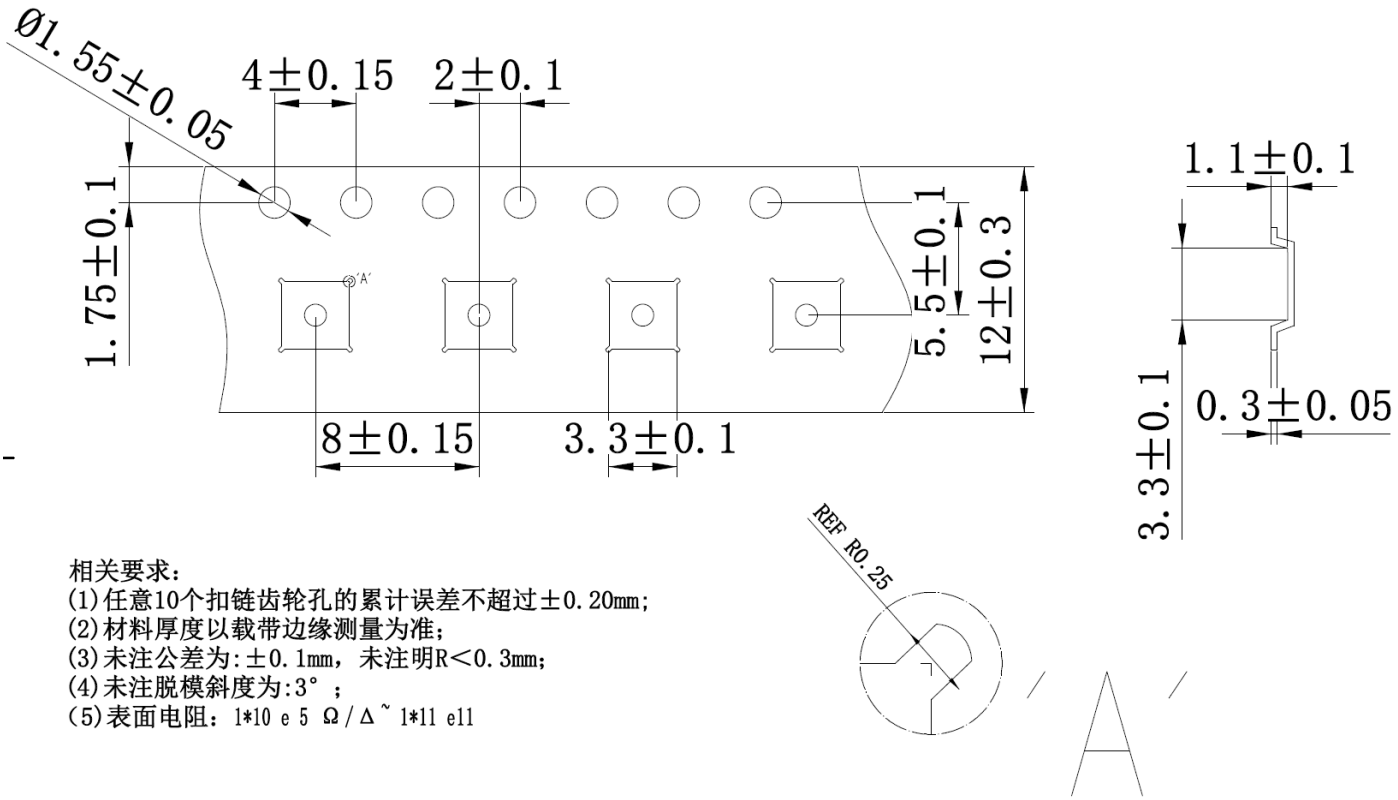
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	075	0.80
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	2.20	2.50	2.70
e		0.50BSC	
E	2.90	3.00	3.10
E1	1.40	1.60	1.80
L	0.30	0.40	0.50
K		0.30REF	





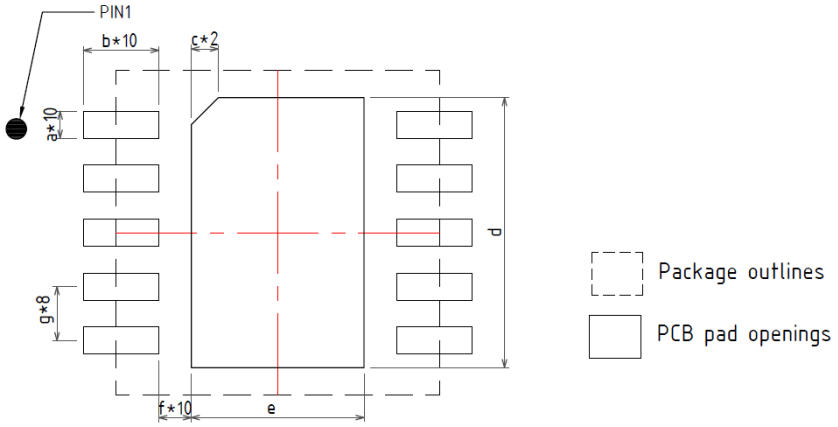
ROW	Description	Example
Row1	Product Code	XXXXXXXX
Row2	Assembly Lot No.	XXXXXXXX
Row3	Date Code	YYWW

17. Tape and Reel Information



相关要求：
(1)任意10个扣链齿轮孔的累计误差不超过±0.20mm;
(2)材料厚度以载带边缘测量为准;
(3)未注公差为:±0.1mm，未注明R＜0.3mm;
(4)未注脱模斜度为:3°；
(5)表面电阻：1*10 e 5 Ω/Δ~ 1*11 e11

18. Recommended Land Pattern



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	0.250	e	1.600
b	0.700	f	0.300
c	0.250	g	0.500
d	2.500		

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale.

19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
INS1001DE	DFN3x3-10L	1001DE	MSL3	13" 2500PCS/reel

Important Notice

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