

INN100EQ016A

100V Enhancement-mode GaN Power Transistor

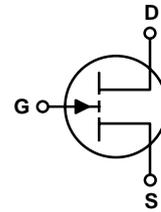
INN100EQ016A

1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in En-FCQFN with 4.0 mm x 6.0 mm package size.

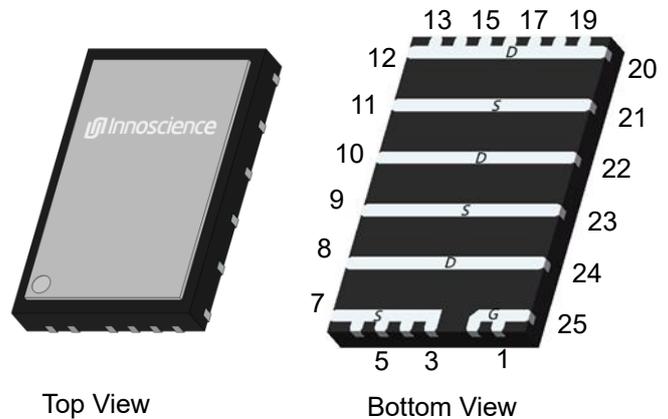
2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small footprint



3. Applications

- High frequency DC-DC converter
- Point of Load
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver



4. Key performance parameters

Table 1 Key performance parameters at $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max}$ @ $V_{GS} = 5\text{ V}$	1.8	m Ω
$Q_{G,typ}$ @ $V_{DS} = 50\text{ V}$	22	nC
$I_{DS,Pulse}$	320	A
Q_{OSS} @ $V_{DS} = 50\text{ V}$	125	nC

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
1,2,25	Gate	Driver Gate
3-7,9,11,21,23	Source	Source
8,10,12-20,22,24	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100EQ016A	En-FCQFN 4X6	J27

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6. Maximum ratings

at $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage (up to 300,000 5ms pulse at 150 °C)	120	V
I_D	Continuous current	100	A
	Pulsed (25 °C, $T_{Pulse} = 100\text{ }\mu\text{s}$)	320	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	°C

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.24	$^{\circ}\text{C}/\text{W}$	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.31	$^{\circ}\text{C}/\text{W}$	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ¹	56.63	$^{\circ}\text{C}/\text{W}$	
T_{sold}	Maximum reflow soldering temperature	260	$^{\circ}\text{C}$	MSL3

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	100	-	-	V	$V_{GS} = 0\text{ V}$, $I_D = 900\text{ }\mu\text{A}$
I_{DSS}	Drain Source Leakage	-	9.5	93	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$
I_{GSS}	Gate-to-Source Forward Leakage	-	2.8	55	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Reverse Leakage	-	0.3	1.2	μA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	$V_{DS} = V_{GS}$, $I_D = 21\text{ mA}$
$R_{DS(on)}$	Drain-Source On-state Resistance	-	1.4	1.8	$\text{m}\Omega$	$V_{GS} = 5\text{ V}$, $I_D = 40\text{ A}$
V_{SD}	Source-Drain Forward Voltage	-	1.5	-	V	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{ISS}	Input Capacitance	-	2500	-	pF	V _{GS} = 0 V, V _{DS} = 50 V
C _{OSS}	Output Capacitance	-	1100	-		V _{GS} = 0 V, V _{DS} = 50 V
C _{RSS}	Reverse Transfer Capacitance	-	19	-		V _{GS} = 0 V, V _{DS} = 50 V
C _{OSS(ER)}	Energy Related C _{OSS}	-	1700	-		V _{GS} = 0 V, V _{DS} = 0 V to 50 V
C _{OSS(TR)}	Time Related C _{OSS}	-	2500	-		V _{GS} = 0 V, V _{DS} = 0 V to 50 V
R _G	Gate resistance	-	1.8	-	Ω	f = 5 MHz, open drain
Q _G	Total Gate Charge	-	22	-	nC	V _{GS} = 5 V, V _{DS} = 50 V, I _D =40 A
Q _{GS}	Gate to Source Charge	-	4.5	-		V _{DS} = 50 V, I _D =40 A
Q _{GD}	Gate to Drain Charge	-	4.5	-		V _{DS} = 50 V, I _D =40 A
Q _{G(TH)}	Gate Charge at Threshold	-	2.5	-		V _{DS} = 50 V, I _D =40 A
Q _{OSS}	Output Charge	-	125	-		V _{GS} = 0 V, V _{DS} = 50 V

9. Electric characteristics diagrams

at $T_J = 25^\circ\text{C}$, unless specified otherwise

Fig. 1 Typical Output Characteristics ($T_J=25^\circ\text{C}$)

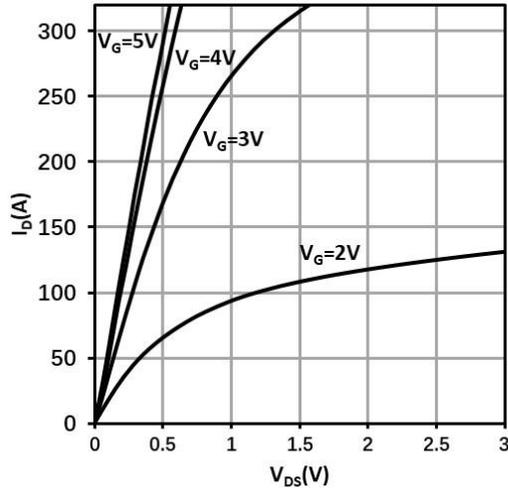


Fig. 2 Typical Output Characteristics ($T_J=125^\circ\text{C}$)

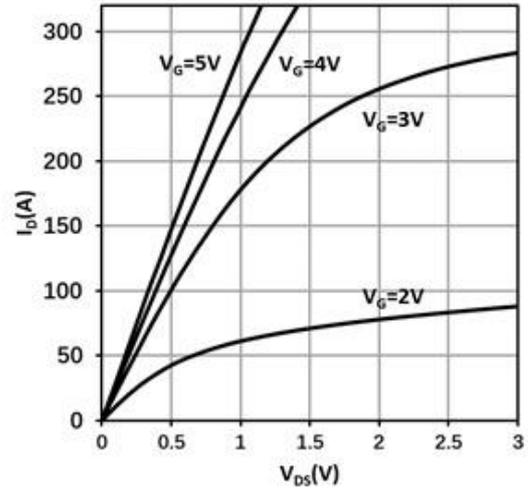


Fig.3 Typical Drain On-state Resistance ($T_J=25^\circ\text{C}$)

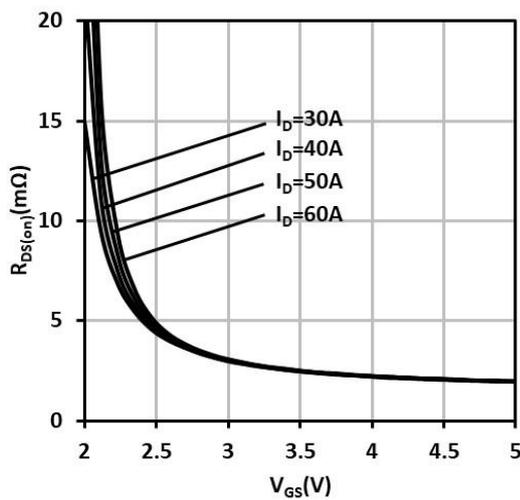


Fig. 4 Typical Drain On-state Resistance ($T_J=125^\circ\text{C}$)

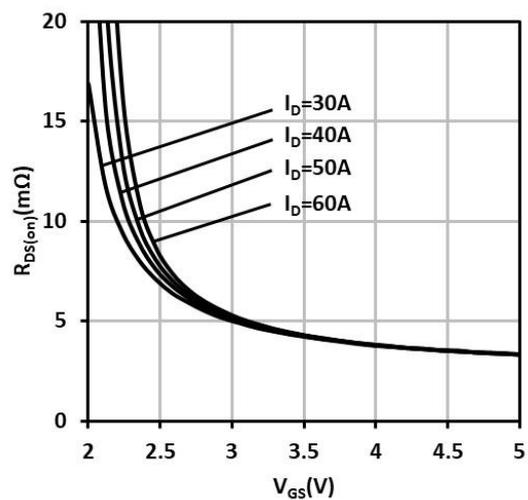


Fig. 5 Normalized On-State Resistance vs. Temp.

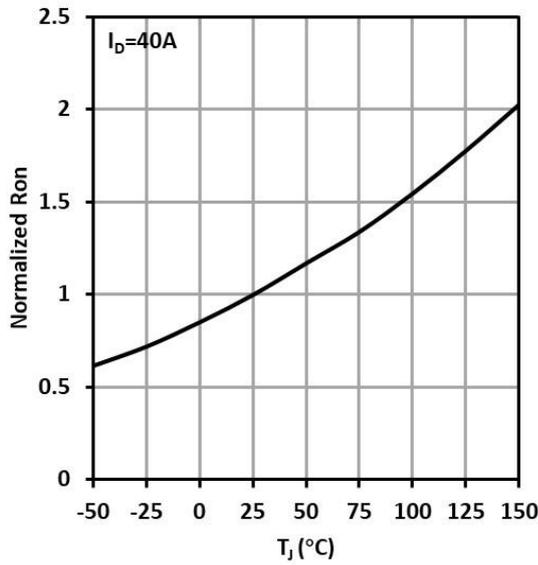


Fig. 6 Typical Transfer Characteristics

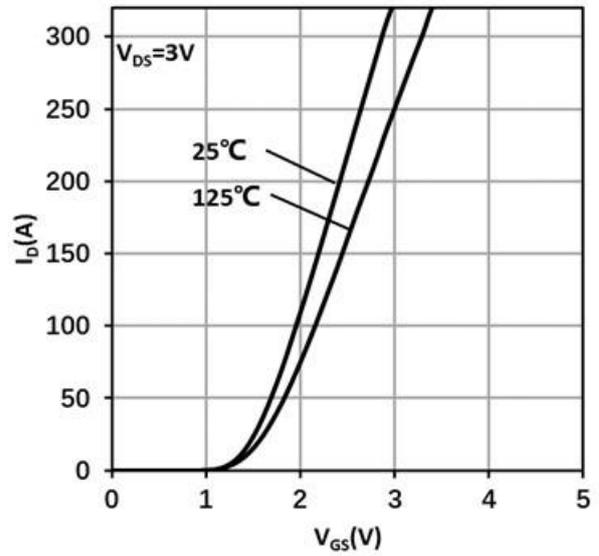


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0, T_J = 25^\circ\text{C}$)

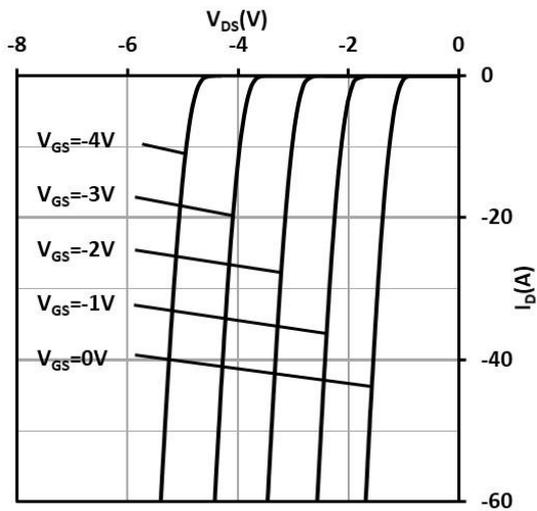


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0, T_J = 25^\circ\text{C}$)

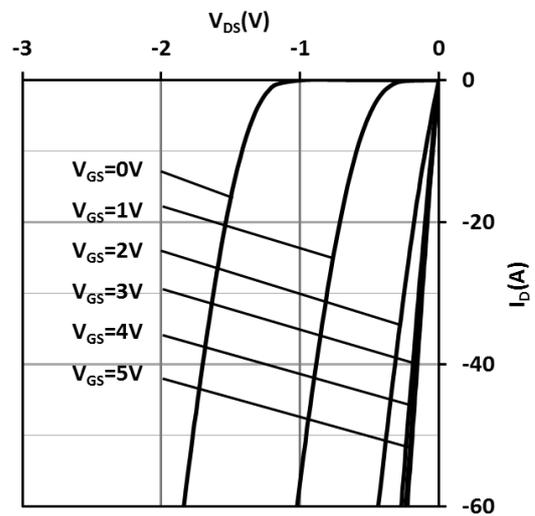


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0, T_J = 125^\circ\text{C}$)

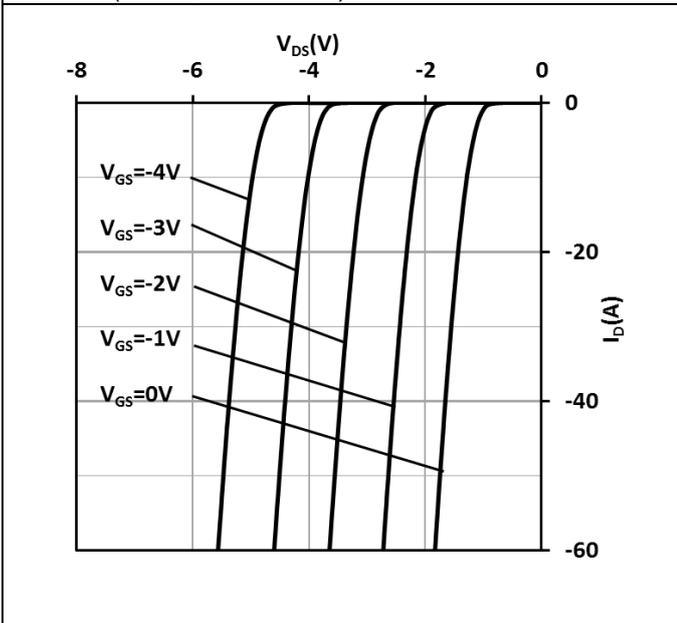


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0, T_J = 125^\circ\text{C}$)

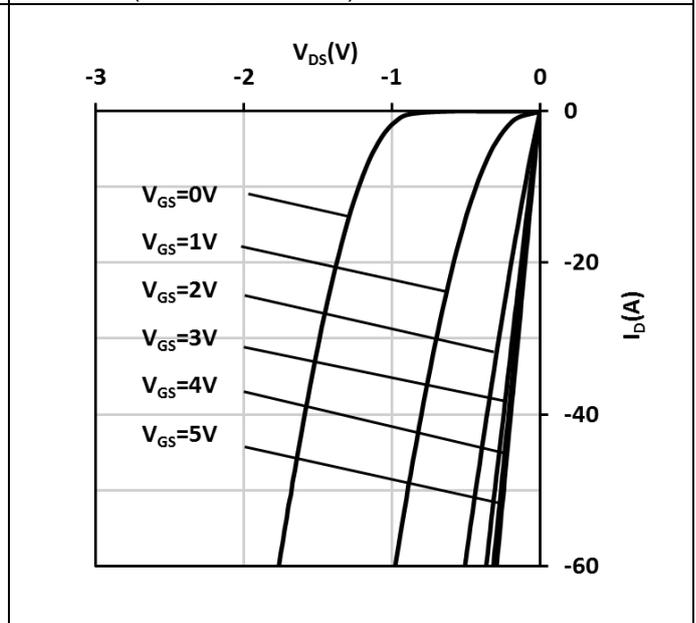


Fig. 11 Typ. Capacitances Characteristics

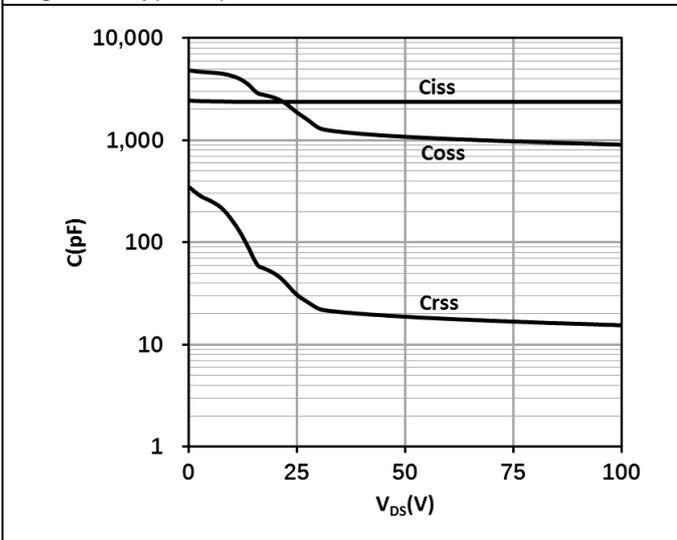


Fig. 12 Typ. Gate Charge

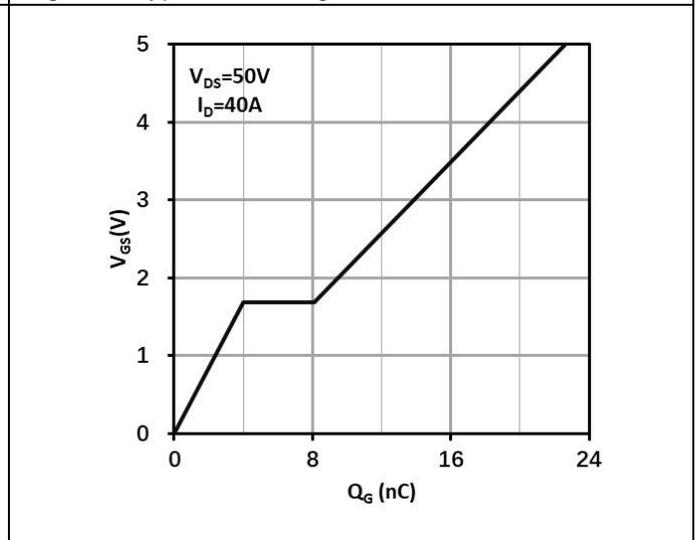


Fig. 13 Normalized Threshold Voltage vs. Temp.

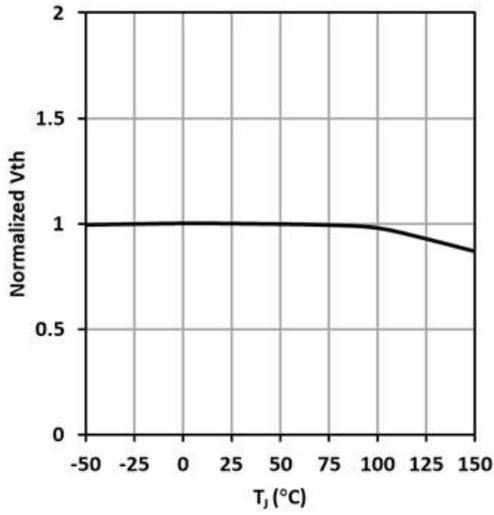


Fig. 14 Output Charge

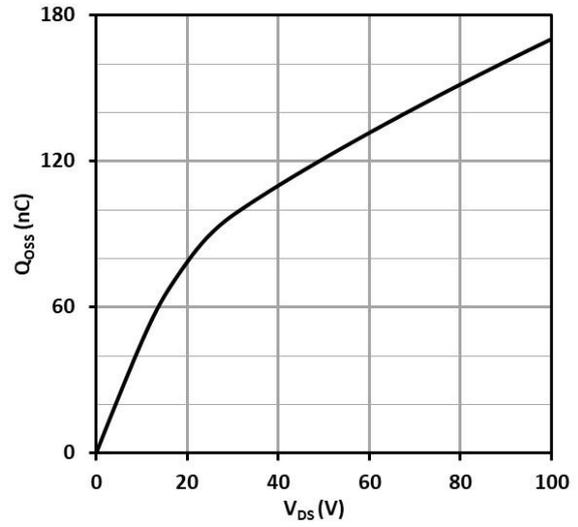


Fig. 15 Output Capacitance Stored Energy

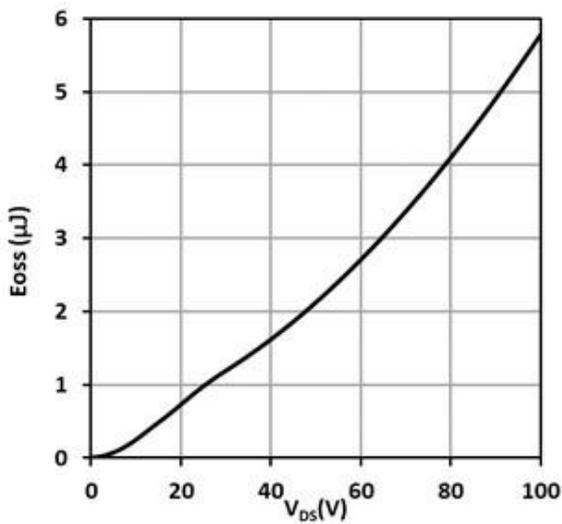


Fig. 16 Power Dissipation

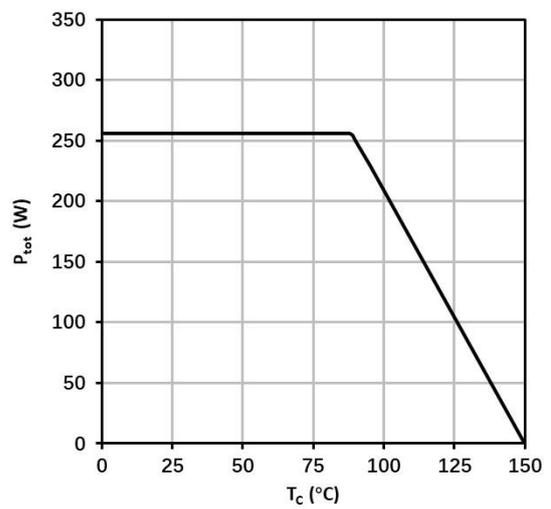


Fig. 17 Safe Operating Area

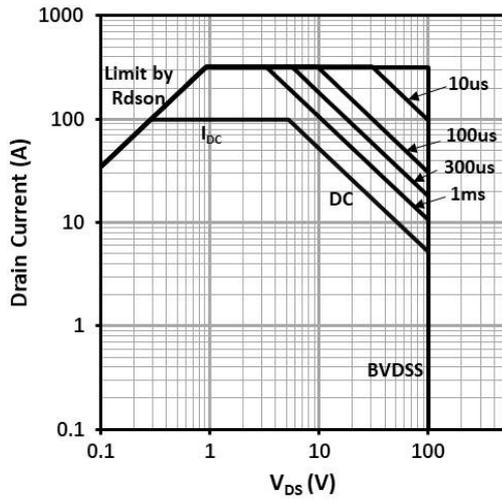
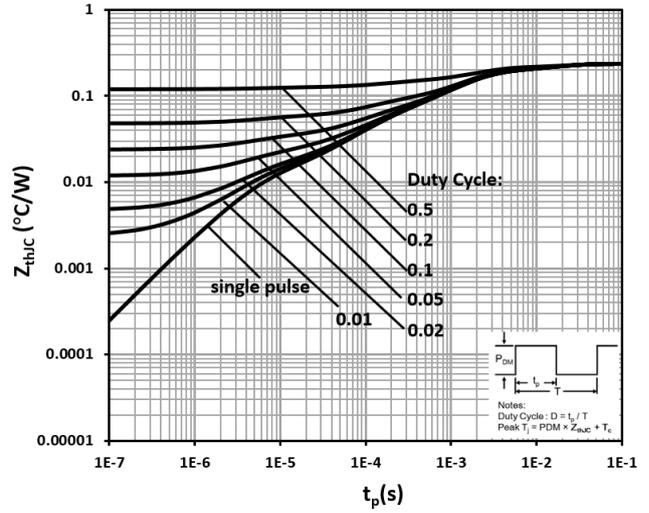


Fig. 18 Max. Transient Thermal Impedance

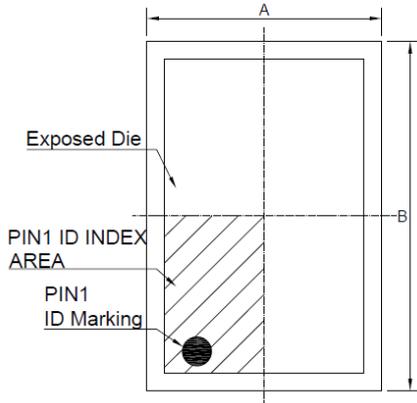


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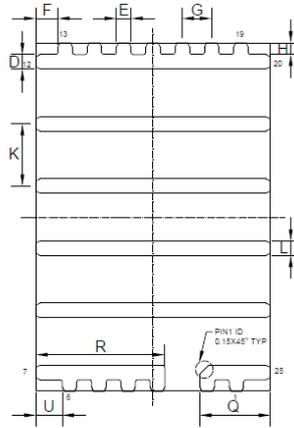
100V Enhancement-mode GaN Power Transistor

10. Package outlines

Package Reference

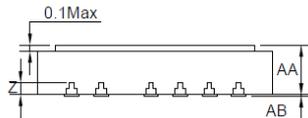


TOP VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	5.9	6.0	6.1	
D	0.20	0.25	0.30	3X
E	0.20	0.25	0.30	13X
F	0.375 REF			2X
G	0.5 BASIC			10X
H	0.2 REF			3X
K	1.07 BASIC			6X
L	0.20	0.25	0.30	4X
Q	1.1	1.2	1.3	
R	2.1	2.2	2.3	
U	0.45 REF			2X
Z	0.203 REF			
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	



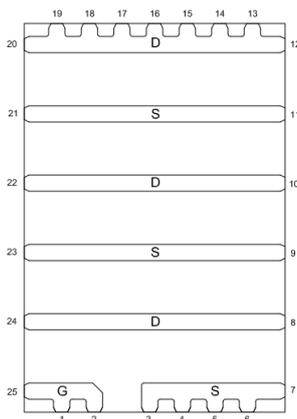
SIDE VIEW

NOTE:

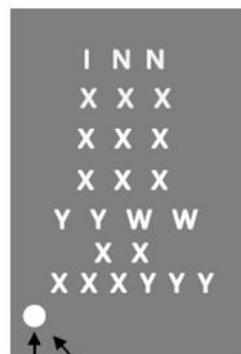
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

Pin information:

Marking Reference:



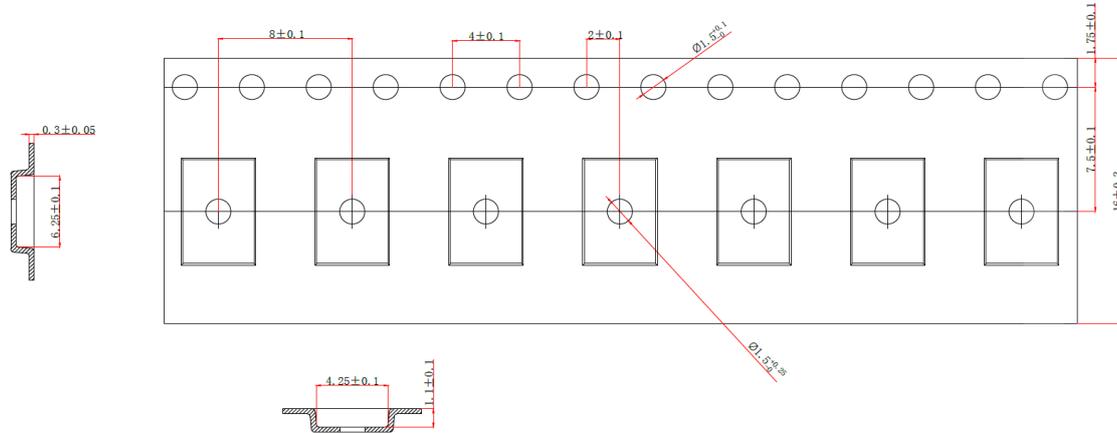
TOP VIEW



Gate Position
Die Orientation Dot

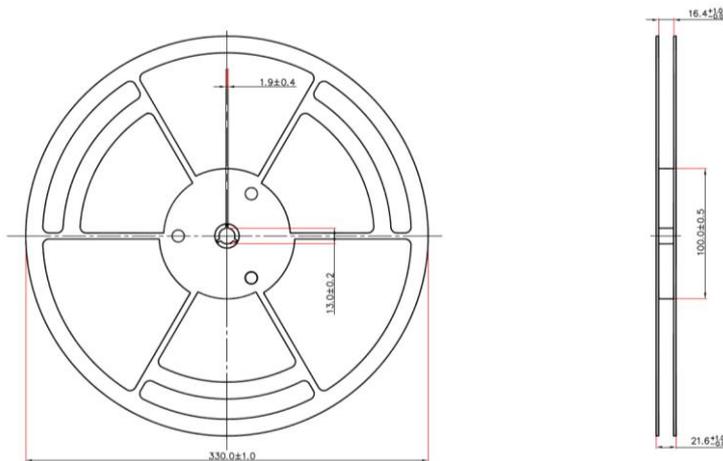
Row	Description	Example
Row1	Company name	INN
Row2	Product code	XXX
Row3	Lot Code	XXX
Row4		XXX
Row5	Date code	YYWW
Row6	Wafer ID	XX
Row7	Location ID	XXXYYY

11. Reel information



NOTES:

1. CARRIER TAPE COLOR: BLACK.
2. COVER TAPE WIDTH: 13.3±0.10.
3. COVER TAPE COLOR: TRANSPARENT.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5. CAMBER NOT TO EXCEED 1MM IN 100MM.
6. MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7. ALL DIMS IN MM.
8. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.

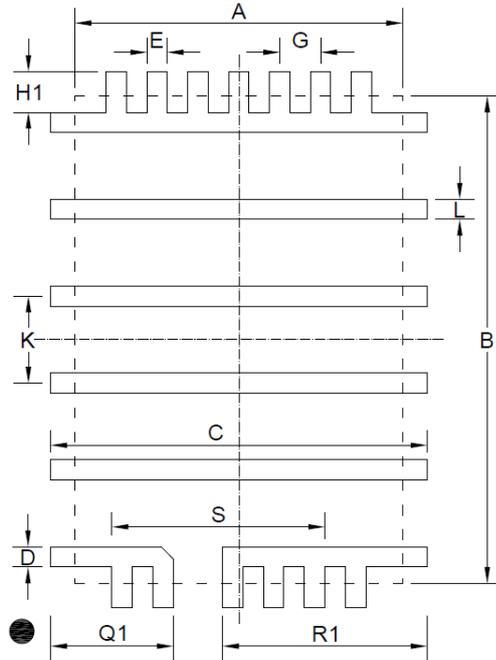


NOTES:

1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW:

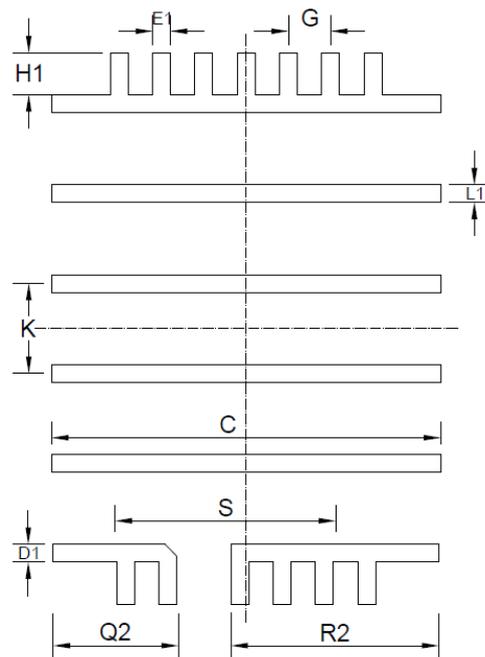
12. Land pattern

Recommended land pattern



SYMBOL	MILLIMETER	NOTE
A	4.0	
B	6.0	
C	4.6	5X
D	0.25	3X
E	0.25	13X
G	0.5	10X
H1	0.5	13X
K	1.07	6X
L	0.25	4X
R1	2.5	
Q1	1.5	
S	2.6	

Recommended Stencil drawing



SYMBOL	MILLIMETER	NOTE
C	4.56	5X
D1	0.21	3X
E1	0.21	13X
G	0.5	10X
H1	0.5	13X
K	1.07	6X
L1	0.21	4X
R2	2.46	
Q2	1.46	
S	2.6	

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-02-29	1.0 Version Release

Important Notice

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