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# FC4150F512 Data Sheet

Rev. A2

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# Chapter 1 Introduction

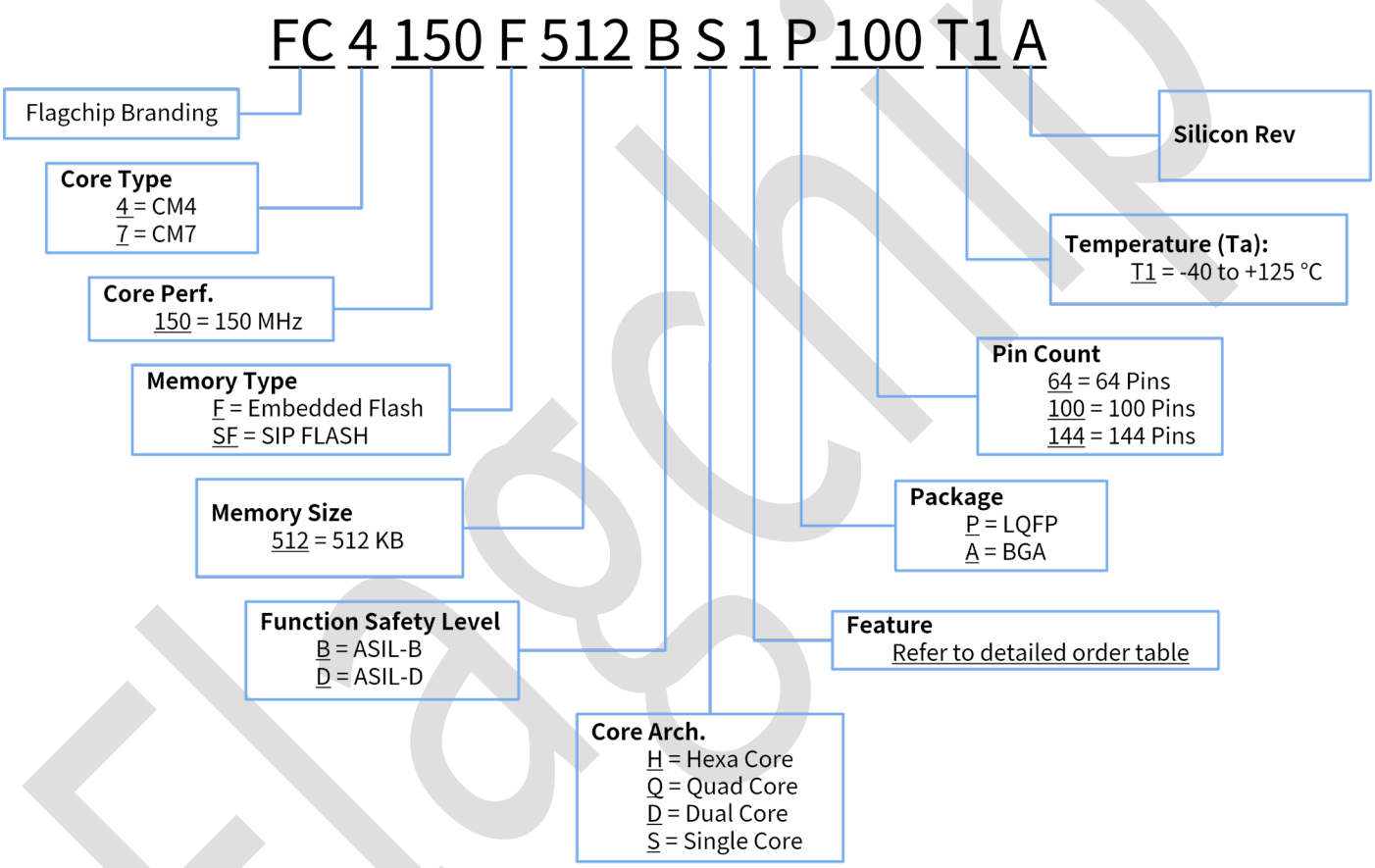
This data sheet provides the ordering information, electrical specifications, package information, and pinout data of the Flagchip FC4150F512 microcontroller (MCU).

## 1.1 Part Ordering

### 1.1.1 Ordering Information

The ordering of the Flagchip MCU follows the rules below. For detailed part information, refer to the Flagchip company.

**Figure 1. Ordering information**




***Note:*** Not all part number combinations are available.

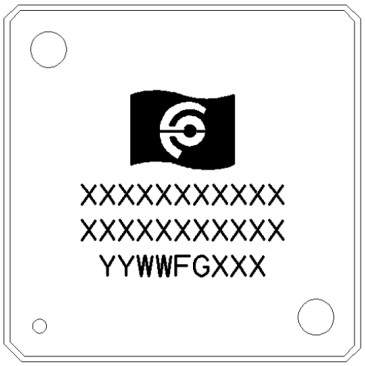
### 1.1.2 Orderable Part Number

The FC4150 series microcontrollers are ASIL B certified according to ISO 26262.

Refer to the attached *FC4150F512_Orderable_Part_Number_List_A2.xlsx* for a list of standard orderable part numbers.

## 1.2 Marking Rule

The followings are the schematic diagram and the picture of a FC4150 chip.





Marking rules of the FC4150 family are listed in the table below.

| Row | Step | Content | Description | Fixed/Dynamic | Align |
|---|---|---|---|---|---|
| 1 | 1 | logo (LL006758.LOG) | Logo | Fixed | Center |
| 2 | 1 | XXXXXXXXXX | Part number | Dynamic | Center |
| 3 | 1 | XXXXXXXXXX | Part number | Dynamic | Center |
| 4 | 1 | YYWW | Date code | Dynamic | Left |
| 4 | 2 | FGXX | Lot schedule number | Dynamic | Left |
| 4 | 3 | X | Engineering information | Optional | Left |

## 1.3 Abbreviations

The following abbreviations are used in this document.

| No. | Abbreviation | Description |
|---|---|---|
| 1. | ADC | Analog-to-Digital Converter |
| 2. | AFCB | Advanced Flagchip Bus (APB Bridge) |
| 3. | AONTIMER | Always-on Timer |
| 4. | APB | Advanced Peripheral Bus |
| 5. | AVB | Audio Video Bridging |
| 6. | CAN | Controller Area Network |
| 7. | CBC | Cipher Block Chaining |
| 8. | CGC | Clock Gating Control |
| 9. | CRC | Cyclic Redundancy Check |
| 10. | DAC | Digital-to-Analog Converter |
| 11. | DMA | Direct Memory Access |
| 12. | DP | Debug Port |
| 13. | DSP | Digital Signal Processing |
| 14. | DWT | Data Watchpoint and Trace |
| 15. | ECB | Electronic Codebook Book |
| 16. | ECC | Error Correction Code |
| 17. | ERM | Error Reporting Module |
| 18. | ESD | Electrostatic Discharge |

| No. | Abbreviation | Description |
|---|---|---|
| 19. | FCIIC | Flagchip (FC) Inter-Integrated Circuit |
| 20. | FCPIT | Flagchip (FC) Programmable Interrupt Timer |
| 21. | FCSPI | Flagchip (FC) Serial Peripheral Interface |
| 22. | FCUART | Flagchip (FC) Universal Asynchronous Receiver Transmitter |
| 23. | FIRC | Fast Internal Reference Clock |
| 24. | FMC | Flash Memory Controller |
| 25. | FOSC | Fast Oscillator |
| 26. | FPB | Flash Patch and Breakpoint |
| 27. | FPM | Full Performance Mode |
| 28. | FPU | Floating Point Unit |
| 29. | FTU | Flexible Timer Unit |
| 30. | FWM | Function Safety Watchdog Monitor |
| 31. | GPIO | General-Purpose Input/Output |
| 32. | HMI | Human-Machine Interface |
| 33. | HSM | Hardware Secure Module |
| 34. | HVD | High-Voltage Detect |
| 35. | I2S | Inter-IC Sound |
| 36. | IIC/I2C | Inter-Integrated Circuit |
| 37. | IRC | Internal Reference Cock |
| 38. | ISM | Interface Safety Monitor |
| 39. | ITM | Instrumentation Trace Macrocell |
| 40. | LDO | Low Dropout |
| 41. | LIN | Local Interconnect Network |
| 42. | LVD | Low-Voltage Detect |
| 43. | LVR | Low-Voltage Reset |
| 44. | MAP | Memory Access Protection |
| 45. | MPU | Memory Protection Unit |
| 46. | NMI | Non-maskable Interrupt |
| 47. | NVM | Non-Volatile Memory |
| 48. | OSC | Oscillator |
| 49. | PCC | Peripheral Clock Controller |
| 50. | PIT | Programmable Interrupt Timer |
| 51. | PLL | Phase-Locked Loop |
| 52. | PMC | Power Management Controller |
| 53. | POR | Power-on Reset |
| 54. | PWM | Pulse Width Modulation |
| 55. | RCM | Reset Control Module |
| 56. | RPM | Reduce Power Mode |
| 57. | RTC | Real-Time Clock |
| 58. | SAR | Successive Approximation |
| 59. | SCG | System Clock Generator |

| No. | Abbreviation | Description |
|---|---|---|
| 60. | SIRC | Slow Internal Reference Clock |
| 61. | SOSC | Slow Oscillator |
| 62. | SPI | Serial Peripheral Interface |
| 63. | SWD | Serial Wire Debug |
| 64. | SWJ-DP | Serial Wire/JTAG Debug Port |
| 65. | TAP | Test Access Port |
| 66. | TCM | Tightly-Coupled Memory |
| 67. | TPIU | Trace Port Interface Unit |
| 68. | TRGSEL | Trigger Select |
| 69. | UART | Universal Asynchronous Receiver and Transmitter |
| 70. | VCO | Voltage-Controlled Oscillator |
| 71. | WDOG | Watchdog |
| 72. | WKU | Wake-up Unit |

# Chapter 2 Features

This chapter summarizes the FC4150F512 features. For detailed information, refer to the FC4150 Reference Manual.

**Figure 2. FC4150F512 block diagram**


* Optional CAN FD support

***Note:*** Not all features in this block diagram are available on all parts, refer to the Reference Manual for details.

- **Operating Environment**
  - Voltage range: 3.0 V to 5.5 V
  - Ambient temperature ($T_A$) range: - 40°C to + 125°C; junction temperature ($T_J$) range: - 40°C to + 150°C
- **Arm Cortex-M4F Core**
  - 150 MHz frequency with 2.66 Dhrystone MIPS per MHz
  - Armv7 Architecture and Thumb-2 ISA
  - Digital Signal Processing (DSP) instruction
  - Single-Precision Floating Point Unit (FPU)
  - Support Memory Protection Unit (MPU) with 8 regions
- **16-channel Direct Memory Access (DMA) with selected DMA source**
- **Clock Sources**
  - 16 - 48 MHz Fast Oscillator (FOSC) with up to 50 MHz DC external input clock in bypass mode
  - 32 kHz Slow Oscillator (SOSC)
  - 96 MHz Fast Internal RC Oscillator (FIRC96M)
  - 12 MHz Slow Internal RC Oscillator (SIRC12M)
  - 32 kHz Slow Internal RC Oscillator (SIRC32k)
  - Up to 200 MHz Phased Lock Loop (PLL0) with reference from FIRC48M or FOSC
- **Power Management**
  - Four power modes: RUN, WAIT, STOP and Standby. Optional 64 KB RAM retention in standby mode
- **Memory**
  - Up to 512 KB program flash memory with Error Correction Code (ECC)
  - Up to 128 KB SRAM with ECC
  - 8 KB instruction cache for Flash
  - 96 KB ROM with CM4 core self-test/Flash program & erase/ Hardware Secure Module (HSM) APIs

- **Analog**
  - Up to two 12-bit Successive Approximation (SAR) Analog-to-Digital Converters (ADCs) with up to 32 channel analog inputs per module
  - Up to three Analog Comparators (CMPs) with internal 8-bit Digital-to-Analog Converter (DAC)
- **Debug Functionality**
  - Serial Wire/JTAG Debug Port (SWJ-DP) combines
  - Data Watchpoint and Trace (DWT)
  - Instrumentation Trace Macrocell (ITM)
  - Trace Port Interface Unit (TPIU)
  - Flash Patch and Breakpoint (FPB) Unit
  - JTAG Test Access Port (TAP) and boundary scan support
- **Human-Machine Interface (HMI)**
  - Up to 120 GPIO pins with interrupt support
  - Non-maskable Interrupt (NMI)
  - GPIO input/output interface
- **Communications Interfaces**
  - Up to six FC Universal Asynchronous Receiver/Transmitter (FCUART) modules with LIN support
  - Up to four FC Serial Peripheral Interface (FCSPI) modules, support 1/2/4 data lines and master/slave mode
  - Up to two FC Inter-Integrated Circuit (FCIIC) modules
  - Up to six FLEXCAN modules with CAN FD (optional) and PNET support on FLEXCAN0-2
  - Support two I2S modules
  - Support four TRGSELs for on-chip bus connection
  - Lookup Unit (LU) module with 4 lookup tables.
- **Safety and Security**
  - Hardware Secure Module (HSM) with crypto algorithms including AES/SM4/ECC/RSA/SHA/SM3/SM2/SM9
  - CCM/GCM/ECB/CTR/CBC etc. mode
  - Support random number generation and pseudo random number generation
  - Key import/export management
  - ECC on flash and SRAM memories
  - Memory Access Protection (MAP) on system SRAM
  - Peripheral Access Protection on APB bridge (AFCB)
  - Cyclic Redundancy Check (CRC) module
  - Up to two Internal watchdogs (WDOG) with window function
  - FunSa Watchdog Monitor (FWM) module
  - Interface Safety Monitor (ISM) module to monitor the critical signals' delay/period/duty etc.
  - CM4 core self-test API in ROM code
- **Timers**
  - Up to six Flexible Timer Unit (FTU) modules with IC/OC/PWM function
  - One Always-on Timer (AONTIMER) with standby wake up capability
  - Two Programmable Timers (PTIMERs)
  - One FC Programmable Interrupt Timer (FCPIT) with 4 channels
  - One Real-Time Clock (RTC)
- **Package**: 64LQFP, 100LQFP, and 144LQFP package options

- **Qualification**:
  - ASIL B certified according to ISO 26262
  - AEC-Q100/Q006 Grade 1 (-40°C to 125°C)

# Chapter 3 General

## 3.1 Absolute Maximum Ratings

The table below lists the maximum allowed conditions for the chip. To avoid the chip damage, the user needs to make sure the conditions are met.

**Table 1. Absolute maximum ratings**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD\_HV}$ | 3.0 V - 5.5 V input supply voltage | -0.3 | 6.0[1] | V |
| $V_{REFH}$ | 3.3 V - 5.0 V high reference voltage | -0.3 | 6.0[1] | V |
| $I_{INJPAD\_DC\_ABS}$ | Continuous DC input current (positive / negative) that can be injected into an I/O pin | - | 3 | mA |
| $V_{IN\_DC}$ | Continuous DC Voltage on any I/O pin with respect to $V_{SS}$ | -0.8 | 6.0[1] | V |
| $I_{INJSUM\_DC\_ABS}$ | Sum of injected currents on all the pins (Continuous DC limit, positive / negative) | - | 25[2] | mA |
| $T_{ramp\_MCU}$ | MCU supply ramp rate | - | 100 V/ms | - |
| $T_A$ | Ambient temperature | -40 | 125 | °C |
| $T_{STG}$ | Storage temperature | -55 | 165 | °C |
| $V_{IN\_TRANSIENT}$ | Transient overshoot voltage allowed on I/O pin beyond $V_{IN\_DC\ limit}$ | - | 6.8 | V |

1. Operation with the 6.0 V maximum is allowed for 10 hours over lifetime.
2. The maximum value is based on VDD_HV_A = VDD_HV_B = 5V condition and continuous pins DC injection current includes sum of injection currents of 16 continuous pins.

***Note:*** For inject current, the user needs to make sure that it won't cause issue if the inject current is above the chip self-power consumption (like standby/stop mode). Otherwise, it may cause damage.

## 3.2 Operation Condition

The table below lists the chip operation condition. To meet the design specifications, these conditions need to be met.

***Note:*** VDD_HV means the supply such as VDD_HV_A/VDD_HV_B.

**Table 2. Operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD\_HV}$ | Supply voltage | 3.0 | 5.5 | V |
| $V_{DD\_OFF}$ | Voltage allowed to be developed on $V_{DD\_HVA}$ pin when it is not powered from any external power supply source. | 0 | 0.1 | V |
| $V_{DDA}$ | Analog supply voltage | 3.0 | 5.5 | V |
| $V_{DD\_HV} - V_{DDA}$ | $V_{DD\_HV}$ to $V_{DDA}$ differential voltage | -0.1 | 0.1 | V |
| $V_{REFH}$ | ADC reference voltage high | 3.0 | $V_{DDA}$ + 0.1 | V |
| $V_{REFL}$ | ADC reference voltage low | -0.1 | 0.1 | V |
| $I_{INJPAD\_DC\_OP}$ | Continuous DC input current (positive / negative) that can be injected into an I/O pin | -1 | +1 | mA |

**Table 2. Operating requirements (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{INJSUM\_DC\_OP}$ | Continuous total DC input current that can be injected across all I/O pins | - | 5 | mA |
| $T_{pulse}$ | Reset/NMI input analog filter pulse width | 42 | - | ns |

## 3.3 Thermal Operating Condition

**Table 3. Thermal operating condition**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | -40 | - | 125 | °C | |
| $T_J$ | Junction temperature | -40 | - | 150 | °C | |

## 3.4 Clock Operating Condition

The table below lists the maximum functional clocks of modules. For the IO-related max clock frequency, refer to each IPs electrical specification. For the SCG DIVH/M/L output, it should be not above the 150 MHz/75 MHz/37.5 MHz range.

**Table 4. Max. functional clock of modules**

| Module/Peripheral | Max. Functional Clock (for STA) | Notes |
|---|---|---|
| **CPU & System Modules** | | |
| CM4 | 150 MHz | |
| DMA | 150 MHz | |
| FWM | 75 MHz | |
| WDOGx | 75 MHz | |
| WKU | 75 MHz | |
| RCM | 75 MHz | |
| SCG | - | |
| PCC | - | |
| TRGSELx | 75 MHz | |
| **Memory Modules** | | |
| ROM | 150 MHz | |
| TCM | 150 MHz | |
| FMC | 150 MHz | |
| FC | 150 MHz | |
| **Security Modules** | | |
| CRC | 150 MHz | |
| HSM | 75 MHz | |
| **Communication Modules** | | |
| FCSPIx | 75 MHz | |
| FCUARTx | 75 MHz | |
| FCIICx | 75 MHz | |

**Table 4. Max functional clock of modules (continued)**

| Module/Peripheral | Max. Functional Clock (for STA) | Notes |
|---|---|---|
| FLEXCAN0-5 | 150 MHz | |
| **Timer Modules** | | |
| AONTIMER0 | 75 MHz | |
| FCPIT0 | 75 MHz | |
| FTU0-5 | 150 MHz | |
| RTC | 32 kHz | |
| PTIMER0-1 | 150 MHz | |
| **HMI Modules** | | |
| GPIOx | 150 MHz | |
| PORTx | 75 MHz | |
| **Analog Modules** | | |
| ADCx | 20 MHz | |
| CMPx | 75 MHz | |
| PMC | 75 MHz | |

## 3.5 LVR, LVD, HVD, and POR Operating Requirements

The chip supports monitors including Power-on Reset (POR)/ Low-Voltage Reset (LVR)/ Low-Voltage Detect (LVD) on the VDD_HV supply.

**Table 5. LVR/LVD/HVD and POR**

| VDD_HV_A/B supply HVD, LVD and POR Operating Ratings | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| $V_{POR}$ | POR re-arm voltage | 1.1 | 1.6 | 2.1 | V | |
| $V_{LVR\_VDD\_HV}$ | LVR on $V_{DD\_HV\_A/B}$ | 2.75 | 2.85 | 2.95 | V | |
| $V_{HVD\_VDD\_HV}$ | HVD on $V_{DD\_HV\_A/B}$ | 5.7 | 5.85 | 6 | V | |
| $V_{LVD\_VDD\_HV}$ | LVD on $V_{DD\_HV\_A/B}$ | 4.2 | 4.35 | 4.5 | V | |
| $V_{HYS}$ | Hysteresis Voltage | - | 0.04 | 0.1 | V | |
| $V_{BG}$ | Bandgap voltage reference voltage | 1.164 | 1.2 | 1.236 | V | |

## 3.6 Power Mode Transition

The table below lists the different power mode transition time.

**Table 6. Power mode transition time**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, the amount of time from the point VDD reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip. | - | 200 | - | µs |
| $t_{STBtoR}$ | Standby → RUN (First code) | - | 130 | - | µs |
| $t_{STtoR}$ | STOP → RUN (FIRC and SIRC are enabled in Stop mode) | - | 3 | - | µs |
| $t_{RtoST}$ | RUN → STOP | - | 5 | - | µs |
| $t_{RtoSTB}$ | RUN → Standby | - | 12 | - | µs |
| $t_{REStoR}$ | Pin reset →RUN (First code) | - | 2 | - | µs |

## 3.7 Chip IDD

The chip supports four power modes: RUN/WAIT/STOP/Standby. During standby mode, the V25 Low Dropout (LDO) and SIRC12M/FOSC etc. can be optionally on. Both code RAM and data RAM can optionally retain 32 KB SRAM during standby mode. Refer to the Reference Manual for detailed settings.

The table below lists the chip RUN IDD current. The peripheral enabled/disabled here means enabling/disabling the peripherals' clock gating control (CGC).

**Table 7. Chip RUN IDD**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{dd\_active}$ | Active mode current - all peripherals disabled, while1, 150 MHz/75 MHz for Core/Bus, Cache enable, 25°C | - | 23.6 | 25.9 | mA | |
| | Active mode current - all peripherals enabled and clock switch 150 MHz PLL0 output, while1, 150 MHz/75 MHz for Core/Bus, Cache enable, 25°C | - | 33.8 | 36.1 | mA | |
| | Active mode current - all peripherals enabled and clock switch 150 MHz PLL0 output, while1, 150 MHz/75 MHz for Core/Bus, Cache enable, 125°C | - | 41.9 | 75.1 | mA | |
| $I_{dd\_wait}$ | Wait mode – all peripherals enable and clock switch 150 MHz PLL0 output, 25°C | - | 25.5 | 27.8 | mA | |
| | Wait mode – all peripherals enable and clock switch 150 MHz PLL0 output, 105°C | - | 29.5 | 62.7 | mA | |
| | Wait mode – all peripherals enable and clock switch 150 MHz PLL0 output, 125°C | - | 32.9 | 66.1 | mA | |

1. Typical value indicates the typical silicon process and the average current values at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0 V, and VDD_HV_B = 5.0 V.

**Table 8. Chip low power IDD**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{dd\_stop}$ | STOP Mode, 25°C | - | 2.6 | 4.2 | mA | |
| | STOP Mode, 105°C | - | 5.8 | 22.1 | mA | |
| | STOP Mode, 125°C | - | 8.7 | 36.2 | mA | |
| $I_{dd\_standby}$ | Standby Mode, all 64K RAM retention, 25°C | - | 59.7 | 122.7 | µA | |
| | Standby Mode, only 32K RAM retention, 25°C | - | 52.0 | 115.0 | µA | |
| | Standby Mode, no RAM retention, 25°C | - | 44.8 | 107.8 | µA | |
| | Standby Mode, no RAM retention, 125°C | - | 453.6 | 2922.7 | µA | |
| | Standby Mode, no RAM retention, SIRC12M Enable, 25°C | - | 161.5 | 224.5 | µA | |
| | Standby Mode, no RAM retention, SIRC32K Enable, 25°C | - | 46.1 | 109.1 | µA | |

1. Typical value indicates the typical silicon process and the average current values at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0 V, and VDD_HV_B = 5.0 V.

## 3.8 PMC Internal LDO

The chip contains two LDO supply outputs: V25 and V11. Both V25 and V11 support the Full Performance Mode (FPM) and Reduce Power Mode (RPM). External cap needs to be put on the V25/V11 pin to make sure LDO function works as expected.

**Table 9. V25 LDO specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD\_HV\_A}$ | V25 input supply voltage | 3 | - | 5.5 | V | |
| V25 | V25 regulator output voltage | 2.25 | - | 2.75 | V | |
| $C_{out}$ | External output capacitor | - | 220 | - | nF | |

**Table 10. Core LDO specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD\_HV\_A}$ | V11 input supply voltage | 3 | - | 5.5 | V | |
| V11 | V11 regulator output voltage | 1.06 | - | 1.21 | V | |
| $C_{out}$ | External output capacitor | - | 1.1 | 2.2 | µF | |

## 3.9 ESD Ratings

The Electrostatic Discharge (ESD) result follows the industry test standard.

**Table 11. ESD ratings**

| Symbol | Description | | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model (HBM) | | -2000 | 2000 | V | 1, 2, 3 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model (CDM) | All pins except the corner pins | -500 | 500 | V | 1, 3, 4 |
| | | Corner pins only | -750 | 750 | V | |
| $I_{LAT}$ | Latch-up current at ambient temperature of 125°C | | -100 | 100 | mA | 1, 3, 5 |

1. Device failure is defined as the situation where the device fails to meet the specification requirements after being exposed to ESD pulses.
2. This parameter is tested in compliance with AEC-Q100-002.
3. All ESD tests comply with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
4. This parameter is tested in compliance with AEC-Q100-011.
5. This parameter is tested in compliance with AEC-Q100-004.

# Chapter 4 I/O Parameter

## 4.1 IO DC Specification

The IO can work with supplies from 3.0 V to 5.5 V. The tables below list specifications for the supplies.

**Table 12. 3V IO DC specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.65*VDD_IO | - | - | V | |
| $V_{IL}$ | Input low voltage | - | - | 0.35*VDD_IO | V | |
| $V_{HYS}$ | Input hysteresis | 0.07*VDD_IO | - | - | V | |
| $V_{oh\_normal}$ | I/O current source capability with Ioh=4mA | VDD_IO - 0.68 | - | - | V | |
| $V_{ol\_normal}$ | I/O current sink capability with Iol=4mA | - | - | 0.712 | V | |
| $V_{oh\_fast}$ | I/O current source capability with Ioh=4mA and DSE=0 | VDD_IO - 0.78 | - | - | V | |
| $V_{ol\_fast}$ | I/O current sink capability with Iol=4mA and DSE=0 | - | - | 0.751 | V | |
| $V_{oh\_fast}$ | I/O current source capability with Ioh=8mA and DSE=1 | VDD_IO - 0.78 | - | - | V | |
| $V_{ol\_fast}$ | I/O current sink capability with Iol=8mA and DSE=1 | - | - | 0.751 | V | |
| $I_{PU}$ | Internal pullup current (Rload=0, output tie to VSS) | 65 | - | 124 | μA | |
| $I_{PD}$ | Internal pulldown current (Rload=0, output tie to VDD_IO) | 68 | - | 133 | μA | |

**Table 13. 5V IO DC specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.65*VDD_IO | - | - | V | |
| $V_{IL}$ | Input low voltage | - | - | 0.35*VDD_IO | V | |
| $V_{HYS}$ | Input hysteresis | 0.07*VDD_IO | - | - | V | |
| $V_{oh\_normal}$ | I/O current source capability with Ioh=4mA | VDD_IO - 0.68 | - | - | V | |
| $V_{ol\_normal}$ | I/O current sink capability with Iol=4mA | - | - | 0.46 | V | |
| $V_{oh\_fast}$ | I/O current source capability with Ioh=4mA and DSE=0 | VDD_IO - 0.5 | - | - | V | |
| $V_{ol\_fast}$ | I/O current sink capability with Iol = 4mA and DSE = 0 | - | - | 0.444 | V | |

**Table 13. 5V IO DC specification (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{oh\_fast}$ | I/O current source capability with Ioh = 8mA and DSE = 1 | VDD_IO - 0.5 | - | - | V | |
| $V_{ol\_fast}$ | I/O current sink capability with Iol = 8mA and DSE = 1 | - | - | 0.444 | V | |
| $I_{PU}$ | Internal pullup current (Rload = 0, output tie to VSS) | 107 | - | 213 | µA | |
| $I_{PD}$ | Internal pulldown current (Rload = 0, output tie to VDD_IO) | 110 | - | 210 | µA | |

## 4.2 IO AC Specification

The below is the IO AC specification, wherein the minimum value is based on 3.6 V/5.5 V/150°C condition and the maximum value is based on 3.0 V/4.5 V/-40°C condition. ***Note:*** The specification is based on simulation data.

**Table 14. 3V IO AC specification**

| Symbol | SRE | DSE | Rise Time (ns) | | Fall Time (ns) | | Capacitance (pF) |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{RFnormal}$ | 0 | | 2.12 | 8.82 | 2.3 | 8.64 | 25, 20%-80% r/f |
| $t_{RFnormal}$ | 1 | | 3.3 | 10.98 | 3.1 | 10.32 | 25, 20%-80% r/f |
| $t_{RFfast}$ | | 1 | 1.52 | 4.63 | 1.39 | 4.53 | 25, 20%-80% r/f |
| $t_{RFfast}$ | | 0 | 2.77 | 8.04 | 2.75 | 8.39 | 25, 20%-80% r/f |

**Table 15. 5V IO AC specification**

| Symbol | SRE | DSE | Rise Time (ns) | | Fall Time (ns) | | Capacitance (pF) |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{RFnormal}$ | 0 | | 2.16 | 6.41 | 2.15 | 6.08 | 25, 20%-80% r/f |
| $t_{RFnormal}$ | 1 | | 2.67 | 7.82 | 2.43 | 7.19 | 25, 20%-80% r/f |
| $t_{RFfast}$ | | 1 | 1.14 | 3.18 | 1.11 | 3.09 | 25, 20%-80% r/f |
| $t_{RFfast}$ | | 0 | 2.16 | 6.7 | 2.31 | 6.06 | 25, 20%-80% r/f |

# Chapter 5 Clock Specification

## 5.1 FOSC Specification

The Fast Oscillator (FOSC) supports the range of 16 - 48 MHz. To avoid the startup noise impact, software should wait enough time before using the clock. The FOSC can keep enabled during standby/stop mode.

**Figure 3. Crystal connection diagram**

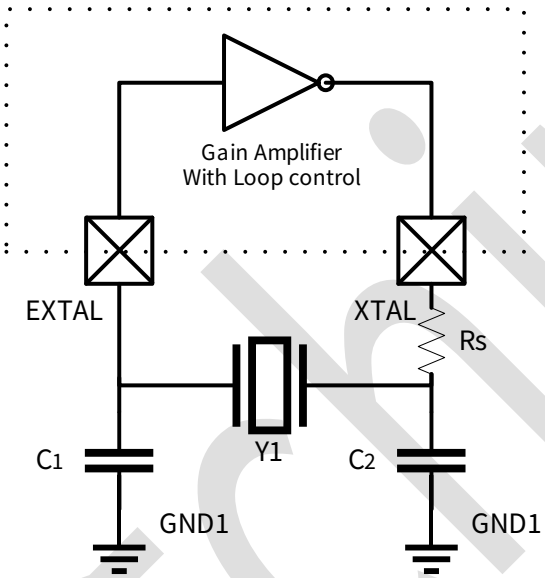



**Table 16. FOSC specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc}$ | Oscillator crystal or resonator frequency | 16 | 40 | 48 | MHz | - |
| $T_{st\_osc}$ | Startup time | - | 600 | - | μs | - |
| $I_{dd\_osc}$ | Current consumption | - | 1200 | - | μA | - |
| GM | Gain Amplifier transconductance | 11.07 | - | 26.24 | mA/V | Select max GM setting |

For crystal selection, usually require $g_m > 5*g_{mcrit}$.

- Formula $\mathbf{gain_{margin} = g_m / g_{mcrit}}$, where:
  - $g_m$ is the oscillator transconductance specified in the data sheet. Note that the oscillator transconductance is in the range of a dozen of mA/V.
  - $g_{mcrit}$ is defined as the minimal transconductance of an oscillator required to maintain a stable oscillation when it is a part of the oscillation loop for which this parameter is relevant.
  - $g_{mcrit}$ is computed from oscillation-loop passive components parameters (Rs is 0 here).
- $\mathbf{g_{mcrit} = 4 \times ESR (2\pi F)^2 \times (C_0 + CL)^2}$, where:
  - ESR is the equivalent series resistance.
  - $C_0$ is the crystal shunt capacitance.
  - $C_L$ is the crystal nominal load capacitance, $C_L = Cs + [C1*C2/(C1+C2)]$ (Note: C1 should be equal to C2).
  - F is the crystal nominal oscillation frequency.

## 5.2 SOSC Specification

The Slow Oscillator (SOSC) supports the 32.768 kHz crystal. To avoid the startup noise impact, software should wait enough time before using the clock. The SOSC will keep enabled during system reset. Only POR/LVD will reset the SOSC.

**Table 17. SOSC specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc32k}$ | Oscillator crystal or resonator frequency | - | 32.768 | - | kHz | |
| $T_{st\_osc32k}$ | Startup time | - | 1 | - | s | |
| $I_{dd\_osc32k}$ | Current consumption | - | 1.8 | - | μA | |
| GM | Gain Amplifier transconductance | 26 | - | 54.5 | μA/V | |

## 5.3 FIRC96M Specification

The FIRC96M is the default system clock after reset. FIRC96M provides two clock sources, one is 96 MHz and the other is 48 MHz. The 96 MHz clock can be selected as the system clock. The 48 MHz clock can be selected as the PLL reference clock and Flash program/erase clock. Software needs to make sure FIRC is enabled and 48 MHz clock output is enabled before a flash program/erase operation or selecting the FIRC as the PLL reference clock. After reset, the FIRC is enabled and both 96 MHz and 48 MHz clock output are enabled.

**Table 18. FIRC96M specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{firc96m}$ | firc96m clock frequency range | - | 96 | - | MHz | |
| $\Delta f_{firc96m}$ | Frequency Deviation with 1T trim | - | - | ±4 | $\%f_{firc96m}$ | |
| $T_{st\_firc96m}$ | Startup time (<20% accuracy), from disable | - | 2.4 | - | μs | |
| | Startup time (<1% accuracy) | - | 30 | - | μs | |

## 5.4 SIRC12M Specification

The SIRC12M is used for system low power mode entry. SIRC12M can keep enabled during standby mode. During RUN mode, SIRC12M is always enabled. Clock sources of WDOGx etc. can be selected from SIRC12M divider outputs.

**Table 19. SIRC12M specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{sirc12m}$ | SIRC12M clock frequency | - | 12 | - | MHz | |
| $\Delta f_{sirc12m}$ | Frequency Deviation with 1T trim | - | - | ±5 | $\%f_{sirc12m}$ | |
| $T_{st\_sirc12m}$ | Startup time from POR | - | 3 | - | μs | |

## 5.5 SIRC32k Specification

The SIRC32k can be used for low power wakeup source. It can keep enabled during standby mode.

**Table 20. SIRC32k specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{sirc32k}$ | SIRC32k clock frequency | - | 32 | - | kHz | |
| $\Delta f_{sirc32k}$ | Frequency Deviation with 1T trim | - | - | ±5 | $\%f_{sirc32k}$ | |
| $T_{st\_sirc32k}$ | Startup time from POR | - | - | 20 | μs | |

## 5.6 PLL0 Specification

The PLL0 can be used for the system clock. The PLL reference clock can select from FIRC96M (48 MHz output) or FOSC. Refer to the Reference Manual for detailed settings.

**Table 21. PLL0 specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{pll\_ref}$ | PLL reference frequency range | 2 | - | 16 | MHz | Reference clock after pre-divider |
| $f_{pll\_out}$ | PLL output frequency | 90 | - | 200 | MHz | VCO clock is 2x of this data |
| Duty | Duty cycle | 45 | - | 55 | % | |
| $I_{pll}$ | PLL operating current | - | 1.5 | - | mA | |
| $T_{pll}$ | Frequency 1% lock time from standby mode | - | 120 | - | μs | Polling lock bit by software, and assume reference clock is ready |
| | Frequency 1% lock time from disabled mode | - | 30 | - | μs | Polling lock bit by software, and assume reference clock is ready |

# Chapter 6 Non-Volatile Memory (NVM)

## 6.1 NVM Retention

**Table 22. NVM retention specification**

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Program/Erase (P/E) cycles | Number of program/erase cycles per block for 256 KB blocks using Sector Erase | - | 100K | - | - | Cycles | |
| | Number of program/erase cycles per block for 1 MB and 2 MB blocks using Sector Erase | - | 1K | - | - | Cycles | |
| Data Retention | Minimum data retention | Blocks with 0 - 1K P/E cycles | 20 | - | - | Years | |
| | | Blocks with 100K P/E cycles | 10 | - | - | Years | |

## 6.2 NVM Program/Erase Time

**Table 23. NVM program/erase time**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{2wpgm}$ | 2 words (64 bits) program time | - | 102 | - | μs | |
| $T_{32wpgm}$ | 32 words (1024 bits) program time | - | 358 | - | μs | |
| $T_{1kpgm}$ | 1K bytes sector program time | - | 2.8 | - | ms | |
| $T_{1kers}$ | 1K bytes sector erase time | - | 3.2 | - | ms | |
| $T_{256kers}$ | 256K block erase time | - | 24.5 | - | ms | |

***Note:*** The program/erase time will be influenced by temperature. The typical values here are measured at the beginning of the chip lifecycle and at the temperature of 25 °C.

## 6.3 NVM Max Read Timing

For FC4150F512, the maximum NVM read frequency is 37.5 MHz.

If system is configured as 150 MHz, the NVM read wait cycle needs to be set to 4 for FC4150F512.

# Chapter 7 Analog

## 7.1 12-bit SAR ADC Specification

The chip supports up to two 12-bit Successive Approximation (SAR) Analog-to-Digital Converters (ADCs). The specification below is based on minimum chip activity, and the external VRH is used. The below is the ADC specification.

**Table 24. ADC specification**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | ADC analog supply | 3 | - | 5.5 | V | |
| $V_{SSA}$ | ADC analog ground | -0.1 | 0 | 0.1 | V | |
| $V_{REFH}$ | ADC reference high | 3 | - | 5.5 | V | <=VDDA 2 |
| $V_{REFL}$ | ADC reference low | -0.1 | 0 | 0.1 | V | 2 |
| $V_{ADIN}$ | ADC input | $V_{REFL}$ | - | $V_{REFH}$ | V | |
| $C_{ADIN}$ | ADC input capacitance | - | 6.4 | - | pF | |
| $R_{ADIN}$ | ADC input resistance | - | 1.5 | - | KΩ | |
| $R_{AS}$ | Input source resistance | - | 1 | - | KΩ | |
| TUE | Total unadjusted error | - | ±4 | ±8 | LSB | 3 |
| $E_Q$ | Quantization error | - | ±1 | - | LSB | |
| ENOB | Effective number of bits with 1MSPS@12bit mode | - | 10.5 | - | bits | If VDD is < 4.5 V, the typical value is 10 bits. |
| SINAD | Signal-to-noise plus distortion | - | ENOB*6.02 + 1.76 | - | dB | @1kHz |
| $F_{ADCK}$ | ADC conversion clock frequency | 6 | - | 20 | MHz | |
| $I_{dd\_adc}$ | Supply current, single mode on $V_{REFH}$ | - | 0.5 | - | mA | |
| | Supply current, single mode on $V_{DDA}$ | - | 1.25 | - | mA | |
| $T_{su}$ | Start-up time | - | 5 | - | μs | |
| $T_{smp}$ | Sample time | 4/(FADCK) | - | 257/(FADCK) | - | |
| $C_{smp}$ | Sample cycles | 4 | - | 257 | cycles | |
| $C_{conv}$ | Conversion cycles | - | 12 | - | cycles | |
| | Conversion rate | - | - | 1.2 | MS/s | 4 |

1. Typical values assume VREFH = VDDA, Temp = 25 °C, ADC clock = 20 MHz, source impedance = 20 Ω, and input filter capacitor =10 nF unless otherwise stated. Typical values are used for reference only, not tested in production.
2. For packages without dedicated VREFH and VREFL pins, VREFH is internally tied to VDDA, and VREFL is internally tied to VSSA.
3. There are dead zones when signals near VREFH and VREFL.
4. Max. Conversion Rate = Max. ADC Clock Frequency / (Sample Cycles + Conversion Cycles). Note: Rounding down to the nearest tenth.
5. Appropriate decoupling capacitors to be used to filter noises on the supplies.
6. VSS and VREFL should be shorted on PCB design.

7. Above specifications are for direct channels which are based on 12-bit resolution. Additional mux channels performance may be degraded.
8. The ADC has a dead zone when input is close to VREFL or VREFH. The results here are obtained after calibration and removing the impact of this effect.

***Note:*** Due to triple bonding in lower pin packages, degradation might be seen in ADC parameters.

## 7.2 CMP Specification

The chip supports high-speed (HS) and low-power (LP) mode. The CMPx can work in standby mode.

**Table 25. CMP specification**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{dd\_cmp}$ | CMP operating current with HS mode | - | 130 | - | μA |
| | CMP operating current with LP mode | - | 6 | - | μA |
| $V_{input}$ | Analog input voltage | 0.1 | - | $V_{DDA}$ - 0.1 | V |
| $V_{input\_offset}$ | Analog input offset voltage with HS mode | - | ±2 | 40 | mV |
| | Analog input offset voltage with LP mode | - | ±4 | 40 | mV |
| HYS | Analog comparator hysteresis: | - | - | - | - |
| | Hyst = 00 | - | 0 | - | mV |
| | Hyst = 01 | - | 15 | - | mV |
| | Hyst = 10 | - | 30 | - | mV |
| | Hyst = 11 | - | 45 | - | mV |
| $T_{init}$ | Initialization delay | - | - | 30 | μs |
| $T_{prop}$ | Propagation delay, 100 mV over drive, supply > 3.0 V (HS mode) | - | 50 | 200 | ns |
| | Propagation delay, 100 mV over drive, supply > 3.0 V (LP mode) | - | 1.6 | 5 | μs |
| $V_{idd\_dac}$ | 8-bit DAC current adder | - | 10 | - | μA |
| INL | 8-bit DAC integral non-linearity | - | ±1 | ±3 | LSB |
| DNL | 8-bit DAC differential non-linearity | - | ±0.5 | ±1 | LSB |

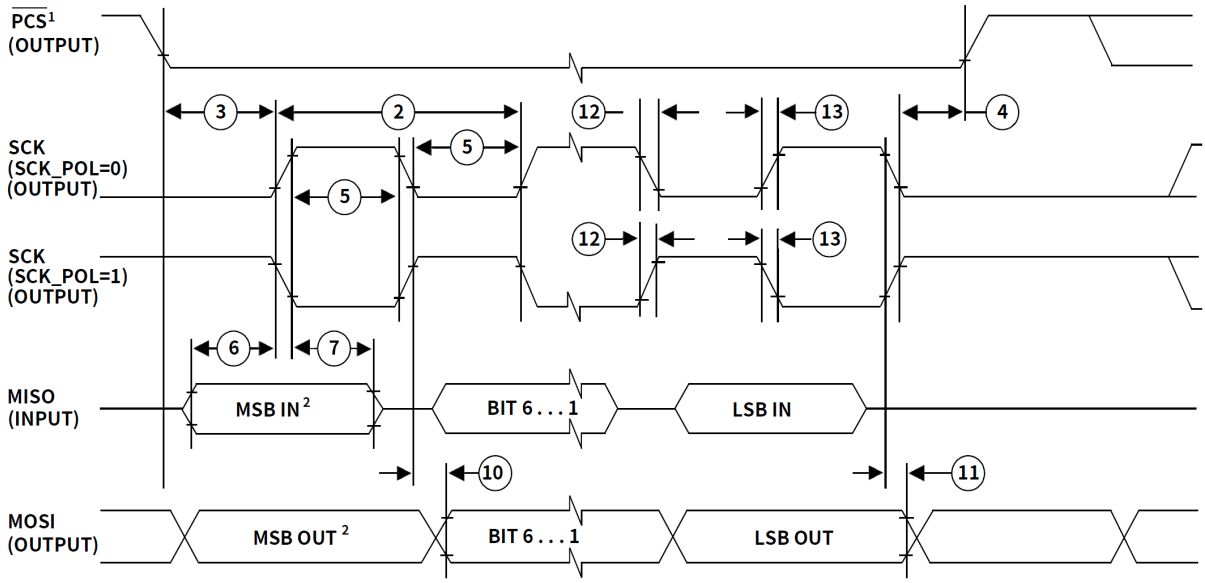
# Chapter 8 Peripherals

All peripherals' timings shown below are based on 25 pF external loading and input transitions of 1 ns. For normal pad, the SRE is set to 0; for fast pad, the DSE is set to 1. The rise/fall timing is based on 20% VDD_HV to 80% VDD_HV thresholds. Besides, the delay time is based on 50% VDD_HV to 50% VDD_HV thresholds.

## 8.1 FCSPI Specification

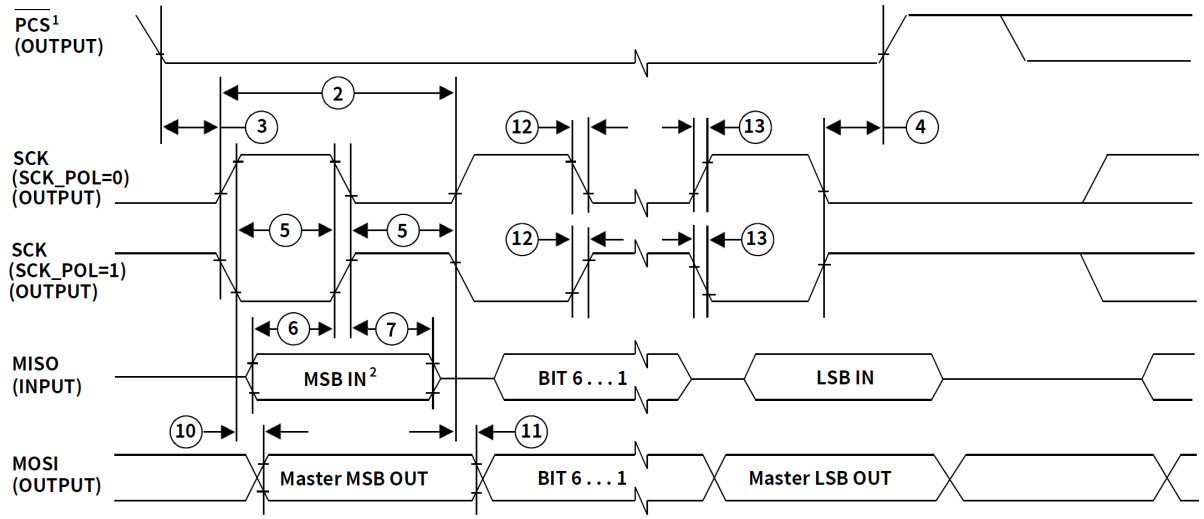
The FCSPI supports a configurable clock by writing the SCK_POL/SCK_PHA bits, as well as both master and slave mode. The figures below show the timing requirements in different settings.

**Figure 4. FCSPI master mode timing (SCK_PHA=0)**



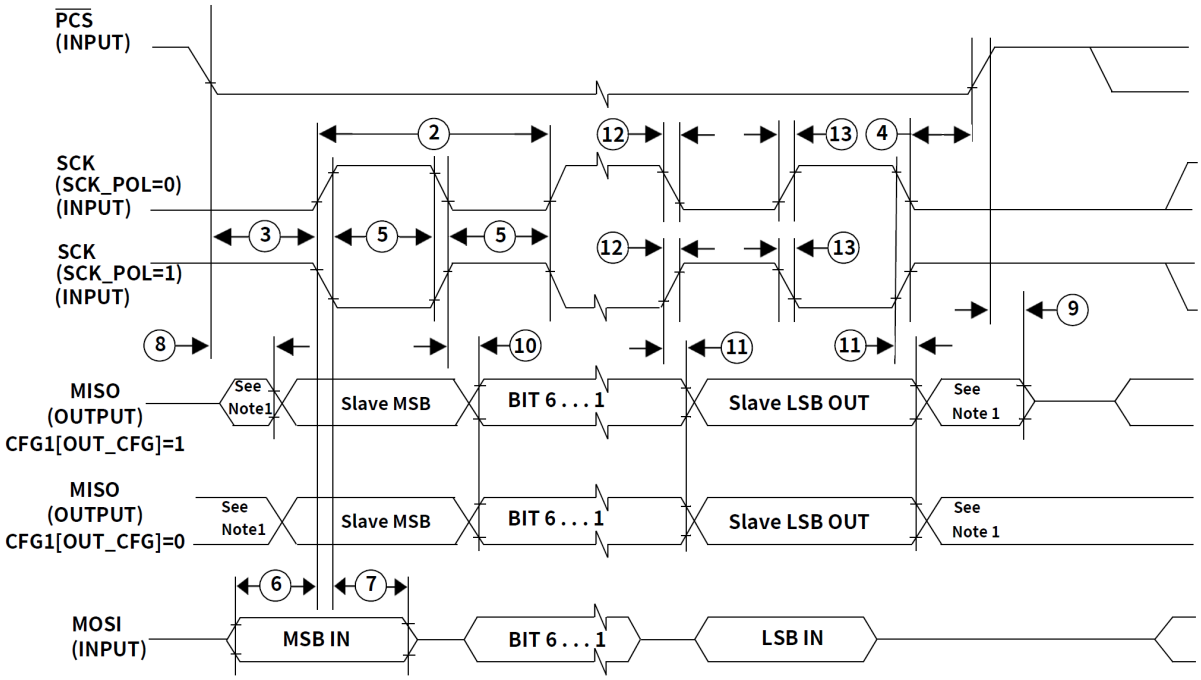

**Note:**
1. If configured as an output.

**Figure 5. FCSPI master mode timing (SCK_PHA=1)**



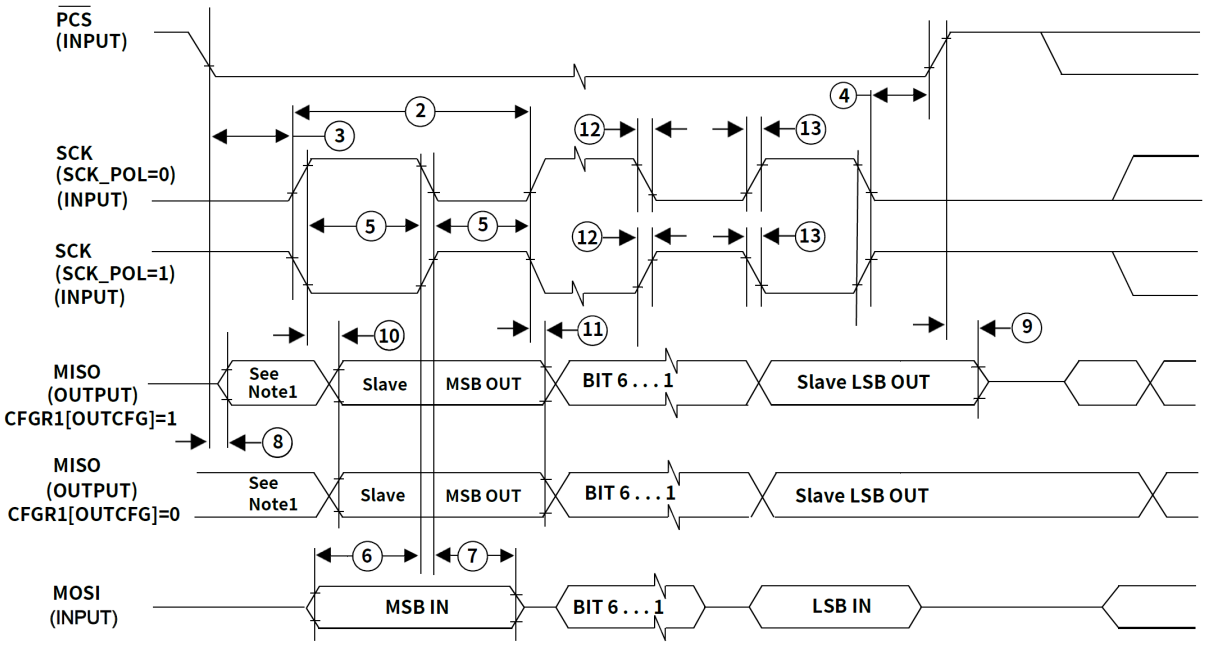

**Note:**
1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 6. FCSPI slave mode timing (SCK_PHA=0)**




Note:
1. The bus is driven but may not be equal to the valid serial data being sent.

**Figure 7. FCSPI slave mode timing (SCK_PHA=1)**




Note:
1.The bus is driven but may not be equal to the valid serial data being sent.

The below is the FCSPI 3.0-3.6V electrical specification.

**Table 26. FCSPI 3V specification**

| 3.0 - 3.6 V | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Normal Pad (master)** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation (loopback) | - | - | 15 | MHz | |
| | | Frequency of operation (internal clock) | - | - | 12.5 | MHz | |
| 2 | $t_{sck}$ | SCK period (loopback) | 66.7 | - | - | ns | |
| | | SCK period (internal clock) | 80 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time (loopback) | 6 | - | - | ns | |
| | | Data Setup time (internal clock) | 30 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time (loopback) | 5.5 | - | - | ns | |
| | | Data Hold time (internal clock) | 0 | - | - | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 5 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | -10 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |
| 13 | $t_{RFo}$ | Rise or Fall time (outputs) | 2.8 | - | 7 | ns | |
| | | | | | | | |
| **Fast Pad (master)** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation (loopback) | - | - | 20 | MHz | |
| | | Frequency of operation (internal clock) | - | - | 18.75 | MHz | |
| 2 | $t_{sck}$ | SCK period (loopback) | 50 | - | - | ns | |
| | | SCK period (internal clock) | 53.28 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time (loopback) | 4 | - | - | ns | |
| | | Data Setup time (internal clock) | 20 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time (loopback) | 5 | - | - | ns | |
| | | Data Hold time (internal clock) | 0 | - | - | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 5 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | -10 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |

**Table 26. FCSPI 3V specification (continued)**

| **Normal Pad (slave)** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation | - | - | 12.5 | MHz | |
| 2 | $t_{sck}$ | SCK period | 80 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time | 4 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time | 4 | - | - | ns | |
| 8 | $t_a$ | Slave access time | - | - | 40 | ns | |
| 9 | $t_{dis}$ | Slave MISO disable time | - | - | 40 | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 30 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | 4 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |
| 13 | $t_{RFo}$ | Rise or Fall time (outputs) | 2.8 | - | 7 | ns | |
| | | | | | | | |
| **Fast Pad (slave)** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation | - | - | 15 | MHz | |
| 2 | $t_{sck}$ | SCK period | 66.7 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time | 4 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time | 4 | - | - | ns | |
| 8 | $t_a$ | Slave access time | - | - | 33.3 | ns | |
| 9 | $t_{dis}$ | Slave MISO disable time | - | - | 33.3 | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 21 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | 4 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |
| 13 | $t_{RFo}$ | Rise or Fall time (outputs) | 1.8 | - | 8 | ns | |

The below is the FCSPI 4.5 to 5.5 V electrical specification.

**Table 27. FCSPI 5V specification**

| 4.5 - 5.5 V | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Normal Pad (master)** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation (loopback) | - | - | 18.75 | MHz | |
| | | Frequency of operation (internal clock) | - | - | 15 | MHz | |
| 2 | $t_{sck}$ | SCK period (loopback) | 53.28 | - | - | ns | |
| | | SCK period (internal clock) | 66.7 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time (loopback) | 5.5 | - | - | ns | |
| | | Data Setup time (internal clock) | 24 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time (loopback) | 5 | - | - | ns | |
| | | Data Hold time (internal clock) | 0 | - | - | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 5 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | -10 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |
| 13 | $t_{RFo}$ | Rise or Fall time (outputs) | 2.8 | - | 7 | ns | |
| | | | | | | | |
| **Fast Pad (master)** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation (loopback) | - | - | 24 | MHz | |
| | | Frequency of operation (internal clock) | - | - | 18.75 | MHz | |
| 2 | $t_{sck}$ | SCK period (loopback) | 41.67 | - | - | ns | |
| | | SCK period (internal clock) | 53.28 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time (loopback) | 4 | - | - | ns | |
| | | Data Setup time (internal clock) | 17 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time (loopback) | 5 | - | - | ns | |
| | | Data Hold time (internal clock) | 0 | - | - | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 5 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | -10 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |
| 13 | $t_{RFo}$ | Rise or Fall time (outputs) | 1.8 | - | 8 | ns | |

**Table 27. FCSPI 5V specification (continued)**

| **Normal Pad (slave)** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation | - | - | 12.5 | MHz | |
| 2 | $t_{sck}$ | SCK period | 80 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time | 4 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time | 4 | - | - | ns | |
| 8 | $t_a$ | Slave access time | - | - | 40 | ns | |
| 9 | $t_{dis}$ | Slave MISO disable time | - | - | 40 | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 25 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | 4 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |
| 13 | $t_{RFo}$ | Rise or Fall time (outputs) | 2.8 | - | 7 | ns | |
| | | | | | | | |
| **Fast Pad (slave)** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{op}$ | Frequency of operation | - | - | 20 | MHz | |
| 2 | $t_{sck}$ | SCK period | 50 | - | - | ns | |
| 3 | $t_{Lead}$ | Enable lead time | - | 1/2 | - | $t_{SCK}$ | |
| 4 | $t_{Lag}$ | Enable Lag time | - | 1/2 | - | $t_{SCK}$ | |
| 5 | $t_{wsck}$ | SCK high/low width | - | - | - | ns | |
| 6 | $t_{SU}$ | Data Setup time | 4 | - | - | ns | |
| 7 | $t_{HI}$ | Data Hold time | 4 | - | - | ns | |
| 8 | $t_a$ | Slave access time | - | - | 25 | ns | |
| 9 | $t_{dis}$ | Slave MISO disable time | - | - | 25 | ns | |
| 10 | $t_v$ | Data Valid (after SCK edge) | - | - | 18 | ns | |
| 11 | $t_{HO}$ | Data Hold time (outputs) | 4 | - | - | ns | |
| 12 | $t_{RFi}$ | Rise or Fall time (inputs) | 0.5 | - | 3 | ns | |
| 13 | $t_{RFo}$ | Rise or Fall time (outputs) | 1.8 | - | 8 | ns | |

## 8.2 I2S Specification

The figures below show the I2S0/1 timing diagram/requirement.

**Figure 8. I2S master mode timing diagram**

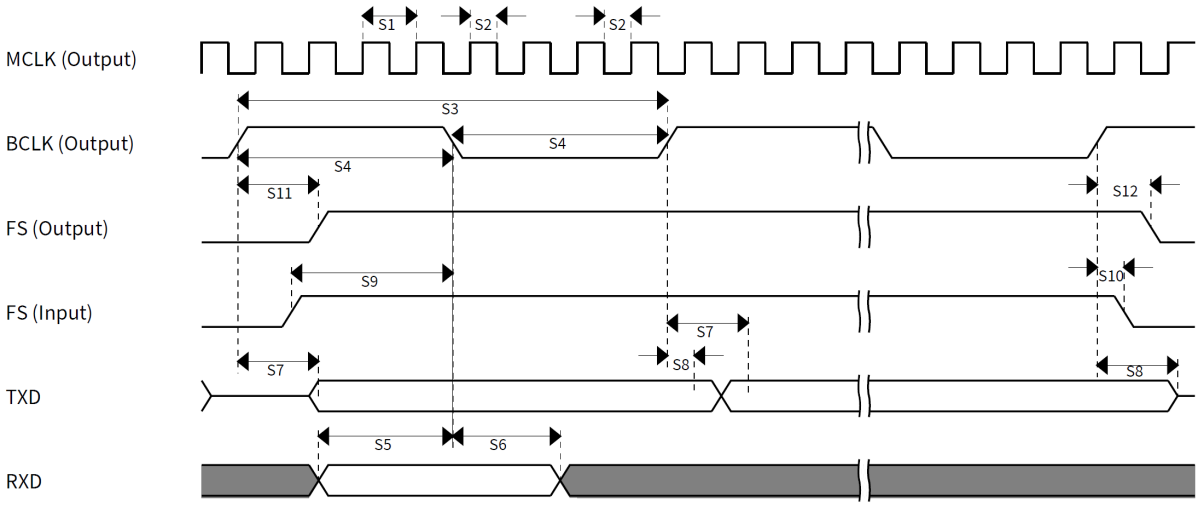



**Figure 9. I2S slave timing diagram**

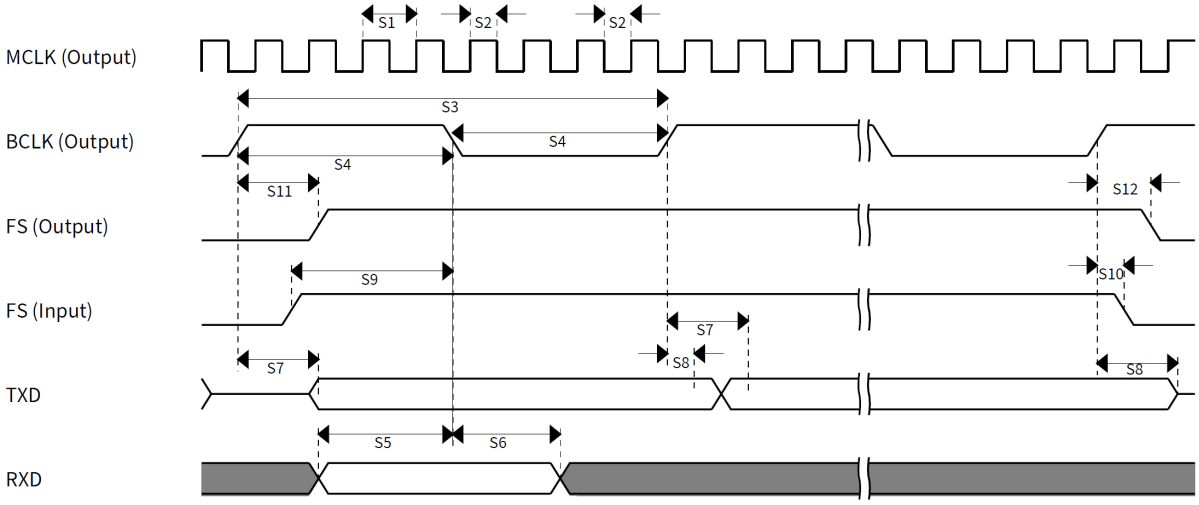



**Table 28. I2S electrical specification**

| I2S Master | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $S_1$ | I2S_MCLK cycle time | - | - | 40 | ns | - |
| 2 | $S_2$ | I2S_MCLK duty | 45% | - | 55% | - | - |
| 3 | $S_3$ | I2S_BCLK cycle time | 80 | - | - | ns | - |
| 4 | $S_4$ | I2S_BCLK duty | 45% | - | 55% | - | - |
| 5 | $S_5$ | I2S_RXD input setup (I2S_BCLK) | 28 | - | - | ns | - |
| 6 | $S_6$ | I2S_RXD input hold (I2S_BCLK) | 0 | - | - | ns | - |
| 7 | $S_7$ | I2S_BCLK to I2S_TXD output valid | - | - | 8 | ns | - |
| 8 | $S_8$ | I2S_BCLK to I2S_TXD output invalid | -2 | - | - | ns | - |

**Table 28. I2S electrical specification (continued)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 9 | $S_9$ | I2S_FS input setup (I2S_BCLK) | 28 | - | - | ns | - |
| 10 | $S_{10}$ | I2S_FS input hold (I2S_BCLK) | 0 | - | - | ns | |
| 11 | $S_{11}$ | I2S_BCLK to I2S_FS output valid | - | - | 8 | ns | |
| 12 | $S_{12}$ | I2S_BCLK to I2S_FS output invalid | -2 | - | - | ns | |
| **I2S Slave** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $S_{13}$ | I2S_BCLK cycle time | 80 | - | - | ns | |
| 2 | $S_{14}$ | I2S_BCLK duty | 45% | - | 55% | - | |
| 3 | $S_{15}$ | I2S_RXD input setup (I2S_BCLK) | 3 | - | - | ns | |
| 4 | $S_{16}$ | I2S_RXD input hold (I2S_BCLK) | 3 | - | - | ns | |
| 5 | $S_{17}$ | I2S_BCLK to I2S_TXD output valid | - | - | 30 | ns | |
| 6 | $S_{18}$ | I2S_BCLK to I2S_TXD output invalid | 0 | - | - | ns | |
| 7 | $S_{19}$ | I2S_FS input setup (I2S_BCLK) | 3 | - | - | ns | |
| 8 | $S_{20}$ | I2S_FS input hold (I2S_BCLK) | 3 | - | - | ns | |
| 9 | $S_{21}$ | I2S_BCLK to I2S_FS output valid | - | - | 30 | ns | |
| 10 | $S_{22}$ | I2S_BCLK to I2S_FS output invalid | 0 | - | - | ns | |

# Chapter 9 Debug Modules

The chip supports both JTAG and Serial Wire Debug (SWD) interface, and it also has the TPIU interface.

## 9.1 SWD Specification

**Figure 10. SWD clock timing diagram**

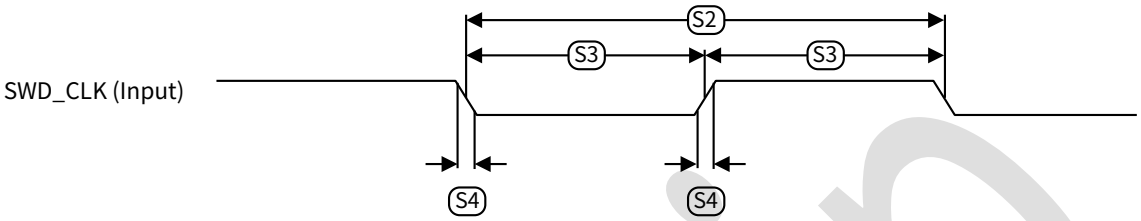



**Figure 11. SWD data timing diagram**

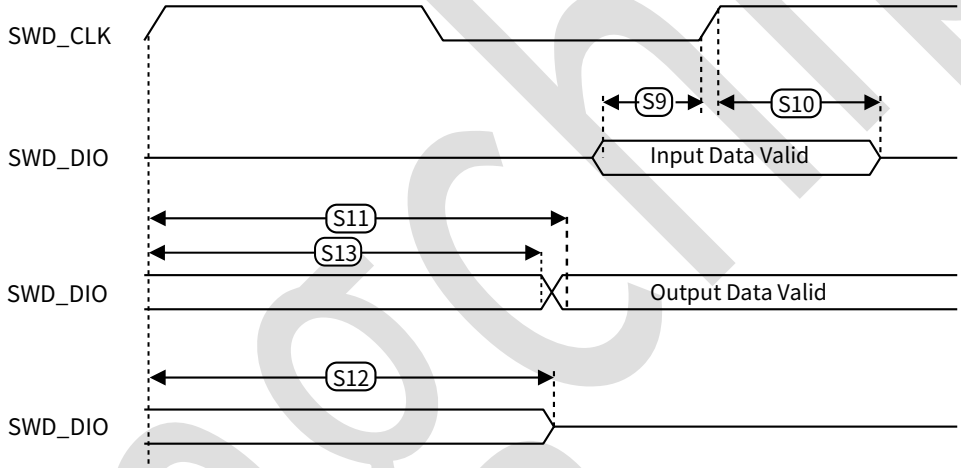



**Table 29. SWD electrical specification**

| SWD | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $S_1$ | SWD_CLK frequency | - | - | 25 | MHz | |
| 2 | $S_2$ | SWD_CLK period | $1/S_1$ | - | - | ns | |
| 3 | $S_3$ | SWD_CLK clock pulse width | $S_2/2 - 5$ | - | $S_2/2 + 5$ | ns | |
| 4 | $S_4$ | SWD_CLK rise or fall time | 1 | - | 3 | ns | |
| 5 | $S_5$ | SCK high/low width | - | - | - | ns | |
| 6 | $S_6$ | SWD_DIO data setup time | 6 | - | - | ns | |
| 7 | $S_7$ | SWD_DIO data hold time | 3 | - | - | ns | |
| 8 | $S_8$ | SWD_CLK to SWD_DIO data valid | - | - | - | ns | |
| 9 | $S_9$ | SWD_CLK to SWD_DIO data high-z | 0 | - | - | ns | |
| 10 | $S_{10}$ | SWD_CLK to SWD_DIO data invalid | 0 | - | - | ns | |

## 9.2 Trace Block

**Figure 12. Trace block timing diagram**

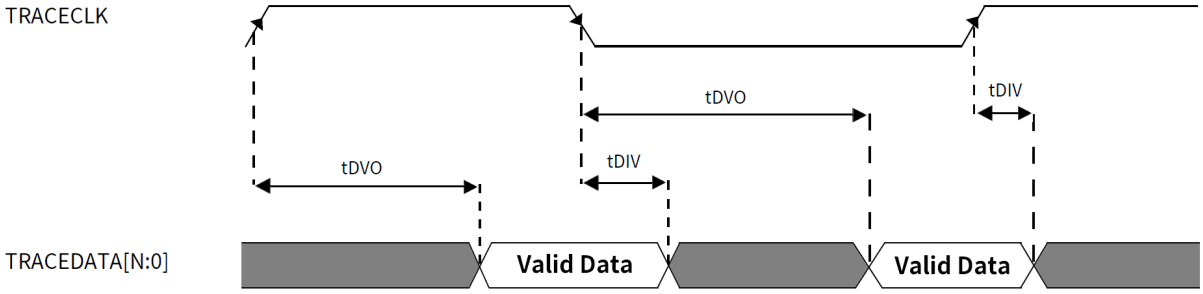



**Table 30. Trace block electrical specification**

| **Trace Interface on normal pad** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{trace}$ | Frequency of operation | - | - | 25 | MHz | |
| 2 | $t_{dvo}$ | Data output valid | - | - | 7.5 | ns | |
| 3 | $t_{dvi}$ | Data output invalid | -4 | - | - | ns | |
| **Trace Interface on HS pad** | | | | | | | |
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $f_{trace}$ | Frequency of operation | - | - | 50 | MHz | |
| 2 | $t_{dvo}$ | Data output valid | - | - | 7 | ns | |
| 3 | $t_{dvi}$ | Data output invalid | 0 | - | - | ns | |

## 9.3 JTAG Interface

**Figure 13. JTAG clock timing diagram**

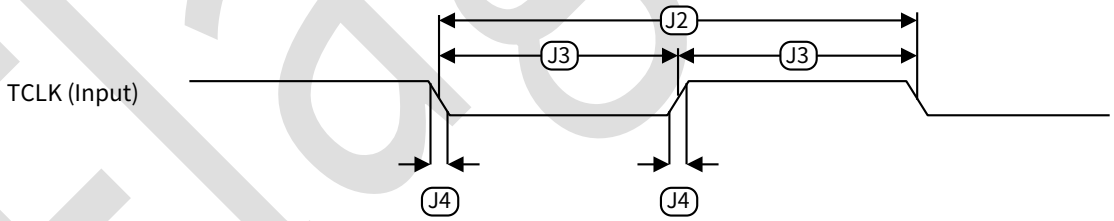



**Figure 14. Boundary timing diagram**

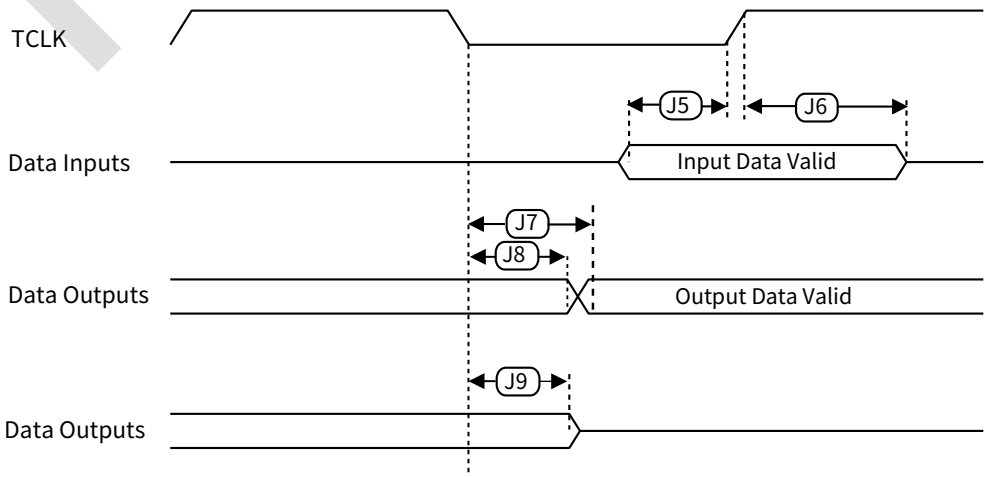


**Figure 15. JTAG TAP timing diagram**

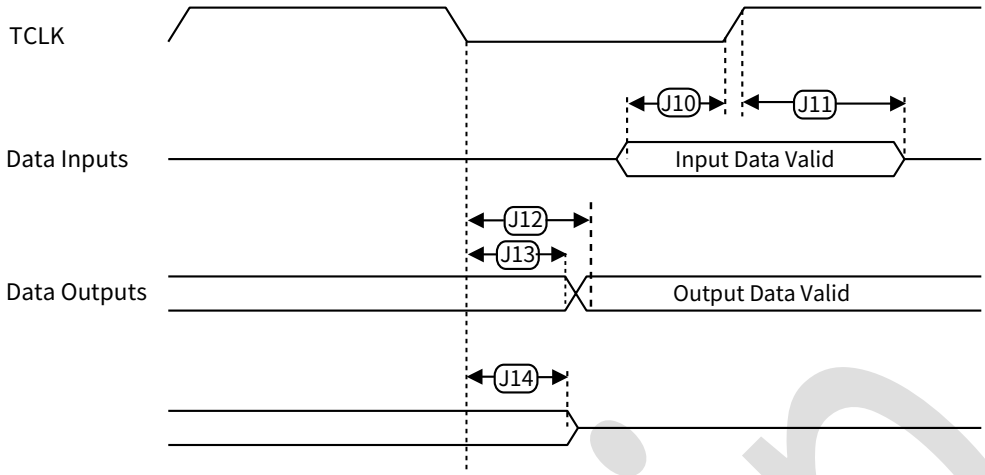



**Table 31. JTAG electrical specification**

| JTAG | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** | **Notes** |
| 1 | $J_1$ | TCLK frequency | - | - | 15 | MHz | |
| 2 | $J_2$ | TCLK period | 64 | - | - | ns | |
| 3 | $J_3$ | TCLK duty | 45% | - | 55% | - | |
| 4 | $J_4$ | TCLK rise and fall times | 1 | - | 3 | ns | |
| 5 | $J_5$ | Boundary input setup (TCLK) | 6 | - | - | ns | |
| 6 | $J_6$ | Boundary input hold (TCLK) | 2 | - | - | ns | |
| 7 | $J_7$ | TCLK low to Boundary output valid | - | - | 32 | ns | |
| 8 | $J_8$ | TCLK low to Boundary output invalid | 0 | - | - | ns | |
| 9 | $J_9$ | TCLK low to Boundary output high-Z | - | - | 32 | ns | |
| 10 | $J_{10}$ | TMS/TDI setup (TCLK) | 6 | - | - | ns | |
| 11 | $J_{11}$ | TMS/TDI hold (TCLK) | 2 | - | - | ns | |
| 12 | $J_{12}$ | TCLK low to TDO output valid | - | - | 32 | ns | |
| 13 | $J_{13}$ | TCLK low to TDO output invalid | 0 | - | - | ns | |
| 14 | $J_{14}$ | TCLK low to TDO output high-Z | - | - | 32 | ns | |

# Chapter 10 Package

## 10.1 Thermal Data

The following table shows the FC4150F512 package thermal data. The user can calculate the maximum junction based on the package type, environment and PCB etc.

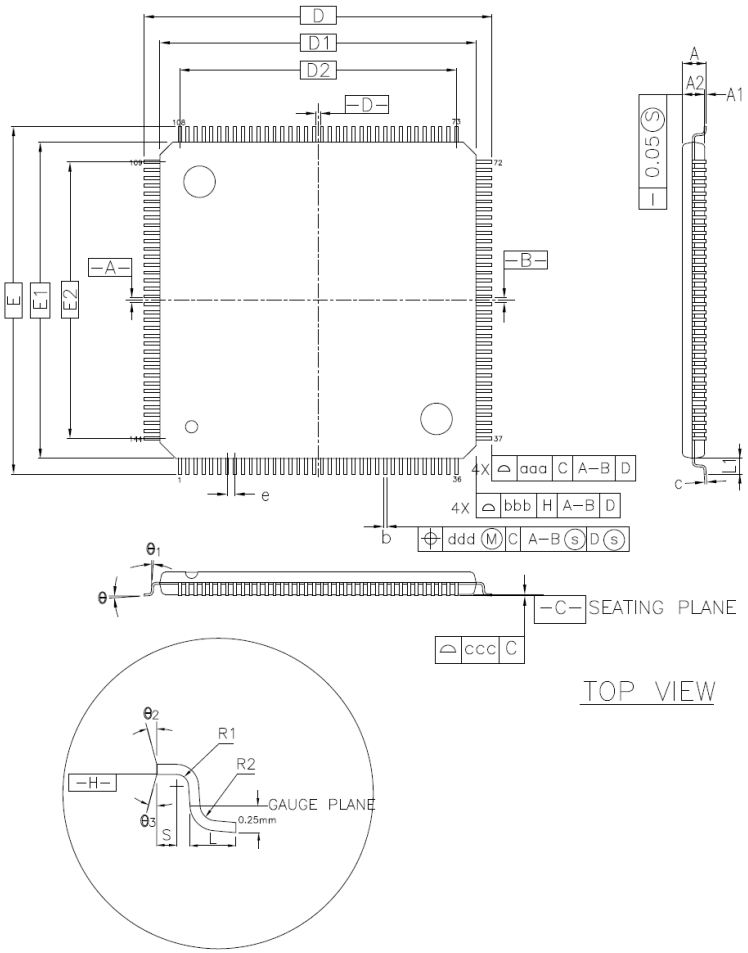
**Table 32. Thermal package simulation data**

| RθJA | Description | Package | FC4150F512 | Unit |
|---|---|---|---|---|
| Thermal resistance, Junction to Ambient (Natural Convection) | Single-layer board (1s) | 144LQFP | 62 | °C/W |
| | Four-layer board (2s2p) | | 55 | |
| | Single-layer board (1s) | 100LQFP | 69 | |
| | Four-layer board (2s2p) | | 61 | |
| | Single-layer board (1s) | 64LQFP | 53 | |
| | Four-layer board (2s2p) | | 45 | |
| Thermal resistance, Junction to Ambient (@1m/s) | Single-layer board (1s) | 144LQFP | 52 | |
| | Four-layer board (2s2p) | | 47 | |
| | Single-layer board (1s) | 100LQFP | 58 | |
| | Four-layer board (2s2p) | | 53 | |
| | Single-layer board (1s) | 64LQFP | 42 | |
| | Four-layer board (2s2p) | | 36 | |

## 10.2 Package Dimension

For FC4150F512, there are 64LQFP, 100LQFP, and 144LQFP package options. The following figures show the package dimensions.

**Figure 16. 144LQFP package**



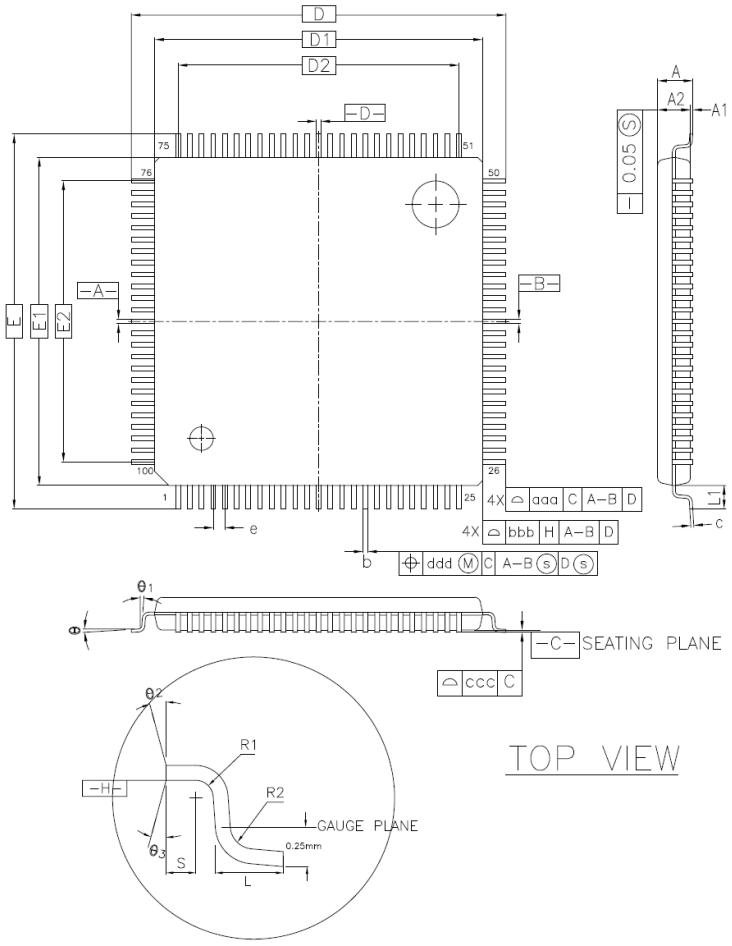

CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | —— | —— | 1.60 | —— | —— | 0.063 |
| $A_1$ | 0.05 | —— | 0.15 | 0.002 | —— | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | | 22 BSC. | | | 0.866 BSC. | |
| $D_1$ | | 20 BSC. | | | 0.787 BSC. | |
| E | | 22 BSC. | | | 0.866 BSC. | |
| $E_1$ | | 20 BSC. | | | 0.787 BSC. | |
| $R_2$ | 0.08 | —— | 0.20 | 0.003 | —— | 0.008 |
| $R_1$ | 0.08 | —— | —— | 0.003 | —— | —— |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $\theta_1$ | 0° | —— | —— | 0° | —— | —— |
| $\theta_2$ | 11° | 12° | 13° | 11° | 12° | 13° |
| $\theta_3$ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | 0.127 | 0.20 | 0.004 | 0.005 | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | | 1.00 REF. | | | 0.039 REF. | |
| S | 0.20 | —— | —— | 0.008 | —— | —— |

| SYMBOL | 144L | | | | | |
|---|---|---|---|---|---|---|
| | MILLIMETER | | | INCH | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | | 0.50 BSC. | | | 0.020 BSC. | |
| D2 | | 17.50 | | | 0.689 | |
| E2 | | 17.50 | | | 0.689 | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | | 0.20 | | | 0.008 | |
| bbb | | 0.20 | | | 0.008 | |
| ccc | | 0.08 | | | 0.003 | |
| ddd | | 0.08 | | | 0.003 | |

NOTES :
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. THE MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.
3. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.

**Figure 17. 100LQFP package**



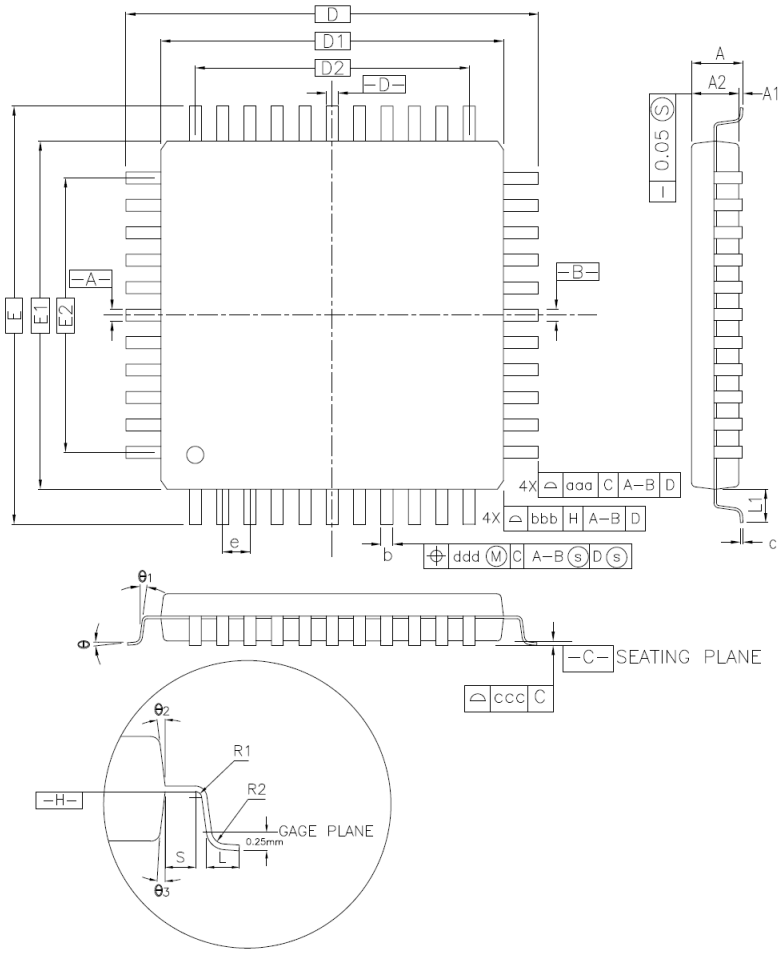

CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | —— | —— | 1.60 | —— | —— | 0.063 |
| $A_1$ | 0.05 | —— | 0.15 | 0.002 | —— | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | | 16 BSC. | | | 0.630 BSC. | |
| $D_1$ | | 14 BSC. | | | 0.551 BSC. | |
| E | | 16 BSC. | | | 0.630 BSC. | |
| $E_1$ | | 14 BSC. | | | 0.551 BSC. | |
| $R_2$ | 0.08 | —— | 0.20 | 0.003 | —— | 0.008 |
| $R_1$ | 0.08 | —— | —— | 0.003 | —— | —— |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $\theta_1$ | 0° | —— | —— | 0° | —— | —— |
| $\theta_2$ | 11° | 12° | 13° | 11° | 12° | 13° |
| $\theta_3$ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | 0.127 | 0.20 | 0.004 | 0.005 | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | | 1.00 REF. | | | 0.039 REF. | |
| S | 0.20 | —— | —— | 0.008 | —— | —— |

| SYMBOL | 100L | | | | | |
|---|---|---|---|---|---|---|
| | MILLIMETER | | | INCH | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | | 0.50 BSC. | | | 0.020 BSC. | |
| D2 | | 12.00 | | | 0.472 | |
| E2 | | 12.00 | | | 0.472 | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | | 0.20 | | | 0.008 | |
| bbb | | 0.20 | | | 0.008 | |
| ccc | | 0.08 | | | 0.003 | |
| ddd | | 0.08 | | | 0.003 | |

NOTES :
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. THE MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.
3. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.

**Figure 18. 64LQFP package**




COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 12.00 BSC. | | | 0.472 BSC. | | |
| D1 | 10.00 BSC. | | | 0.393 BSC. | | |
| E | 12.00 BSC. | | | 0.472 BSC. | | |
| E1 | 10.00 BSC. | | | 0.393 BSC. | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |

| SYMBOL | 44L | | | | | | 64L | | | | | | 80L | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MILLIMETER | | | INCH | | | MILLIMETER | | | INCH | | | MILLIMETER | | | INCH | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| b | 0.22 | 0.30 | 0.38 | 0.009 | 0.012 | 0.015 | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 | 0.13 | 0.16 | 0.23 | 0.005 | 0.006 | 0.009 |
| e | 0.80 BSC. | | | 0.031 BSC. | | | 0.50 BSC. | | | 0.020 BSC. | | | 0.40 BSC. | | | 0.016 BSC. | | |
| D2 | 8.00 | | | 0.315 | | | 7.50 | | | 0.295 | | | 7.60 | | | 0.299 | | |
| E2 | 8.00 | | | 0.315 | | | 7.50 | | | 0.295 | | | 7.60 | | | 0.299 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | | | | | | | | | | | | | |
| aaa | 0.20 | | | 0.008 | | | 0.20 | | | 0.008 | | | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | | 0.20 | | | 0.008 | | | 0.20 | | | 0.008 | | |
| ccc | 0.10 | | | 0.004 | | | 0.08 | | | 0.003 | | | 0.08 | | | 0.003 | | |
| ddd | 0.20 | | | 0.008 | | | 0.08 | | | 0.003 | | | 0.07 | | | 0.003 | | |

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
3. DIMENSION OF 44L "b" DIFFERENT WITH JEDEC SPEC ( ASE: 0.22/0.30/0.38 )
   ( JEDEC: 0.30/0.37/0.45 )

# Chapter 11 Pinout

The figures below demonstrate the pinouts for packages of the FC4150F512.

**Figure 19. 144LQFP pinout**

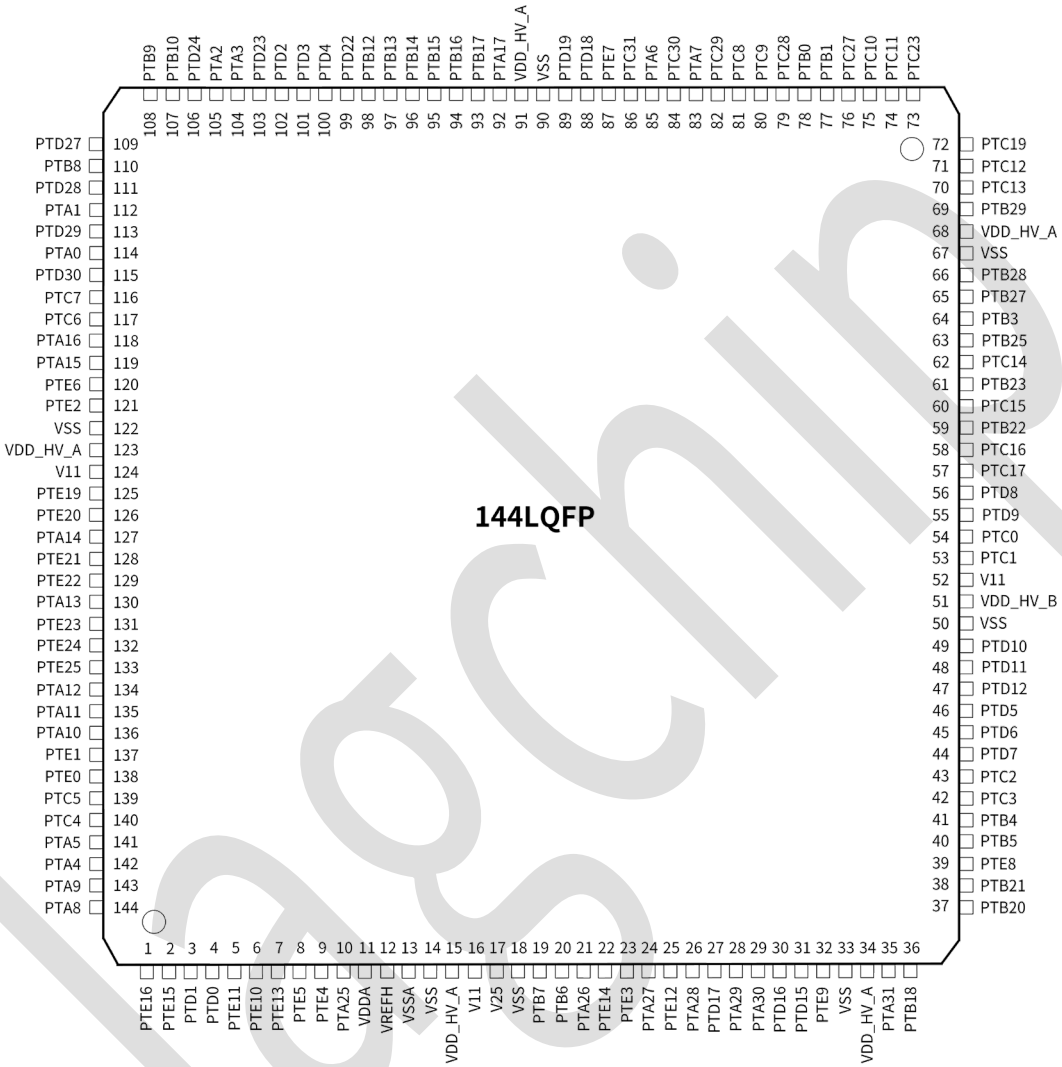


**Figure 20. 100LQFP pinout**

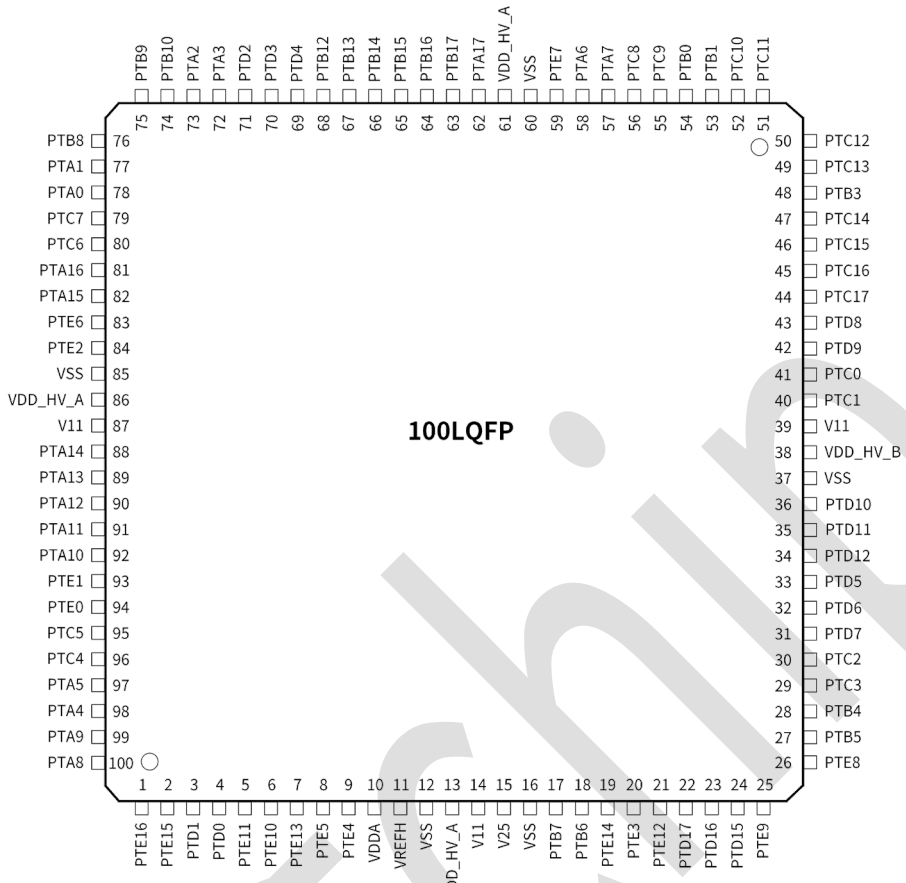
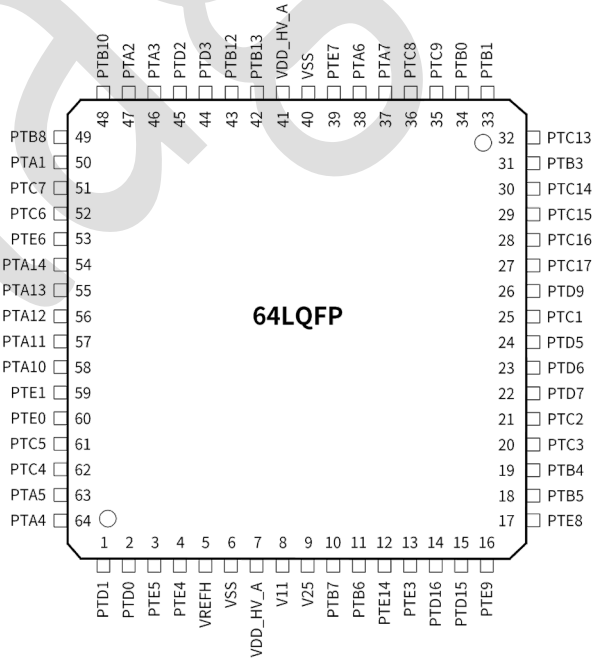



**Figure 21. 64LQFP pinout**




The table below lists the different peripheral functions mapped to different pins.

For detailed function pinout mapping, refer to the FC4150 Pinout.xlsx attached in FC4150 Reference Manual.

**Table 33. FC4150F512 pin functions**

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| - | 1 | 1 | PTE16 | ADC1_SE6 | - | - | - | - | - | FCSPI2_SIN | FCUART1_RTS | - | FTU2_CH7 | - | - | - | - | TRGSEL_OUT7 | - | - |
| - | 2 | 2 | PTE15 | ADC1_SE2 | - | - | - | - | - | FCSPI2_SCK | FCUART1_CTS | - | FTU2_CH6 | - | - | - | - | TRGSEL_OUT6 | - | - |
| 1 | 3 | 3 | PTD1 | ADC1_SE5 | - | - | - | - | - | FCSPI1_SIN | - | - | FTU0_CH3/FTU2_CH1 | - | I2S0_MCLK | - | - | TRGSEL_OUT2 | - | - |
| 2 | 4 | 4 | PTD0 | ADC1_SE1 | - | - | TRACE_D0 | - | - | FCSPI1_SCK | - | - | FTU0_CH2/FTU2_CH0 | - | - | - | - | TRGSEL_OUT1 | - | - |
| - | 5 | 5 | PTE11 | ADC1_SE4 | AONTIMER0_CLK1 | - | - | - | - | FCSPI2_PCS0 | - | - | FTU2_CH5 | - | - | - | - | TRGSEL_OUT5 | - | - |
| - | 6 | 6 | PTE10 | ADC1_SE0 | - | - | - | - | - | FCSPI2_PCS1 | - | FLEXCAN5_TX | FTU2_CH4 | - | | | | TRGSEL_OUT4 | | SCG_CLKOUT |
| - | 7 | 7 | PTE13 | ADC0_SE5 | - | - | - | - | - | FCSPI2_PCS2 | - | FLEXCAN5_RX | FTU4_CH5 | - | - | - | - | - | - | - |
| 3 | 8 | 8 | PTE5 | ADC0_SE1 | - | - | - | - | - | FCSPI1_SOUT | - | - | FTU_TCK2/FTU2_QD_PHA/FTU2_CH3 | FWM_IN | - | - | - | - | - | - |
| 4 | 9 | 9 | PTE4 | ADC0_SE4 | - | - | TRACE_D1 | - | - | FCSPI1_PCS0 | - | - | FTU2_QD_PHB/FTU2_CH2 | FWM_OUT_b | - | - | - | - | - | - |
| - | - | 10 | PTA25 | ADC0_SE0 | | | | | | FCSPI2_SOUT | - | - | FTU5_CH0 | - | - | - | - | - | - | - |
| 5 | 10 | 11 | VDDA | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | 11 | 12 | VREFH | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| 6 | 12 | 13 | VREFL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | | | VSSA | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | | 14 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 7 | 13 | 15 | VDD_HV_A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 8 | 14 | 16 | V11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 9 | 15 | 17 | V25 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | 16 | 18 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 10 | 17 | 19 | PTB7 | - | - | - | - | EXTAL | FCIIC0_SCL | - | - | - | - | - | - | - | - | - | - | - |
| 11 | 18 | 20 | PTB6 | - | - | - | - | XTAL | FCIIC0_SDA | - | - | - | - | - | - | - | - | - | - | - |
| - | - | 21 | PTA26 | - | - | CMP0_IN0 | - | - | - | FCSPI1_PCS0 | - | - | FTU5_CH1 | - | - | - | - | - | - | - |
| 12 | 19 | 22 | PTE14 | - | AONTIMER0_CLK1 | - | - | - | - | - | - | FLEXCAN0_RX | FTU2_CH7/FTU_FLT0 | - | - | - | OSC32K_XTAL | - | - | - |
| 13 | 20 | 23 | PTE3 | - | - | - | - | - | - | - | FCUART2_RX | - | FTU2_CH6/FTU_FLT1/FTU_TCK0 | FWM_IN | - | - | OSC32K_EXTAL | TRGSEL_IN6 | - | - |
| - | - | 24 | PTA27 | ADC0_SE2 | - | - | - | - | - | FCSPI1_SOUT | FCUART0_TX | FLEXCAN0_TX | FTU5_CH2 | - | - | - | - | - | - | - |
| - | 21 | 25 | PTE12 | ADC0_SE6 | - | CMP0_OUT | - | - | - | - | FCUART2_TX | - | FTU_FLT2 | - | - | - | - | - | - | - |
| - | - | 26 | PTA28 | ADC0_SE3 | - | - | - | - | - | FCSPI1_SCK | FCUART0_RX | FLEXCAN0_RX | FTU5_CH3 | - | - | - | - | - | - | - |
| - | 22 | 27 | PTD17 | ADC0_SE7 | - | - | - | - | - | - | FCUART2_RX | - | FTU_FLT3 | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| - | - | 28 | PTA29 | ADC0_SE8 | - | - | - | - | - | FCSPI1_SIN | FCUART2_TX | - | FTU5_CH4 | - | - | - | - | - | - | - |
| - | - | 29 | PTA30 | ADC0_SE9 | - | - | - | - | - | FCSPI0_SOU | FCUART2_RX | - | FTU5_CH5 | - | - | - | - | - | - | - |
| 14 | 23 | 30 | PTD16 | ADC0_SE10 | - | - | TRACE_D2 | - | - | FCSPI0_SIN | - | - | FTU0_CH1 | - | - | - | - | - | - | - |
| 15 | 24 | 31 | PTD15 | ADC0_SE11 | - | CMP0_IN1 | TRACE_D3 | - | - | FCSPI0_SCK | FCUART2_RTS | - | FTU0_CH0 | - | - | - | - | - | - | - |
| 16 | 25 | 32 | PTE9 | ADC0_SE12 | - | CMP0_IN2 | TRACE_CLKOUT | - | - | FCSPI0_PCS0 | FCUART2_CTS | - | FTU0_CH7 | - | - | - | - | - | - | - |
| - | - | 33 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | 34 | VDD_HV_A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | 35 | PTA31 | ADC0_SE13 | - | CMP0_IN3 | - | - | - | FCSPI0_PCS1 | - | FLEXCAN3_TX | FTU5_CH6 | - | - | - | - | - | - | - |
| - | - | 36 | PTB18 | - | - | CMP0_IN4 | - | - | - | FCSPI1_PCS1 | - | FLEXCAN3_RX | FTU5_CH7 | - | - | - | - | - | - | - |
| - | - | 37 | PTB20 | ADC0_SE14 | - | - | - | - | - | - | FCUART1_TX | - | FTU2_CH5 | - | - | - | - | - | - | SCG_CLKOUT |
| - | - | 38 | PTB21 | ADC0_SE15 | - | - | - | - | - | - | FCUART1_RX | - | FTU2_CH4 | - | - | - | - | - | RTC_CLKOUT | - |
| 17 | 26 | 39 | PTE8 | - | - | - | - | - | - | FCSPI0_SCK | - | - | FTU0_CH6 | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| 18 | 27 | 40 | PTB5 | - | - | - | - | - | FCIIC1_SCL | FCSPI0_PCS0 | - | - | FTU0_CH5 | - | - | - | - | TRGSEL_IN0 | - | SCG_CLKOUT |
| 19 | 28 | 41 | PTB4 | - | - | - | - | - | FCIIC1_SDA | FCSPI0_SOUT | - | - | FTU0_CH4 | - | - | - | - | TRGSEL_IN1 | - | - |
| 20 | 29 | 42 | PTC3 | - | - | CMP1_IN0 | - | - | - | - | FCUART0_TX | FLEXCAN0_TX | FTU0_CH3 | - | - | - | - | - | - | - |
| 21 | 30 | 43 | PTC2 | - | - | CMP1_IN1 | TRACE_CLKOUT | - | - | - | FCUART0_RX | FLEXCAN0_RX | FTU0_CH2 | - | - | - | - | - | - | - |
| 22 | 31 | 44 | PTD7 | - | - | CMP1_IN2 | TRACE_D0 | - | - | FCSPI0_SIN | FCUART2_TX | FLEXCAN3_TX | - | - | - | - | - | - | - | - |
| 23 | 32 | 45 | PTD6 | - | - | CMP1_IN3 | - | - | - | FCSPI3_SCK | FCUART2_RX | FLEXCAN3_RX | FTU_FLT4 | - | - | - | - | - | - | - |
| 24 | 33 | 46 | PTD5 | - | AONTIMER0_CLK2 | - | - | - | - | FCSPI3_SIN | - | - | FTU2_CH3/FTU_FLT5 | - | - | - | - | TRGSEL_IN7 | - | - |
| - | 34 | 47 | PTD12 | - | - | - | TRACE_D1 | - | - | FCSPI3_SOUT | FCUART2_RTS | - | FTU2_CH2 | - | - | - | - | - | - | - |
| - | 35 | 48 | PTD11 | - | - | - | TRACE_D2 | - | - | FCSPI3_PCS0 | FCUART2_CTS | - | FTU2_CH1/FTU2_QD_PHA | - | - | - | - | - | - | - |
| - | 36 | 49 | PTD10 | - | - | - | TRACE_D3 | - | - | FCSPI3_PCS1 | - | - | FTU2_CH0/FTU2_QD_PHB | - | - | - | - | - | - | SCG_CLKOUT |
| - | 37 | 50 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | 38 | 51 | VDD_HV_B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | 39 | 52 | V11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| 25 | 40 | 53 | PTC1 | - | - | - | - | - | - | FCSPI2_SOUT | FCUART3_TX | - | FTU0_CH1/FTU1_CH7 | - | - | - | - | - | - | - |
| - | 41 | 54 | PTC0 | - | - | - | - | - | - | FCSPI3_PCS2 | - | - | FTU0_CH0/FTU1_CH6 | - | - | - | - | - | - | - |
| 26 | 42 | 55 | PTD9 | - | - | - | - | - | FCIIC1_SCL | FCSPI2_PCS1 | FCUART3_RX | - | FTU1_CH5 | - | - | - | - | - | - | - |
| - | 43 | 56 | PTD8 | - | - | - | - | - | FCIIC1_SDA | FCSPI2_PCS2 | FCUART4_RX | - | FTU1_CH4 | - | - | - | - | - | - | - |
| 27 | 44 | 57 | PTC17 | - | - | - | - | - | - | FCSPI2_PCS3 | FCUART4_TX | FLEXCAN2_TX | FTU_FLT6 | - | - | - | - | - | - | - |
| 28 | 45 | 58 | PTC16 | - | - | - | - | - | - | FCSPI2_SIN | FCUART5_RX | FLEXCAN2_RX | FTU_FLT7 | - | - | - | - | - | - | - |
| - | - | 59 | PTB22 | - | - | CMP1_IN4 | - | - | - | FCSPI3_PCS3 | FCUART1_TX | - | FTU_FLT8 | - | - | - | - | - | - | - |
| 29 | 46 | 60 | PTC15 | - | - | CMP1_IN5 | - | - | - | FCSPI2_SCK | FCUART5_TX | - | FTU1_CH3 | - | - | - | - | TRGSEL_IN8 | - | - |
| - | - | 61 | PTB23 | - | - | CMP1_IN6 | - | - | - | - | FCUART1_RX | - | FTU_FLT9 | - | - | - | - | - | - | - |
| 30 | 47 | 62 | PTC14 | - | - | CMP1_IN7 | - | - | - | FCSPI2_PCS0 | - | - | FTU1_CH2 | - | - | - | - | TRGSEL_IN9 | - | - |
| - | - | 63 | PTB25 | - | - | - | - | - | - | FCSPI2_PCS0 | - | - | FTU1_CH2 | - | - | - | - | - | - | - |
| 31 | 48 | 64 | PTB3 | - | - | - | - | - | - | FCSPI0_SIN | - | - | FTU1_CH1/FTU1_QD_PHA | - | - | - | - | TRGSEL_IN2 | - | - |
| - | - | 65 | PTB27 | - | - | - | - | - | - | FCSPI2_SOUT | - | - | - | - | - | - | - | - | - | - |
| - | - | 66 | PTB28 | - | - | - | - | - | - | FCSPI2_SIN | - | - | - | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| - | - | 67 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | 68 | VDD_HV_A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | 69 | PTB29 | - | - | - | - | - | - | FCSPI2_SCK | - | - | FTU1_CH0/FTU1_QD_PHB | - | - | - | - | TRGSEL_IN3 | - | - |
| 32 | 49 | 70 | PTC13 | ADC1_SE15 | - | CMP2_IN0 | - | - | - | - | FCUART2_RTS | FLEXCAN5_TX | FTU3_CH7/FTU2_CH7 | - | - | - | - | TRGSEL_OUT6 | - | - |
| - | 50 | 71 | PTC12 | - | - | CMP2_IN1 | - | - | - | - | FCUART2_CTS | FLEXCAN5_RX | FTU3_CH6/FTU2_CH6 | - | - | - | - | TRGSEL_OUT5 | - | - |
| - | - | 72 | PTC19 | - | - | CMP2_IN2 | - | - | - | FCSPI2_PCS1 | - | - | - | - | - | - | - | - | - | - |
| - | - | 73 | PTC23 | - | - | - | - | - | - | FCSPI0_SCK | - | - | - | - | - | - | - | - | - | - |
| - | 51 | 74 | PTC11 | - | - | - | - | - | - | FCSPI1_PCS0 | - | FLEXCAN4_TX | FTU3_CH5/FTU4_CH2 | - | - | - | - | TRGSEL_IN10 | - | - |
| - | 52 | 75 | PTC10 | ADC1_SE14 | - | - | - | - | - | - | - | FLEXCAN4_RX | FTU3_CH4 | - | - | - | - | TRGSEL_IN11 | - | - |
| - | - | 76 | PTC27 | - | - | - | - | - | - | - | - | - | FTU4_CH4 | - | - | - | - | - | - | - |
| 33 | 53 | 77 | PTB1 | ADC1_SE13 | - | - | - | - | - | FCSPI0_SOUT | FCUART0_TX | FLEXCAN0_TX | FTU_TCK0/FTU4_CH5 | - | - | - | - | - | - | - |
| 34 | 54 | 78 | PTB0 | ADC1_SE12 | AONTIMER0_CLK3 | - | - | - | - | FCSPI0_PCS0 | FCUART0_RX | FLEXCAN0_RX | FTU4_CH6 | - | - | - | - | - | - | - |
| - | - | 79 | PTC28 | - | | - | - | - | - | - | - | FLEXCAN3_TX | FTU4_CH7 | - | - | - | - | - | - | - |
| 35 | 55 | 80 | PTC9 | - | - | CMP2_IN3 | - | - | - | FCSPI1_SOUT | FCUART1_TX/ | - | FTU_FLT10/FTU5_CH0 | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| | | | | | | | | | | | FCUART0_RTS | | | | | | | | | |
| 36 | 56 | 81 | PTC8 | - | - | CMP2_IN4 | - | - | - | FCSPI1_SIN | FCUART1_RX/FCUART0_CTS | - | FTU_FLT11/FTU5_CH1 | - | - | - | - | - | - | - |
| - | - | 82 | PTC29 | - | - | - | - | - | - | - | - | FLEXCAN3_RX | FTU5_CH2 | - | - | - | - | - | - | - |
| 37 | 57 | 83 | PTA7 | - | - | CMP2_IN5 | - | - | - | FCSPI1_SCK | FCUART1_RTS | - | FTU_FLT12/FTU5_CH3 | - | - | - | - | - | - | - |
| - | - | 84 | PTC30 | ADC1_SE11 | - | - | - | - | - | - | - | - | FTU5_CH4 | - | - | - | - | - | - | - |
| 38 | 58 | 85 | PTA6 | ADC1_SE10 | - | - | - | - | - | FCSPI1_PCS1 | FCUART1_CTS | - | FTU_FLT13/FTU5_CH5 | - | - | - | - | TRGSEL_OUT4 | - | - |
| - | - | 86 | PTC31 | - | - | - | - | - | FCIIC1_SDA | - | - | - | FTU5_CH6 | - | - | - | - | - | - | - |
| 39 | 59 | 87 | PTE7 | ADC1_SE9 | - | - | - | - | - | - | - | - | FTU0_CH7/FTU_FLT14 | - | - | - | - | TRGSEL_OUT3 | - | - |
| - | - | 88 | PTD18 | ADC1_SE8 | - | - | - | - | - | - | - | - | FTU5_CH7 | - | - | - | - | - | - | - |
| - | - | 89 | PTD19 | - | - | - | - | - | FCIIC1_SCL | - | - | - | - | FWM_OUT_b | - | - | - | - | - | - |
| 40 | 60 | 90 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 41 | 61 | 91 | VDD_HV_A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | 62 | 92 | PTA17 | - | - | - | - | - | - | - | - | FLEXCAN4_TX | FTU0_CH6/FTU_FLT15 | FWM_OUT_b | - | - | - | - | - | - |
| - | 63 | 93 | PTB17 | - | - | - | - | - | - | FCSPI1_PCS3 | - | FLEXCAN4_RX | FTU0_CH5 | - | - | - | - | TRGSEL_OUT3 | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| - | 64 | 94 | PTB16 | ADC1_SE16 | - | - | - | - | - | FCSPI1_SOUT | - | - | FTU0_CH4 | - | - | - | - | - | - | - |
| - | 65 | 95 | PTB15 | ADC1_SE17 | - | - | - | - | - | FCSPI1_SIN | - | - | FTU0_CH3 | - | - | - | - | - | - | - |
| - | 66 | 96 | PTB14 | ADC1_SE18 | - | - | - | - | - | FCSPI1_SCK | - | - | FTU0_CH2 | - | - | - | - | - | - | - |
| 42 | 67 | 97 | PTB13 | ADC1_SE19 | - | - | - | - | - | - | - | FLEXCAN2_TX | FTU0_CH1 | - | - | - | - | - | - | - |
| 43 | 68 | 98 | PTB12 | ADC1_SE20 | - | - | - | - | - | - | - | FLEXCAN2_RX | FTU0_CH0 | - | - | - | - | - | - | - |
| - | - | 99 | PTD22 | ADC1_SE21 | - | - | - | - | - | - | - | - | - | - | I2S1_D3 | - | - | - | - | - |
| - | 69 | 100 | PTD4 | ADC1_SE22 | - | CMP2_IN6 | - | - | - | - | - | - | FTU_FLT16 | - | - | - | - | - | - | - |
| 44 | 70 | 101 | PTD3 | ADC1_SE23 | - | - | - | - | - | FCSPI1_PCS0 | - | - | FTU3_CH5 | - | - | - | - | TRGSEL_IN4 | - | - |
| 45 | 71 | 102 | PTD2 | ADC0_SE24 | - | - | - | - | - | - | - | - | FTU3_CH4 | - | - | - | - | TRGSEL_IN5 | - | - |
| - | - | 103 | PTD23 | ADC0_SE25 | - | CMP2_IN7 | - | - | - | - | - | - | - | - | I2S1_D2 | - | - | - | - | - |
| 46 | 72 | 104 | PTA3 | ADC0_SE26 | - | - | - | - | FCIIC0_SCL | - | FCUART0_TX | - | FTU3_CH1 | FWM_IN | - | - | - | - | - | - |
| 47 | 73 | 105 | PTA2 | ADC0_SE27 | - | - | - | - | FCIIC0_SDA | - | FCUART0_RX | - | FTU3_CH0 | FWM_OUT_b | - | - | - | - | - | - |
| - | - | 106 | PTD24 | ADC0_SE31/ADC1_SE31 | - | CMP2_OUT | - | - | - | - | - | - | FTU3_CH3 | - | I2S1_D1 | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| 48 | 74 | 107 | PTB10 | - | - | - | - | - | - | - | - | FLEXCAN0_TX | FTU3_CH2/FTU2_QD_PHA | - | I2S1_MCLK | - | - | TRGSEL_OUT2 | - | - |
| - | 75 | 108 | PTB9 | ADC0_SE30/ADC1_SE30 | - | - | - | - | - | - | - | - | FTU3_CH1 | - | I2S1_D0 | - | - | TRGSEL_OUT1 | - | - |
| - | - | 109 | PTD27 | - | - | - | - | - | - | - | - | FLEXCAN4_TX | - | - | - | - | - | - | - | - |
| 49 | 76 | 110 | PTB8 | ADC0_SE29/ADC1_SE29 | - | CMP2_OUT | - | - | - | - | FCUART1_CTS | FLEXCAN0_RX | FTU3_CH0 | - | I2S1_BCLK | - | - | - | - | - |
| - | - | 111 | PTD28 | - | - | - | - | - | - | - | - | FLEXCAN4_RX | - | - | - | - | - | - | - | - |
| 50 | 77 | 112 | PTA1 | ADC0_SE28/ADC1_SE28 | - | - | - | - | - | - | FCUART0_RTS | - | FTU1_CH1/FTU1_QD_PHA | - | - | - | - | TRGSEL_OUT0 | - | - |
| - | - | 113 | PTD29 | ADC1_SE27 | - | - | - | - | - | - | - | FLEXCAN5_RX | - | - | - | - | - | - | - | - |
| - | 78 | 114 | PTA0 | ADC1_SE26 | - | - | - | - | - | - | FCUART0_CTS | - | FTU2_CH1/FTU2_QD_PHA | - | - | - | - | TRGSEL_OUT3 | - | - |
| - | - | 115 | PTD30 | ADC1_SE25 | - | - | - | - | - | - | - | FLEXCAN5_TX | - | - | - | - | - | - | - | - |
| 51 | 79 | 116 | PTC7 | ADC1_SE24 | - | - | - | - | - | - | FCUART1_TX | FLEXCAN1_TX | FTU3_CH3/FTU1_QD_PHA | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| 52 | 80 | 117 | PTC6 | ADC0_SE23 | - | - | - | - | - | - | FCUART1_RX | FLEXCAN1_RX | FTU3_CH2/FTU1_QD_PHB | - | - | - | - | - | - | - |
| - | 81 | 118 | PTA16 | ADC0_SE22 | - | - | - | - | - | FCSPI1_PCS2 | - | FLEXCAN3_TX | FTU1_CH3 | - | - | - | - | - | - | - |
| - | 82 | 119 | PTA15 | ADC0_SE21 | - | - | - | - | - | FCSPI2_PCS3 | - | FLEXCAN3_RX | FTU1_CH2 | - | - | - | - | TRGSEL_OUT0 | - | - |
| 53 | 83 | 120 | PTE6 | ADC0_SE20 | - | CMP1_OUT | - | - | - | - | FCUART1_RTS | - | FTU3_CH7 | - | - | - | - | - | - | - |
| - | 84 | 121 | PTE2 | ADC0_SE19 | AONTIMER0_CLK3 | - | - | - | - | - | FCUART1_CTS | - | FTU3_CH6 | - | I2S1_SYNC | - | - | - | - | - |
| - | 85 | 122 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | 86 | 123 | VDD_HV_A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | 87 | 124 | V11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | 125 | PTE19 | ADC0_SE18 | - | - | - | - | FCIIC0_SCL | - | - | - | - | - | - | - | - | TRGSEL_IN12 | - | SCG_CLKOUT |
| - | - | 126 | PTE20 | ADC0_SE17 | - | - | - | - | FCIIC0_SDA | - | - | - | FTU4_CH0 | - | - | - | - | - | - | - |
| 54 | 88 | 127 | PTA14 | - | AONTIMER0_CLK2 | - | - | - | - | - | FCUART0_TX | - | FTU_FLT17 | FWM_IN | I2S0_D3 | - | - | TRGSEL_IN13 | - | - |
| - | - | 128 | PTE21 | ADC0_SE16 | AONTIMER0_CLK3 | - | - | - | - | - | FCUART0_RTS | FLEXCAN0_TX | FTU4_CH1 | | | - | - | | - | - |
| - | - | 129 | PTE22 | - | - | - | - | - | - | - | FCUART0_CTS | FLEXCAN0_RX | FTU4_CH2 | - | - | - | - | - | - | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| 55 | 89 | 130 | PTA13 | - | - | CMP1_OUT | - | - | - | - | FCUART0_RX | FLEXCAN1_TX | FTU1_CH7/FTU2_QD_PHA | - | I2S0_D0 | - | - | - | - | - |
| - | - | 131 | PTE23 | - | - | - | - | - | - | FCSPI0_PCS3 | - | - | FTU4_CH3 | - | - | - | - | - | - | - |
| - | - | 132 | PTE24 | - | - | - | - | - | - | FCSPI0_PCS2 | - | FLEXCAN2_TX | FTU4_CH4 | - | - | - | - | - | - | - |
| - | - | 133 | PTE25 | - | - | - | - | - | - | FCSPI0_PCS1 | - | FLEXCAN2_RX | FTU4_CH5 | - | - | - | - | - | - | - |
| 56 | 90 | 134 | PTA12 | - | - | CMP2_OUT | - | - | - | FCSPI0_SOUT | - | FLEXCAN1_RX | FTU1_CH6/FTU2_QD_PHB | - | I2S0_BCLK | - | - | - | - | - |
| 57 | 91 | 135 | PTA11[1] | - | - | - | - | - | - | FCSPI0_PCS0 | - | - | FTU1_CH5 | - | I2S0_SYNC | - | - | - | - | - |
| 58 | 92 | 136 | PTA10 | - | AONTIMER0_CLK1 | - | - | - | FCIIC0_SCL | - | - | - | FTU1_CH4 | - | - | JTAG_TDO/TRACE_SWO | - | - | - | - |
| 59 | 93 | 137 | PTE1 | - | - | - | - | - | FCIIC1_SCL | FCSPI0_SIN | FCUART0_RTS | - | FTU_FLT18 | - | I2S0_D1 | - | - | - | - | - |
| 60 | 94 | 138 | PTE0 | - | - | - | - | - | FCIIC1_SDA | FCSPI0_SCK | FCUART0_CTS | - | FTU_TCK1/FTU_FLT19 | - | I2S0_D2 | - | - | - | - | - |
| 61 | 95 | 139 | PTC5 | - | - | CMP1_OUT | - | - | FCIIC0_SDA | - | - | - | FTU2_CH0/FTU2_QD_PHB | - | - | JTAG_TDI | - | - | RTC_CLKOUT | - |

| 64LQFP | 100LQFP | 144LQFP | Pin Name | Functions | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ADC | AONTIMER | CMP | TRACE | EXTAL/XTAL | FCIIC | FCSPI | FCUART | FLEXCAN | FTU | FWM | I2S | JTAG/SWD/TRACE | OSC32K | TRGSEL | RTC | SCG |
| 62 | 96 | 140 | PTC4 | - | - | - | - | - | - | - | - | - | FTU1_CH0/FTU1_QD_PHB | FWM_IN | - | JTAG_TCLK/SWD_CLK | - | TRGSEL_IN14 | RTC_CLKOUT | - |
| 63 | 97 | 141 | PTA5[2] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 64 | 98 | 142 | PTA4 | - | - | CMP0_OUT | - | - | - | - | - | - | - | FWM_OUT_b | - | JTAG_TMS/SWD_DIO | - | TRGSEL_OUT7 | - | - |
| - | 99 | 143 | PTA9 | ADC1_SE7 | - | - | - | - | - | - | FCUART2_TX/FCUART0_TX | - | FTU_FLT20 | - | I2S0_MCLK | - | - | - | - | - |
| - | 100 | 144 | PTA8 | ADC1_SE3 | - | - | - | - | - | - | FCUART2_RX/FCUART0_RX | - | FTU_FLT21 | - | - | - | - | - | - | - |

***Note:*** 1. The function "NMI_b" is mapped to the pin "PTA11" only;

2. The function "RESET_b" is mapped to the pin "PTA5" only.

# Revision History

| Revision | Date | Changes |
|---|---|---|
| A0 | 2023/03/30 | PPAP release |
| A1 | 2023/11/28 | • In *Chapter 1 Introduction:*<br>- Updated *Figure 1. Ordering information* and the Note in *Section 1.1.1 Ordering Information;*<br>- Updated the description in *Section 1.1.2 Orderable Part Number;*<br>- Added a new section *Marking Rule.*<br>• Added qualification-related descriptions to *Chapter 2 Features;*<br>• In *Table 1. Absolute maximum ratings* in *Section 3.1 Absolute Maximum Ratings:*<br>- Changed the Max. data for "VDD_HV_A", "VDD_HV_B", "VREFH" and "VIN_DC" from "5.8" to "6.0";<br>- Updated the Note.<br>• In *Chapter 11 Pinout:*<br>- Updated figures for 144LQFP, 100LQFP, and 64LQFP;<br>- Fixed typos by removing "FTU1_CH2" and "FTU1_CH1" for 144LQFP (67, 68).<br>• Replaced the attachment *FC4150_Family_Orderable_Part_Number_List* with a new one *FC4150F512_Orderable_Part_Number_List_A1* |
| A2 | 2024/05/10 | • Replaced "FRO" with "FIRC" in the block diagram in *Chapter 2 Features;*<br>• In *Chapter 3 General:*<br>- Added the Max. value "0.1" for $V_{HYS}$ to T*able 5. LVR/LVD/HVD and POR* in *Section 3.5 LVR, LVD, HVD, and POR Operating Requirements;*<br>- Added the Max. values to both *Table 7. Chip RUN IDD* and *Table 8. Chip Low Power IDD* in *Section 3.7 Chip IDD;*<br>- Updated the notes for *Table 11. ESD ratings* in *Section 3.9 ESD Ratings.*<br>• Added the "Symbol" column to both *Table 16. FOSC Specification* and *Table 17. SOSC Specification* in *Chapter 5 Clock Specification;*<br>• Changed "page" into "word" for program time in *Table 23. NVM program/erase time* in *Section 6.2 NVM Program/Erase Time;*<br>• In *Chapter 7 Analog:*<br>- In *Table 24. ADC specification* of *Section 7.1 12-bit SAR ADC Specification:*<br>■ Changed the Max. value of Conversion Rate from "1" to "1.2";<br>■ Added a note for the formula for calculating the max. conversion rate.<br>- In *Table 25. CMP specification* of *Section 7.2 CMP Specification:*<br>■ Added the Max. value "±3" for INL;<br>■ Changed the Typ. value for DNL from "±1" to "±0.5", and added the Max. value "±1".<br>• Replaced "ETM_TRACE" with "TRACE" in *Table 33. FC4150F512 pin functions* in *Chapter 11 Pinout;*<br>• Updated the attachment *FC4150F512_Orderable_Part_Number_List* from version A1 to version A2;<br>• Editorial changes |

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