# FC7300Fxx Product Brief

## [FC7300F8MDT, FC7300F4MDD, FC7300F4MDS]

The FC7300F8MDT, FC7300F4MDD, and FC7300F4MDS constitute the FC7300 family of microcontrollers with diverse memory sizes, packages, and peripherals for design scalability.

The FC7300 product series extends the FC4150 family in the automotive industry with the Arm Cortex-M7 core at higher performance, larger memory, and ASILD rating. It also supports security requirements including the secure boot and EVITA full. The FC7300 is suitable for a wide range of applications in automotive.

## Key Features

- 32-bit ARM® Cortex®-M7 core (Multi)
- Up to 300 MHz execution speed
- Up to 8 MB PFlash, 256 KB DFlash, and 1088 KB RAM
- Temp Grade1/-40°C to +125°C
- ISO 26262 ASIL-D support
- Package: 176LQFP-EP and BGA320

### Target Applications

- Domain/Zonal controller
- Chassis domain
- Advanced Driver Assistant System (ADAS)
- Active suspension control system
- One-box
- EV main inverter
- Motor control
- Sensor fusion
- 800/400V Battery Management System (BMS)
- Gateway
- Electric Power Steering (EPS)
- Electronic Stability Control (ESC)
- Anti-lock Brake System (ABS)
- Auto Parking Assist (APA)

# 1 Block Diagram

The following figures show the block diagrams of the FC7300 family. For a detailed comparison, refer to *Table 1. FC7300 feature list*.

**Figure 1. FC7300F8MDT block diagram**

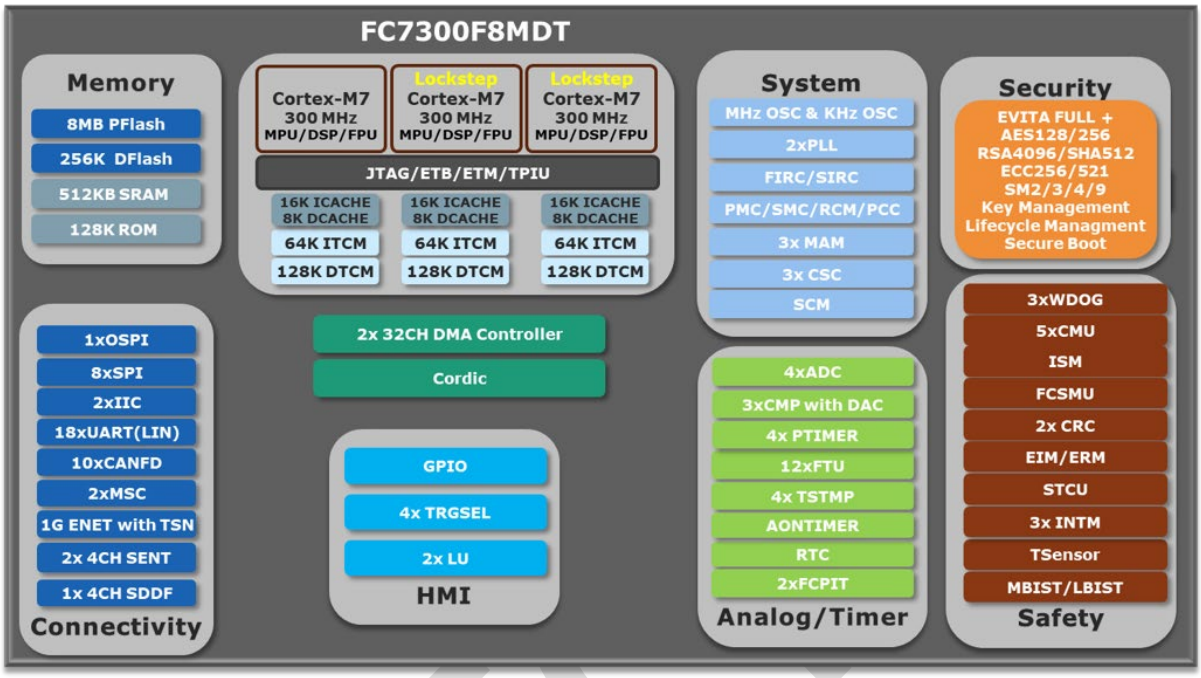



**Figure 2. FC7300F4MDD block diagram**

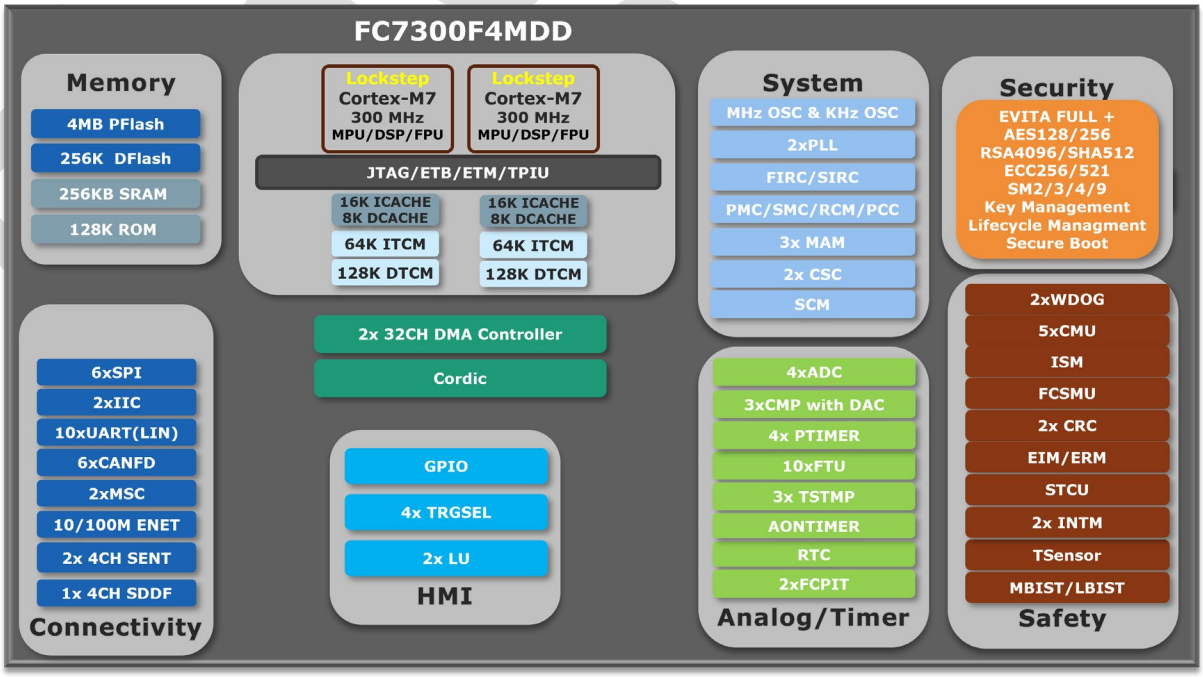
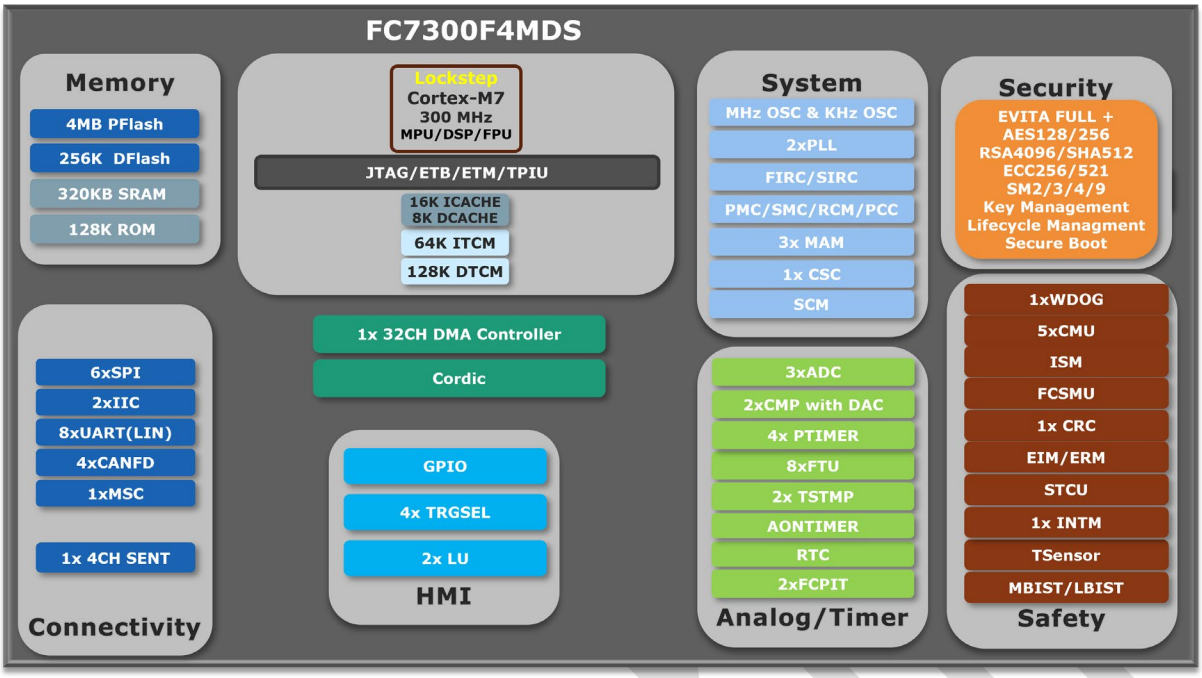


**Figure 3. FC7300F4MDS block diagram**



# 2 Features

The FC7300 product series has the following features:

## 2.1 Overview

- **Operating Environment**
  - Voltage range: 3.0 V to 5.5 V
  - Support separate 3.3 V and 5 V IO rings
  - Ambient temperature range: -40°C to +125°C; junction temperature: -40°C to +150°C
- **Arm Cortex-M7 Core**
  - 300 MHz frequency with 3.23 Dhrystone MIPS per MHz
  - Armv7 Architecture and Thumb-2 ISA
  - Digital Signal Processing (DSP) instruction
  - Single-precision Floating Point Unit (FPU)
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Support Memory Protection Unit (MPU) with 16 regions
  - Each core has 16 KB ICACHE and 8 KB DCACHE
  - Each core has 64 KB ITCM and 64 KB DTCM0 and 64 KB DTCM1
- **Up to three CM7 running cores (CPU0/1/2)**: CPU0 and CPU1 with extra checker cores (CPU3/4) to form lockstep operation. The lockstep monitor also covers the CM7 AXI2AHB and ITCM/DTCM0&1 ECC logic.
- **CORDIC accelerator for mathematical operations such as angles**
- **Mailbox (MB) with up to 16 communication channels and 4 interrupt channels for on-chip CPU and HSM;** support the hardware semaphore function.
- **Three Matrix Access Monitors (MAMs)**, which monitor all on-chip matrix access, and support watchdog timeout function for matrix access.
- **Up to three Core System Control (CSC) modules**; used for the stop mode related handle etc. control.
- **One System Control Module (SCM)**; used for the on-chip connection control, lock step control, CPU low power status, interrupt routing control, etc.
- **One Security Controller (SEC)**; used for on-chip debug/test mode/lifecycle related control.
- **Up to two 32-channel Direct Memory Access (DMA) modules** with selectable DMA sources.
- **Clock Sources**
  - 16 - 48 MHz Fast Oscillator (FOSC) with up to 50 MHz DC external input clock in bypass mode
  - 32 kHz Slow Oscillator (SOSC)
  - 96 MHz Fast Internal RC Oscillator (FIRC96M)
  - 12 MHz Slow Internal RC Oscillator (SIRC12M)
  - 32 kHz Slow Internal RC Oscillator (SIRC32k)
  - Up to 300 MHz Phased Lock Loop (PLL0 and PLL1) with the reference clock from FIRC 48 MHz or FOSC
- **Power Management**
  - Four power modes: RUN, WAIT, STOP and Standby. Optional 64 KB System RAM retention in standby mode.
- **Memory**
  - Up to 8 MB program flash memory with Address and Data Single-bit Error Correction and Double-bit Error Detection (SECDED)
  - Up to 256 KB data flash memory with Address and Data SECDED
  - Up to 512 KB SRAM with Address and Data SECDED

- One Octal Serial Peripheral Interface (OSPI) with up to 75 MHz DDR support. (Only available for FC7300F8MDT)
- 128 KB ROM with Address and Data SECDED, which contains CM7 core self-test/flash program & erase/ Hardware Secure Module (HSM) secure boot etc.

- **Analog**
  - Up to four 12-bit Successive Approximation (SAR) Analog-to-Digital Converters (ADCs) with up to 32 channel analog inputs per module
  - Up to three Analog Comparators (CMPs) with internal 8-bit Digital-to-Analog Converter (DAC)
- **Debug Functionality**
  - Serial Wire/JTAG Debug Port (SWJ-DP) combines
  - Data Watchpoint and Trace (DWT)
  - Instrumentation Trace Macrocell (ITM)
  - Embedded Trace Macrocell (ETM)
  - Trace Port Interface Unit (TPIU) with up to 16-bit
  - Flash Patch and Breakpoint (FPB) Unit
  - Cross Trigger Interface (CTI)
  - Embedded Trace Buffer (ETB)
  - FUNNEL
  - JTAG Test Access Port (TAP) and boundary scan support
- **Human-Machine Interface (HMI)**
  - Up to 248 GPIO pins (excl. reset pin) with separated core interrupt support
  - Non-Maskable Interrupt (NMI)
  - GPIO interface with separated core control
- **Communication Interfaces**
  - Up to 18 FC Universal Asynchronous Receiver/Transmitter (FCUART) modules with LIN support
  - Up to eight FC Serial Peripheral Interface (FCSPI) modules; support 1/2/4 data lines and master/slave mode
  - Two FC Inter-Integrated Circuit (FCIIC) modules
  - Up to ten FLEXCAN modules with optional CAN-FD support
  - One 10/100/1000 Mbps Ethernet with IEEE1588 and TSN, MII/RMII/RGMII support. (Not available for FC7300F4MDS)
  - Up to two Micro Second Channel (MSC) modules
  - Up to two 4-channel Sent Edge Nibble Transmit (SENT) modules
  - Up to one 4-channel Sigma Delta Digital Filter (SDDF) module
  - Four Trigger Selects (TRGSELs) for on-chip bus connection
  - Two Lookup Unit (LU) modules; each supports 4 lookup tables
- **Security**
  - Hardware Secure Module (HSM) with crypto algorithms including AES/SM4/ECC/RAS/SHA/SM3/SM4/SM9
  - EVITA full capability
  - Support random number generation and pseudo random number generation
  - Key import/export management
  - Monotonic counter support
  - Support secure boot and non-secure boot mode
  - Support In-System Program (ISP) mode
- **Safety**
  - Up to five Clock Monitor Units (CMUs) for all internal critical root clock source monitor

- Power Management Controller (PMC) with LVR/LVD/HVD etc. on internal generate supply and external supply protection
- ECC with both address and data protection on ROM, flash and SRAM memories
- Memory Access Monitor on the system memory, including peripheral slots such as the APB bridge (AFCB0 and AFCB1)
- Up to two Cyclic Redundancy Check (CRC) modules
- Up to three internal Watchdogs (WDOGs) with window function
- One Error Injection Module (EIM) for ECC logic and lock step logic check
- One Error Reporting Module (ERM) for ECC-related monitor errors
- One Fault Control and Safety Management Unit (FCSMU) for on-chip error handling and optionally outputting the chip status to external pins
- LockStep Monitor for CPU0/1
- End-to-End ECC protection on all CPUx-related access paths
- One Safety Test Control Unit (STCU) for Logic BIST (LBIST) and Memory BIST (MBIST) controller
- One Interface Safety Monitor (ISM) module to monitor up to 32 delays/periods/duties of critical signals
- Up to three Interrupt Monitor (INTM) modules; each supports up to 4 channels and can monitor the interrupt keep-active timeout or interrupt generation timeout
- CM7 core self-test API in ROM code

- **Timers**
  - Up to 12 Flexible Timer Unit (FTU) modules with IC/OC/PWM function; FTU2/3/4/5 also support Quadrature Decoder function
  - One Always-on Timer (AONTIMER) with standby wake up capability
  - Four Programmable Timers (PTIMERs)
  - Two FC Programmable Interrupt Timers (FCPITs); each has 4 channels
  - One Real-Time Clock (RTC)
  - Up to four 56-bit Timer Stamps (TSTMPs) with four 32-bit compare channels, TSTMP0 runs at 1 MHz clock and TSTMP1/2/3 run at Bus clock
  - One Frequency Measurement (FREQM) module; with up to 64 input clock sources
- **Package**
  - 176LQFP-EP and LFBGA320 package options

## 2.2 Feature Comparison

The table below lists the differences in major features and peripheral counts of three chips from the FC7300 family.

**Table 1. FC7300 feature list**

| Features | | | | Chips | | |
|---|---|---|---|---|---|---|
| | | | | FC7300F8MDT | FC7300F4MDD | FC7300F4MDS |
| Automotive cert. | Temp. Grade | | | Grade1/ -40°C to +125°C | | |
| Function Safety | | | | ASIL-D | | |
| Power Design | Voltage Range | | | 3.0V to 5.5V | | |
| | $T_A$ | | | -40°C to +125°C | | |
| | $T_J$ | | | -40°C to +150°C | | |
| CPU | Core | | | Cortex-M7; 2*Lockstep + 1 | Cortex-M7; 2*Lockstep | Cortex-M7; 1*Lockstep |
| | Frequency | | | 300 MHz | | |
| | MPU | | | Yes | | |
| | I CACHE | | | 16 KB | | |
| | D CACHE | | | 8 KB | | |
| Memory | PFlash/Bank | | | 8 MB/4 | 4 MB/2 | |
| | DFlash | | | 256 KB | | |
| | RAM | SRAM | | 512 KB | 256 KB | 320 KB |
| | | TCM | | 3 × 192 KB | 2 × 192 KB | 192 KB |
| | ROM | | | 128 KB | | |
| Clock | | | | Multi clocks, including FIRC96M/SIRC12M/SIRC32K/FOSC48M/SOSC32K/PLL | | |
| Digital IOs | | | | 248 | | |
| Peripherals | System | CPM | | Yes | | |
| | | DMA | | 2 × 32-channel | | 1 × 32-channel |
| | | WKU | | Yes | | |
| | | PMC | | Yes | | |
| | | SMC | | Yes | | |
| | | RGM | | Yes | | |
| | | SEC | | Yes | | |
| | | CORDIC | | Yes | | |
| | | CSC | | 3 | 2 | 1 |
| | | SCM | | Yes | | |
| | | MAM | | 3 | | |
| | | MB | | Yes | | |
| | Memory | FMC | | Yes | | |
| | | ACC | | Yes | | |
| | | OSPI | | Yes | No | |
| | Clocking | SCG | | Yes | | |
| | | PCC | | Yes | | |
| | Function Safety | WDOG | | 3 | 2 | 1 |
| | | EIM | | Yes | | |

| Features | | | Chips | | |
|---|---|---|---|---|---|
| | | | FC7300F8MDT | FC7300F4MDD | FC7300F4MDS |
| Peripherals | Function Safety | ERM | Yes | | |
| | | INTM | 3 | 2 | 1 |
| | | CMU | 5 | | |
| | | ISM | Yes | | |
| | | FCSMU | Yes | | |
| | | STCU | Yes | | |
| | Security | CRC | 2 | | 1 |
| | HMI | GPIO | Yes | | |
| | | PORT | Yes | | |
| | | TRGSEL | 4 | | |
| | | LU | 2 | | |
| | Analog | ADC | 4 | | 3 |
| | | CMP | 3 | | 2 |
| | | TMU | Yes | | |
| | Timer | FTU | 12 | 10 | 8 |
| | | FCPIT | 2 | | |
| | | TSTMP | 4 | 3 | 2 |
| | | RTC | Yes | | |
| | | AONTIMER | Yes | | |
| | | PTIMER | 4 | | |
| | | FREQM | Yes | | |
| | Comm. | FCSPI | 8 | 6 | |
| | | FCIIC | 2 | | |
| | | FCUART | 18 | 10 | 8 |
| | | FLEXCAN | 10 | 6 | 4 |
| | | SENT | 2 | | 1 |
| | | SDDF | Yes | | No |
| | | MSC | 2 | | 1 |
| | | ENET | Yes (1 Gbit) | Yes (10/100 Mbit) | No |
| Security | | | HSM, EVITA Full | | |
| Package | | 176LQFP-EP | Yes | | |
| | | BGA320 | Yes | | |

# Revision History

| Revision | Date | Changes |
|---|---|---|
| 0.1 | 2022/07/14 | Initial release |

## Contact Us

**Headquarters:**
Room 213, 2nd Floor, Suite Z104, Building 2, NO.78, East Jinshan RD, New District, Suzhou, Jiangsu 215011, P.R. China **Website:** www.flagchip.com.cn

**TEL:** +86-512-66166689

## Disclaimer

单击下面可查看定价，库存，交付和生命周期等信息

>>Flagchip(旗芯微)