

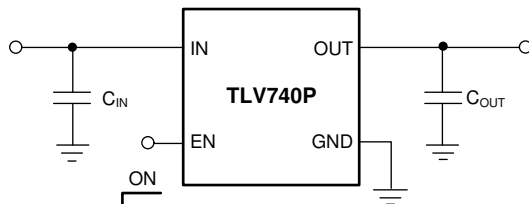
TLV740P 300-mA, Low-Dropout Regulator With Foldback Current Limit

1 Features

- Foldback overcurrent protection
- Packages:
 - 1-mm × 1-mm, 4-pin X2SON
 - 5-pin SOT-23
- Very low dropout: 460 mV at 300 mA
- Accuracy: 1%
- Low I_Q : 50 μ A
- Input voltage range: 1.4 V to 5.5 V
- Available in fixed-output voltages: 1 V to 3.3 V
- High PSRR: 65 dB at 1 kHz
- Active output discharge

2 Applications

- [Portable media players](#)
- [Standard notebook PCs](#)
- [Streaming media players](#)
- [Home printers](#)
- [STB and DVR](#)



Typical Application Circuit

3 Description

The TLV740P low-dropout (LDO) linear regulator is a low quiescent current LDO with excellent line and load transient performance designed for power-sensitive applications. This device provides a typical accuracy of 1%.

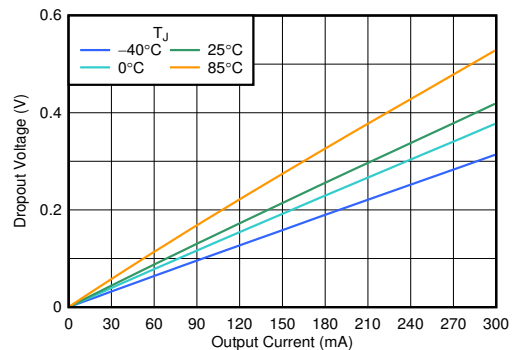
The TLV740P also provides inrush current control during device power up and enabling. The TLV740P limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

The TLV740P is available in standard DQN and DBV packages. The TLV740P also provides an active pulldown circuit to quickly discharge output loads.

Device Information (1)

DEVICE NAME	PACKAGE	BODY SIZE
TLV740P	SOT-23 (5)	2.90 mm × 1.60 mm
	X2SON (4)	1.00 mm × 1.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Dropout Voltage vs Output Current (3.3 V_{OUT})



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• Changed status of DQN package from preview to production data.....	1

5 Pin Configuration and Functions

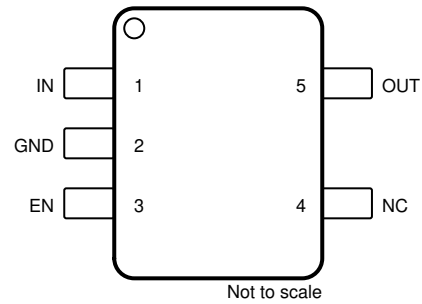
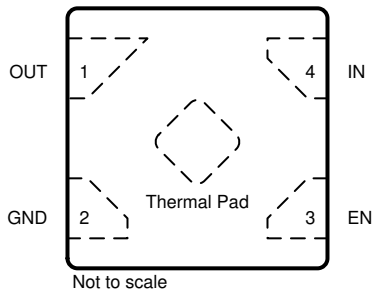


Figure 5-1. DQN Package, 4-Pin X2SON, Top View

Figure 5-2. DBV Package, 5-Pin SOT-23, Top View

Table 5-1. Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	X2SON	SOT-23		
EN	3	3	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. Do not float this pin. If not used, connect EN to IN.
GND	2	2	—	Ground pin. This pin must be connected to ground on the board.
IN	4	1	I	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the <i>Recommended Operating Conditions</i> table. Place the input capacitor as close to the input of the device as possible.
NC	—	4	—	No connect pin. This pin is not internally connected. Connect to ground for best thermal performance or leave floating.
OUT	1	5	O	Regulated output pin. A 1- μ F or greater effective capacitance is required from OUT to ground for stability. see the <i>Recommended Operating Conditions</i> table. For best transient response, use a 1- μ F or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible.
Thermal pad	—	—	—	The thermal pad is electrically connected to the GND pin. Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{IN}	-0.3	6.0	V
	V_{EN}	-0.3	$V_{IN}^{(2)}$	
	V_{OUT}	-0.3	$V_{IN} + 0.3$ or 3.6 ⁽³⁾	
Temperature	Operating junction, T_J	-55	125	°C
	Storage, T_{stg}	-55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum is V_{IN} or smaller.
- (3) Maximum is $V_{IN} + 0.3$ V or 3.6 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.4		5.5	V
V_{OUT}	Output voltage	0		$V_{IN} + 0.3$	V
V_{EN}	Enable voltage	0		$V_{IN}^{(1)}$	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor	1			μF
C_{OUT}	Output capacitor ⁽²⁾	1		100	μF
f_{EN}	Enable toggle frequency			10	kHz
T_J	Junction temperature	-40		85	°C

- (1) V_{EN} is V_{IN} or smaller.
- (2) Effective output capacitance of 0.5 μF minimum required for stability.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV740P		UNIT
		DQN (X2SON)	DBV (SOT-23-5)	
		4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.3	216	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	161.5	123.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	164.6	88.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.9	62.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	164.0	87.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	154.8	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at operating temperature range ($T_J = +25^\circ\text{C}$), $V_{IN} = V_{OUT(NOM)} + 2.1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\ \mu\text{F}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output accuracy	$1\text{ V} \leq V_{OUT} \leq 3.3\text{ V}$	-1		1	%
	Maximum output current ⁽¹⁾				300	mA
	Output voltage temperature coefficient	$I_{OUT} = 0.1\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$		0.0017		%/°C
	Line regulation	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		1	5	mV
	Load regulation	$1\text{ mA} \leq I_{OUT} \leq 300\text{ mA}$		10	30	mV
V_{DO}	Dropout voltage	$V_{OUT} = 0.95 \times V_{OUT(nom)}$ $1\text{ V} \leq V_{OUT} < 1.8\text{ V}$, $I_{OUT} = 300\text{ mA}$		1200	1300	mV
		$V_{OUT} = 0.95 \times V_{OUT(nom)}$ $1.8\text{ V} \leq V_{OUT} < 2.1\text{ V}$, $I_{OUT} = 300\text{ mA}$		700	800	
		$V_{OUT} = 0.95 \times V_{OUT(nom)}$ $2.1\text{ V} \leq V_{OUT} \leq 3.3\text{ V}$, $I_{OUT} = 300\text{ mA}$		460	500	
I_{GND}	Ground current	$I_{OUT} = 0\text{ mA}$		50	80	μA
I_{SHDN}	Shutdown current	$V_{EN} \leq 0.4\text{ V}$, $3.1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$		0.1	1	μA
PSRR	Power-supply rejection ratio	$V_{IN} = 5.4\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 150\text{ mA}$	$f = 100\text{ Hz}$		67	dB
			$f = 10\text{ kHz}$		45	
			$f = 1\text{ MHz}$		32	
V_n	Output noise voltage	$BW = 100\text{ Hz to } 100\text{ kHz}$, $V_{OUT} = 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$		65		μV_{RMS}
t_{STR}	Startup time ⁽²⁾	$C_{OUT} = 1\ \mu\text{F}$, $I_{OUT} = 300\text{ mA}$		100		μs
V_{HI}	EN pin high voltage (enabled)	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$	1.0		V_{IN}	V
V_{LO}	EN pin low voltage (disabled)		0		0.4	V
I_{EN}	Enable pin current	$V_{IN} = 5.5\text{ V}$, $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$		10		nA
$R_{PULLDOWN}$	Pulldown resistance	$V_{IN} = 5.5\text{ V}$, $V_{EN} = 0\text{ V}$		120		Ω
I_{CL}	Output current limit		360			mA
I_{SC}	Short circuit current limit	$V_{OUT} = 0\text{ V}$		40		mA
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		158		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		140		

- (1) Maximum output current is affected by the PCB layout, metal trace width, number of layers, ambient temperature and other environmental factors. Thermal limitations of the system must be carefully considered.
- (2) Startup time = time from EN assertion to $0.95 \times V_{OUT(NOM)}$.

6.6 Typical Characteristics

over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 85°C), $V_{IN} = V_{OUT(nom)} + 2.1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$

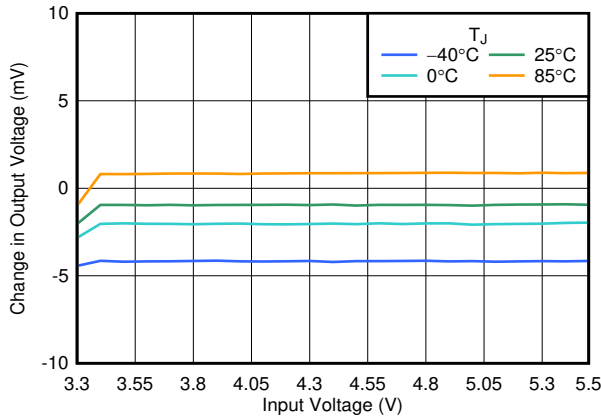


Figure 6-1. Line Regulation vs V_{IN}

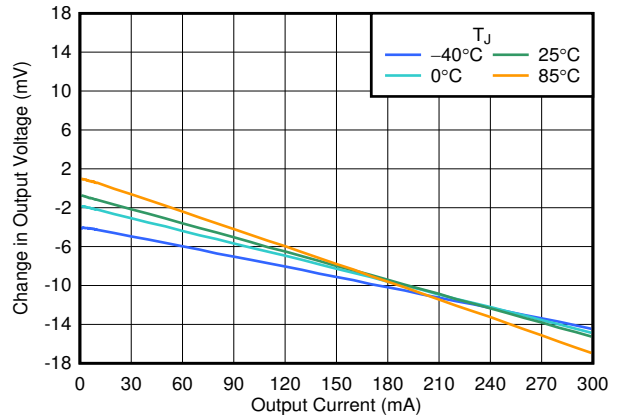


Figure 6-2. Load Regulation vs I_{OUT}

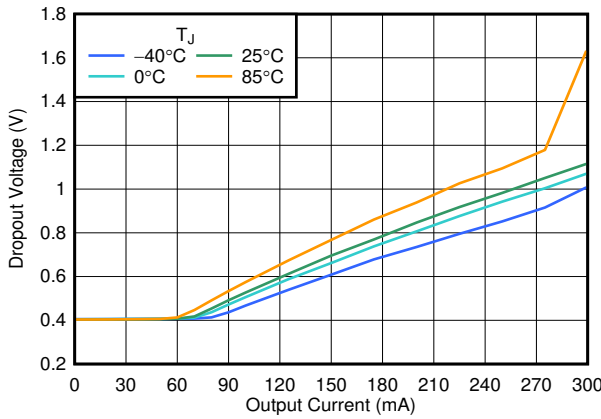


Figure 6-3. Dropout Voltage vs I_{OUT}

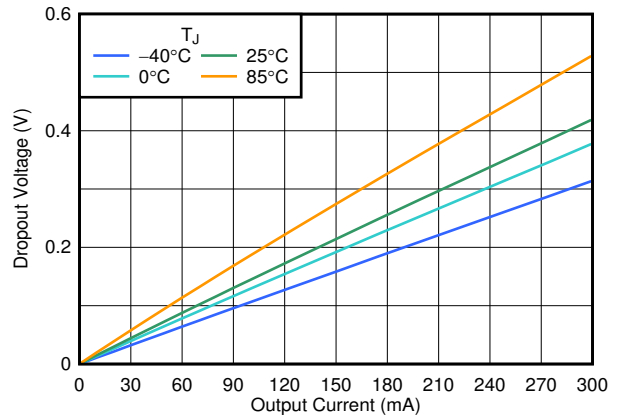


Figure 6-4. Dropout Voltage vs I_{OUT}

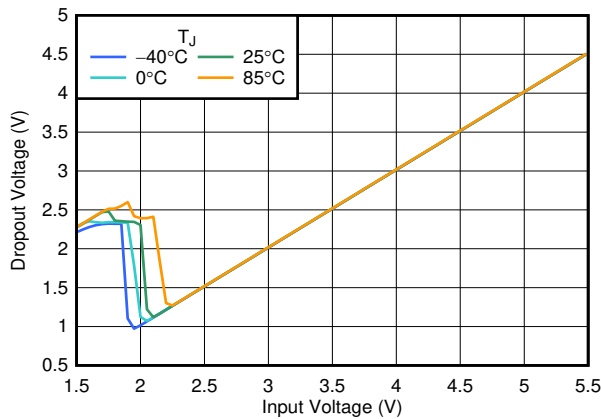


Figure 6-5. Dropout Voltage vs V_{IN}

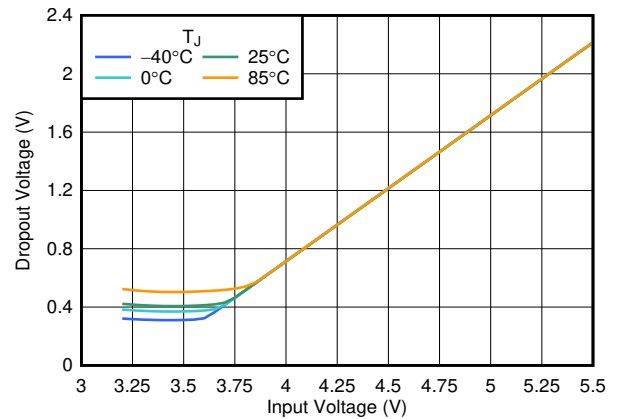


Figure 6-6. Dropout Voltage vs V_{IN}

6.6 Typical Characteristics (continued)

over operating temperature range ($T_J = -40^\circ\text{C}$ to 85°C), $V_{IN} = V_{OUT(nom)} + 2.1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); typical values are at $T_J = 25^\circ\text{C}$

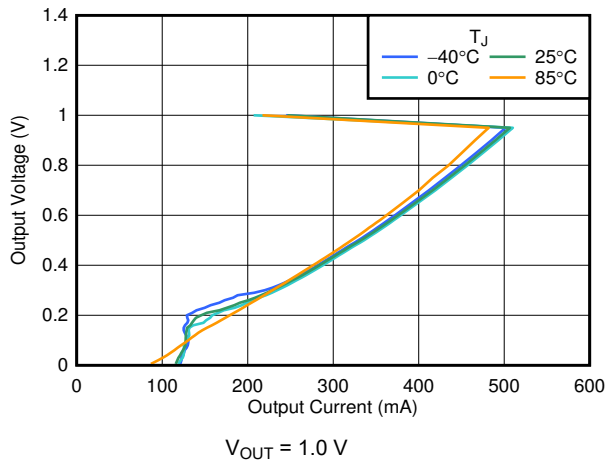


Figure 6-7. Foldback Current Limit vs I_{OUT}

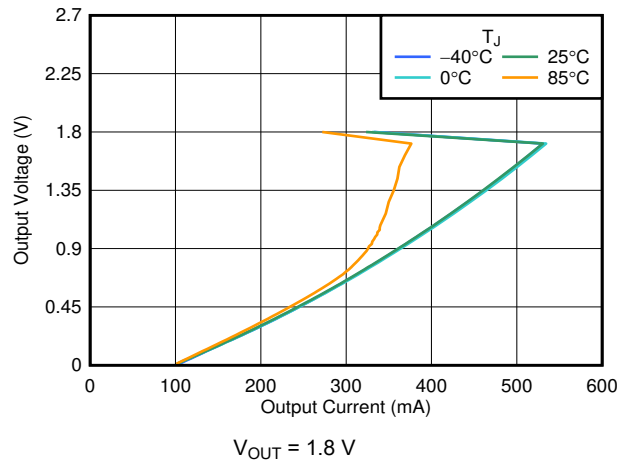


Figure 6-8. Foldback Current Limit vs I_{OUT}

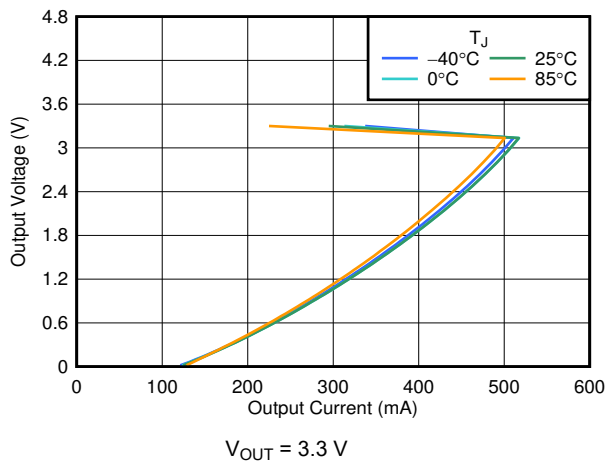


Figure 6-9. Foldback Current Limit vs I_{OUT}

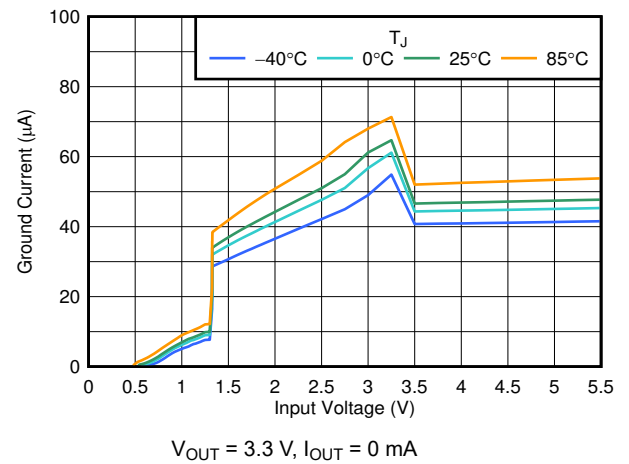


Figure 6-10. I_{GND} vs V_{IN}

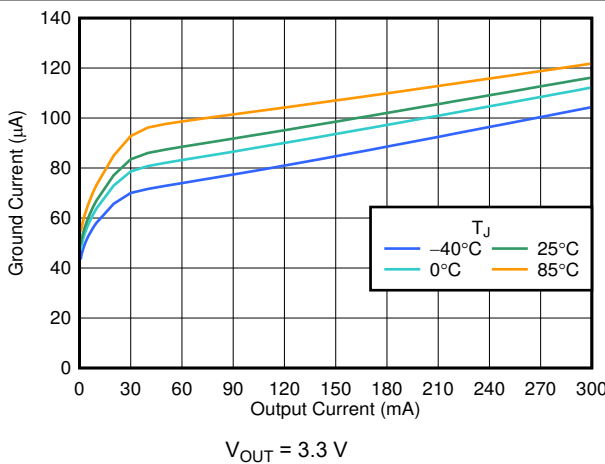


Figure 6-11. I_{GND} vs I_{OUT}

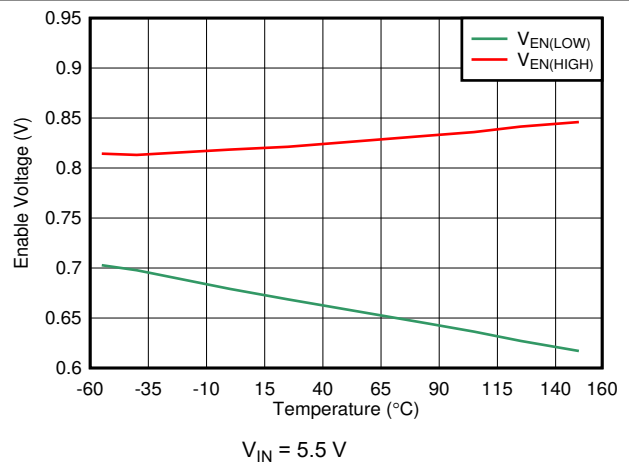


Figure 6-12. EN High and Low Threshold vs Temperature

6.6 Typical Characteristics (continued)

over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 85°C), $V_{IN} = V_{OUT(nom)} + 2.1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$

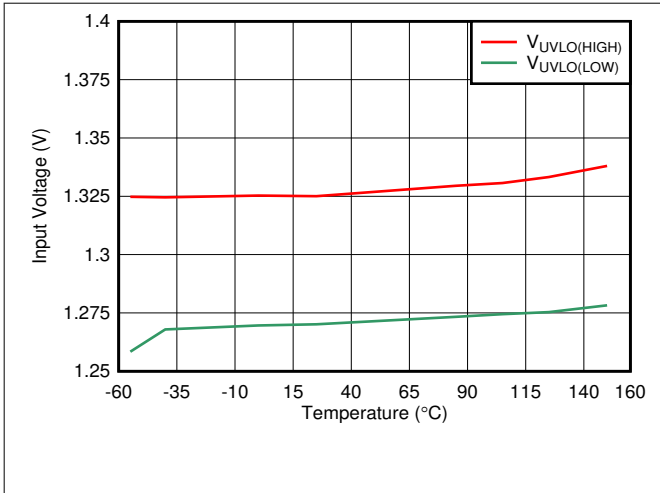


Figure 6-13. UVLO Rising and Falling Threshold vs Temperature

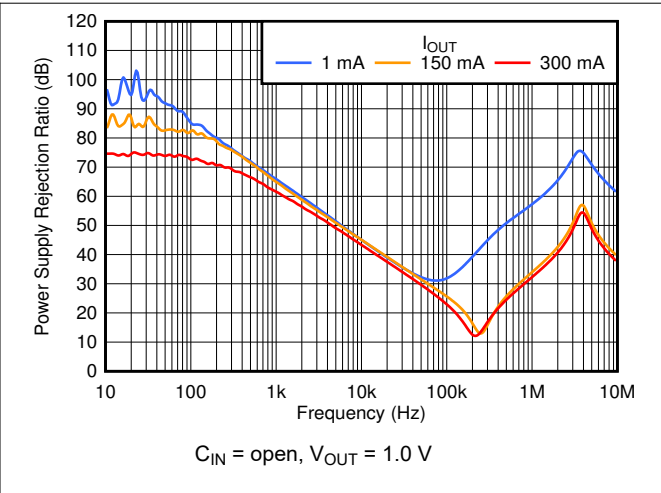


Figure 6-14. PSRR vs Frequency and I_{OUT}

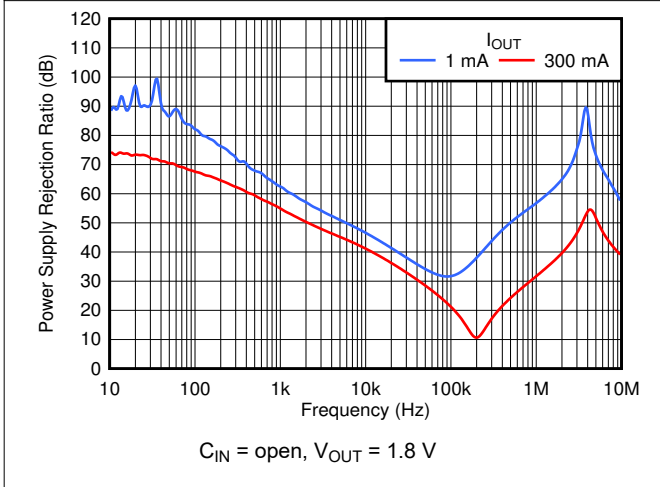


Figure 6-15. PSRR vs Frequency and I_{OUT}

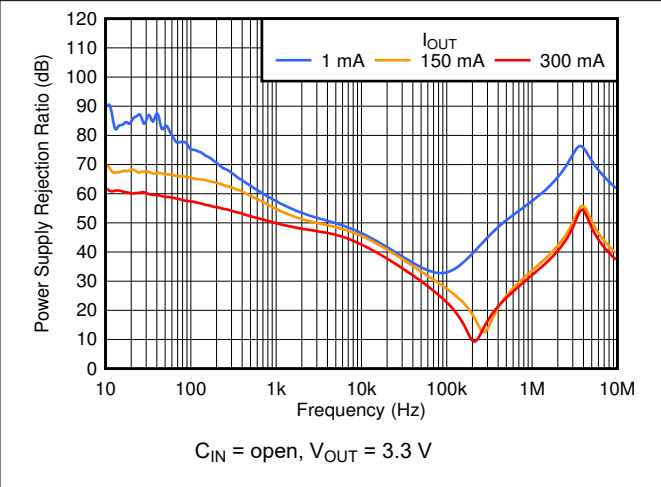


Figure 6-16. PSRR vs Frequency and I_{OUT}

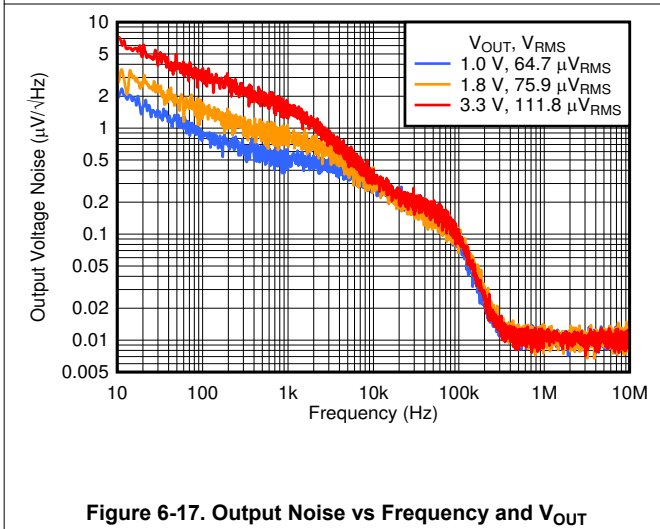


Figure 6-17. Output Noise vs Frequency and V_{OUT}

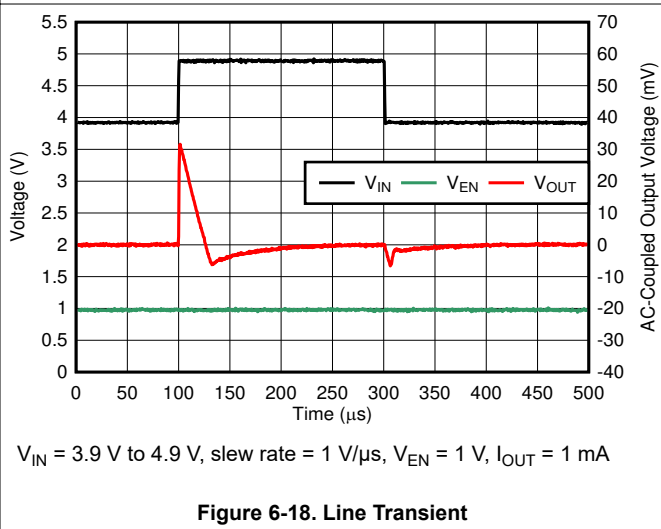
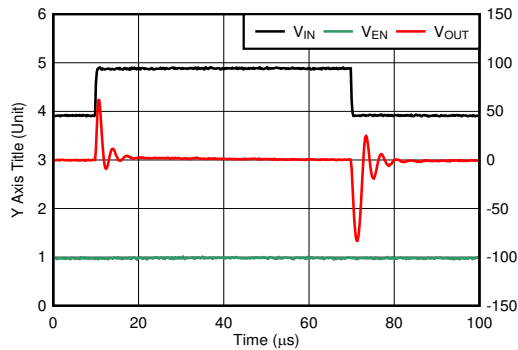


Figure 6-18. Line Transient

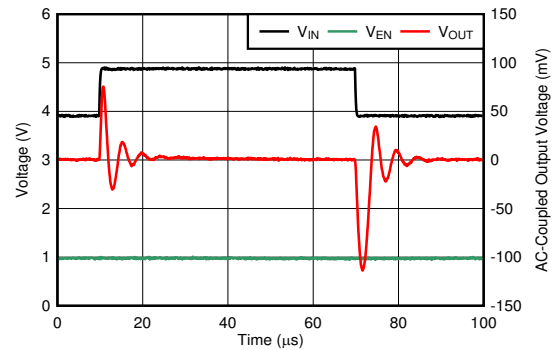
6.6 Typical Characteristics (continued)

over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 85°C), $V_{IN} = V_{OUT(nom)} + 2.1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$



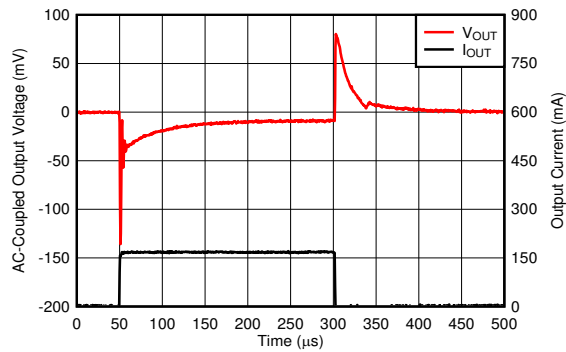
$V_{IN} = 3.9\text{ V}$ to 4.9 V , slew rate = $1\text{ V}/\mu\text{s}$, $V_{EN} = 1\text{ V}$, $I_{OUT} = 150\text{ mA}$

Figure 6-19. Line Transient



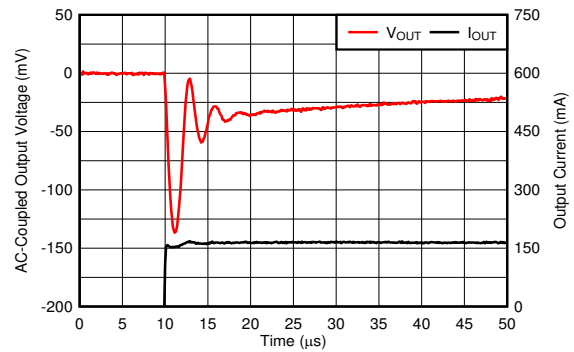
$V_{IN} = 3.9\text{ V}$ to 4.9 V , slew rate = $1\text{ V}/\mu\text{s}$, $V_{EN} = 1\text{ V}$, $I_{OUT} = 300\text{ mA}$

Figure 6-20. Line Transient



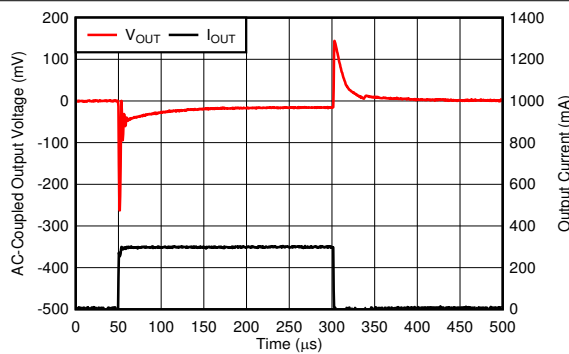
$V_{IN} = 3.9\text{ V}$, $V_{EN} = 1\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 150 mA , slew rate = $1\text{ A}/\mu\text{s}$

Figure 6-21. Load Transient



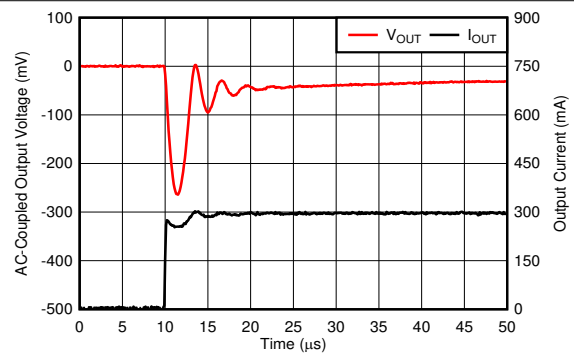
$V_{IN} = 3.9\text{ V}$, $V_{EN} = 1\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 150 mA , slew rate = $1\text{ A}/\mu\text{s}$, rising edge

Figure 6-22. Load Transient



$V_{IN} = 3.9\text{ V}$, $V_{EN} = 1\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , slew rate = $1\text{ A}/\mu\text{s}$

Figure 6-23. Load Transient

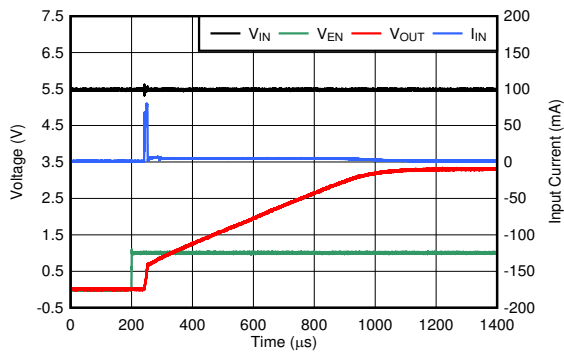


$V_{IN} = 3.9\text{ V}$, $V_{EN} = 1\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , slew rate = $1\text{ A}/\mu\text{s}$, rising edge

Figure 6-24. Load Transient

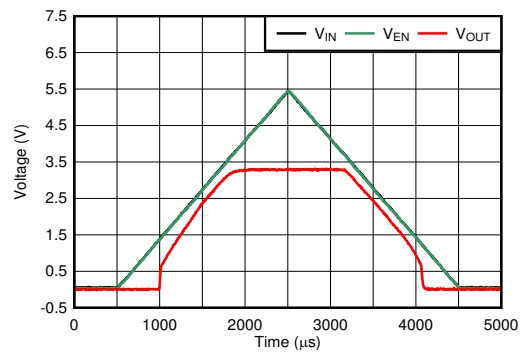
6.6 Typical Characteristics (continued)

over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 85°C), $V_{IN} = V_{OUT(nom)} + 2.1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$



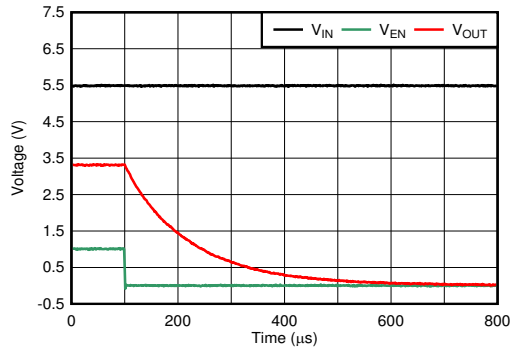
$V_{IN} = 5.5\text{ V}$, $C_{IN} = \text{open}$, $I_{OUT} = \text{open}$

Figure 6-25. Start-Up With EN, Inrush Current



$V_{IN} = 0\text{ V}$ to 5.5 V to 0 V , $I_{OUT} = 150\text{ mA}$

Figure 6-26. Start-Up and Shutdown



$V_{IN} = 5.5\text{ V}$, $V_{EN} = 1\text{ V}$ to 0 V , $I_{OUT} = \text{open}$

Figure 6-27. Shutdown Response With Enable

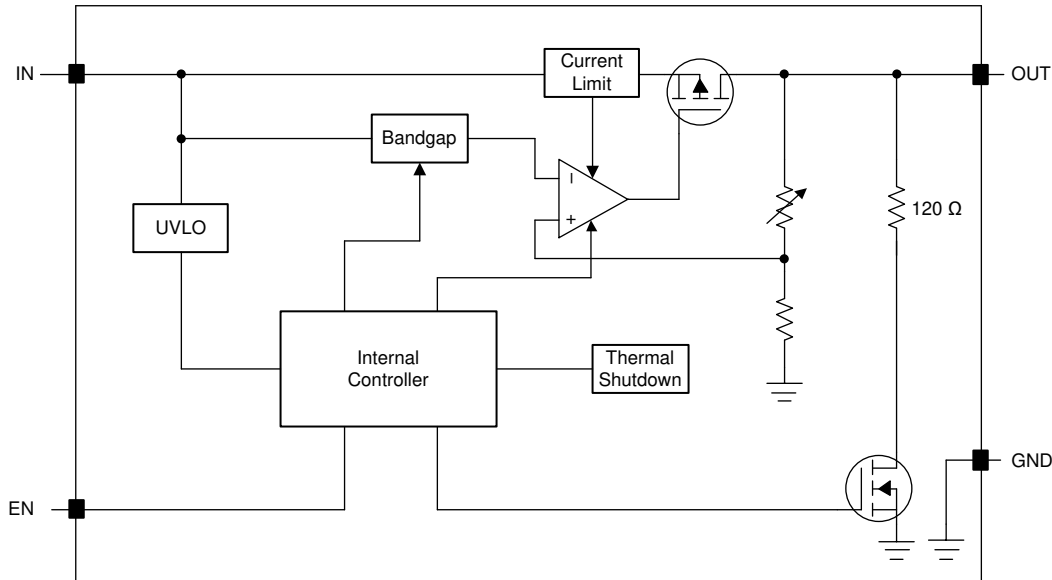
7 Detailed Description

7.1 Overview

The TLV740P is a cost-effective low-dropout (LDO) regulator that consumes low quiescent current and delivers excellent line and load transient performance. These characteristics make the device ideal for a wide range of portable applications.

This LDO offers foldback current limit, output enable, active discharge, undervoltage lockout (UVLO), and thermal protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.95 \text{ V} \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

Figure 7-1 shows a diagram of the foldback current limit.

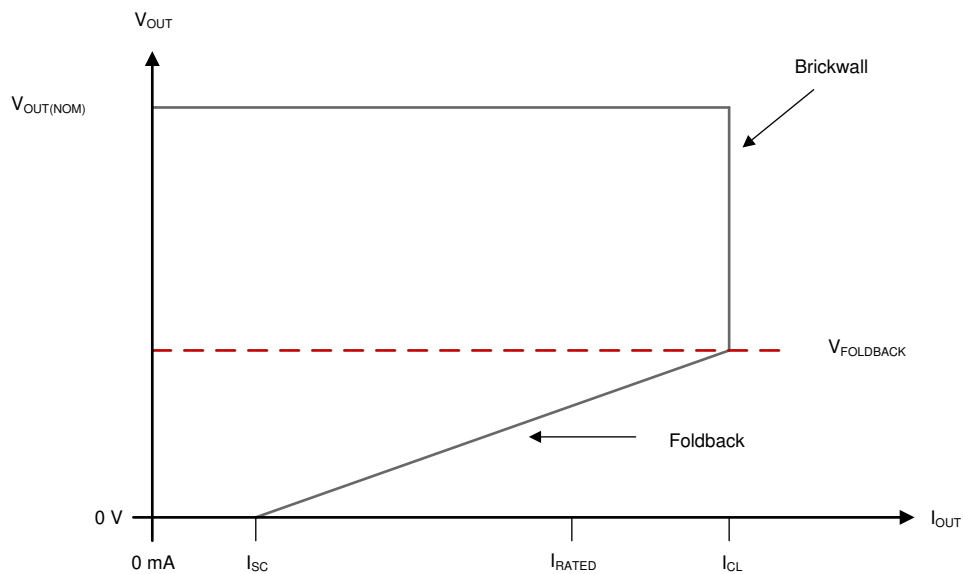


Figure 7-1. Foldback Current Limit

7.3.2 Output Enable

The enable pin (EN) is active high. Enable the device by forcing the voltage of the enable pin to exceed the minimum EN pin high-level input voltage (see the *Electrical Characteristics* table). Turn off the device by forcing the voltage of the enable pin to drop below the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

7.3.3 Active Discharge

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.3.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. Figure 7-2 illustrates the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.

- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

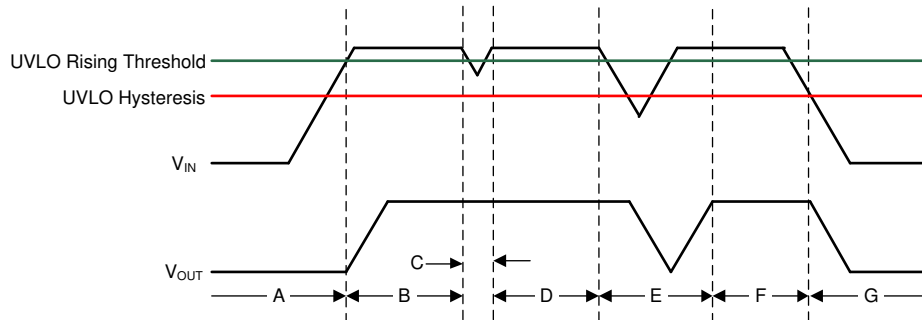


Figure 7-2. Typical UVLO Operation

7.3.5 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

The device requires an input capacitor of 1.0 μF or larger, as specified in the *Recommended Operating Conditions* table for stability. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

The device also requires an output capacitor of 1.0 μF or larger, as specified in the *Recommended Operating Conditions* table for stability. Dynamic performance of the device is improved by using a higher capacitor than the minimum output capacitor.

8.1.3 Dropout Voltage

The device uses a PMOS pass transistor to achieve low dropout. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{\text{DS(on)}}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as $(V_{\text{IN}} - V_{\text{OUT}})$ approaches dropout.

8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in [Figure 8-1](#), when the slew rate and voltage levels are in the correct range. Use an enable signal to delay the LDO startup to avoid V_{OUT} overshoot resulting from dropout exit. The enable signal can be set high after V_{IN} is greater than $V_{OUT(nom)}$.

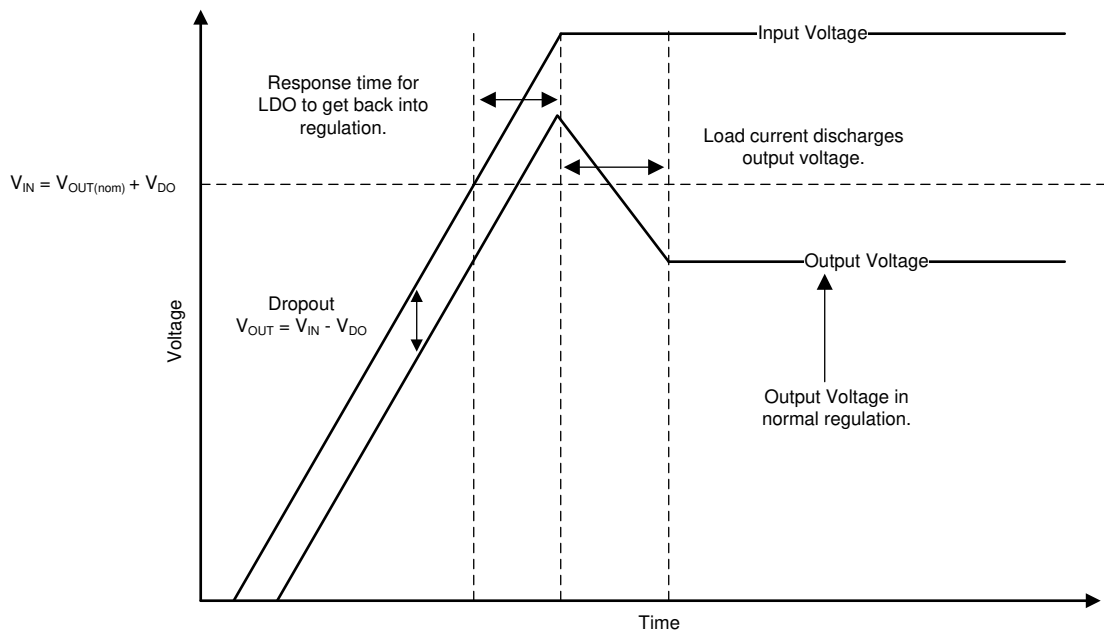


Figure 8-1. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. [Figure 8-2](#) illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

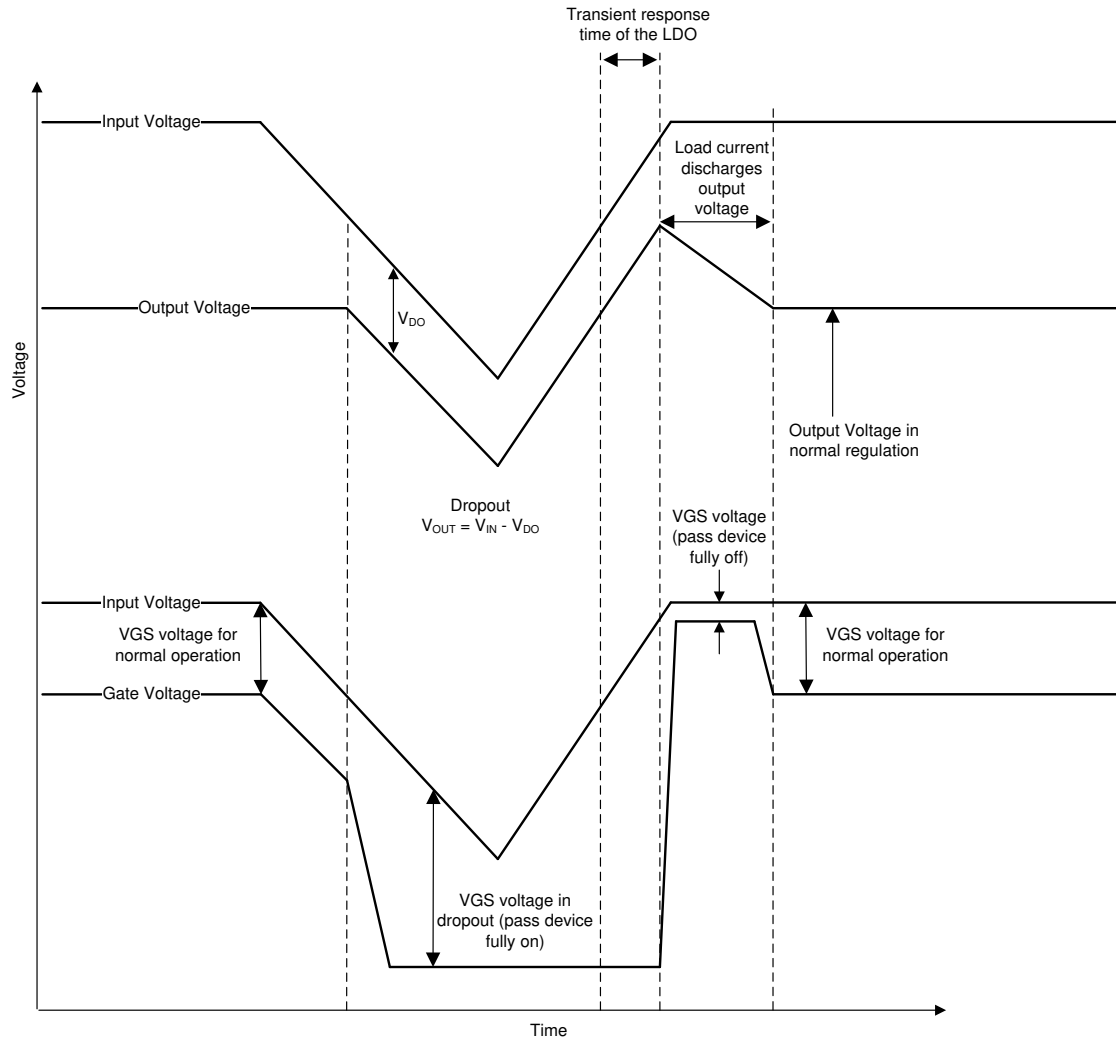


Figure 8-2. Line Transients From Dropout

8.1.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.1.6 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3 \text{ V}$:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. [Figure 8-3](#) shows one approach of protecting the device.

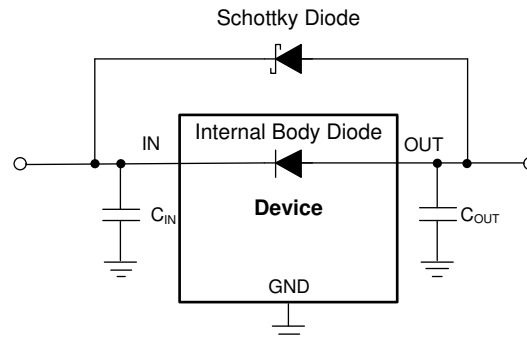


Figure 8-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.7 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use [Equation 2](#) to approximate P_D :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TLV740P allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the DQN package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to [Equation 3](#), power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). [Equation 4](#) rearranges [Equation 3](#) for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Recommended Operating Conditions* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.7.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 5 and are given in the *Recommended Operating Conditions* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- P_D is the power dissipated as explained in Equation 2
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.7.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 8-4 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Voltage* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
 - The shape of the slope is given by Equation 4. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} - V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

Figure 8-4 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Recommended Operating Conditions* table.

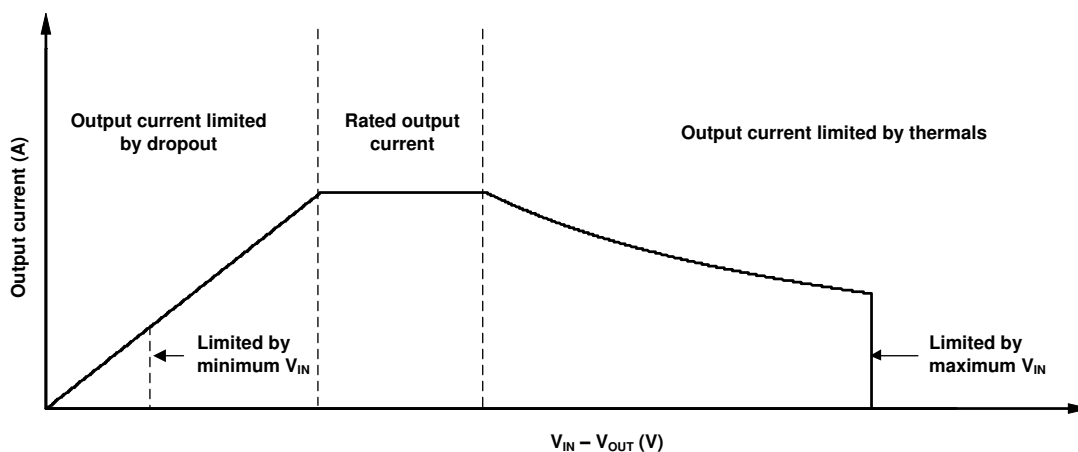


Figure 8-4. Region Description of Continuous Operation Regime

8.2 Typical Application

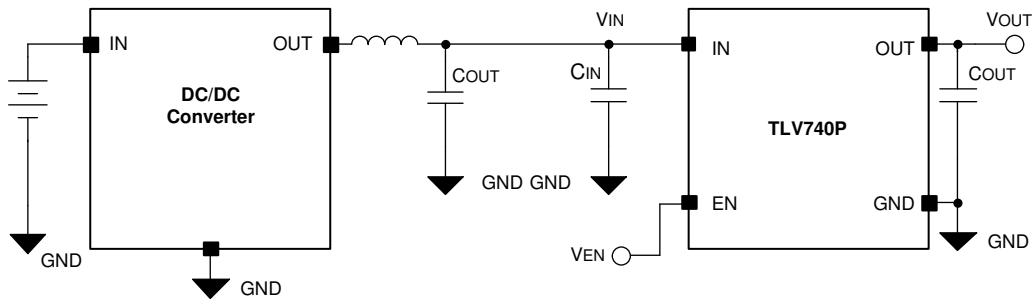


Figure 8-5. Operation From a DC/DC Converter

8.2.1 Design Requirements

Table 8-1 summarizes the design requirement for this application.

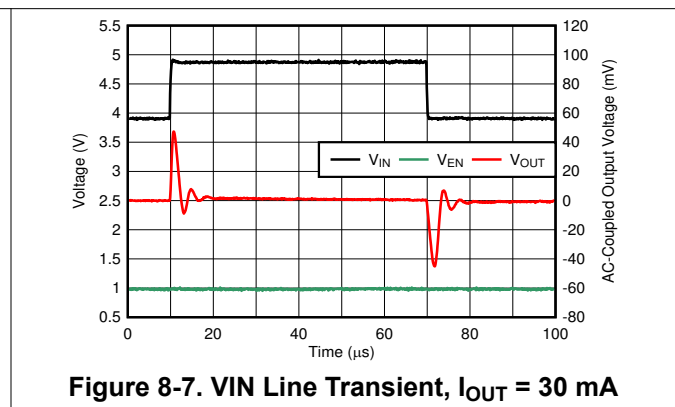
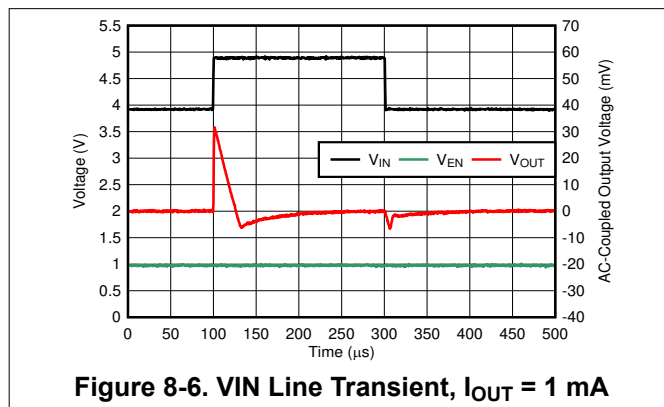
Table 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.9 V
Output voltage	1.8 V
Output load	30 mA
Output Capacitor	1 μ F

8.2.2 Detailed Design Procedure

For this design example, the 1.8-V output voltage device is selected. The device is powered by DC/DC converter connected to a battery. A 2.1-V headroom between V_{IN} and V_{OUT} is used to keep the device within the dropout voltage specification and to ensure the device stays in regulation under all load conditions for this design.

8.2.3 Application Curves



8.3 What to Do and What Not to Do

Place at least one 1- μ F ceramic capacitor as close as possible to the OUT pin of the regulator for best transient performance.

Place at least one 1- μ F capacitor as close as possible to the IN pin for best transient performance.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not continuously operate the device in current limit or near thermal shutdown.

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.4 V to 5.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)} + 2.1$ V. TI requires using a 1 μ F or greater input capacitor to reduce the impedance of the input supply, especially during transients.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Only place tented thermal vias directly beneath the thermal pad of the DQN package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

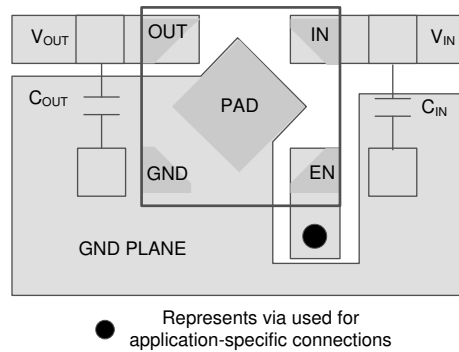


Figure 10-1. Layout Example for the DQN Package

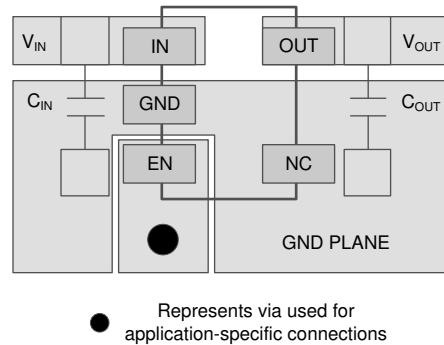


Figure 10-2. Layout Example for the DBV Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Device Nomenclature

Table 11-1. Ordering Information (1) (2)

PRODUCT	V _o
TLV740xx(x)Pyyyz	<p>XX(X) is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 175 = 1.75 V).</p> <p>P is optional; devices with P have an LDO regulator with an active output discharge.</p> <p>YYY is the package designator.</p> <p>Z is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
- (2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Universal Low-Dropout \(LDO\) Linear Voltage Regulator MultiPkgLDOEVM-823 Evaluation Module user's guide](#)
- Texas Instruments, [Using New Thermal Metrics application report](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV74010PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	74010	Samples
TLV74010PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	10	Samples
TLV74012PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	12	Samples
TLV74018PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	74018	Samples
TLV74018PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	18	Samples
TLV74028PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	28	Samples
TLV74033PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	74033	Samples
TLV74033PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	33	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74010PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74010PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74012PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74018PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74028PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74033PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74033PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74010PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74010PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74012PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74018PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74028PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74033PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74033PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQN 4

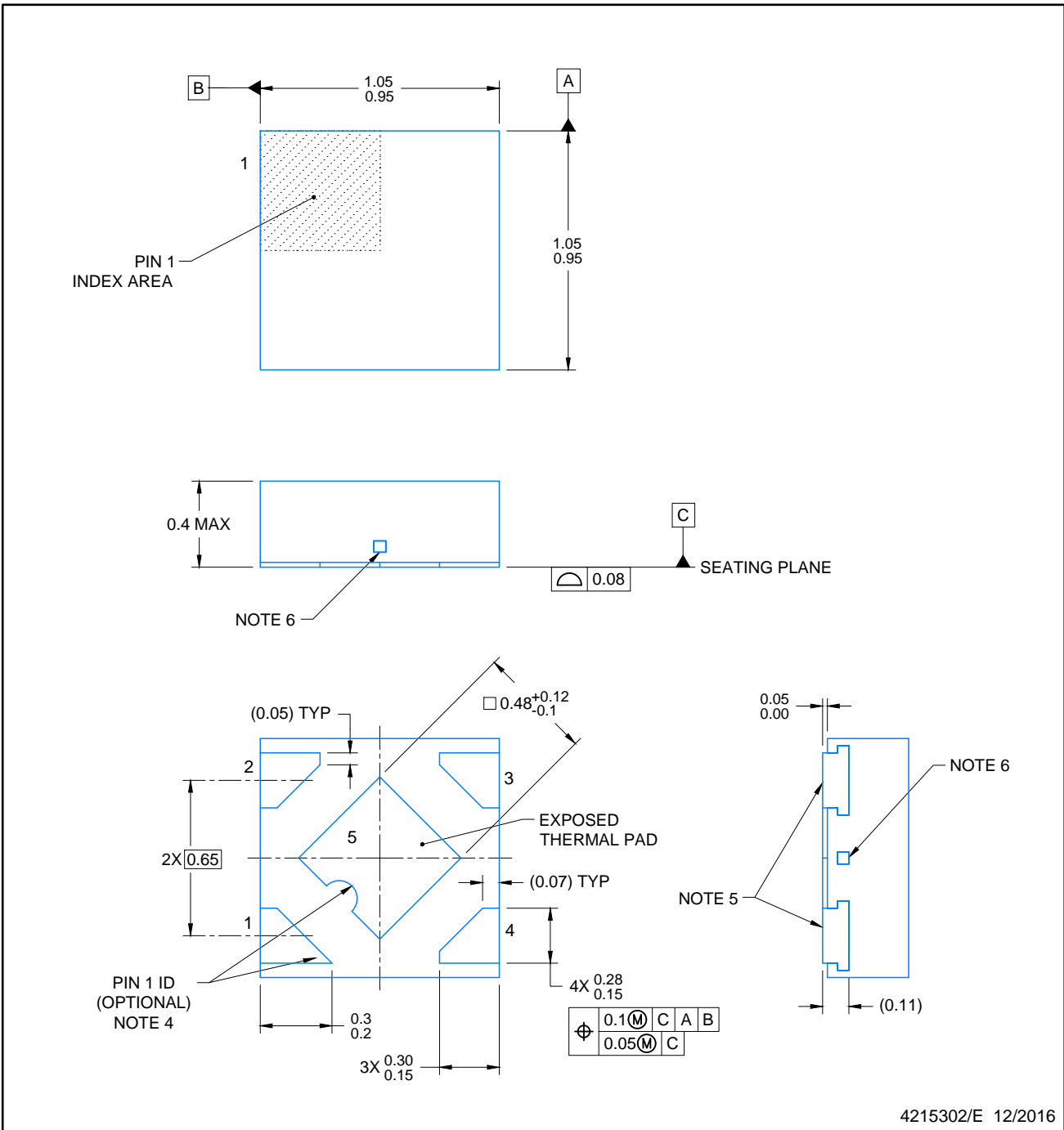
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

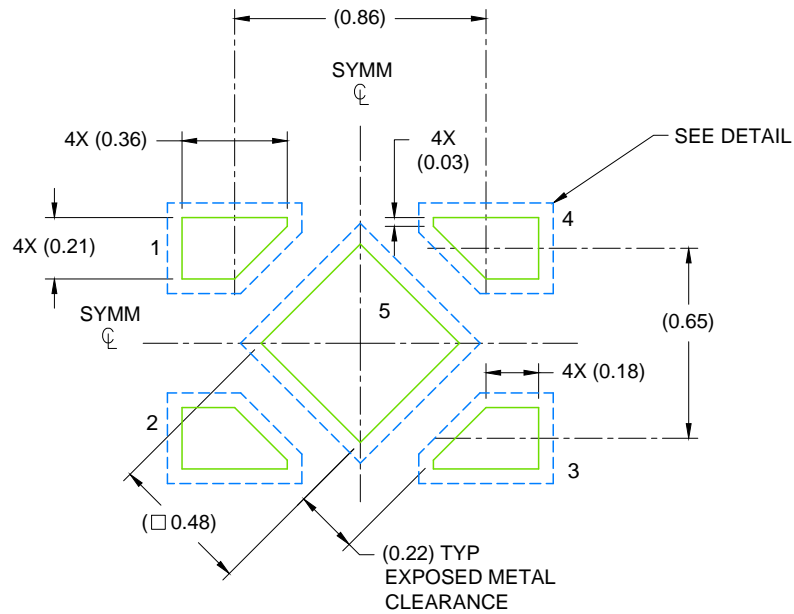
4210367/F



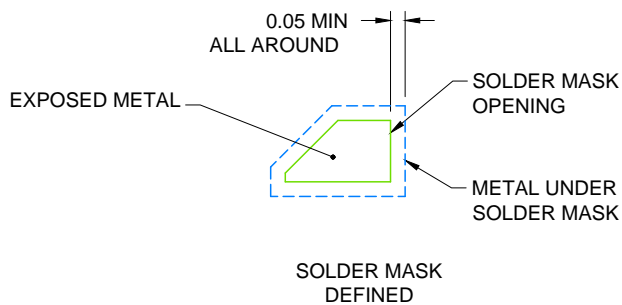
4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X

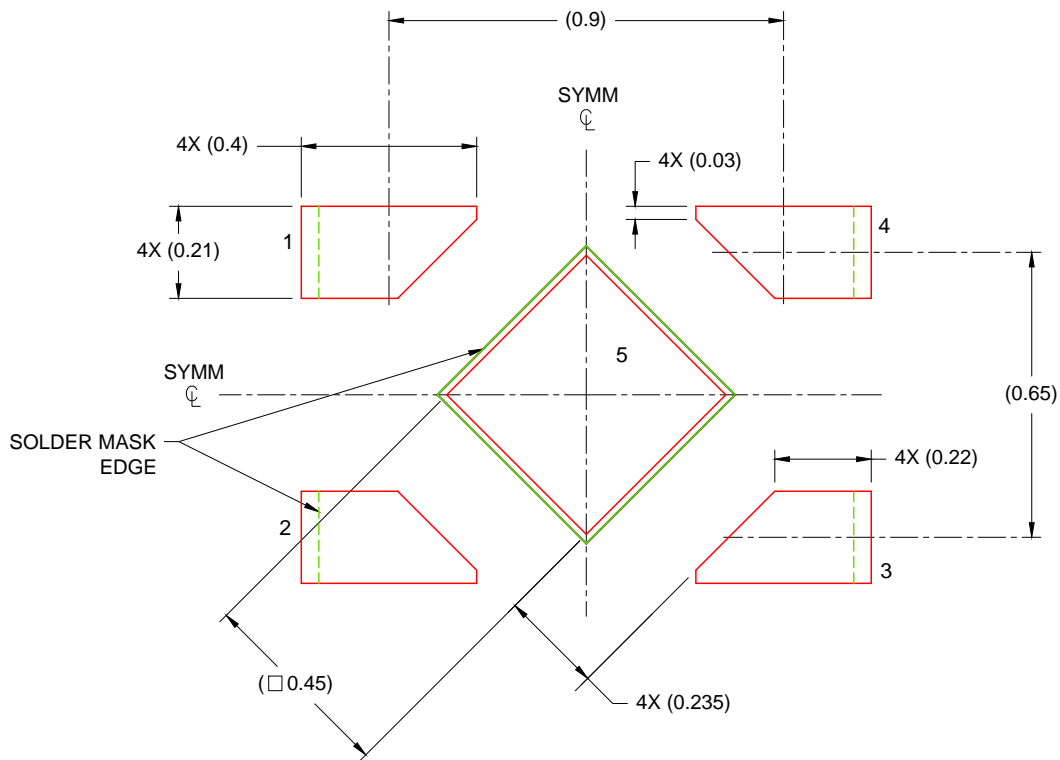


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1mm THICK STENCIL
 EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

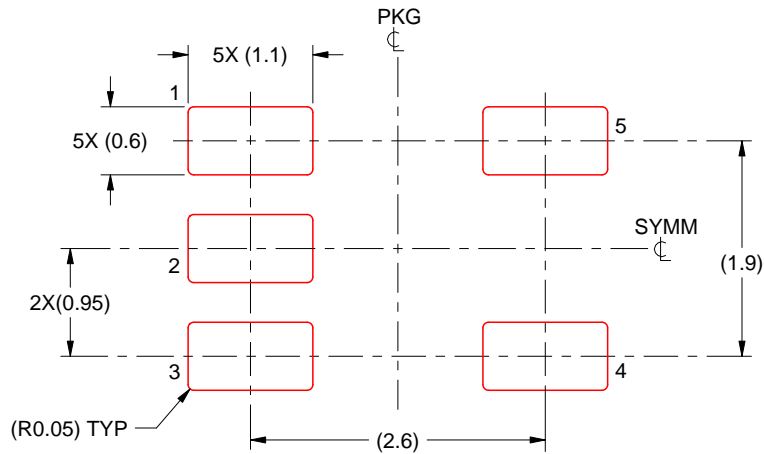
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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