Application Note: SQ52201

36V High-accuracy Current/Power Monitor With Programmable Alert Function

General Description

The SQ52201 is a high accuracy current shunt, bus voltage and power monitor with an I²C or SMBUS-compatible interface.

The shunt voltage drop and the bus supply voltage are both sampled accurately in the device. The sampled data are processed inside the device to generate the power data with programmable calibration, averaging technique and internal multiplier. Programmable alert function provides abundant alert sources settings and makes the application system more reliable.

The SQ52201 senses current on common mode bus voltages that can vary from 0V to 36V, independent of the supply voltage. The device operates from a single 2.7V to 5.5V supply. The SQ52201 is specified over the operating temperature range between –40℃ and +125℃ and features up to 16 programmable addresses on the I²C-compatible interface.

The SQ52201 is available in the MSOP-10 package.

Ordering Information

SQ52201 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SQ52201FBC	MSOP10	--

Features

- Senses Bus Voltages from 0 V to 36 V
- High-Side or Low-Side Sensing
- Bi-directional Current Sensing
- Reports Current, Voltage, and Power
- High Accuracy:
  - 0.02% Gain Error (Typ) for Shunt Voltage
    0.02% Gain Error (Typ) for Bus Voltage
  - 2.5μV Offset (Typ) for Shunt Voltage
  - 1.25mV Offset (Typ) for Bus Voltage
- Configurable Averaging Options
- Configurable Conversion Time
- Abundant Alert Sources Setting
- 16 Programmable Addresses
- High Speed I²C Mode Compatible
- Operates from 2.7V to 5.5V Power Supply

Applications

- Servers
- Telecom Equipment
- Computing
- Power Management
- Battery Chargers
- Power Supplies
- Test Equipment

Typical Application

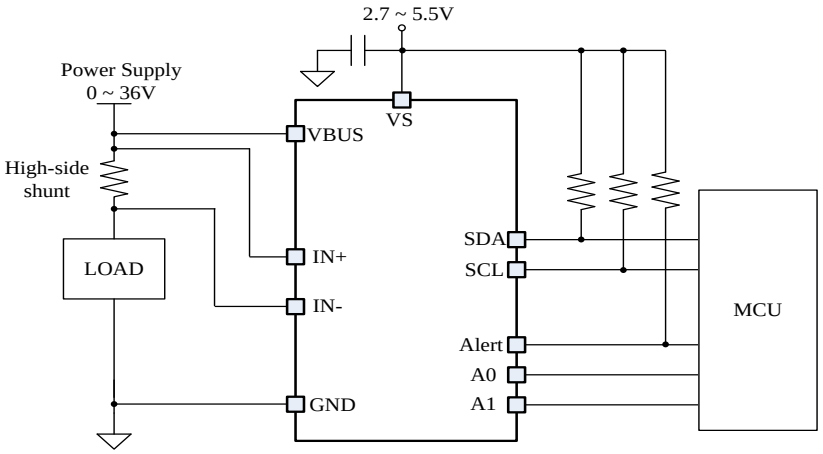
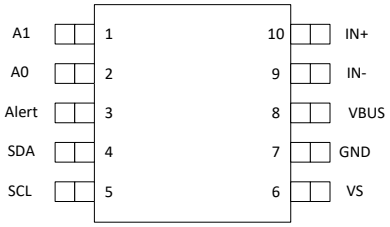


Figure 1. Typical Application

Pin out (Top View)



(MSOP10)

Top Mark: **CXE*xyz*, (**Device code: CXE, ***x=year code, y=week code, z= lot number code***)

Pin No.	Pin Name	Pin Description
1	A1	Address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Address pin. Connect to GND, SCL, SDA, or VS.
3	Alert	Multi-functional alert, open-drain output.
4	SDA	Serial bus data line, open-drain input/output.
5	SCL	Serial bus clock line, open-drain input.
6	VS	Power supply, 2.7 V to 5.5 V.
7	GND	Ground.
8	VBUS	Bus voltage input.
9	IN −	Negative differential voltage input. Connect to load side of shunt resistor.
10	IN+	Positive differential voltage input. Connect to supply side of shunt resistor.

Block Diagram

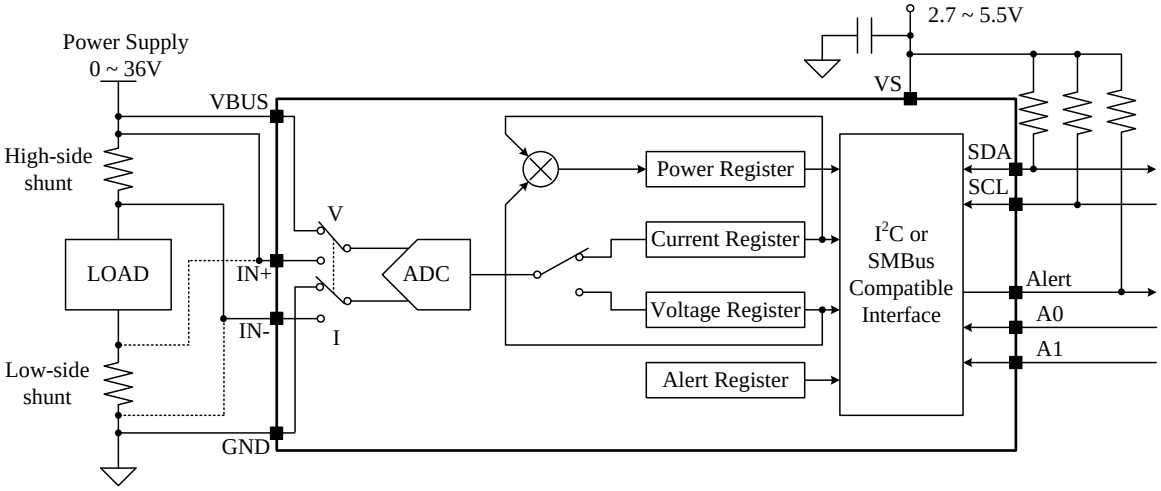


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

VS ---------- -0.3V to 6V
Differential Analog input (V_{IN+} – V_{IN-}) ---------- -40V to +40V
Common Mode Analog input (V_{IN+} + V_{IN-}) / 2 ---------- -0.3V to 40V
VBUS---------- -0.3V to 40V
V_{SDA} ---------- -0.3V to 6V
V_{SCL} ---------- -0.3V to VS+0.3V
Input current into any pin ---------- 5mA
Open-drain digital output current---------- 10mA
Power Dissipation, PD @ T_A = 25℃---------- 0.74W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 136℃/W
θ_{JC} ---------- 25℃/W
Junction Temperature Range---------- 150℃
Storage Temperature Range ---------- -65℃ to 150℃
ESD Susceptibility
HBM (Human Body Mode) ---------- 2kV
CDM ---------- 1kV

Recommended Operating Conditions

VS ---------- 3.3V
Common Mode Analog input (V_{IN+} + V_{IN-}) / 2 ---------- 12V
Operation Temperature Range---------- -40℃ to 125℃

Electrical Characteristics

VS = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV and V_{VBUS} = 12V, T_A = 25℃ unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Shunt Voltage Input Range			-81.92		+81.9175	mV
Bus Voltage Input Range (Note 3)			0		36	V
Common-Mode Rejection	CMRR	0V≤V_{IN+}≤36V	126	140		dB
Shunt Offset Voltage, RTI (Note 4)	V_{OS}			±2.5	±10	μV
Shunt Offset Voltage, RTI vs. Temperature (Note 4)		–40°C≤T_A≤125°C		0.02	0.1	μV/°C
Shunt Offset Voltage, RTI vs. Power Supply (Note 4)	PSRR	2.7V≤VS≤5.5V		2.5		μV/V
Bus Offset Voltage, RTI (Note 4)	V_{OS}			±1.25	±7.5	mV
Bus Offset Voltage, RTI vs. Temperature (Note 4)		–40°C≤T_A≤125°C		10	40	μV/°C
Bus Offset Voltage, RTI vs. Power Supply (Note 4)	PSRR			0.5		mV/V
Input Bias Current (I_{IN+}, I_{IN})	I_B			7		μA
VBUS Input Impedance				830		kΩ
Input Leakage (Note 5)		(IN+ pin) + (IN– pin), Power-down mode		0.1	0.5	μA
DC Accuracy						
ADC Native Resolution				16		Bits
1 LSB Step Size		Shunt voltage		2.5		μV
		Bus voltage		1.25		mV
Shunt Voltage Gain Error				0.02	0.15	%
Shunt Voltage Gain Error vs. Temperature		–40°C≤T_A≤125°C		10	50	ppm/℃
Bus Voltage Gain Error				0.02	0.2	%
Bus Voltage Gain Error vs. Temperature		–40°C≤T_A≤125°C		10	50	ppm/℃
Differential Nonlinearity				±0.1		LSB
ADC Conversion Time	t_{CT}	CT bit = 000		140	165	μs
		CT bit = 001		204	232	
		CT bit = 010		332	366	
		CT bit = 011		588	633	
		CT bit = 100		1.1	1.165	ms
		CT bit = 101		2.116	2.224	
		CT bit = 110		4.156	4.349	
		CT bit = 111		8.244	8.608	
SMBus						
Smbus Timeout (Note 6)				28	35	ms
Digital Input/Output						
Input Capacitance				3		pF
Leakage Input Current		0V≤V_{SCL}≤VS, 0V≤V_{SDA}≤VS, 0V≤V_{Alert}≤VS, 0V≤V_{A0}≤VS, 0V≤V_{A1}≤VS		0.1	1	μA

High Level Input Voltage	V_{IH}		0.7×VS		6	V
Low Level Input Voltage	V_{IL}		-0.5		0.3×VS	V
Low Level Output Voltage, SDA, Alert	V_{OL}	I_{OL}=3mA	0		0.4	V
Hysteresis				400		mV
Power Supply						
Operating Supply Range			2.7		5.5	V
Quiescent Current	I_Q			396	460	μA
		Power down (shutdown) mode		0.5	1	
Power-on Reset Threshold	V_{POR}			2		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: $_{JA}$ is measured on silergy two layers PCB under natural convection. $_{JC}$ top is measured in accordance with JESD51-14

Note 3: While the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V. Do not apply more than 36 V.

Note 4: RTI = Referred-to-input.

Note 5: Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.

Note 6: SMBus timeout in the SQ52201 resets the interface any time SCL is low for more than 28ms.

Detailed Description

Bus Voltage and Current Sample

The SQ52201 provides two direct measurements on the power supply bus of interest: shunt voltage and bus voltage. The shunt voltage, which indicates the current, is measured at the IN+ and IN– pins; the power supply bus voltage is measured by the VBUS pin. The differential shunt voltage is measured with respect to the IN– pin while the bus voltage is measured with respect to ground.

Operation Mode

The device has two operating modes for data conversion: continuous and triggered, that determine how the ADC operates following these conversions.

Continuous Operating Mode:

When the MODE bits of the Configuration Register (00h) are set to '111', SQ52201 is in the continuous operating mode. At first, the number of averages should be set in the Configuration Register. In each sampling sequence, the shunt voltage is sampled and converted first and followed by the bus voltage. After the shunt voltage is sampled, the current value is calculated. This current value is then used to calculate the power result. These values are subsequently stored in an accumulator, and the measurement/calculation sequence repeats until the number of averages set in the Configuration Register is reached. Following every sequence, the present set of values measured and calculated is appended to previously collected values. After all of the averaging has been completed, the final values for shunt voltage, bus voltage, current, and power are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. Reading the data output registers does not affect a conversion in progress.

All the calculations are performed in the background and do not contribute to conversion time.

The mode control in the Conversion Register (00h) also permits selecting modes to convert only the shunt voltage or the bus voltage in order to further allow the user to configure the monitoring function to fit the specific application requirements

Triggered Operating Mode:

When the MODE bits of the Configuration Register (00h) are set to ‘001’, ‘010’, or ‘011’, SQ52201 is in triggered mode. Writing any of the triggered convert modes into the Configuration Register triggers a single-shot conversion. This action produces a single set of measurements; thus, to trigger another single-shot conversion, the Configuration Register must be written to a second time, even if the mode does not change.

Power-Down Mode:

In addition, the SQ52201 also has a power-down mode that reduces the quiescent current and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. Full recovery from power-down mode requires 40μs. The registers of the device can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active modes settings are written into the Configuration Register.

Conversion Ready Flag

Although the SQ52201 can be read at any time, and the data from the last conversion remain available, the Conversion Ready flag bit (Mask/Enable Register, CVRF bit) is provided to help coordinate one-shot or triggered conversions. The Conversion Ready flag (CVRF) bit is set after all conversions, averaging, and multiplication operations are complete.

The Conversion Ready flag (CVRF) bit clears under these conditions:

- Writing to the Configuration Register (00h) , except when configuring the MODE bits for power-down mode.
- Reading the Mask/Enable Register (06h)

Averaging and Conversion Time

The conversion times (t_{CT}) for both the shunt voltage and bus voltage measurements can be configured in the device. The conversion times can be selected from as fast as 140μs to as long as 8.244ms. The device could also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation can allow for the time focused on the bus voltage measurement to be reduced relative to the shunt voltage measurement.

There are trade-offs associated with the settings for conversion time and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the device to reduce any noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the device to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an impact on the measurement accuracy. In order to

achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages based on the timing requirements of the system.

Power Calculation

The Current and Power are calculated following shunt voltage and bus voltage measurements as shown in Figure 3. Current is calculated following a shunt voltage measurement based on the value set in the Calibration Register. If there is no value loaded into the Calibration Register, the current value stored is zero. Power is calculated following the bus voltage measurement based on the previous current calculation and bus voltage measurement. If there is no value loaded in the Calibration Register, the power value stored is also zero. Again, these calculations are performed in the background and do not add to the overall conversion time. These current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register, not the corresponding output registers. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged based on the number of averages set in the Configuration Register (00h).

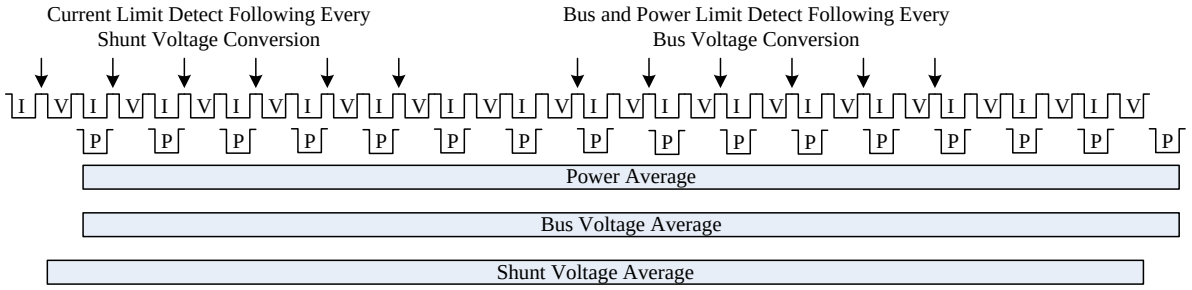


Figure 3. Power Calculation Scheme

In addition, the shunt and bus voltage measurements are also collected. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers, where they can then be read.

Alert Pin

The SQ52201 has a single Alert Limit Register (07h), which allows the Alert pin to be programmed to respond to a single user-defined event or to a Conversion Ready notification if desired. The Mask/Enable Register allows the user to select from one of the five available functions to monitor and/or set the Conversion Ready bit to control the response of the Alert pin. Based on the function being monitored, the user would then enter a value into the Alert Limit Register to set the corresponding threshold value that asserts the Alert pin

The Alert pin allows one of five alert functions that can be monitored:

- Shunt Voltage Over-Limit (SOL)
- Shunt Voltage Under-Limit (SUL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

The Alert pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable Register exceeds the value programmed into the Alert Limit Register. Only one of these alert functions can be enabled and monitored at a time. If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority. For example, if the Shunt Voltage Over-Limit function and the Shunt Voltage Under-Limit function are both enabled, the Alert pin asserts when the Shunt Voltage Register exceeds the value in the Alert Limit Register.

The Conversion Ready state of the device can also be monitored at the Alert pin to inform the user when SQ52201 has completed the previous conversion and is ready to begin a new conversion. Conversion Ready can be monitored at the Alert pin along with one of the alert functions. If an alert function and the Conversion Ready are both enabled to be monitored at the Alert pin, after the Alert pin is asserted, the Mask/Enable Register must be read following the alert to determine the source of the alert. By reading the Conversion Ready Flag (CVRF, bit 3), and the Alert Function Flag (AFF, bit 4) in the Mask/Enable Register, the source of the alert can be determined. If the Conversion Ready feature is not desired and the CNVR bit is not set, the Alert pin only responds to an exceeded alert limit based on the alert function enabled.

Figure 3 shows when the value in the Alert Limit Register is compared to the corresponding converted value.

The Shunt Voltage alert functions compare the measured shunt voltage to the Alert Limit Register following every shunt voltage conversion and assert the AFF bit and Alert pin if the limit threshold is exceeded.

The Bus Voltage alert functions compare the measured bus voltage to the Alert Limit Register following every bus voltage conversion and assert the AFF bit and Alert pin if the limit threshold is exceeded.

The Power Over-Limit alert function is also compared to the calculated power value following every bus voltage measurement conversion and asserts the AFF bit and Alert pin if the limit threshold is exceeded.

For example, if the alert function that is enabled is Shunt Voltage Over-Limit (SOL), following every shunt voltage conversion the value in the Alert Limit Register is compared to the measured shunt voltage to determine if the measurement has exceeded the programmed limit. The AFF, bit 4 of the Mask/Enable Register, asserts high any time the measured voltage exceeds the value programmed into the Alert Limit Register. In addition to the AFF being asserted, the Alert pin is asserted based on the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register). If the Alert Latch is enabled, the AFF and Alert pin remain asserted until either the Configuration Register (00h) is written to or the Mask/Enable Register is read.

If the alert function is not used, the Alert pin can be left floating without impacting the operation of the device.

Configuration for the Readouts

In order to report the current and power values properly, several registers should be configured as the steps followed.

Step1: select the resolution of the Current Register (04h): Current_LSB.

The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current I_{MAX} as shown in Equation (1). While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively.

$$Current\_LSB = \frac{I_{MAX}}{2^{15}} \quad (1)$$

Where Current_LSB is the resolution of the Current Register (04h); I_{MAX} is the maximum expected current.

In addition, the value of the shunt resistor is selected based on the shunt voltage measurement range and I_{MAX}.

Step2: configure the Calibration Register (05h)

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) to the most useful value for a given application. With correct configuration of the Calibration Register (05h), the real current can read out by simply multiply the Current Register and Current_LSB. The value of the Calibration Register (05h) is named as CAL[R], which should be configured as the Equation (2) below:

$$CAL[R] = \frac{2048 \times Shunt\_LSB}{Current\_LSB \times R_{Shunt}} \quad (2)$$

Where CAL[R] is the value of the Calibration Register (05h); Shunt_LSB is the resolution of the Shunt Voltage Register (01h), Shunt_LSB is 2.5uV/LSB; Current_LSB is the resolution of the Current Register (04h); R_{Shunt} is the shunt resistor.

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) update accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration Register is programmed, the Current Register (04h) and Power Register (03h) remain at zero.

Step3: readouts of the current

With the sample operation of the device, the value of the Shunt Register is shown as the equation (3)

$$Shunt[R] = \frac{Current \times R_{Shunt}}{Shunt\_LSB} \quad (3)$$

In the device, the Current Register value is calculated based on the value of the Shunt Voltage Register (01h) and the Calibration Register(05h).

$$Current[R] = \frac{Shunt[R] \times CAL[R]}{2048} \quad (4)$$

Where Current[R] is the value of the Current Register (04h); Shunt[R] is the value of the Shunt Register (01h); CAL[R] is the value of the Calibration Register (05h)

Then the user can read out the real current by the equation (5)

$$Current = Current[R] \times Current\_LSB \quad (5)$$

Step5: readout of the bus voltage

The bus voltage is read by the equation (6)

$$Bus = Bus[R] \times Bus\_LSB \quad (6)$$

Where Bus_LSB is the resolution of the Bus Voltage Register(02h), which is a fixed 1.25mV/LSB.

Step6: readout of the power

The value of the Power Register (03h) is calculated based on the equation (7)

$$Power[R] = \frac{Current[R] \times Bus[R]}{20000} \quad (7)$$

Where Current[R] is the value of the Current Register (04h); Bus[R] is the value of the Bus Voltage Register (02h); Power[R] is the value of the Power Register(03h).

As the calculation equation (1)~(7), the resolution of the Power Register is fixed as 25 times of the resolution of the Current Register. The real power is read as the equation (8)

$$Power = Power[R] \times Power\_LSB \quad (8)$$

Configuration Example

The following figure shows a nominal 10A load that creates a differential voltage of 20mV across 2mΩ shunt resistor. The bus voltage for The SQ52201 is measured at the external VBUS input pin, which in this example is connected to the IN– pin to measure the voltage level delivered to the load. For this example, the VBUS pin measures less than 12 V because the voltage at the IN– pin is 11.98 V as a result of the voltage drop across the shunt resistor.

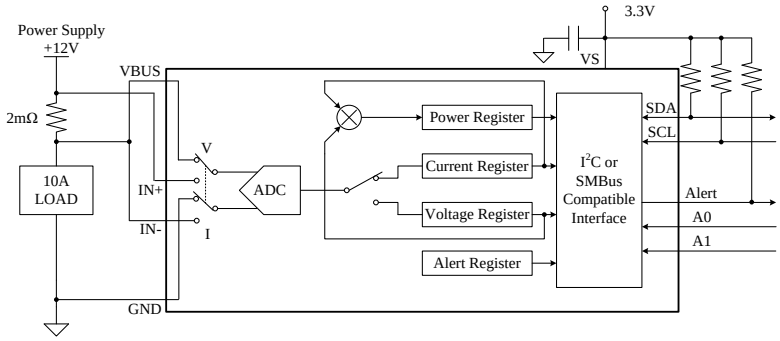


Figure 4. High-Side Sensing Circuit Application Example

For this example, assuming a maximum expected current of 15 A, the Current_LSB is calculated to be 457.7μA/bit using Equation (1). Using a value for the Current_LSB of 500μA/Bit or 1mA/Bit would significantly simplify the conversion from the Current Register (04h) and Power Register (03h) to amperes and watts. For this example, a value of 1mA/bit was chosen for the Current_LSB. Using this value for the Current_LSB does trade a small amount of resolution for having a simpler conversion process on the user side. Using Equation (2) in this example with a Current_LSB value of 1mA/bit and a shunt resistor of 2mΩ results in a Calibration Register value of 2560 or A00h.

The Current Register (04h) is then calculated by multiplying the decimal value of the Shunt Voltage Register (01h) contents by the decimal value of the Calibration Register and then dividing by 2048, as shown in Equation (4). For this example, the Shunt Voltage Register contains a value of 8,000 (representing 20mV), which is multiplied by the Calibration Register value of 2560 and then divided by 2048 to yield a decimal value for the Current Register (04h) of 10000, or 2710h. Multiplying this value by 1mA/bit results in the original 10A level stated in the example.

The LSB for the Bus Voltage Register (02h) is a fixed 1.25mV/bit, which means that the 11.98V present at the VBUS pin results in a register value of 2570h, or a decimal equivalent of 9584. Note that the MSB of the Bus Voltage Register (02h) is always zero because the VBUS pin is only able to measure positive voltages.

The Power Register (03h) is then be calculated by multiplying the decimal value of the Current Register, 10000, by the decimal value of the Bus Voltage Register (02h), 9584, and then dividing by 20,000, as defined in Equation (7). For this example, the result for the Power Register (03h) is 12B8h, or a decimal equivalent of 4792. Multiplying this result by the power LSB (25 times Current_LSB]) results in a power calculation of (4792 × 25mW/bit), or 119.82 W. The power LSB has a fixed ratio to the Current_LSB of 25. For this example, 1mA/bit Current_LSB results in a power LSB of 25mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 11.98 V multiplied by the load current of 10 A to give a result of 119.8 W.

The following table lists the results of configuring, measuring, and calculating the values for current and power for The SQ52201. when Load = 10 A, V_{CM}=12V, R_{SHUNT}=2mΩ, and V_{VBUS}=12V.

Table 1. Calculating Current and Power

REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Configuration Register	00h	4127h			
Shunt Register	01h	1F40h	8000	2.5μV	20mV
Bus Voltage Register	02h	2570h	9584	1.25mV	11.98V
Calibration Register	05h	0A00h	2560		
Current Register	04h	2710h	10000	1mA	10A
Power Register	03h	12B8h	4792	25mW	119.82W

Simple Monitor Usage

The device can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default power-on reset configuration and continuous conversion of shunt and bus voltages.

Without programming the device Calibration Register, the device is unable to provide either a valid current or power value, because these outputs are both derived using the values loaded into the Calibration Register.

Basic I²C/SMBus Overview

The SQ52201 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another.

The I²C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is discussed. Two lines, SCL and SDA, connect the device to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. Register bytes are sent most significant byte first, followed by the least significant byte. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

After all data have been transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The device includes a 28 ms timeout on its interface to prevent locking up the bus.

The SQ52201 supports the transmission protocol for fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 3.4MHz). All data bytes are transmitted most significant byte first.

Serial Bus Address

To communicate with SQ52201, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. The following table lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin states before any activity on the interface occurs.

Table 2. Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011

VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Writing Command

Accessing a specific register on SQ52201 is accomplished by writing the appropriate value to the register pointer. The value for the register pointer is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/W bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register which data is written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

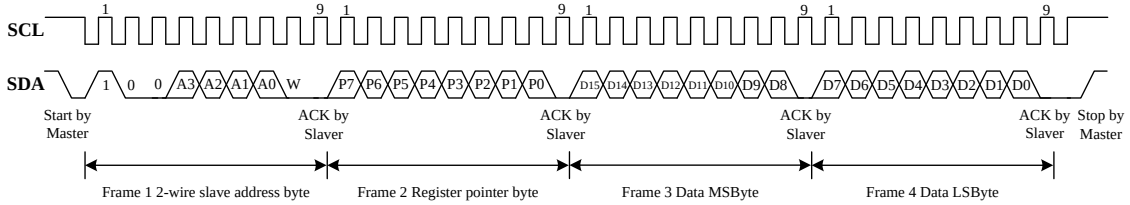


Figure 5. Timing Diagram for Write Word Format

Read Command

When reading from SQ52201, a new value must be written to the register pointer, as shown in Figure 6. This write is accomplished by issuing the slaver address byte with the R/W bit low, followed by the register pointer byte. No additional data are required.

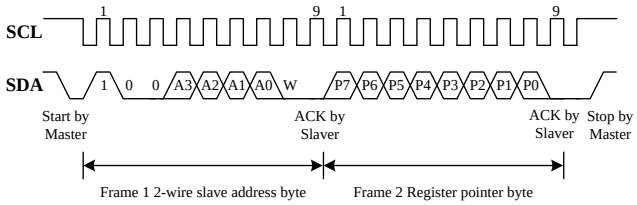


Figure 6. Typical Register Pointer Set

The master then generates a start condition and sends the slave address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a Not-Acknowledge after receiving any data byte, or generating a start or stop condition.

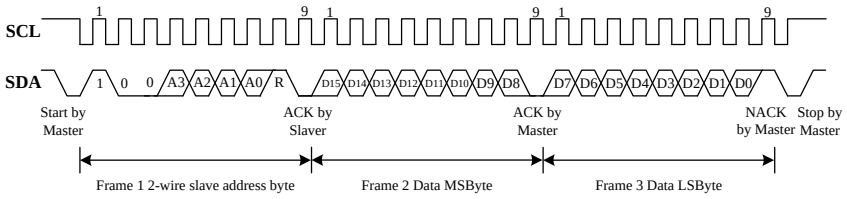


Figure 7. Timing Diagram for Read Word Format

High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up resistors. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code 00001XXX. This transmission is made in fast (400kHz) or standard (100kHz) (F/S) mode at no more than 400kHz. The device does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

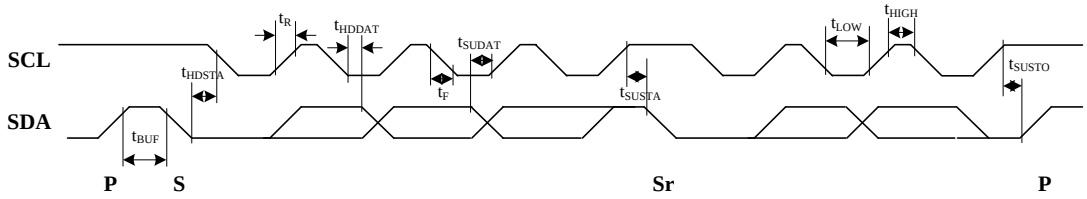


Figure 8. Bus Timing Diagram

Table 3. Bus Timing Diagram Definitions

PARAMETERS	SYMBOL	FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL operating frequency	f_{SCL}	0.001	0.4	0.001	3.4	MHz
Bus free time between stop and start conditions	t_{BUF}	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	t_{HDSTA}	100		100		ns
Repeated start condition setup time	t_{SUSTA}	100		100		ns
STOP condition setup time	t_{SUSTO}	100		100		ns
Data hold time	t_{HDDAT}	10	900	10	100	ns
Data setup time	t_{SUDAT}	100		20		ns
SCL clock low period	t_{LOW}	1300		200		ns
SCL clock high period	t_{HIGH}	600		60		ns
Data fall time	t_F		300		80	ns
Clock fall time	t_F		300		40	ns
Clock rise time	t_R		300		40	ns
Clock/data rise time for SCLK≤100kHz	t_R		1000			ns

SMBus Alert Response

The SQ52201 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple slave devices. When an Alert occurs, the master can broadcast the Alert Response slave address (0001 100) with the Read/Write bit set high. Following this Alert Response, any slave device that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus.

The Alert Response can activate several different slave devices simultaneously, similar to the I²C General Call. If more than one slave attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until the interrupt is cleared.

The following figure shows the timing diagram for the SMBus Alert response operation.

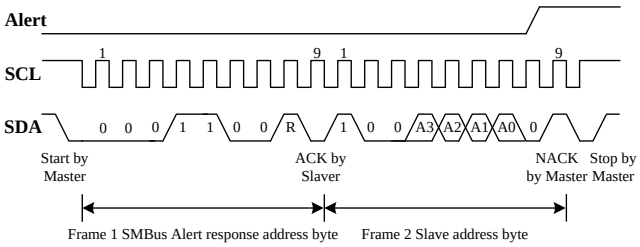


Figure 9. Timing Diagram for SMBus ALERT

Register Maps

SQ52201 uses a bank of registers for holding configuration settings, measurement results, minimum/maximum limits, and status information. The following table summarizes the device registers. All 16-bit device registers are two 8-bit bytes via the I^2C interface.

Table 4. Register Set Summary

REGISTER ADDRESS (HEX)	REGISTER NAME	FUNCTION	POWER-ON RESET (HEX)	TYPE
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	4127h	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	0000h	R
02h	Bus Voltage Register	Bus voltage measurement data.	0000h	R
03h	Power Register	Contains the value of the calculated power being delivered to the load.	0000h	R
04h	Current Register	Contains the value of the calculated current flowing through the shunt resistor.	0000h	R
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	0000h	R/W
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	0000h	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	0000h	R/W
FEh	Manufacturer ID Register	Contains unique manufacturer identification number.	190Fh	R
FFh	Die ID Register	Contains unique die identification number.	0000h	R

Configuration Register (00h) (Read/Write)

The Configuration Register settings control the operating modes for the device. This register controls the conversion time settings for the shunt and bus voltage measurements as well as the averaging mode used. The operating mode that controls what signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration Register halts any conversion in progress until the write sequence is completed resulting in a new conversion starting based on the new contents of the Configuration Register (00h). This halt prevents any uncertainty in the conditions used for the next completed conversion.

Table 5. Configuration Register (00h) (Read/Write) Descriptions

<table>
<tr><th>BIT NO.</th><th>BIT NAME</th><th>POR VALUE</th><th>DESCRIPTION</th></tr>
<tr><td>D15</td><td>RST</td><td>0</td><td>Reset Bit
Setting this bit to '1' generates a system reset that is the same as power-on reset. Reset all registers to default values; this bit self-clears.</td></tr>
<tr><td>D14</td><td></td><td>1</td><td></td></tr>
<tr><td>D13</td><td></td><td>0</td><td></td></tr>
<tr><td>D12</td><td></td><td>0</td><td></td></tr>
<tr><td>D11</td><td>AVG2</td><td>0</td><td rowspan="3">Averaging Mode
Determines the number of samples that are collected and averaged. The following table shows all the AVG bit settings and related number of averages for each bit setting.
<table><tr><th>AVG[2:0]</th><th>NUMBER OF AVERAGES</th></tr><tr><td>000</td><td>1</td></tr><tr><td>001</td><td>4</td></tr><tr><td>010</td><td>16</td></tr><tr><td>011</td><td>64</td></tr><tr><td>100</td><td>128</td></tr><tr><td>101</td><td>256</td></tr><tr><td>110</td><td>512</td></tr><tr><td>111</td><td>1024</td></tr></table></td></tr>
<tr><td>D10</td><td>AVG1</td><td>0</td></tr>
<tr><td>D9</td><td>AVG0</td><td>0</td></tr>
<tr><td>D8</td><td>VBUSCT2</td><td>1</td><td rowspan="2">Bus Voltage Conversion Time
Sets the conversion time for the bus voltage measurement. The following table shows the VBUSCT bit options and related conversion times for each bit setting.
<table><tr><th>VBUSCT[2:0]</th><th>CONVERSION TIME</th></tr><tr><td>000</td><td>140us</td></tr><tr><td>001</td><td>204us</td></tr><tr><td>010</td><td>332us</td></tr></table></td></tr>
<tr><td>D7</td><td>VBUSCT1</td><td>0</td></tr>
</table>

D6	VBUSCT0	0	011: 588us 100: 1.1ms 101: 2.116ms 110: 4.156ms 111: 8.244ms
D5	VSHCT2	1	**Shunt Voltage Conversion Time** Sets the conversion time for the shunt voltage measurement. The following table shows the VSHCT bit options and related conversion times for each bit setting. 000: 140us 001: 204us 010: 332us 011: 588us 100: 1.1ms 101: 2.116ms 110: 4.156ms 111: 8.244ms
D4	VSHCT1	0	
D3	VSHCT0	0	
D2	MODE2	1	**Operating Mode** Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown as below. 000: Power-Down (or Shutdown) 001: Shunt Voltage, Triggered 010: Bus Voltage, Triggered 011: Shunt and Bus, Triggered 100: Power-Down (or Shutdown) 101: Shunt Voltage, Continuous 110: Bus Voltage, Continuous 111: Shunt and Bus, Continuous
D1	MODE1	1	
D0	MODE0	1	

Shunt Voltage Register (01h) (Read-Only)

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT}. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

If averaging is enabled, this register displays the averaged value.

Full-scale range = 81.9175mV (decimal = 7FFF); LSB= 2.5μV.

Table 6. Shunt Voltage Register (01h) (Read-Only) Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Register (02h) (Read-Only)

The Bus Voltage Register stores the most recent bus voltage reading, VBUS. If averaging is enabled, this register displays the averaged value.

Full-scale range = 40.96V (decimal = 7FFF); LSB = 1.25mV.

Table 7. Bus Voltage Register (02h) (Read-Only) Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Power Register (03h) (Read-Only)

If averaging is enabled, this register displays the averaged value.

The Power Register LSB is internally programmed to equal 25 times the programmed value of the Current_LSB.

The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register according to Equation 4.

Table 8. Power Register (03h) (Read-Only) Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current Register (04h) (Read-Only)

If averaging is enabled, this register displays the averaged value.

The value of the Current Register is calculated by multiplying the decimal value in the Shunt Voltage Register with the decimal value of the Calibration Register, according to Equation 3.

Table 9. Current Register (04h) (Read-Only) Register Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD 14	CD 13	CD 12	CD 11	CD 10	CD 9	CD 8	CD 7	CD 6	CD 5	CD 4	CD 3	CD 2	CD 1	CD 0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Calibration Register (05h) (Read/Write)

This register provides the device with the value of the shunt resistor that was present to create the measured differential voltage. It also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB. This register is also suitable for use in overall system calibration.

Table 10. Calibration Register (05h) (Read/Write) Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask/Enable Register (06h) (Read/Write)

The Mask/Enable Register selects the function that is enabled to control the Alert pin as well as how that pin functions. If multiple functions are enabled, the highest significant bit position Alert Function (D15-D11) takes priority and responds to the Alert Limit Register.

Table 11. Mask/Enable Register (06h) (Read/Write)

BIT NO.	BIT NAME	POR VALUE	DESCRIPTION
D15	SOL	0	**Shunt Voltage Over-Voltage** Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
D14	SUL	0	**Shunt Voltage Under-Voltage** Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
D13	BOL	0	**Bus Voltage Over-Voltage** Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
D12	BUL	0	**Bus Voltage Under-Voltage** Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
D11	POL	0	**Power Over-Limit** Setting this bit high configures the Alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register.
D10	CNVR	0	**Conversion Ready** Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.
D9	-	0	
D8	-	0	

D7	-	0	
D6	-	0	
D5	-	0	
D4	AFF	0	**Alert Function Flag** While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.
D3	CVRF	0	**Conversion Ready Flag** Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Mask/Enable Register
D2	OVF	0	**Math Overflow Flag** This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid.
D1	APOL	0	**Alert Polarity bit; sets the Alert pin polarity.** 1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default)
D0	LEN	0	**Alert Latch Enable** Configures the latching feature of the Alert pin and Alert Flag bits. 1 = Latch enabled 0 = Transparent (default) When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remains active following a fault until the Mask/Enable Register has been read.

Alert Limit Register (07h) (Read/Write)

The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded.

Table 12. Alert Limit Register (07h) (Read/Write) Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL 15	AUL 14	AUL 13	AUL 12	AUL 11	AUL 10	AUL 9	AUL 8	AUL 7	AUL 6	AUL 5	AUL 4	AUL 3	AUL 2	AUL 1	AUL 0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Manufacturer ID Register (FEh) (Read-Only)

The Manufacturer ID Register stores a unique identification number for the manufacturer.

Table 13. Manufacturer ID Register (FEh) (Read-Only) Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
POR VALUE	0	0	0	1	1	0	0	1	0	0	0	0	1	1	1	1

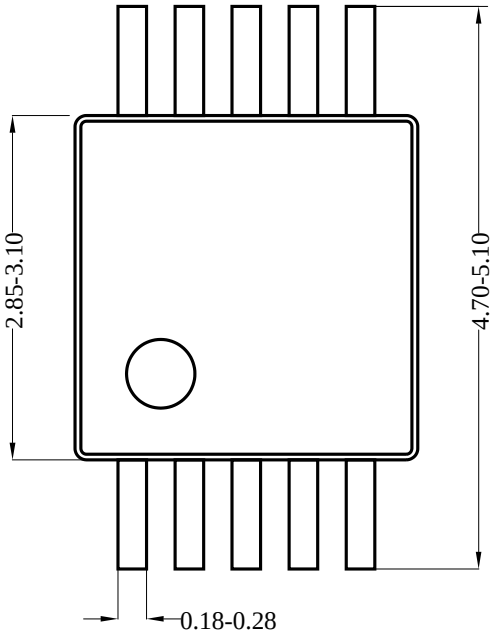
Die ID Register (FFh) (Read-Only)

The Die ID Register stores a unique identification number and the revision ID for the die.

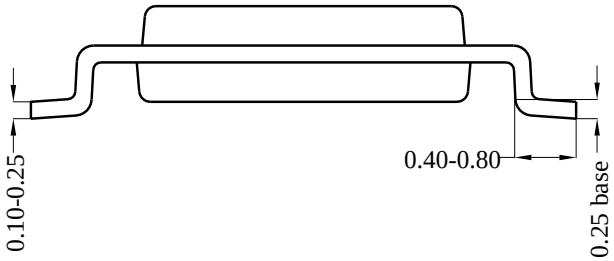
Table 14. Die ID Register (FFh) (Read-Only) Description

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DID 11	DID 10	DID 9	DID 8	DID 7	DID 6	DID 5	DID 4	DID 3	DID 2	DID 1	DID 0	RID 3	RID 2	RID 1	RID 0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

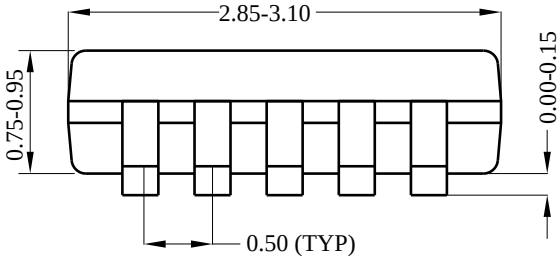
MSO10 Package outline & PCB layout



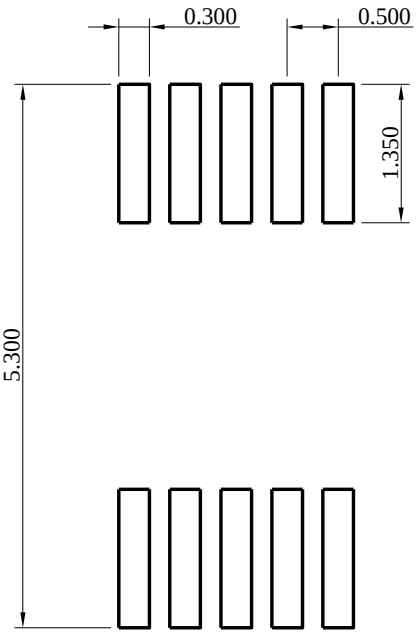
Top view



Side view



Front view



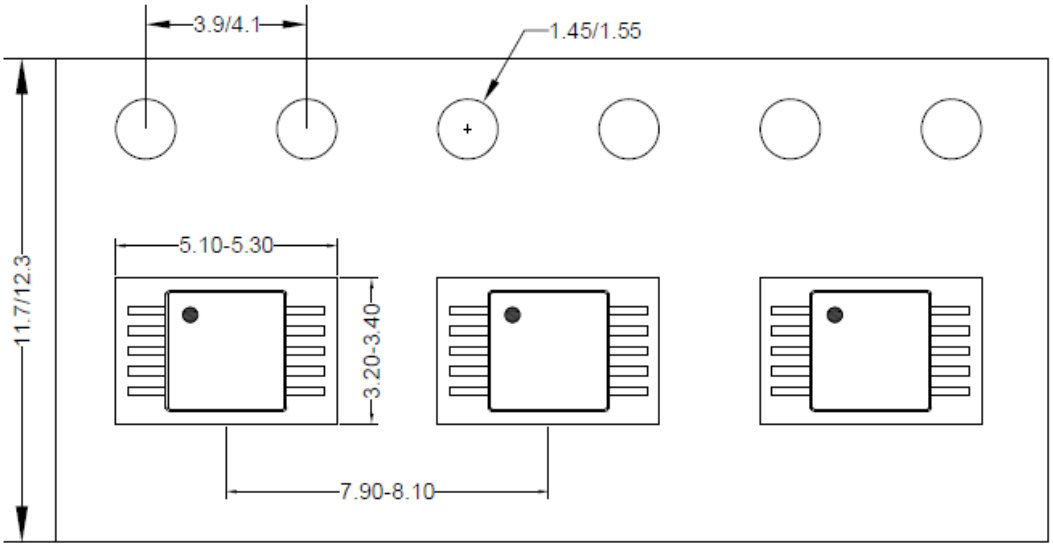
Recommended Pad Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

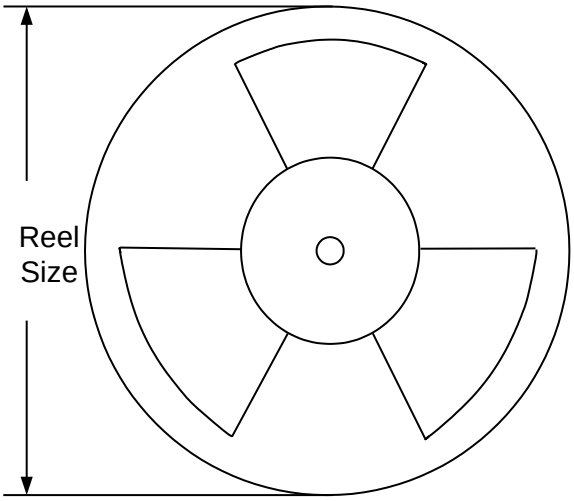
1. Taping Orientation

MSOP10



Feeding direction ⟶

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

3. Others: NA

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