

Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

FEATURES

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- Ultra low noise figure(NF)=0.55dB;
- High power gain=18dB;
- High linearity IIP3oob=0dBm;
- High input 1dB-compression point=-9.5dBm;
- GPS L1 requires only one input matching inductor;
- RF output internally matched to 50 ohm for GPS L1;
- Supply voltage: 1.5V to 3.3V;
- Operating frequencies: 1550~1615MHz; 1164~1215MHz;
- FCDFN-6L package:1.1mmX0.7mmX0.37mm
- 2000V HBM ESD protection (including RFIN and RFOUT pin)

APPLICATIONS

- Smart Phones, Feature Phones;
- Tablet PCs;
- Personal Navigation Devices;
- Digital Still Cameras, Digital Video Cameras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

GENERAL DESCRIPTION

- The AW15045FDR is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, Beidou, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW15045FDR can be close to the antenna, requires only one external input matching inductor, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.
- The AW15045FDR with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.3V. All these features make AW15045FDR an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provide better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.
- The AW15045FDR is available in a small lead-free, RoHS-Compliant, 1.1mm x 0.7mm x 0.37mm 6-pin FCDFN package.

TYPICAL APPLICATION CIRCUIT

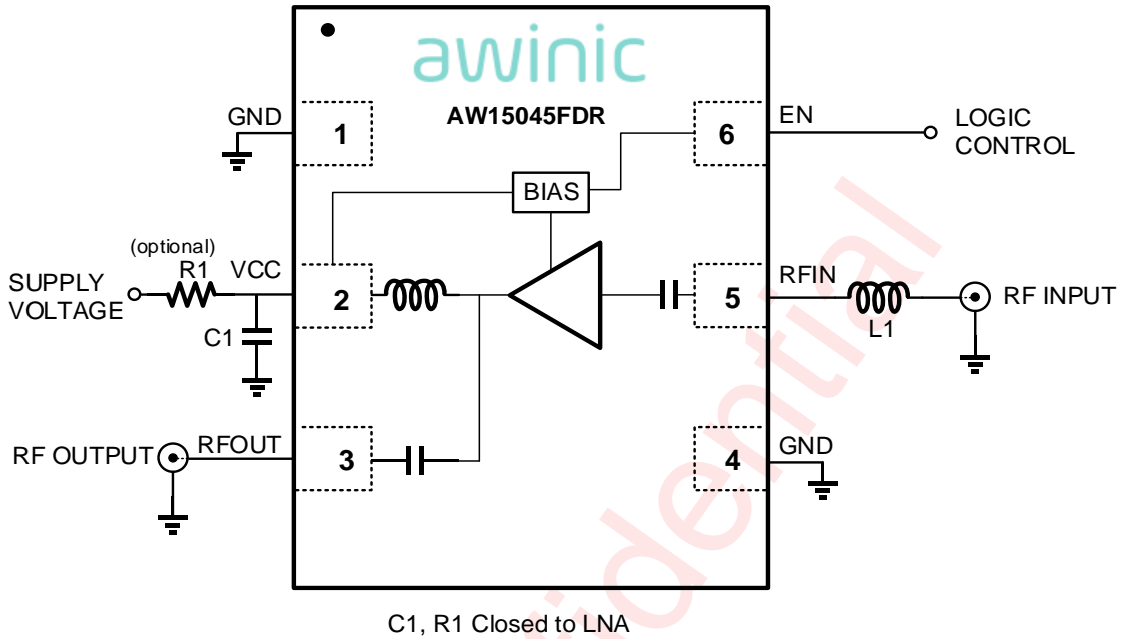


Figure 1(a) Typical Application Circuit of AW15045FDR for GPS L1

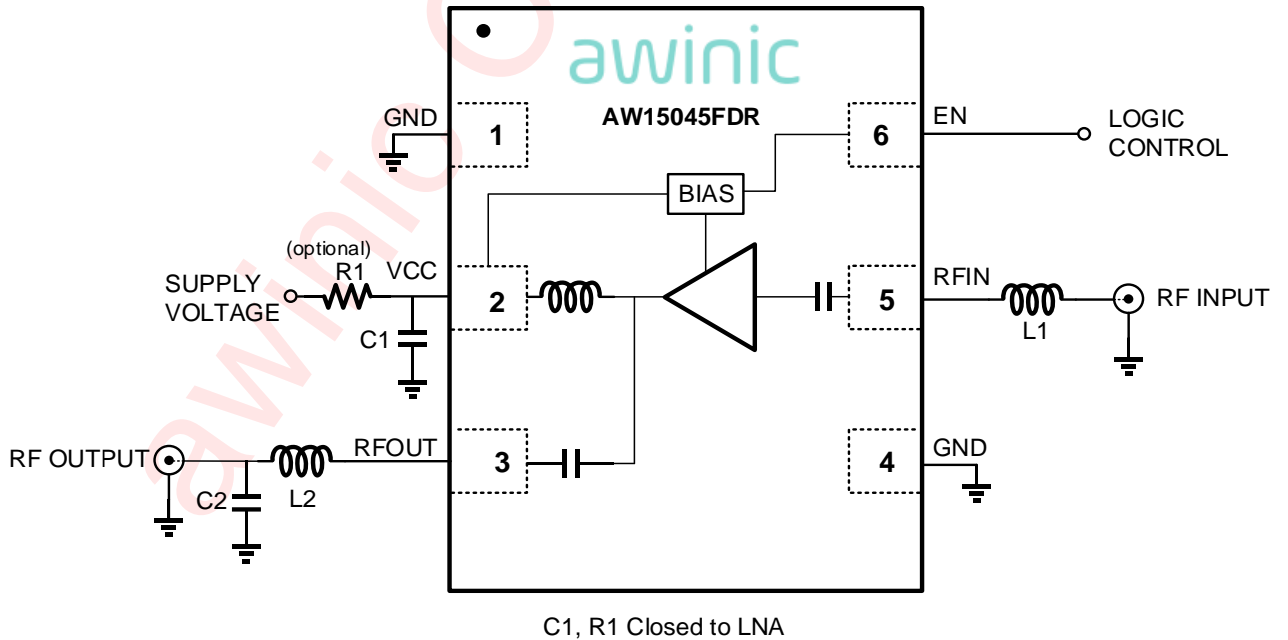


Figure 1(b) Typical Application Circuit of AW15045FDR for GPS L5

RECOMMENDED COMPONENTS LIST

Table1 and table2 list the recommended components types and values.

Table1: list of inductor for GPS L1

Component	Part Number	Inductance (nH)	Q(min)	Q Test Frequency (MHz)	Supplier	Size
L1	LQW15A	10	25	250	Murata	0402
L1	SDWL1005C	10	24	250	Sunlord	0402
Component	Part Number	Capacitance (pF)	Rated Voltage (V)		Supplier	Size
C1	GRM155	1000	50		Murata	0402

Table2: list of inductor for GPS L5

Component	Part Number	Inductance (nH)	Q(min)	Q Test Frequency (MHz)	Supplier	Size
L1	LQW15A	20	25	250	Murata	0402
L2	LQW15A	12	25	250	Murata	0402
Component	Part Number	Capacitance (pF)	Rated Voltage (V)		Supplier	Size
C1	GRM155	1000	50		Murata	0402
C2	GRM155	5.6	50		Murata	0402

PIN CONFIGURATION AND TOP MARK

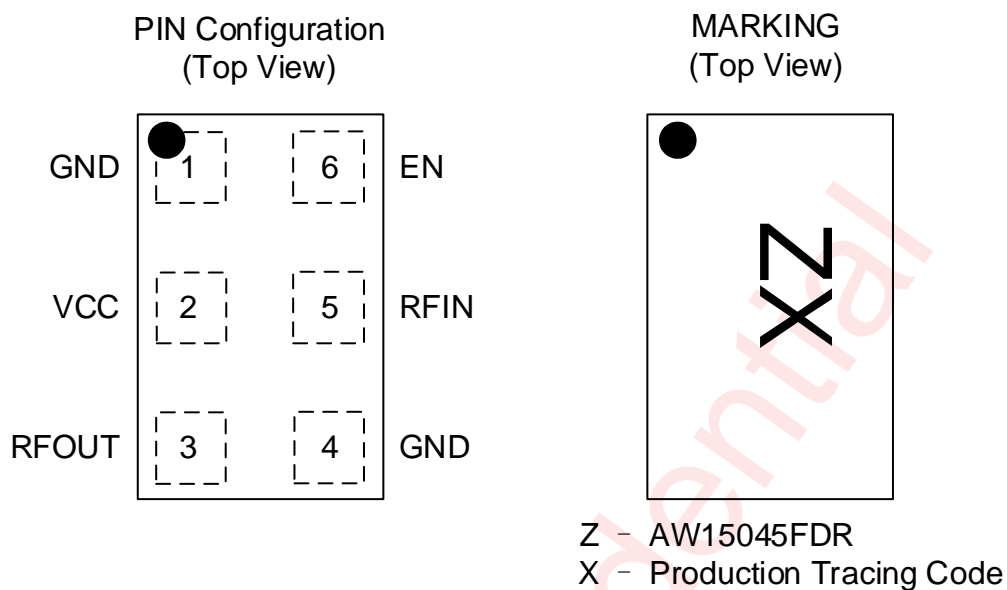


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	DC Supply
3	RFOUT	LNA output
4	GND	Ground
5	RFIN	LNA input
6	EN	Logic control

FUNCTIONAL BLOCK DIAGRAM

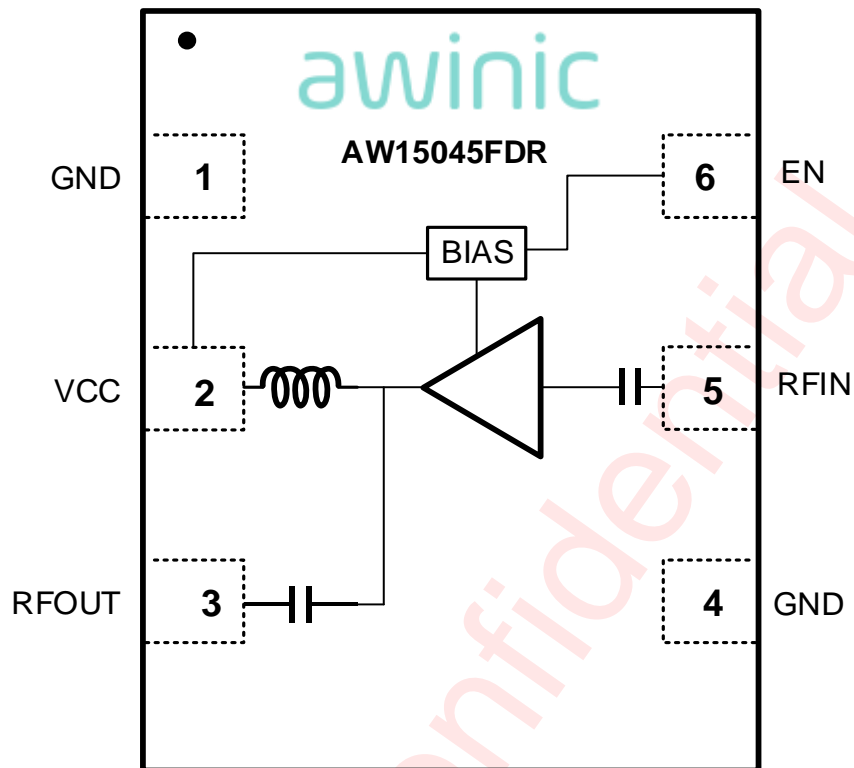


Figure 3 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15045FDR	-40°C ~ 85°C	FCDFN 1.1mmx0.7mm-6L	Z	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS^[1]

PARAMETERS	Symbol	Values			
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	V _{CC}	-0.3	-	3.6	V
Voltage at pin EN ^[2]	V _{EN}	-0.3	-	3.6	V
Current into pin VCC	I _{CC}	-	-	30	mA
RF input power ^[3]	P _{IN}	-	-	15	dBm
Package thermal resistance	θ _{JA}	-	148	-	°C/W
Junction temperature	T _J	-	-	150	°C
Storage temperature range	T _{STG}	-65	-	150	°C
Ambient temperature range	T _{amb}	-40	-	85	°C
Solder temperature(10s)		-	260	-	°C
ESD range					
HBM ^[4]			±2000		V
CDM ^[4]			±1000		V
Latch-up					
Standard: JEDEC EIA/JESD78E			+IT: +400 -IT: -400		mA mA

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note2: Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 5.0V in order to avoid excess current.

Note3: The RF input and RF output are AC coupled through internal DC blocking capacitor.

Note4: HBM standard: MIL-STD-883H Method 3015.9. CDM standard: JEDEC EIA/JESD22-C101F.

ELECTRICAL CHARACTERISTICS

(AW15045FDR EVB; Typical values are at VCC=2.8V and TA=+25°C, f=1550-1615MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.3	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		6.0	8.0	mA
V _{EN}	Digital Input-Logic High		0.80		3.3	V
V _{EN}	Digital Input-Logic Low				0.45	V
I _{EN}	Digital Input-Logic High				15	μA
AC ELECTRICAL CHARACTERISTICS						
G _p	Power Gain		15.5	18.0	19.5	dB
R _L in	Input Return Loss		6.0	9.0		dB
R _L out	Output Return Loss		6.0	14.0		dB
ISL	Reverse Isolation		20.0	30.0		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer		0.55	1.0	dB
K _f	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-13.0	-9.5		dBm
IIP3 _{ib}	Inband input 3 rd -order intercept point	f1=1575.42MHz; f2=1576.42MHz; Pin=-30dBm;	-5.0	-3.0		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz; f2=1850MHz; Pin=-30dBm;	-5.0	0.0		dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	3.0	μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	3.0	μs

Note1: input matched to 50 ohm using a high quality-factor 10nH inductor.

Note2: 0.08dB PCB losses are subtracted.

(AW15045FDR EVB; Typical values are at VCC=1.8V and TA=+25°C, f=1550-1615MHz, unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS					
V _{CC}	Supply Voltage	1.5	-	3.3	V
I _{SD}	Shut-Down Current	EN=Low		1	μA
I _{CC}	Supply Current	EN=High	6.0	8.0	mA
V _{EN}	Digital Input-Logic High	0.80		3.3	V
V _{EN}	Digital Input-Logic Low			0.45	V
I _{EN}	Digital Input-Logic High			15	μA
AC ELECTRICAL CHARACTERISTICS					
G _p	Power Gain	15.5	17.7	19.5	dB
R _L _{in}	Input Return Loss	6.0	8.5		dB
R _L _{out}	Output Return Loss	6.0	14.0		dB
ISL	Reverse Isolation	20.0	30.0		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer	0.55	1.0	dB
K _f	Stability factor	f=20MHz...10GHz	1		
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-13.0	-10.0	dBm
IIP3 _{ib}	Inband input 3 rd -order intercept point	f1=1575.42MHz; f2=1576.42MHz; Pin=-30dBm;	-7.0	-4.0	dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz; f2=1850MHz; Pin=-30dBm;	-5.0	-0.8	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	3.0 μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	3.0 μs

Note1: input matched to 50 ohm using a high quality-factor 10nH inductor.

Note2: 0.08dB PCB losses are subtracted.

(AW15045FDR EVB; Typical values are at VCC=2.8V and TA=+25°C, f=1164-1215MHz, unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS					
V _{CC}	Supply Voltage	1.5	-	3.3	V
I _{SD}	Shut-Down Current	EN=Low		1	μA
I _{CC}	Supply Current	EN=High	6.0	8.0	mA
V _{EN}	Digital Input-Logic High	0.80		3.3	V
V _{EN}	Digital Input-Logic Low			0.45	V
I _{EN}	Digital Input-Logic High			15	μA
AC ELECTRICAL CHARACTERISTICS					
G _p	Power Gain	15.5	17.7	19.5	dB
R _L _{in}	Input Return Loss	8.0	12.0		dB
R _L _{out}	Output Return Loss	6.0	14.0		dB
ISL	Reverse Isolation	20.0	40.0		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer	0.5	1.0	dB
K _f	Stability factor	f=20MHz...10GHz	1		
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-15.0	-13.3	dBm
IIP3 _{ib}	Inband input 3 rd -order intercept point	f1=1176.45MHz; f2=1177.45MHz; Pin=-30dBm;	-6.0	-4.0	dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1800MHz; f2=2400MHz; Pin=-30dBm;	-3	8.7	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	3.0 μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	3.0 μs

Note1: input matched to 50 ohm using a high quality-factor 20nH inductor. Output matching using 12nH inductor and 5.6pF capacitor.

Note2: 0.08dB PCB losses are subtracted.

(AW15045FDR EVB; Typical values are at VCC=1.8V and TA=+25°C, f=1164-1215MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.3	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		6.0	8.0	mA
V _{EN}	Digital Input-Logic High		0.80		3.3	V
V _{EN}	Digital Input-Logic Low				0.45	V
I _{EN}	Digital Input-Logic High				15	μA
AC ELECTRICAL CHARACTERISTICS						
G _p	Power Gain		15.5	17.5	19.5	dB
R _L _{in}	Input Return Loss		8.0	12.0		dB
R _L _{out}	Output Return Loss		6.0	14.0		dB
ISL	Reverse Isolation		20.0	40.0		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer		0.5	1.0	dB
K _f	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-17.0	-14.0		dBm
IIP3ib	Inband input 3rd-order intercept point	f1=1176.45MHz; f2=1177.45MHz; Pin=-30dBm;	-10.0	-5.0		dBm
IIP3oob	Out-of-band input 3rd-order intercept point	f1=1800MHz; f2=2400MHz; Pin=-30dBm;	-3	8.7		dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	3.0	μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	3.0	μs

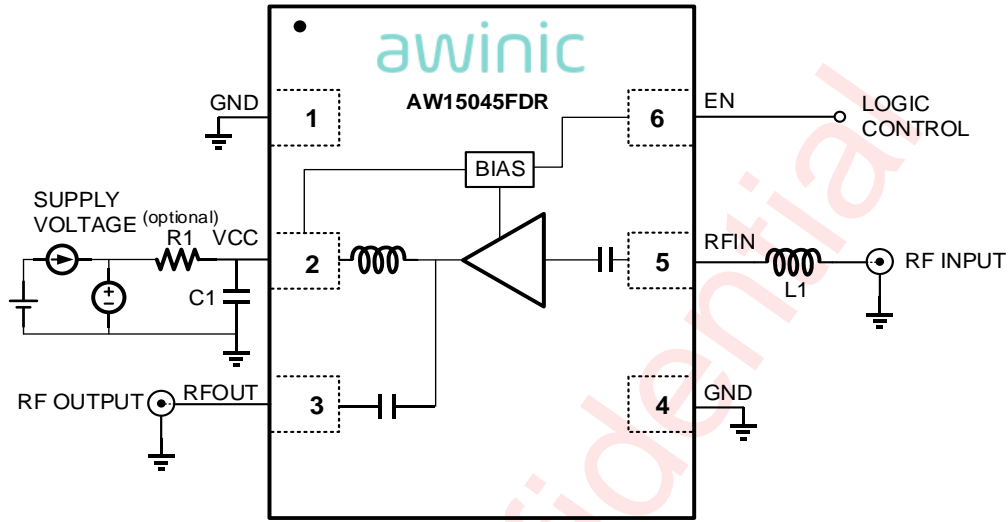
Note1: input matched to 50 ohm using a high quality-factor 20nH inductor. Output matching using 12nH inductor and 5.6pF capacitor.

Note2: 0.08dB PCB losses are subtracted.

TEST CIRCUITS

DC Characteristics

The following is the test bench for power supply, pin voltage, supply current, standby current



C1, R1 Closed to LNA

Figure 4 Test Circuits

S Parameter

The following is the test bench for input return loss, output return loss, reverse isolation, forward gain, and 1dB gain compression.

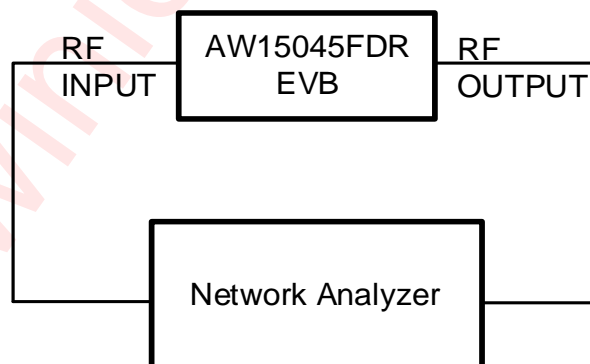


Figure 5 S Parameter Test Bench

Noise Figure

The following is the test bench for noise figure, power gain.

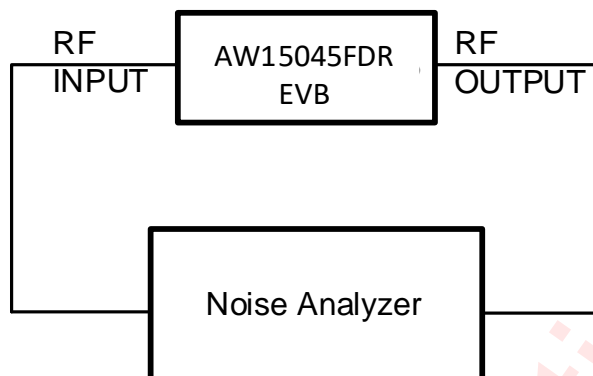


Figure 6 Noise Figure Test Bench

Intermodulation distortion

The following is the test bench for third-order intercept point and second-order intercept point.

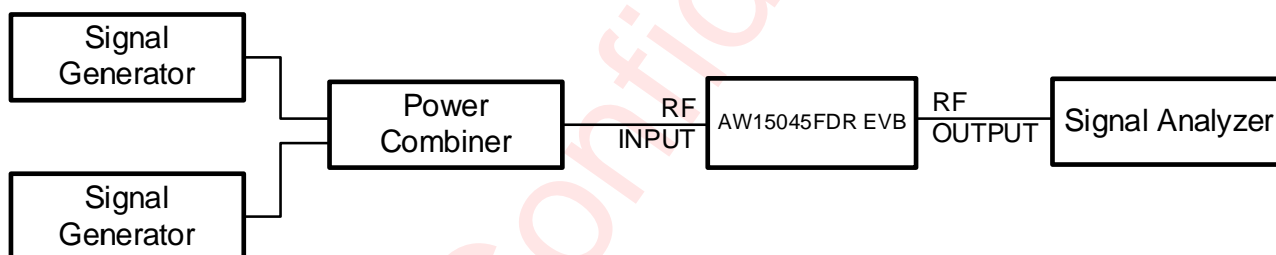
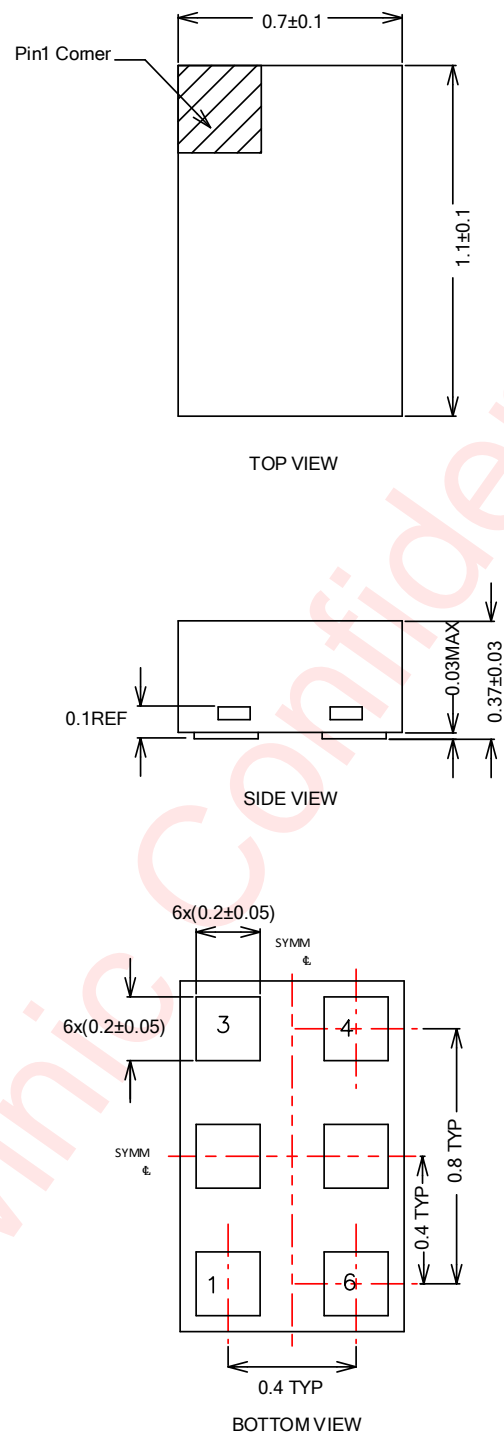


Figure 7 IIP3 Test Bench

PACKAGE DESCRIPTION



Unit: mm

Figure 8 Package Outline

LAND PATTERN

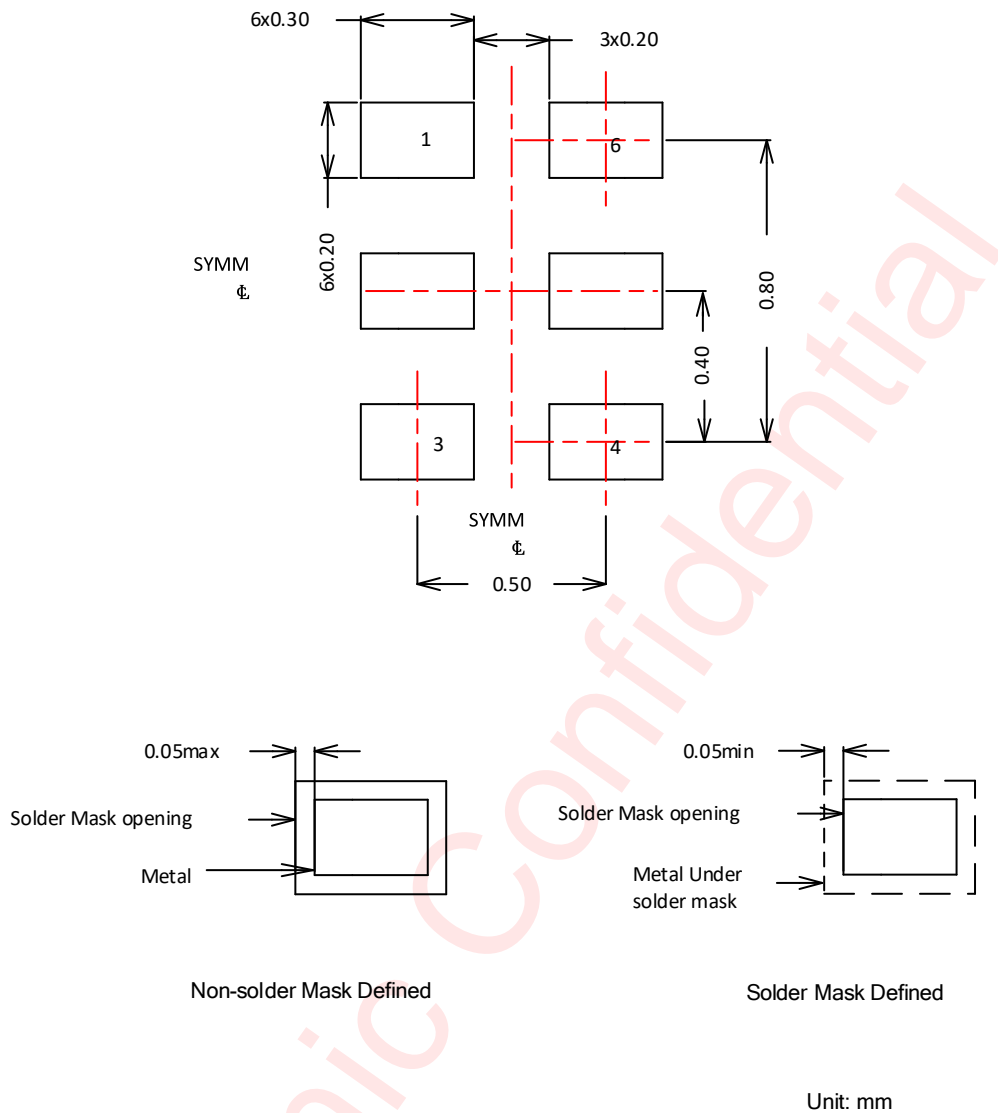
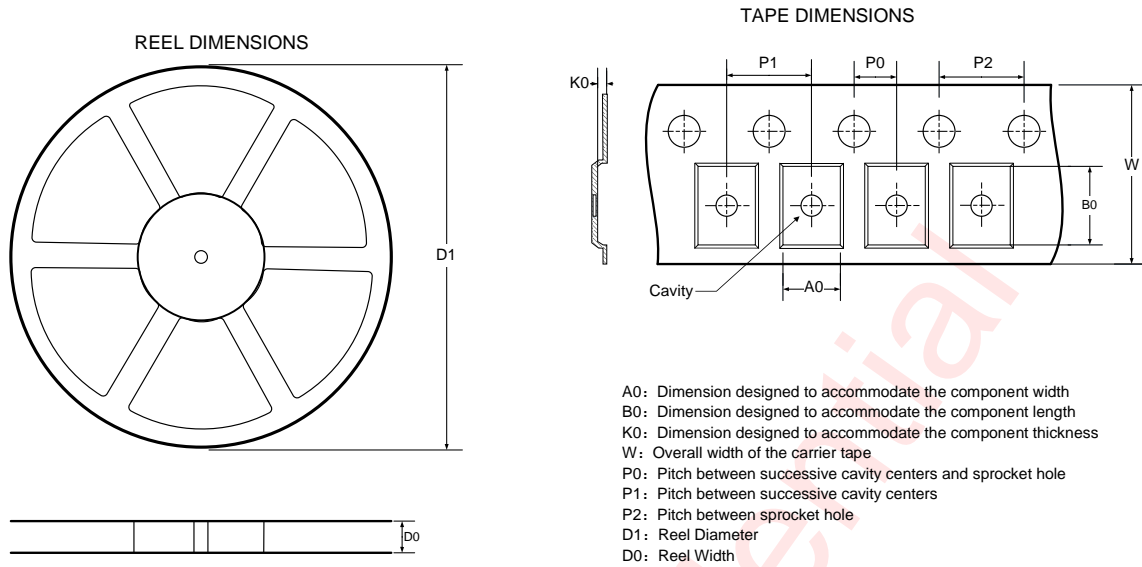
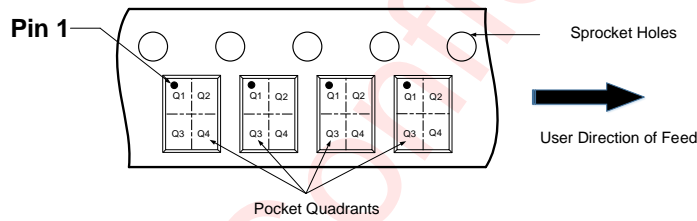


Figure 9 Land Pattern

TAPE & REEL DESCRIPTION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.8	1.2	0.55	2	2	4	8	Q1

All dimensions are nominal

Figure 10 Tape & Reel Description

REVISION HISTORY

Version	Date	Change Record
V1.0	Jun. 2019	Officially Released
V1.1	Nov. 2019	Updated Electrical Characteristics
V1.2	Jan. 2020	Updated Electrical Characteristics
V1.3	Apr. 2020	Updated Document Pattern
V1.4	Aug. 2020	Updated Electrical Characteristics
V1.5	Aug. 2020	Updated Electrical Characteristics
V1.6	Apr. 2021	Updated Electrical Characteristics
V1.7	Jul. 2021	Updated Electrical Characteristics
V1.8	Nov. 2021	Change the spec of L1 and L5; Change the spec of gain and RL_{out} in L5

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