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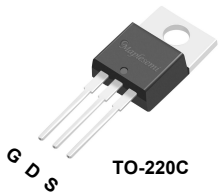
SLP160N10G
100V N -Channel MOSFET

General Description

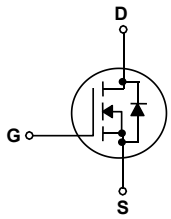
This Power MOSFET is produced using Msemitek's advanced Shielding Gate MOSFET technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters and high efficiency switching for power management in portable and battery operated products.

Features

- N-Channel:100V 160A
  $R_{DS(on)Typ}$= 3.7mΩ@V_{GS} = 10 V
  - Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220C



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLP160N10G	Units
V_{DSS}	Drain-Source Voltage	100	V
I_D	Drain Current - Continuous (T_C = 25℃)	160	A
	- Continuous (T_C = 100℃)	102	A
I_{DM}	Drain Current - Pulsed (Note 1)	480	A
V_{GSS}	Gate-Source Voltage	±25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1050	mJ
P_D	Power Dissipation (T_C = 25℃)	210	W
	Power Dissipation (T_C = 100℃)	1.4	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.72	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to ambient	-	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLP160N10G	SLP160N10G	TO-220C	Tube	1000	5000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =100 V, V_{GS} = 0 V	--	--	1.0	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 25V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -25V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	-	4.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 40A	--	3.7	4.2	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	6100	-	pF
C_{oss}	Output Capacitance		--	730	-	pF
C_{rss}	Reverse Transfer Capacitance		--	35	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= 10 V, V_{DS}=50V, R_L = 4.7Ω ,,I_D=40A (Note 3)	--	19	--	ns
t_r	Turn-On Rise Time		--	76	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	48	--	ns
t_f	Turn-Off Fall Time		--	14	--	ns
Q_g	Total Gate Charge	V_{DS} = 50 V, I_D =40A, V_{GS} = 10V (Note 3)	--	92	--	nC
Q_{gs}	Gate-Source Charge		--	35.2	--	nC
Q_{gd}	Gate-Drain Charge		--	18.8	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	160	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	480	A
V_{SD}	Drain to Source Diode Forward Voltage,V_{GS} = 0V, I_{SD} =40A,T J = 25℃		--	-	1.2	V
T_{rr}	Reverse recovery time,I F =160A DI F /dt=100A/μs			63		ns
Q_{rr}	Reverse recovery charge,I F =160A DI F /dt=100A/μs			142		nC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T J =25℃, V DD =50V, V_G =10V, L=0.5mH,
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

N- Channel Typical Characteristics

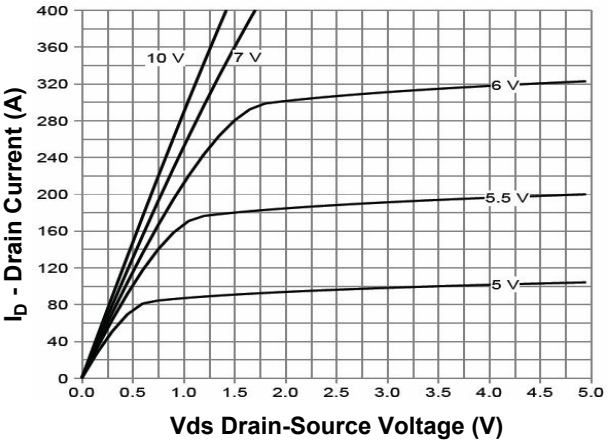


Figure 1. On-Region Characteristics

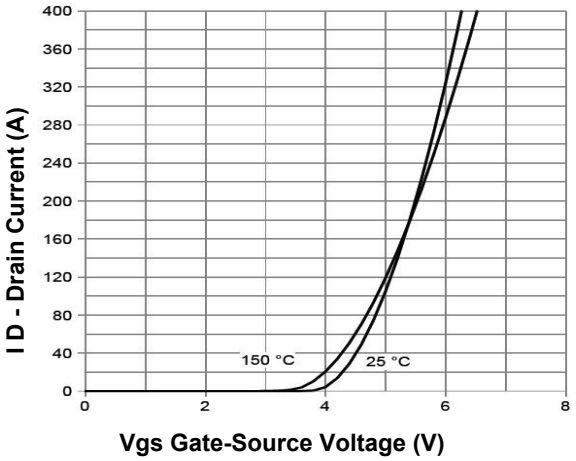


Figure 2. Transfer Characteristics

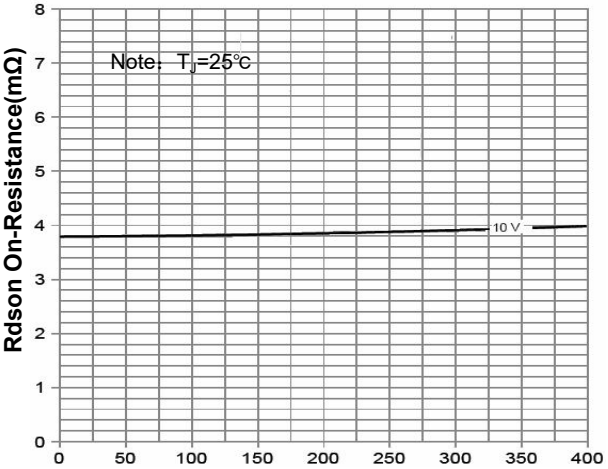


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

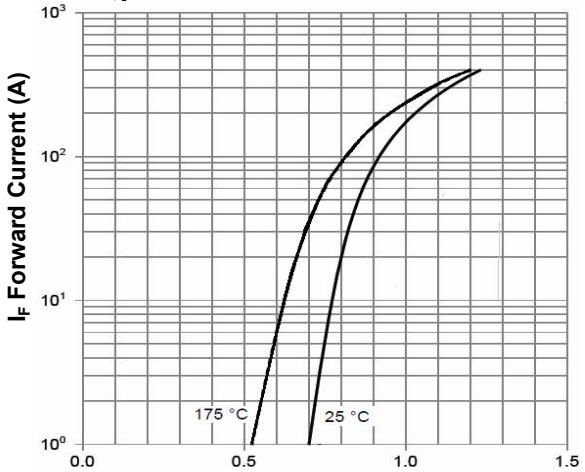


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

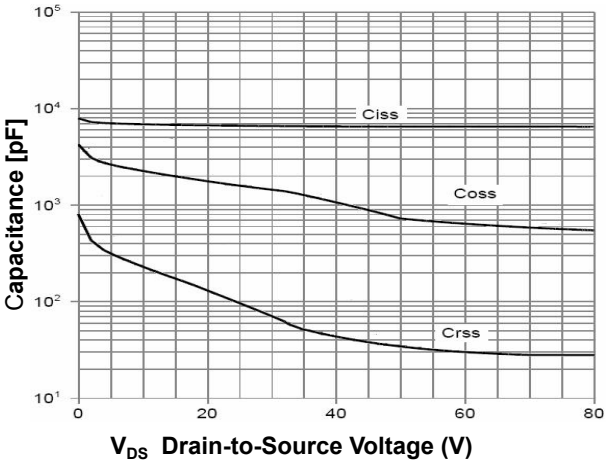


Figure 5. Capacitance Characteristics

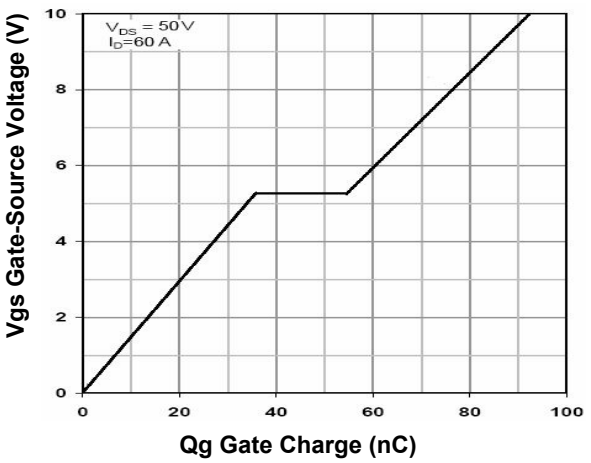


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

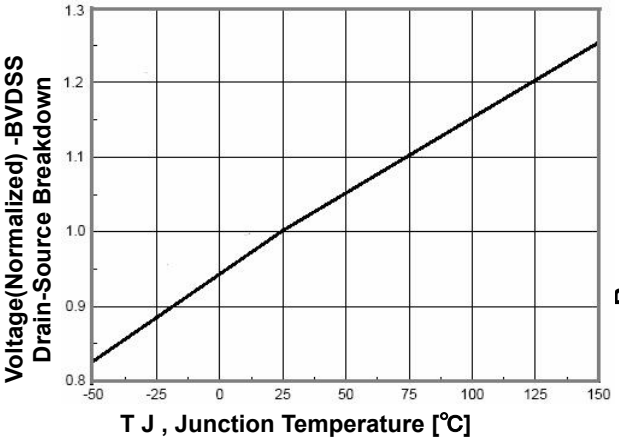


Figure 7. Breakdown Voltage Variation vs Temperature

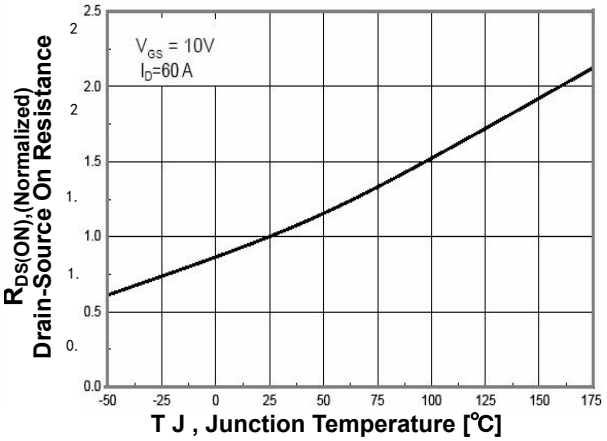


Figure 8. On-Resistance Variation vs Temperature

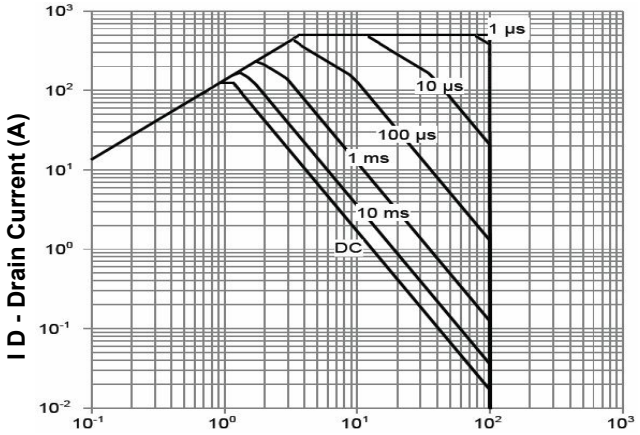


Figure 9. Maximum Safe Operating Area

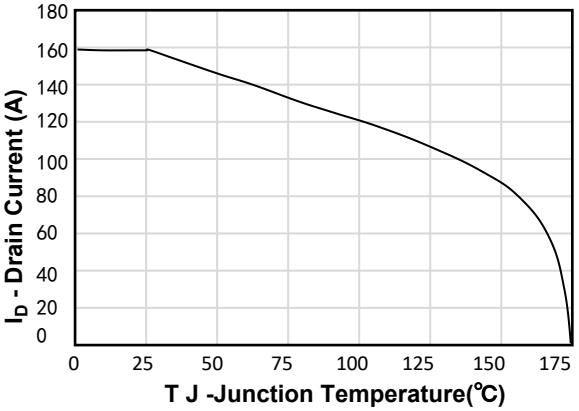


Figure 10. Maximum Continuous Drain Current vs Temperature

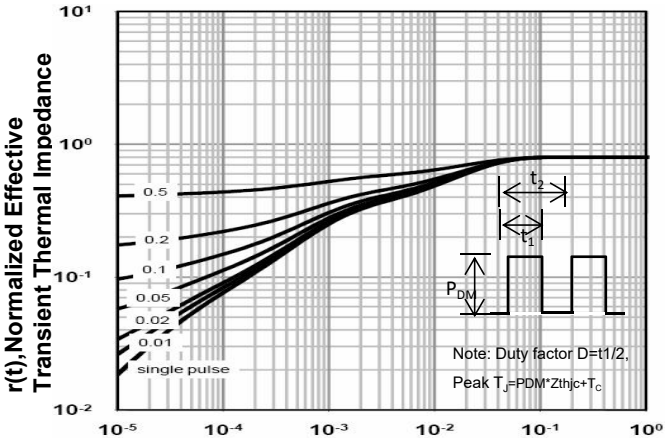
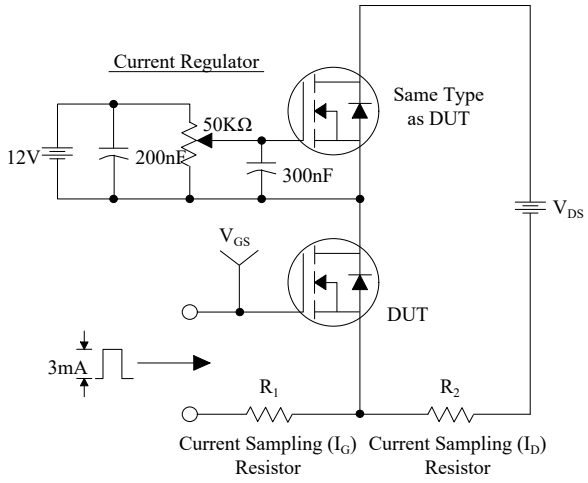
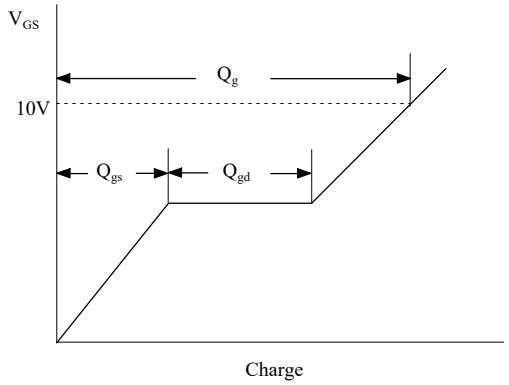


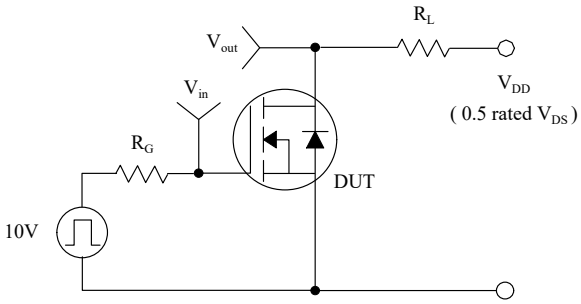
Figure 11. Transient Thermal Response Curve

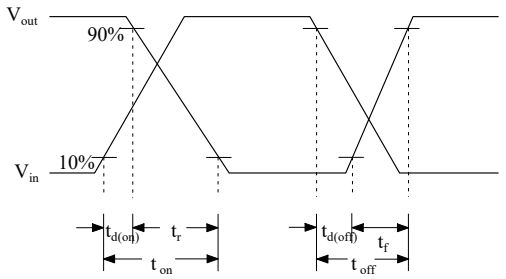
Gate Charge Test Circuit & Waveform



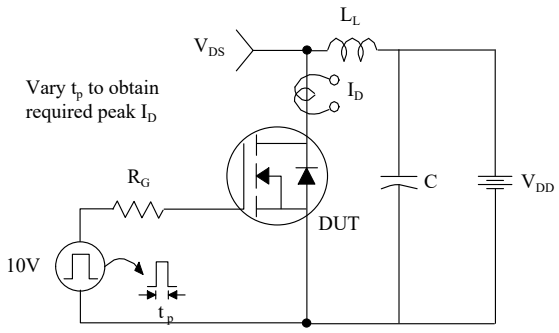


Resistive Switching Test Circuit & Waveforms

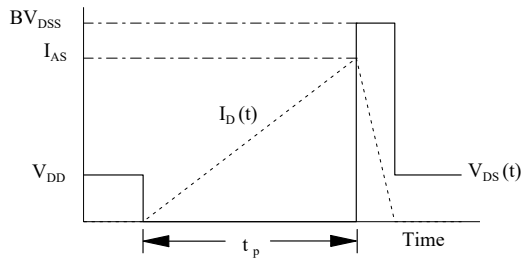




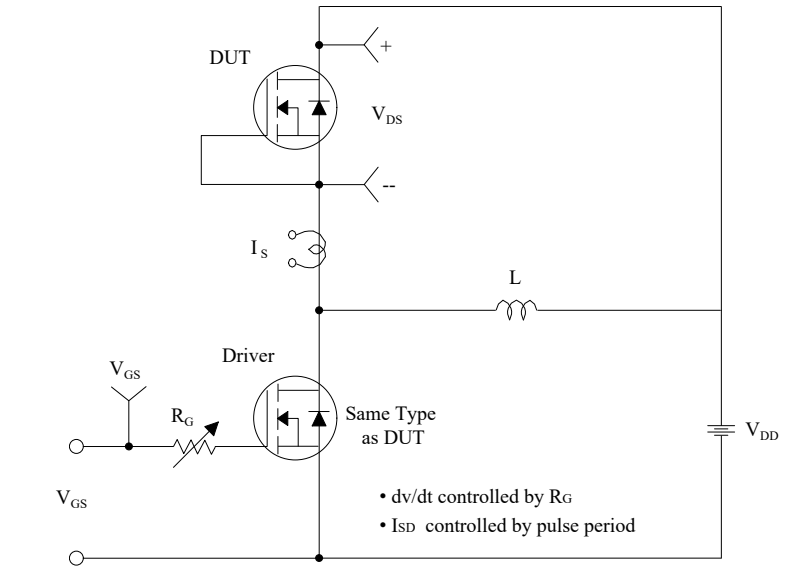
Unclamped Inductive Switching Test Circuit & Waveforms

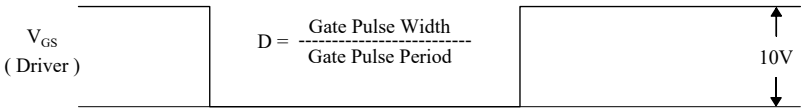


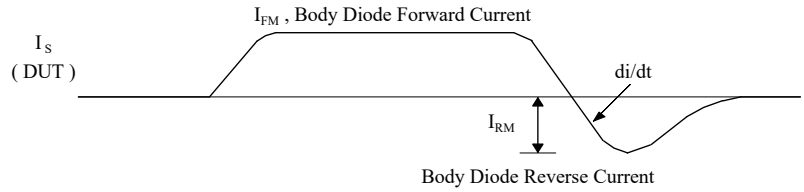
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

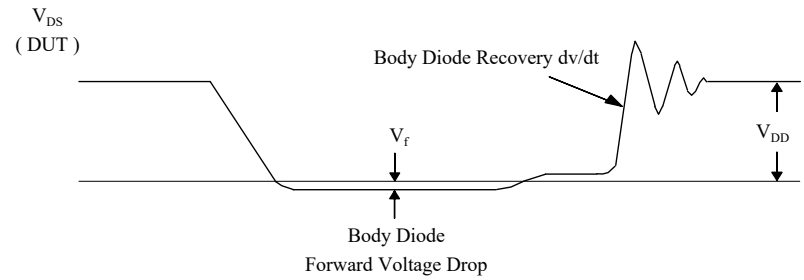


Peak Diode Recovery dv/dt Test Circuit & Waveforms

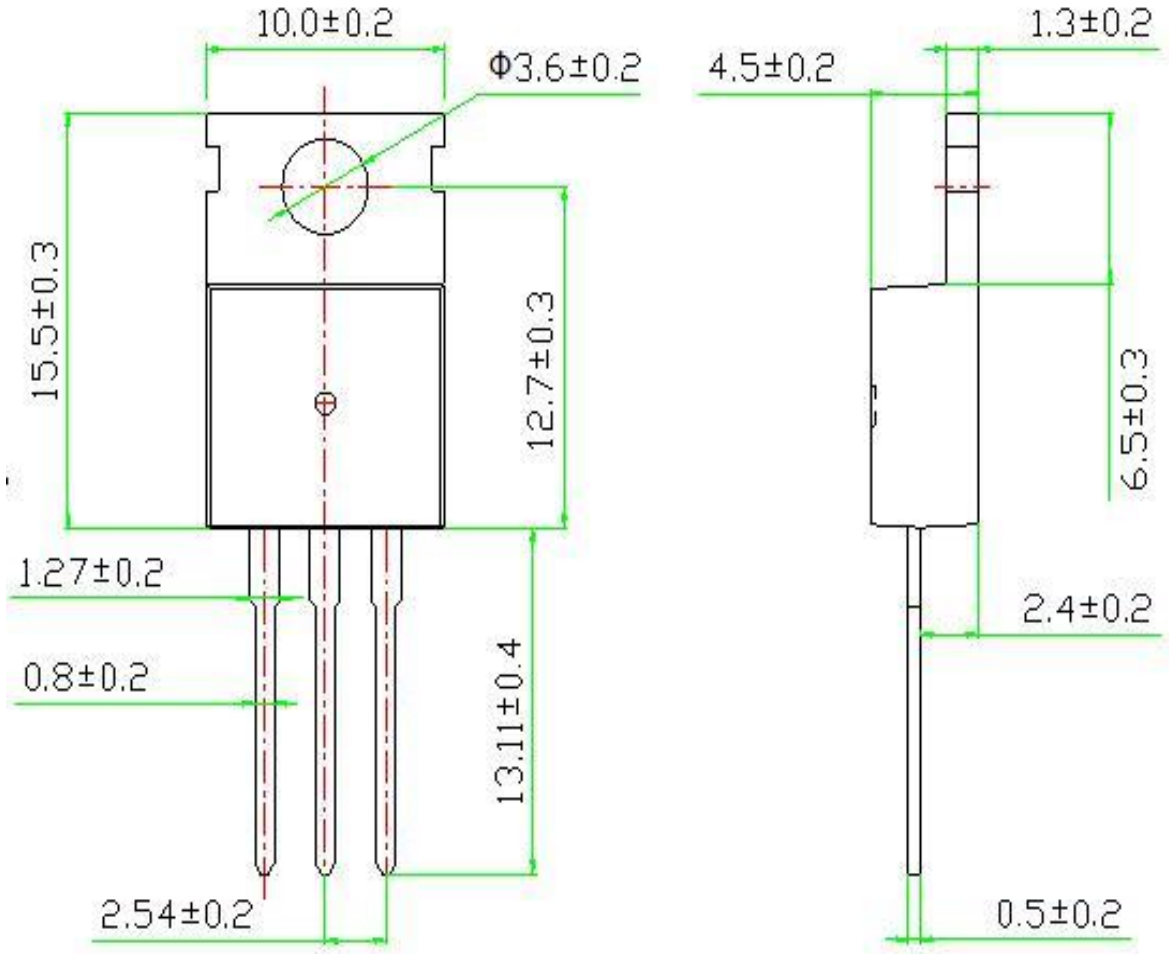








TO-220C OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

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