

### Product Overview

NSD1624x is a high voltage, high side-low side gate driver having capability to deliver 4A source and 6A sink current to drive power MOSFETs or IGBTs.

The high side section is designed to endure a DC voltage over 1200V with innovative and proven isolation technology. NSD1624x offers best in class propagation delay, low quiescent current, high negative and dv/dt immunity on SW pin.

Both high side and low side driver section work from 10V to 20V supply voltages having independent under voltage lockout (UVLO) protection. NSD1624x has two independent input pins (HIN and LIN) which are compatible for TTL and CMOS logic. NSD1624x is available in LGA10, SOP8, and SOP14 package with operating temperature range from -40°C to 125°C.

### Key Features

- High voltage range: Up to 1200V (SOP14) / 700V (SOP8)
- Less than 35ns Propagation Delay
- Less than 7ns Delay Matching
- 4A Source / 6A Sink Currents
- High Negative and Transient Immunity up to 150V/ns on SW Pin
- Gate Drive Supply Voltage from 10V to 20V
- TTL and CMOS Compatible Input Logic
- UVLO Protection for High-side and Low-side Drivers
- Separated Grounds for Logic (SGND) and Driver in SOP14 package
- High and Low Voltage Pins Separated for Maximum Creepage and Clearance in SOP14 Package

- RoHS & REACH Compliant
- Lead-free component, suitable for lead-free soldering profile: 260°C

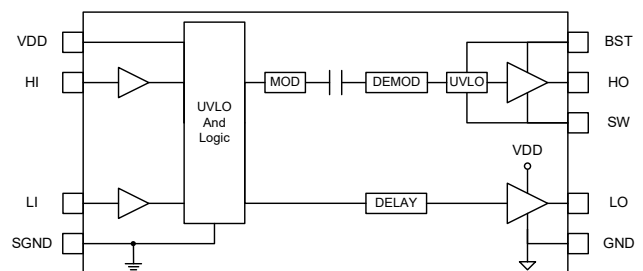
### Applications

- Half-bridge, full-bridge, and LLC converters.
- High density switching power supplies for Server, Telecom and Industrial
- Solar inverters, Motor controls and EV charges

### Device Information

Part Number	Package	Body Size
NSD1624-DLAJR	LGA10	4.0 mm × 4.0 mm x 0.85mm
NSD1624-DSPKR	SOP14	8.6 mm × 3.9 mm x 1.75mm
NSD1624-DSPR	SOP8	4.9 mm × 3.9 mm x 1.75mm
NSD16241-DSPKR	SOP14	8.6 mm × 3.9 mm x 1.75mm
NSD16241-DSPR	SOP8	4.9 mm × 3.9 mm x 1.75mm
NSD16242-DSPR	SOP8	4.9 mm × 3.9 mm x 1.75mm

### Functional Block Diagram



NSD1624x Block Diagram

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### 1. Pin Configuration and Functions

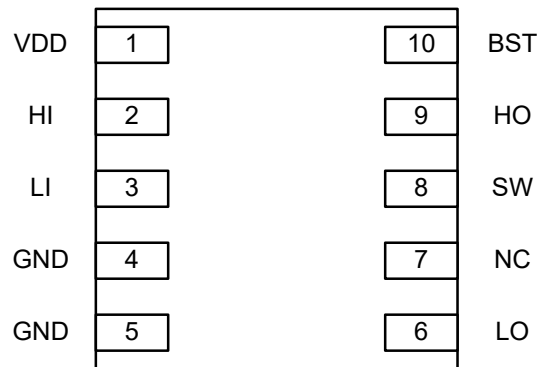


Figure 1.1 NSD1624 LGA10 Package

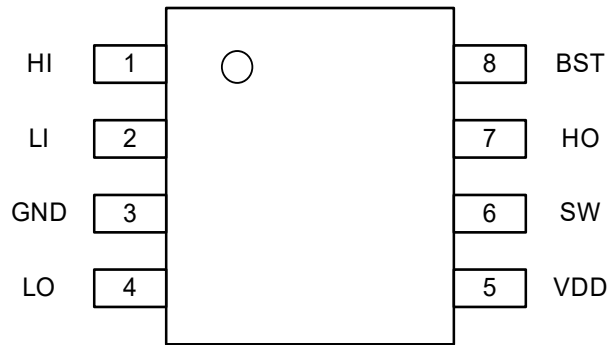


Figure 1.2 NSD1624 SOP8 Package

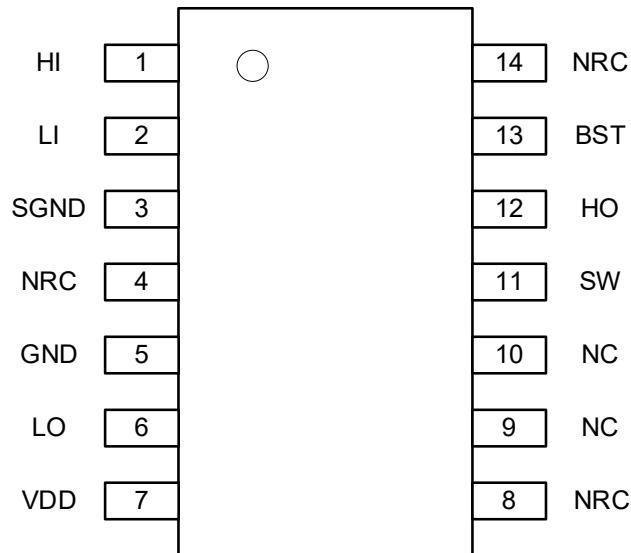


Figure 1.3 NSD1624 SOP14 Package

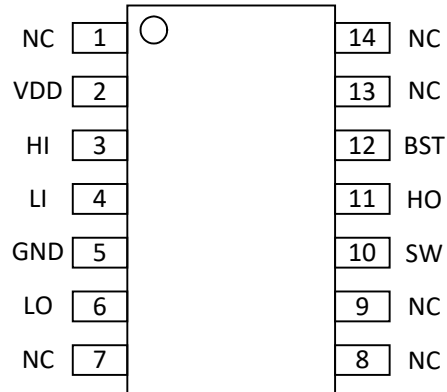


Figure 1.4 NSD16241 SOP14 Package

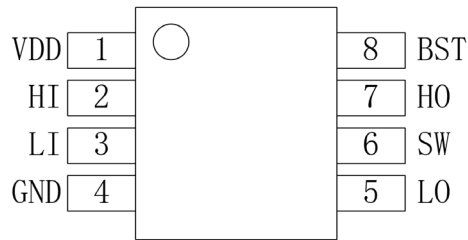


Figure 1.5 NSD16241 SOP8 Package

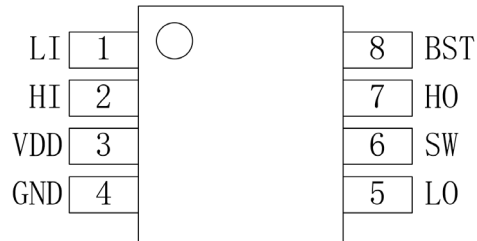


Figure 1.6 NSD16242 SOP8 Package

Table 1.1 NSD1624x Pin Configuration and Description

PIN NO.						SYMBOL	FUNCTION
LGA10 (NSD1624)	SOP8 (NSD1624)	SOP14 (NSD1624)	SOP14 (NSD16241)	SOP8 (NSD16241)	SOP8 (NSD16242)		
4, 5	3	5	5	4	4	GND	Power Ground, return for low-side driver.
2	1	1	3	2	2	HI	Logic input for high-side driver.
3	2	2	4	3	1	LI	Logic input for low-side driver.
1	5	7	2	1	3	VDD	Power supply for the input logic part and low-side driver.
6	4	6	6	5	5	LO	Low-side driver output.
9	7	12	11	7	7	HO	High-side driver output.
10	8	13	12	8	8	BST	High-side floating supply.
8	6	11	10	6	6	SW	High-side supply return.
/	/	3	/	/	/	SGND	Signal ground, reference for input
7	/	9,10	1, 7, 8, 9, 13, 14	/	/	NC	Floating internally
/	/	4	/	/	/	NRC <sup>1)</sup>	Not recommend connected on PCB
/	/	8	/	/	/	NRC <sup>2)</sup>	Not recommend connected on PCB
/	/	14	/	/	/	NRC <sup>3)</sup>	Not recommend connected on PCB

- 1) It is not insulated with SGND internally.
- 2) It is not insulated with GND internally.
- 3) It is not insulated with SW internally.

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Supply Voltage	$V_{DD}$	-0.3	24	V
High side SW pin voltage (SOP14)	$V_{SW}$	-1200	1200	V
High side SW pin voltage (LGA&SOP8)	$V_{SW}$	-700	700	V
High side floating voltage	$V_{BST} - V_{SW}$	-0.3	24	V
High side output voltage	$V_{HO}$	$V_{SW}-0.3$	$V_{BST}+0.3$	V
	$V_{HO}$ , Transient for 100ns	$V_{SW}-2$	$V_{BST}+0.3$	V
Low side output voltage	$V_{LO}$	-0.3	$V_{DD}+0.3$	V
	$V_{LO}$ , Transient for 100ns	-2	$V_{DD}+0.3$	V
Signal ground to GND <sup>1)</sup>	$V_{SGND}$	-5	5	V

Input voltage to Signal ground	$V_{HI}, V_{LI}, V_{VDD}$	$V_{SGND} - 0.3$	$V_{SGND} + 20$	V
Junction Temperature	$T_J$	-40	150	°C
Storage Temperature	$T_{J\_ST}$	-40	150	°C

Parameters	Symbol	Value	Unit
Electronic Discharge (ESD)	Human-body model (HBM), per AEC-Q100-002 Rev D	±2000	V
	Charged-device model (CDM), per AEC-Q100-011 Rev D	±1000	V

- 1) Only for NSD1624 SOP14 Package

### 3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Comments
Input Supply Voltage Range	$V_{VDD}$	10	20	V	
High Side Floating Voltage	$V_{BST} - V_{SW}$	10	20	V	
High Side SW Pin Voltage	$V_{SW}$	-1200	1200	V	for SOP14 package
	$V_{SW}$	-700	700	V	for SOP8 & LGA package
High Side Output Voltage	$V_{HO}$	$V_{SW}$	$V_{BST}$	V	
Low Side Output Voltage	$V_{LO}$	0	$V_{VDD}$	V	
Input Signal Voltage Range	$V_{HI}, V_{LI}$	$V_{SGND}$	$V_{SGND} + 17$	V	
Signal ground	$V_{SGND}$	-3	3	V	
Junction Temperature	$T_J$	-40	140	°C	
Ambient Temperature	$T_a$	-40	125	°C	

### 4. Thermal Information

Parameters	Symbol	LGA10	SOP8	SOP14	Unit
Junction-to-ambient thermal resistance <sup>1)</sup>	$\theta_{JA}$	106	103	85	°C/W
Junction-to-case(top) thermal resistance <sup>1)</sup>	$\theta_{JC (top)}$	81	63	41	°C/W
Junction-to-board characterization parameter	$\Psi_{JB}$	95	70	47	°C/W

- 1) Standard JESD51-7 High Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.  
 2) Obtained by Simulating in an environment described in JESD51-2a.

## 5. Specifications

### 5.1. Electrical Characteristics

At  $V_{DD} = V_{BST} = 15V$ ,  $V_{SGND} = V_{SW} = 0V$ , all voltages are with respect to GND, no load on LO and HO,  $-40^{\circ}C < T_J < 125^{\circ}C$

Parameter	Symbol	Min	Typ	Max	Unit	Comments
<b>Supply Section</b>						
VDD quiescent current	$I_{VDD\_Q}$		0.4	0.5	mA	$V_{LI} = V_{HI} = 0V$
High-side supply quiescent current	$I_{BST\_Q}$		0.6	0.76	mA	$V_{LI} = V_{HI} = 0V$
VDD operating current	$I_{VDD\_O}$		1.1		mA	$f = 500\text{ kHz}$ , $C_{LOAD} = 0nF$
High-side supply operating current	$I_{BST\_O}$		1.3		mA	$f = 500\text{ kHz}$ , $C_{LOAD} = 0nF$
SW to GND leakage current	$I_{SW\_LK}$		/	0.01	$\mu A$	$V_{SW} = 700V$
<b>INPUT SECTION</b>						
Input rising threshold	$V_{HI\_H}, V_{LI\_H}$	1.8	2.1	2.4	V	
Input falling threshold	$V_{HI\_L}, V_{LI\_L}$	0.9	1.2	1.5	V	
Input voltage Hysteresis	$V_{HI\_HYS}, V_{LI\_HYS}$		0.9		V	
High Level Logic Input Bias Current	$I_{IN+}$		17		$\mu A$	$V_{LI} / V_{HI} = 5V$
Low Level Logic Input Bias Current	$I_{IN-}$		0	10	$\mu A$	$V_{LI} = V_{HI} = 0.3V$
Input pulldown resistance	$R_{IN}$		260		kOhm	$V_{LI} = V_{HI} = 3V$
<b>UNDER VOLTAGE LOCKOUT</b>						
turn-on threshold voltage of VDD	$V_{DD\_UV+}$	8.6	9.1	9.5	V	
turn-off threshold voltage of VDD	$V_{DD\_UV-}$	8.2	8.7	9.1	V	
V CC hysteresis	$V_{DD\_UVH}$		0.4		V	
UVLO positive Threshold on $V_{BST}-V_{SW}$	$V_{BST\_UV+}$	7.9	8.4	8.9	V	
UVLO negative Threshold on $V_{BST}-V_{SW}$	$V_{BST\_UV-}$	7.4	7.9	8.3	V	
VBST hysteresis	$V_{BST\_UVH}$		0.5		V	
<b>Output SECTION</b>						
Low level output voltage	$V_{OL}$		0.06		V	$I_{LO} = 100\text{ mA}$
High level output voltage	$V_{OH}$		0.12		V	$I_{LO} = -100\text{ mA}$ , $V_{LOH} = V_{VDD}-V_{LO}$
Low level output Resistance	$R_{OL}$		0.6	1.2	Ohm	
High level output Resistance	$R_{OH}$		1.2	2	Ohm	
Peak source current	$I_{OSRC}$		4		A	$V_O = 0V$
Peak sink current	$I_{OSNK}$		6		A	$V_O = V_{DD}$

**5.2. Switching Characteristics**

At  $V_{DD} = V_{BST} = 15V$ ,  $V_{SGND} = V_{SW} = 0V$ , all voltages are with respect to GND, no load on LO and HO if not mentioned,  $-40^{\circ}C < T_j < 125^{\circ}C$

Parameter	Symbol	Min	Typ	Max	Unit	Comments
High Side Startup Time	$T_{startup}$		10	15	us	between $V_B > UVLO$ and First HO Pulse
Rise Time LO, HO	$T_R$		10		ns	$C_{load} = 1000pF$
Fall Time LO, HO	$T_F$		9		ns	$C_{load} = 1000pF$
Low-to-high delay matching	$T_{LHDM}$			7	ns	Pulse width = 1us
High-to-low delay matching	$T_{HLDM}$			7	ns	Pulse width = 1us
Minimum Input Filter	$T_{MPW}$		11	30	ns	
Turn-on delay, LI to LO	$T_{LDLH}$		22	35	ns	
Turn-off delay, LI to LO	$T_{LDHL}$		22	35	ns	
Turn-on delay, HI to HO	$T_{HDLH}$		22	35	ns	
Turn-off delay, HI to HO	$T_{HDHL}$		22	35	ns	
Dead time	$T_{dt}$		2		ns	

**5.3. Typical Performance Characteristics**

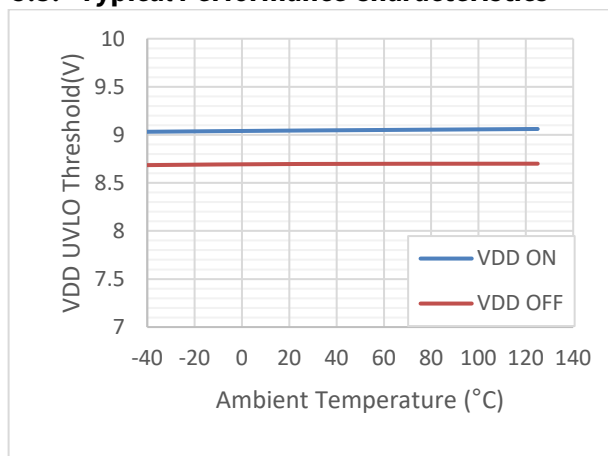


Figure 5.1 VDD UVLO Threshold vs Temperature

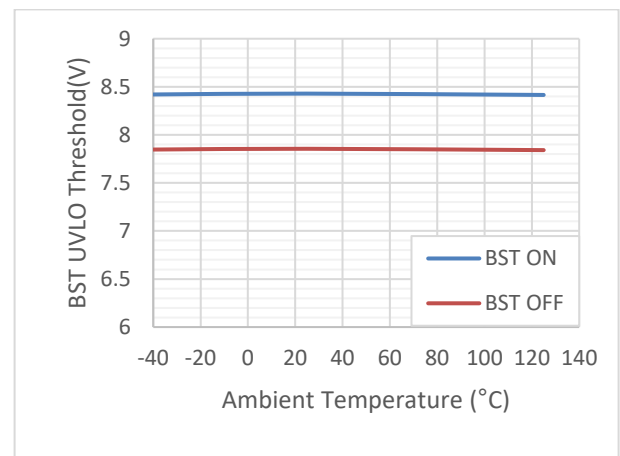


Figure 5.2 BST UVLO Threshold vs Temperature



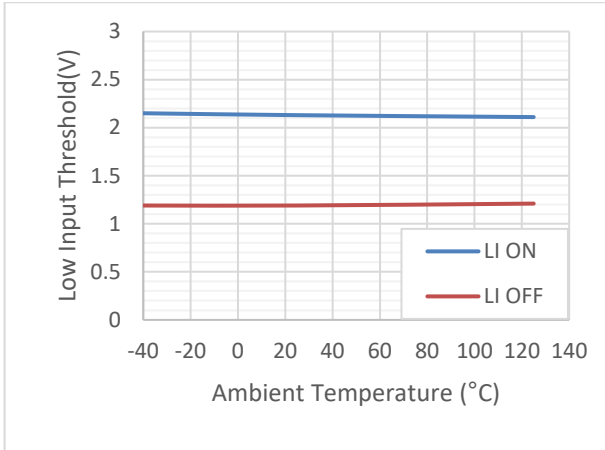


Figure 5.3 Low Input Logic Threshold vs Temperature

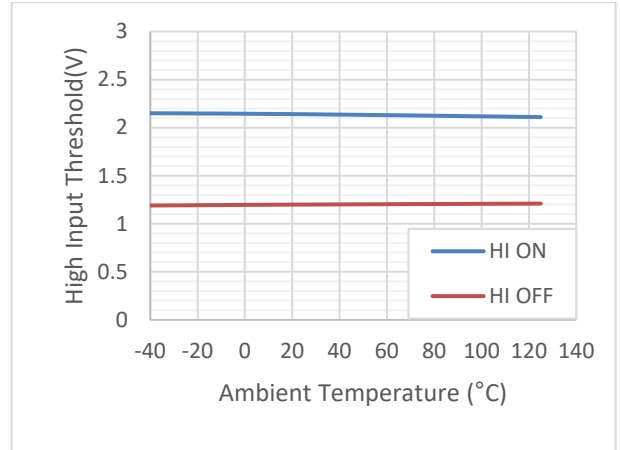


Figure 5.4 High Input Logic Threshold vs Temperature

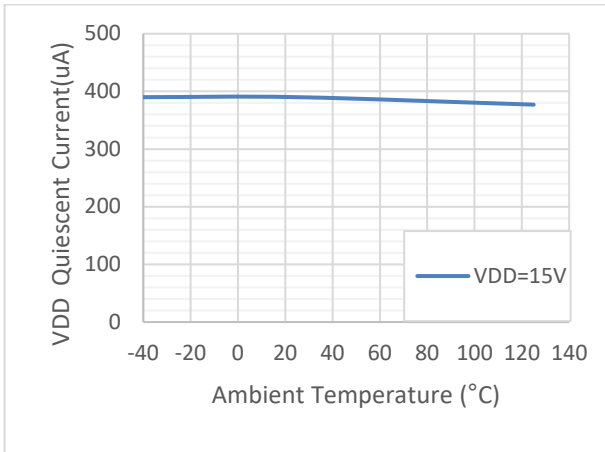


Figure 5.5 VDD Quiescent Current vs Temperature

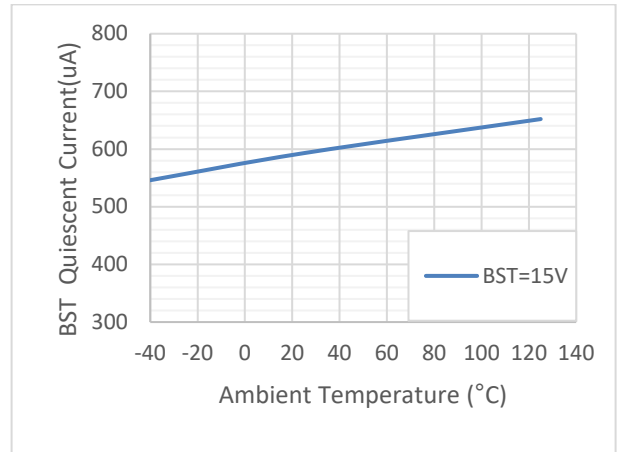


Figure 5.6 BST Quiescent Current vs Temperature

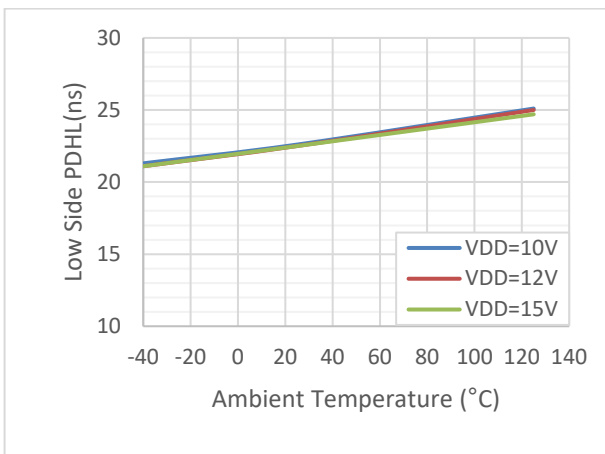


Figure 5.7 Low Side Turn-off Delay vs Temperature

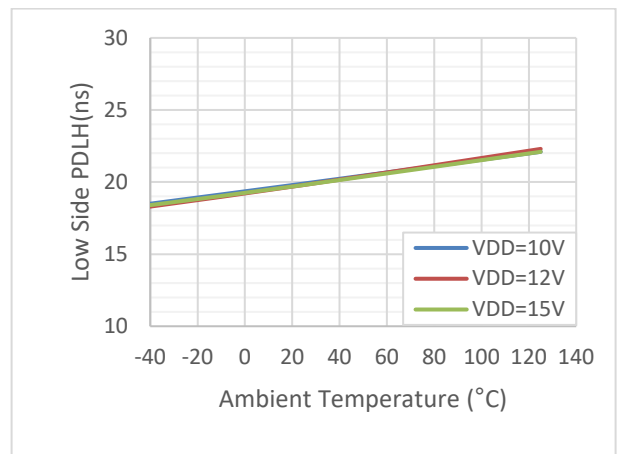


Figure 5.8 Low Side Turn-on Delay vs Temperature

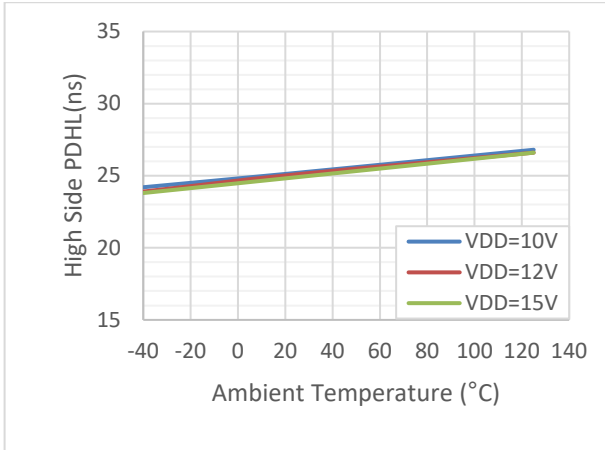


Figure 5.9 High Side Turn-off Delay vs Temperature

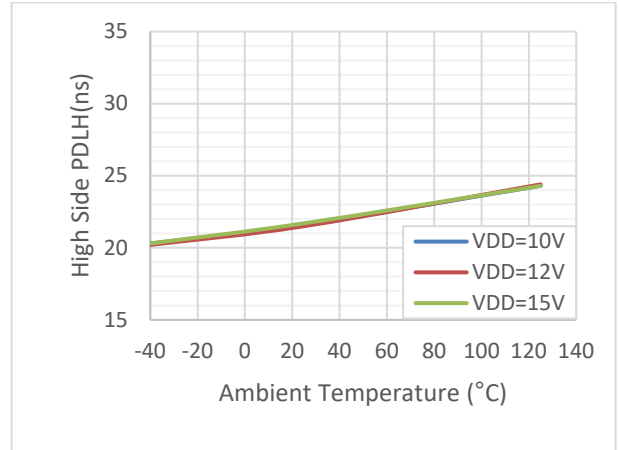


Figure 5.10 High Side Turn-on Delay vs Temperature

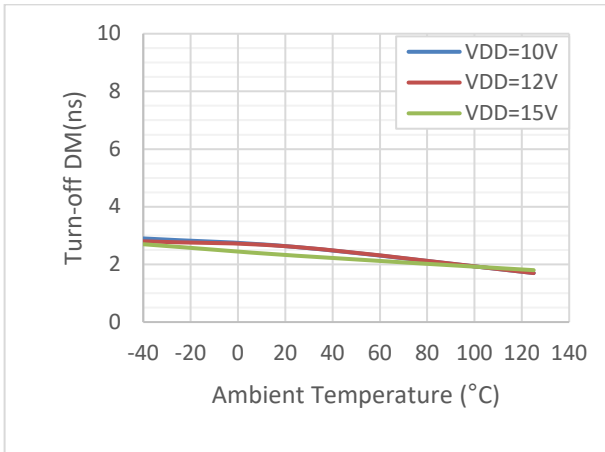


Figure 5.11 Turn-off Delay Match vs Temperature

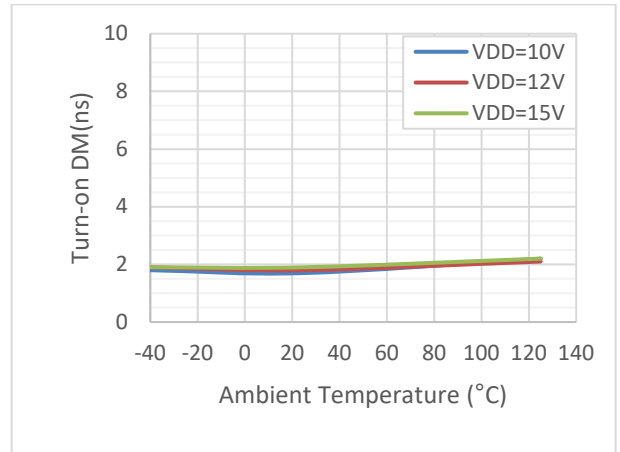


Figure 5.12 Turn-on Delay Match vs Temperature

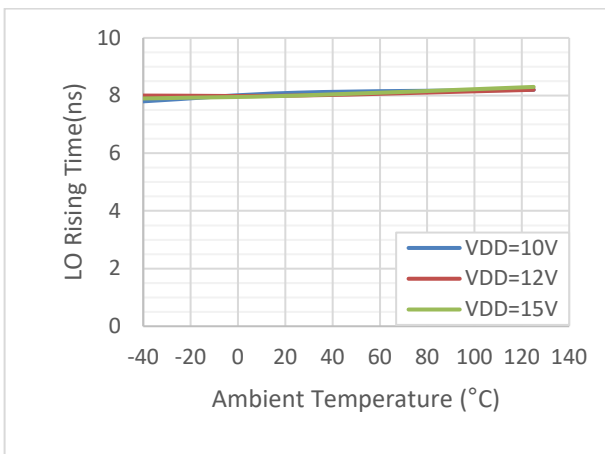


Figure 5.13 LO Rising Time (Co=1000pF) vs Temperature

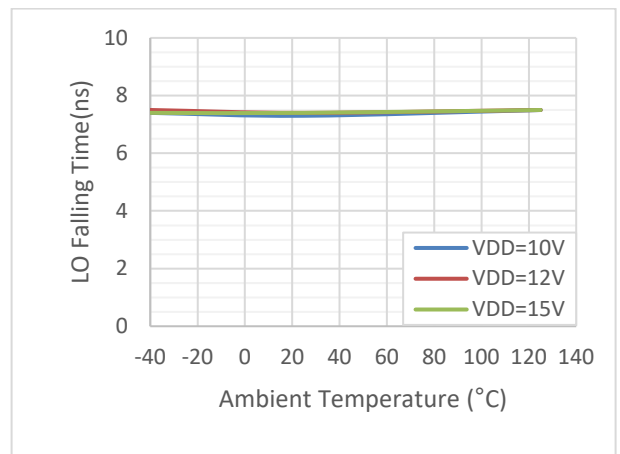


Figure 5.14 LO Falling time (Co=1000pF) vs Temperature

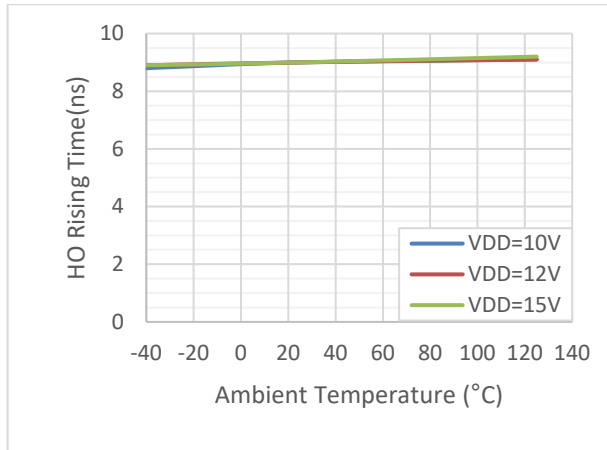


Figure 5.15 HO Rising Time (Co=1000pF) vs Temperature

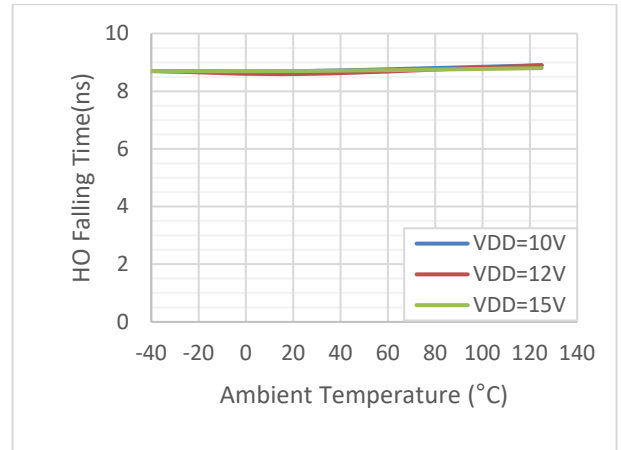


Figure 5.16 HO Falling Time (Co=1000pF) vs Temperature

## 5.4. Parameter Measurement Information

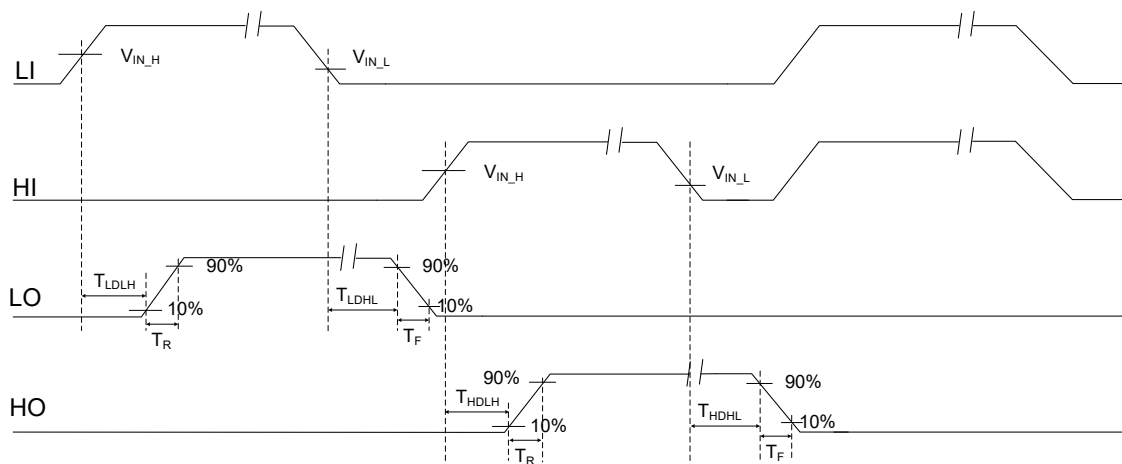


Figure 5.17 Propagation Delay, rise and fall time

## 6. General Description

### 6.1. Overview

NSD1624x is a high reliability low side-high side gate driver with two independent input pins HIN and LIN dedicated to be used in AC-DC and DC-AC power applications. Driver inputs are compatible with CMOS and TTL logic hence it provides easy interface with analog and digital controllers. The high side is a floating section that usually require an effective bootstrap circuit to bias. High side Isolated driver has high negative and dv/dt immunity on SW pin that improve the robustness of the driver. NSD1624x has independent under voltage lock out feature for both high and low side gate drivers which ensure the working of both channels at  $V_{DD\_UV+}$  and  $V_{BST\_UV+}$ .

In popular power converter topologies such as half bridge, full bridge converter, LLC, two switch forward converter and phase-shift full bridge, low and high side gate driver provides a function of buffer and level shifter. This driver can drive the top side MOSFET

and IGBT whose source and emitter node is a dynamically changing. Therefore, to make them stable referenced to a fixed potential, floating-driver devices are necessary to use in these topologies.

NSD1624x offers best in class propagation delay, less than 7ns delay matching, low quiescent and operating current at high frequencies. Input pins (HI and LI) allow full and independent flexible ON-OFF state of the output.

## 6.2. Functional Block Diagram

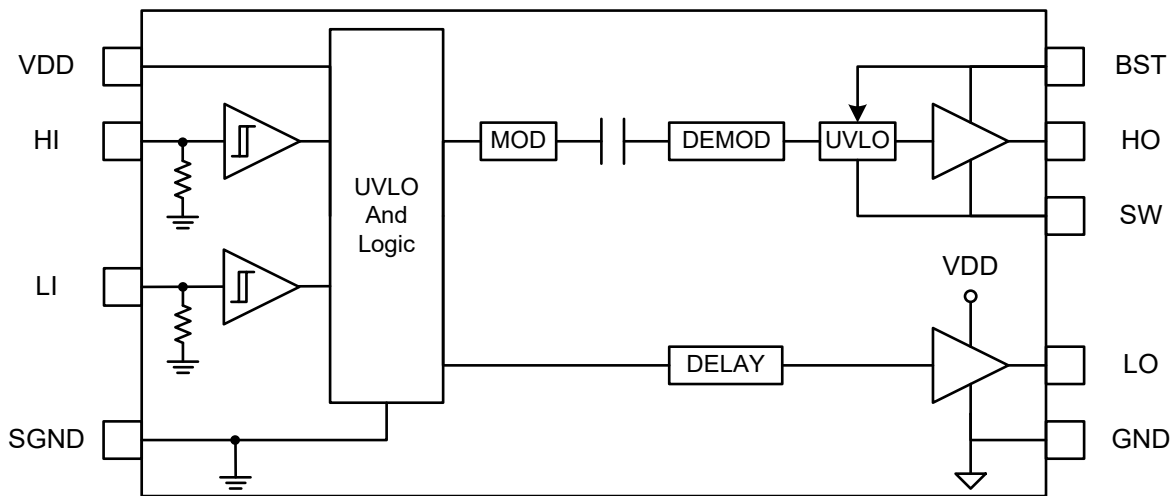


Figure 6.1 Functional Block Diagram

## 6.3. Feature Description

### 6.3.1 Under Voltage Lock Out (UVLO)

NSD1624x has independent under voltage lock out feature for both high and low side gate drivers which ensure the working of both channels at  $VDD_{UV+}$  and  $VBST_{UV+}$ . If the VDD is below the  $VDD_{UV+}$ , the output of both high and low side channel will remain low. Similarly, if the VBST is below the  $VBST_{UV+}$ , the output of high side channel will remain low. So the high side bias voltage has no influence on the low side output channel, regardless of the state of the input signal.

The VDD and VBST ULVO protection circuits have hysteresis ( $VDD_{HYS}$ ) to prevent ground noise in power supply. Hysteresis also allows small drops in supply power which are usually happen in startup.

### 6.3.2 Input Stage

NSD1624x is a low side-high side gate driver with two independent input pins HIN and LIN. Both the inputs are compatible with CMOS and TTL logic which ensures that the inputs can be driven with analog and digital controllers.

The typical value of high input threshold ( $VIN\_H$ ) is 2.1V whereas the low threshold ( $VIN\_L$ ) 1.2V. The typical value of hysteresis on input pins is 0.9V which offers higher noise immunity compared to traditional TTL logic implementations. NSD1624x also feature tight control of the input pin threshold voltage levels which ease system design consideration and ensure stable operation across temperature.

Both the input pins are internally pulled down through a resistor of 260kΩ which indicates its logic state in case of floating pin. This feature can be regarded as important because the outputs stay low in case of any input is floating. It is recommended to ground the unused input pin especially in the practical applications.

The device has dead-time control function which means the outputs will be low as soon as both inputs are high. The dead-time is about 10ns and unadaptable.

The input logic is explained in the following table.

6.3.3 Input Table

INPUTS		OUTPUTS	
LI	HI	LO	HO
L	H	L	H
H	L	H	L
H	H	L	L
L	L	L	L

6.3.4 Output Stage

NSD1624x is equipped with two independent drivers. The device has ability to provide 4A source and sink current which can effectively charge and discharge a load capacitor of 1nF in 10ns.

7. Application Note

7.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSD1624x which could be used in several popular power converter topologies such as half-bridge/full bridge/LLC isolated topologies applications.

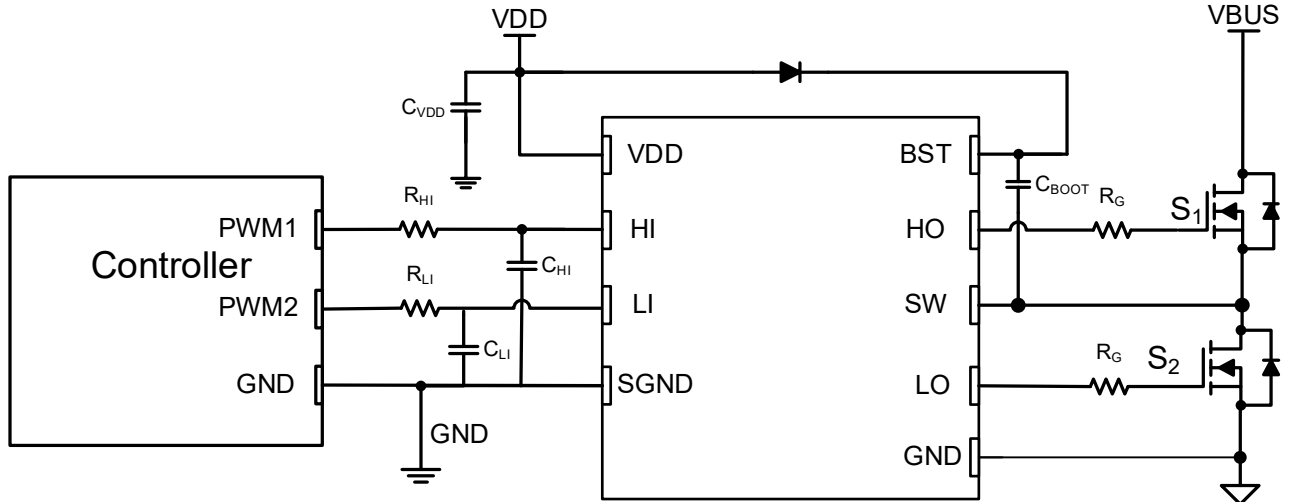


Figure 7.1 Simplified Half-Bridge Schematic

## 7.2. ESD Structure

Figure.7.2 illustrates the multiple parasitic diodes involved in the ESD protection components of NSD1624x device. For the SOP8 and LGA package, SGND and GND have been connected internally.

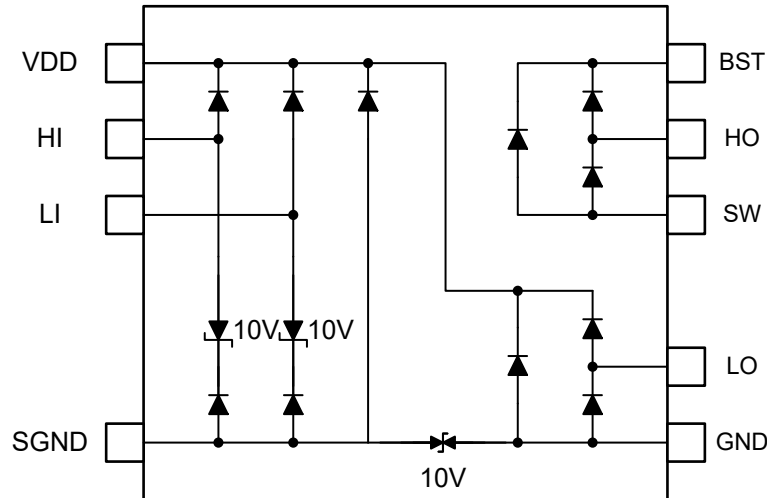


Figure 7.2 ESD Structure for SOP14

## 7.3. Layout Recommendations

PCB layout is important to get optimal performance. Some of the layout guidelines to be followed are listed below:

- High frequency switching current that charges and discharges the gate of external power transistor, that causes EMI and ringing issues. To minimize the parasitic inductance and ringing on the gate terminal of the low side MOSFET S2, keep the low side loop 'LO-S2-GND' as small as possible. Similarly, keep the path of high side driver 'HO-S1-SW' as minimum as possible.
- Place a bypass capacitor  $C_{VDD}$  as close to VDD pin as possible and minimized the path of 'VDD- $C_{VDD}$ -GND'. Similarly, follow the same rule for 'VBST- $C_{BOOT}$ -SW' loop.
- Place a RC input filter with  $R=2$  to  $5\Omega$ , &  $C=100\text{pF}$  close to the driver input pins (HI, LI)
- Use of SMD type devices with low-ESR and low-ESL capacitor are highly recommended.
- Large amount of copper should be placed at VDD, BST, GND, and SW pins for thermal dissipation.

### 8. Package information

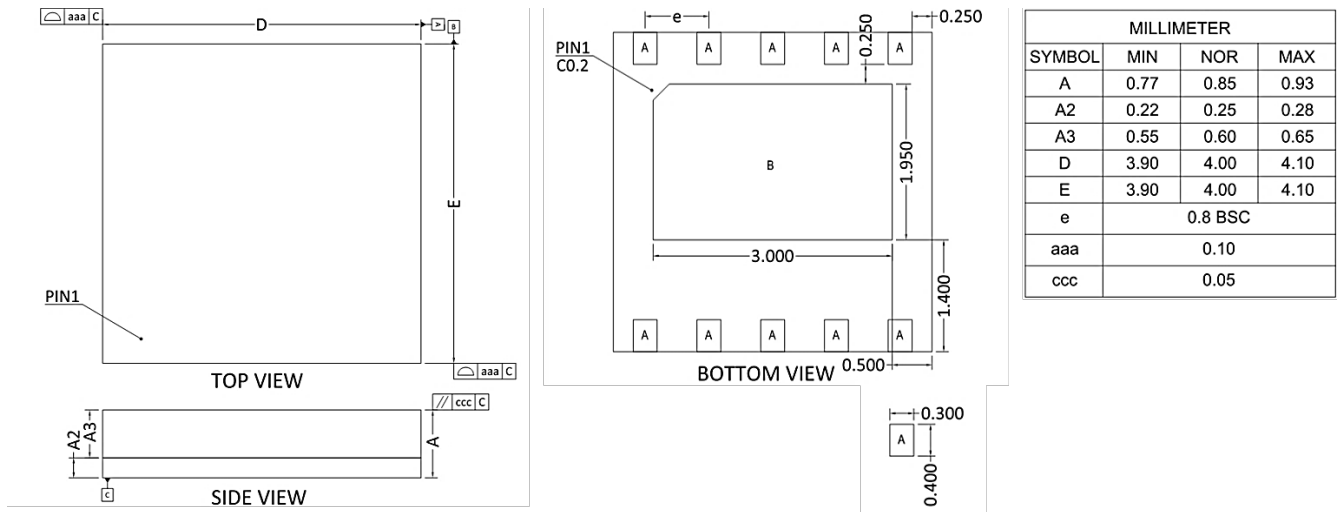
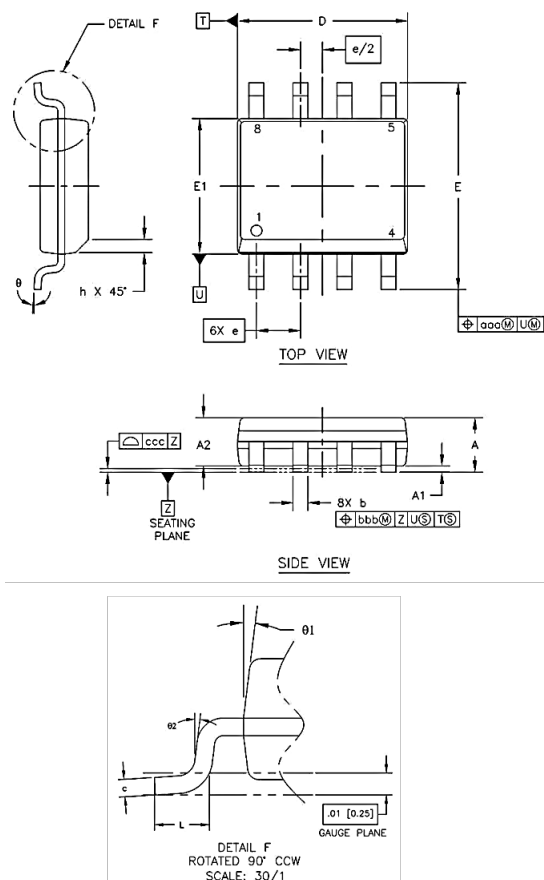
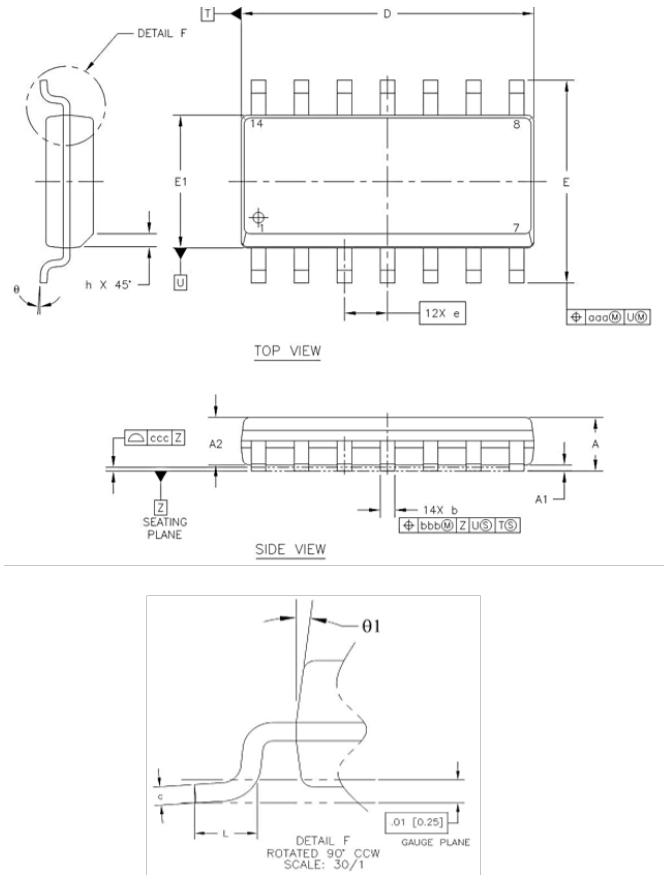


Figure 8.1 LGA10 4X4 Package Shape and Dimension



DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	1.35		1.75
STAND OFF	A1	0.10		0.25
MOLD THICKNESS	A2	1.25		---
LEAD WIDTH	b	0.35		0.49
L/F THICKNESS	c	0.19		0.25
BODY SIZE	D	4.80		5.00
	E1	3.80		4.00
	E	5.80		6.20
LEAD PITCH	e	1.27 BSC		
	L	0.40		1.25
	h	0.25		0.50
	θ	0°		7°
	θ1	5°		15°
	θ2	2°	7°	12°
LEAD EDGE OFFSET	aaa	0.25		
LEAD OFFSET	bbb	0.25		
COPLANARITY	ccc	0.10		

Figure 8.2 SOP8 Package Shape and Dimension



DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	1.35	----	1.75
STAND OFF	A1	0.10	----	0.25
MOLD THICKNESS	A2	1.25	----	----
LEAD WIDTH	b	0.33	----	0.51
L/F THICKNESS	c	0.19	----	0.25
BODY SIZE	D	8.55	----	8.75
	E1	3.80	----	4.00
	E	5.80	----	6.20
LEAD PITCH	e	1.27 BSC		
	L	0.40	----	1.27
	h	0.25	----	0.50
	$\theta$	0°	----	8°
	$\theta$ 1	5°	----	15°
LEAD EDGE TOLERANCE	aaa	0.25		
LEAD OFFSET	bbb	0.25		
COPLANARITY	ccc	0.10		

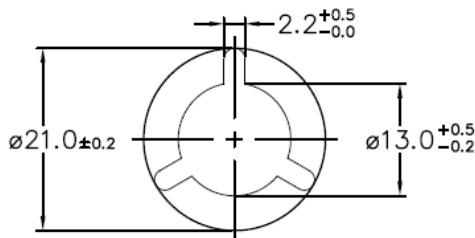
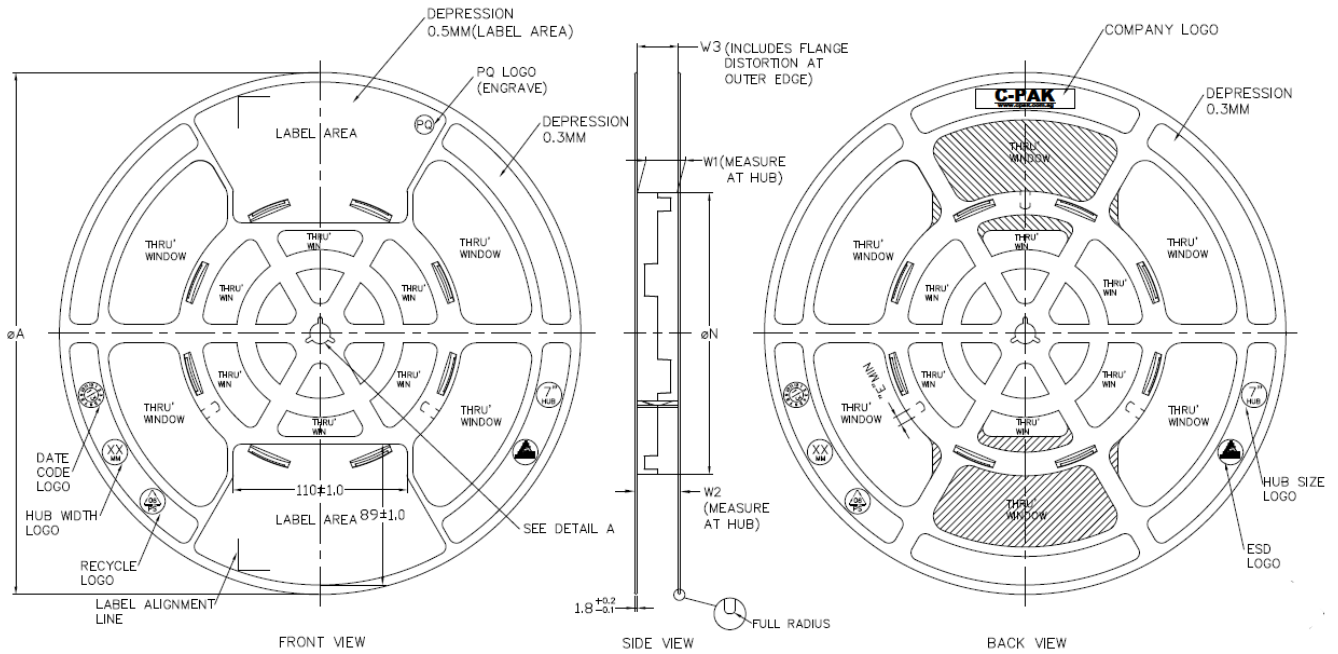
Figure 8.3 SOP14 Package Shape and Dimension



### 9. Ordering Information

Part No.	Temperature	Automotive	Package Drawing	MSL	SPQ
NSD1624-DLAJR	-40 to 125°C	NO	LGA10	3	2500
NSD1624-DSPR	-40 to 125°C	NO	SOP8	3	2500
NSD1624-DSPKR	-40 to 125°C	NO	SOP14	3	2500
NSD16241-DSPKR	-40 to 125°C	NO	SOP14	3	2500
NSD16241-DSPR	-40 to 125°C	NO	SOP8	3	2500
NSD16242-DSPR	-40 to 125°C	NO	SOP8	3	2500

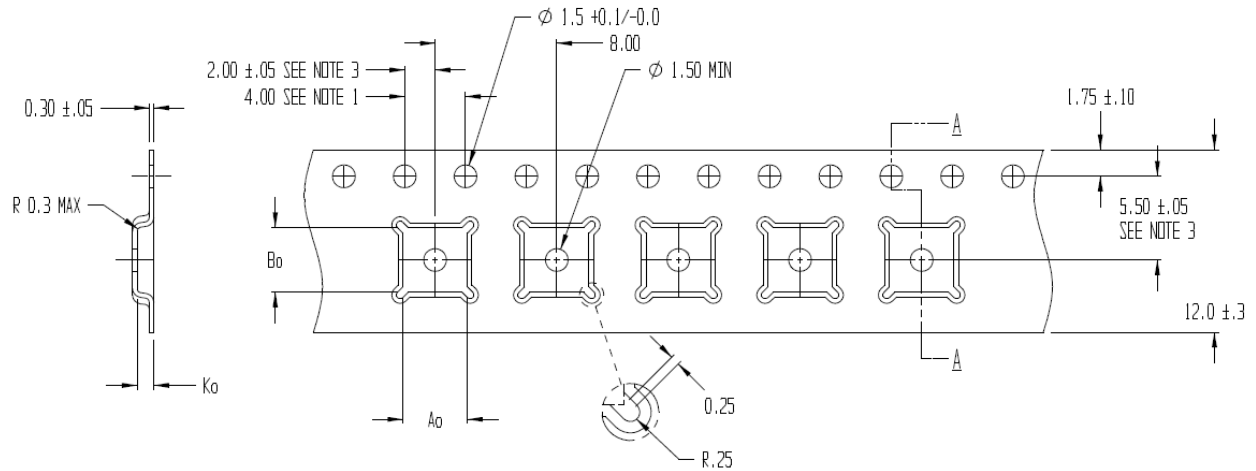
### 10. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 ±0.5/-0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ±2.0/-0.0	18.4		5.5
16MM	330	178	16.4 ±2.0/-0.0	22.4		5.5
24MM	330	178	24.4 ±2.0/-0.0	30.4		5.5
32MM	330	178	32.4 ±2.0/-0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 <sup>12</sup>	ANTISTATIC	ALL TYPES
B	10 <sup>9</sup> TO 10 <sup>11</sup>	STATIC DISSIPATIVE	BLACK ONLY
C	10 <sup>5</sup> & BELOW 10 <sup>5</sup>	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 <sup>9</sup> TO 10 <sup>11</sup>	ANTISTATIC (COATED)	ALL TYPES

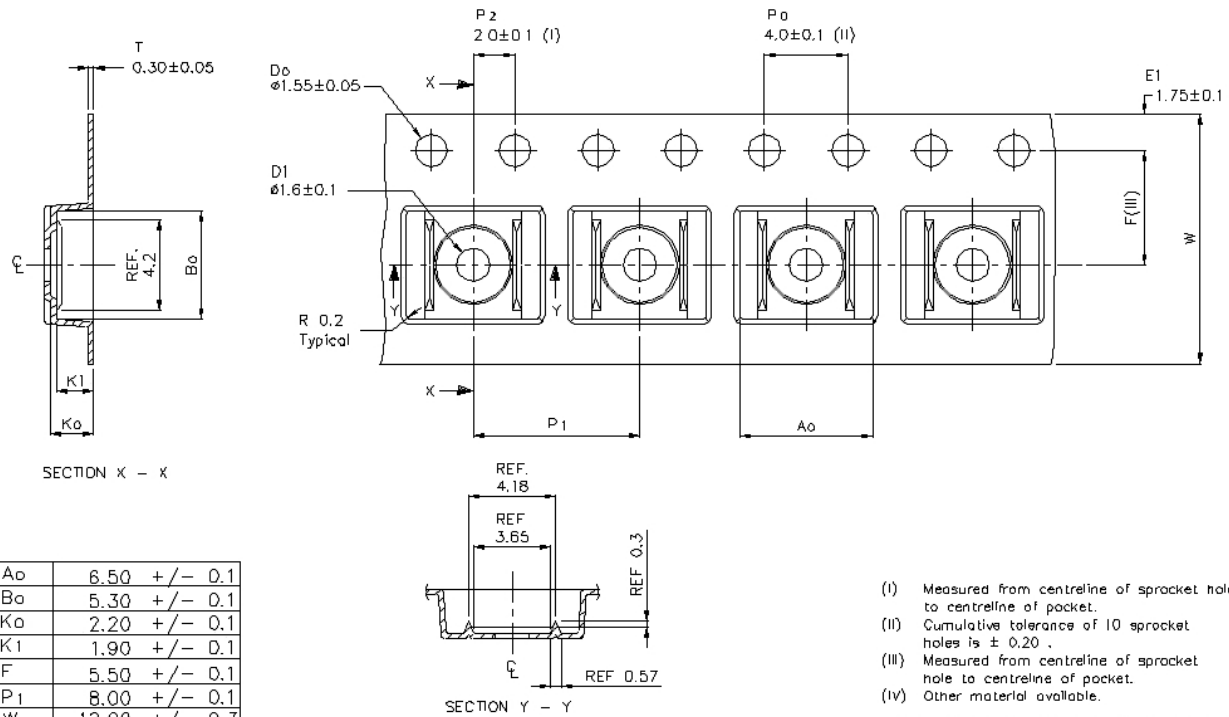
Figure 10.1 Tape Information



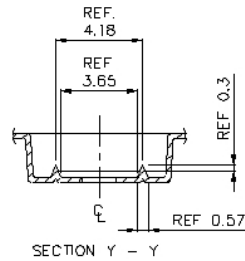
SECTION A - A

$A_0 = 4.25$   
 $B_0 = 4.25$   
 $K_0 = 1.10$

Figure 10.2 Reel information of LGA10



SECTION X - X



$A_0$	6.50	+/- 0.1
$B_0$	5.30	+/- 0.1
$K_0$	2.20	+/- 0.1
$K_1$	1.90	+/- 0.1
$F$	5.50	+/- 0.1
$P_1$	8.00	+/- 0.1
$W$	12.00	+/- 0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

Figure 10.3 Reel information of SOP8

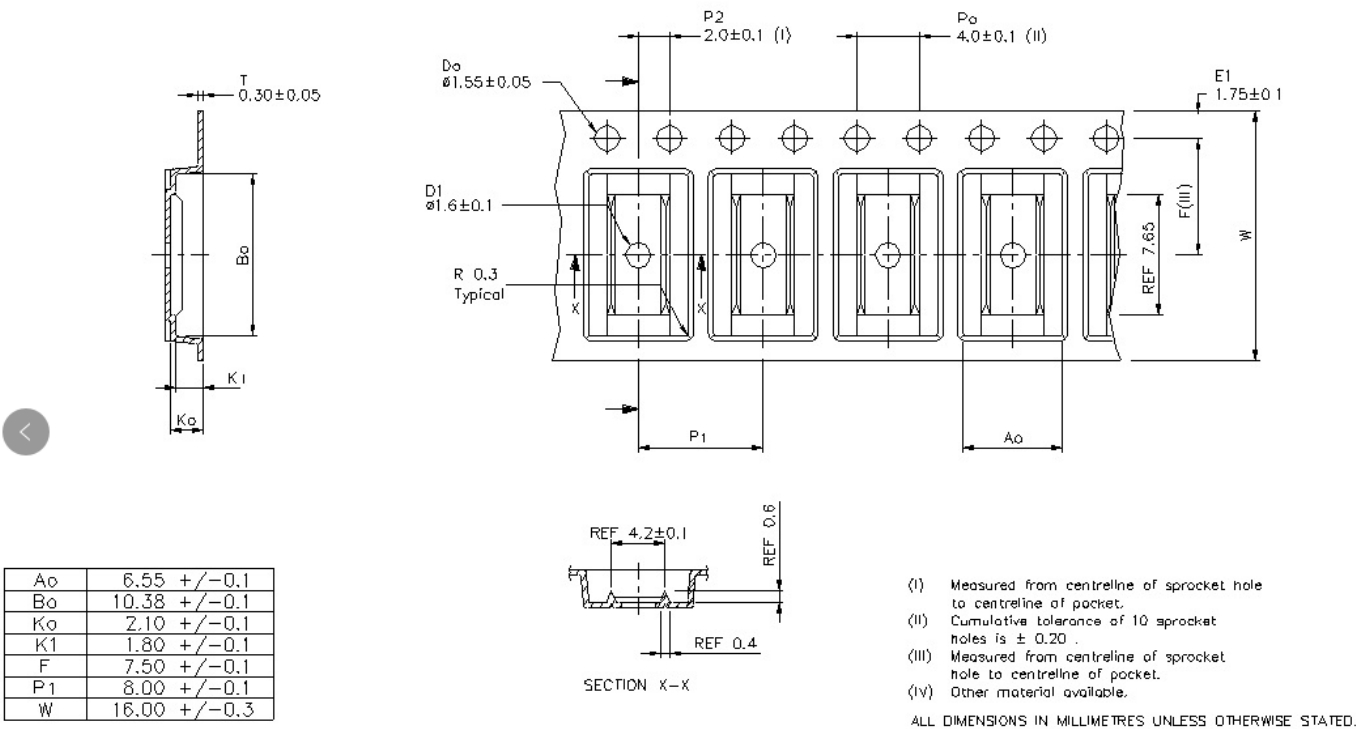


Figure 10.4 Reel information of SOP14

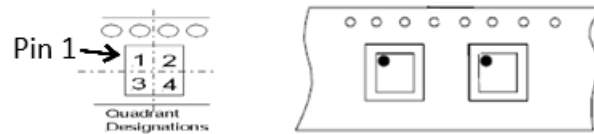


Figure 10.5 Quadrant Designation for Pin1 Orientation in Tape

## 11. Revision History

Revision	Description	Date
1.0	Initial version	2022/6/19
1.1	<ol style="list-style-type: none"><li>1. Add the notes for Pin Configuration and Description.</li><li>2. update the maximum of <math>I_{BST\_Q}</math> from 0.7mA to 0.76mA.</li><li>3. Add the part number information of NSD16241 and NSD16242.</li><li>4. The SPQ of NSD1624-DLAJR changed from 3000 to 2500 in ordering information.</li></ol>	2023/8/10

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