

IVCO1A01/2 8.5A/10A Isolated Single Channel Gate Driver

1. Features

- Split Outputs (IVCO1A01) or Miller Clamp (IVCO1A02)
- Industry standard SOIC-8 pinout supports 3.75kVrms isolation voltage with Narrow Body (D) and 5kVrms isolation voltage with Wide Body (DW) options
- 8.5A peak source and 10A peak sink drive current
- Wide driver VCC2 range up to 36V
- VCC2 UVLO protection
 - 8.4V UVLO (IVCO1A01)
 - 12V UVLO (IVCO1A02)
- 100V/ns minimum CMTI
- CMOS inputs
- 50ns typical propagation delays
- Outputs held low when floating inputs
- Safety and regulatory certifications:
 - UL (pending)
 - VDE (pending)
 - CQC (pending)
- Operating temperature range -40°C to 125°C
- AEC-Q100 qualified

2. Applications

- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- EV/HEV inverters and DC/DC converters
- PV boosters and inverters
- UPS
- Motor Control
- Emerging Wide Band-Gap Power Devices

3. Description

The IVCO1A01/2 is an AEC-Q100 qualified, 8.5A peak source and 10A peak sink single-channel isolated gate driver with 3.75kVrms (D) and 5kVrms (DW) isolation. It is capable of effectively and safely driving SiC/Si MOSFETs and Si IGBTs. Low propagation delay and compact SOIC-8 package enables MOSFETs to switch at hundreds of kHz.

Wide output VCC2 operating range from 9.5V to 33V enables effective driving with Si or SiC MOSFET and IGBT power switches. Integrated UVLO protection ensures output held at low under abnormal conditions. The input VCC1 operates from 2.5V to 5.5V, which supports most digital controllers.

With integrated isolation barrier, IVCO1A01/2 can support isolation up to 3.75kVrms (D) and 5kVrms (DW). It is very convenient to control MOSFET/IGBT gate drive across isolation barrier or with level shifting.

Device Information

PART NUMBER	PACKAGE	PACKING
IVCO1A01DQR	SOIC-8	Tape and Reel
IVCO1A01DWQR	SOIC(W)-8	Tape and Reel
IVCO1A02DQR	SOIC-8	Tape and Reel
IVCO1A02DWQR	SOIC(W)-8	Tape and Reel

Pin Configuration

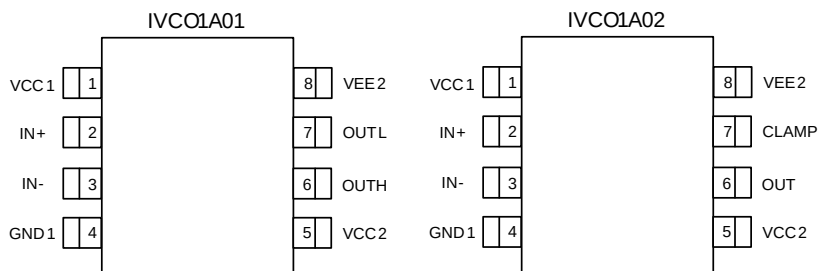


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4. Pin Configuration and Functions

IVCO1A01	IVCO1A02	NAME	I/O	DESCRIPTION
1	1	VCC1	P	Input Power Supply
2	2	IN+	I	Positive Input
3	3	IN-	I	Negative Input
4	4	GND1	G	Input Ground
5	5	VCC2	P	Output Power Supply
6	/	OUTH	O	Pull High Output
7	/	OUTL	O	Pull Low Output
/	6	OUT	O	Output
/	7	CLAMP	I/O	Active Miller Clamp
8	8	VEE2	G	Output Ground

Truth Table

IVCO1A01

VCC1	IN+	IN-	VCC2	OUTH	OUTL
X	X	X	below UVLO	High impedance	L
below UVLO	X	X	X	High impedance	L
above UVLO	L or floating	X	above UVLO	High impedance	L
above UVLO	X	H or floating	above UVLO	High impedance	L
above UVLO	H	L	above UVLO	H	High impedance

IVCO1A02

VCC1	IN+	IN-	VCC2	OUT	CLAMP
X	X	X	below UVLO	L	L
below UVLO	X	X	X	L	L
above UVLO	L or floating	X	above UVLO	L	L
above UVLO	X	H or floating	above UVLO	L	L
above UVLO	H	L	above UVLO	H	High impedance

5. Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC1}	Input supply voltage (reference to GND1)	-0.3	7	V
IN+, IN-	Signal input voltage	-0.3	V _{CC1} +0.3	V
V _{CC2}	Output supply voltage (reference to VEE2)	-0.3	36	V
OUTH, OUTL	Gate driver output voltage	-0.3	V _{CC2} +0.3	V
OUT	Gate driver output voltage	-0.3	V _{CC2} +0.3	V
CLAMP	Miller Clamp input voltage	-0.3	V _{CC2} +0.3	
T _J	Junction temperature	-40	150	°C
T _{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

		Value	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), AEC Q100-002	+/-6000	V
	Charged-device model (CDM), AEC Q100-011	+/-2000	

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V _{CC1}	Input supply voltage	2.5	5.5	V
V _{INx}	Input voltage	0	V _{CC1}	V
V _{CC2}	IVCO1A01 output supply voltage	9.5	33	V
V _{CC2}	IVCO1A02 output supply voltage	13.2	33	V
T _A	Ambient temperature	-40	125	°C

5.4 Thermal Information

		D	DW	UNIT
R _{θJA}	Junction-to-Ambient	110	100	°C/W
ψ _{JT}	Junction-to-Top characterization parameter	18	16	°C/W

5.5 Electrical Specifications

Unless otherwise noted, $V_{CC1} = 3.3\text{ V}$, $V_{CC2} = 15\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C

Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT					
I_{CC1q} V_{CC1} quiescent current	$IN+=0V$, $IN-=0V$.		0.8	1.2	mA
I_{CC2q} V_{CC2} quiescent current	$IN+=0V$, $IN-=0V$.		1.8	2.7	mA
UVLO (VCC1)					
V_{ON}	V_{CC1} Rising threshold	2.0	2.2	2.4	V
V_{OFF}	V_{CC1} Falling threshold	1.9	2.07	2.25	V
IVCO1A01 UVLO (VCC2)					
V_{ON} Under voltage	V_{CC2} Rising threshold		8.4	9.4	V
V_{OFF} thresholds	V_{CC2} Falling threshold	7.1	7.9		V
IVCO1A02 UVLO (VCC2)					
V_{ON}	V_{CC2} Rising threshold		12	13	V
V_{OFF}	V_{CC2} Falling threshold	9.8	10.8		V
INPUT					
V_{INH} Input rising threshold			$0.5 \cdot V_{CC1}$	$0.6 \cdot V_{CC1}$	V
V_{INL} Input falling threshold		$0.3 \cdot V_{CC1}$	$0.35 \cdot V_{CC1}$		V
OUTPUTS					
I_{OH} Peak source current	$C_{LOAD} = 1\mu\text{F}$, with external current limiting resistors, 1kHz switching frequency		8.5		A
I_{OL} Peak sink current	$C_{LOAD} = 1\mu\text{F}$, with external current limiting resistors, 1kHz switching frequency		10		A
V_{OH} Output high voltage	$I_{OUTH} = -20\text{mA}$		$V_{CC}-0.09$	$V_{CC}-0.17$	V
V_{OL} Output low voltage	$I_{OUTL} = 20\text{mA}$		8	23	mV
R_{OH} Output static pull-up resistance			4.4	8.6	Ω
R_{OL} Output pull-down resistance			0.4		Ω
IVCO1A02 ACTIVE MILLER CLAMP					
$I_{CLAMP}^{(*)}$ Clamp current	$V_{CLAMP} = V_{EE2}+2V$		10		A
V_{CLAMP} Clamp low voltage	$I_{CLAMP} = 20\text{mA}$		7		mV
$V_{CLAMP-TH}$ Clamp threshold voltage			2.1	2.3	V
Timing					
TD_r Output rising delay	$C_{LOAD} = 1.8\text{nF}$		50	65	ns
TD_f Output falling delay			50	65	ns
T_r Rise time	$C_{LOAD} = 1.8\text{nF}$		10	15	ns
T_f Fall time			10	14	ns
T_{PWD} Pulse Width Distortion	$C_{LOAD} = 1.8\text{nF}$		1		ns
$CMTI^{(*)}$		100			V/ns
ACTIVE PULLDOWN					
V_{OPD} Active Pull Down	$I_{OUT} = 0.1 \cdot I_{OUTL(typ)}$, $V_{CC2}=\text{open}$		2	2.5	V

(*) Guaranteed by design

5.6 Insulation and Safety Related Specifications

PARAMETER		TEST CONDITIONS	D	DW	UNIT
	Rated Dielectric Insulation Voltage	1-minute duration	3750	5000	V _{RMS}
CLR	External Clearance	Measured from input terminals to output terminals, shortest distance through air	≥4	≥8	mm
CPG	External Creepage	Measured from input terminals to output terminals, shortest distance alone body	≥4	≥8	mm
	Internal Clearance	Insulation distance through insulation	≥21	≥21	μm
CTI	Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	>400	>400	V
	Material Group	IEC 60664-1	II	II	
R _{IO} -R _s	Isolation Resistance (Input to Output)		10 ¹²	10 ¹²	Ω
C _{IO}	Barrier Capacitance (Input to Output)	Freq = 1 MHz	1.5	1.5	pF
	Installation Classification per DIN VDE 0110	For rated mains voltage < 150 VRMS	I to IV	I 至 IV	
		For rated mains voltage < 300 VRMS	I to IV	I 至 IV	
		For rated mains voltage < 600 VRMS	NA	I 至 III	
		For rated mains voltage <1000 VRMS	NA	I 至 II	
	Climatic Classification		40/125/21	40/125/21	
	Pollution Degree per DIN VDE 0110, Table 1		2	2	
V _{IORM}	Maximum Working Insulation Voltage		1200	1200	V _{PK}
V _{IOTM}	Maximum Transient Isolation Voltage		5300	7071	V _{PK}
V _{IOSM}	Maximum Surge Isolation Voltage	Basic isolation, 1.2/50 μs combination wave	5300	5000	V _{PK}
V _{pd(m)}	Input to Output Test Voltage, Method B1	V _{IORM} × 1.5 = V _{pd(m)} , 100% production test, t _{ini} = t _m = 1 s, partial discharge < 5 pC	1800	1800	V _{PK}
V _{pd(m)}	Input to Output Test Voltage, Method A: After Environmental Tests Subgroup 1	V _{IORM} × 1.3 = V _{pd(m)} , 100% production test, t _{ini} = 60 s, t _m = 10 s, partial discharge < 5 pC	1560	1560	V _{PK}
V _{pd(m)}	Input to Output Test Voltage, Method A: After Input and/or Safety Test Subgroup 2 and Subgroup 3	V _{IORM} × 1.2 = V _{pd(m)} , 100% production test, t _{ini} = 60 s, t _m = 10 s, partial discharge < 5 pC	1440	1440	V _{PK}
T _s	Maximum Safety Temperature		150	150	°C
R _s	Isolation Resistance at T _s	V _{IO} = 500 V, T _a = 25°C	> 10 ¹²	> 10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _a ≤ 25°C	> 10 ¹¹	> 10 ¹¹	Ω
		V _{IO} = 500 V, T _a = 150°C	> 10 ⁹	> 10 ⁹	Ω

5.7 Regulatory Information

Regulatory	D	DW
UL	Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 3750V _{RMS} Isolation Voltage	Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 5000V _{RMS} Isolation Voltage
VDE	DIN EN IEC 60747-17 (VDE 0884- 17):2021-10 ² Basic Insulation, V _{IORM} =1200V _{PK} , V _{IOSM} = 5000V _{PK}	DIN EN IEC 060747-17(VDE 0884- 17):2021-10 ² Basic insulation, VIORM = 1200V _{PK} , VIOSM = 5000V _{PK}
CQC	Certified under GB4943.1-2022 Basic insulation at 557V _{RMS} (787V _{PK})	Certified under GB4943.1-2022 Basic insulation at 1118V _{RMS} (1580V _{PK}) Reinforced insulation at 557V _{RMS} (787V _{PK})

- (1) In accordance with UL 1577, each IVCO1A0xD is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec, and IVCO1A0xDW is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
- (2) In accordance with VDE 0884-17, each IVCO1A0x is proof tested by applying an insulation test voltage ≥ 1800 V rms for 1 sec.

6. Typical Characteristics

VCC1=2.5VDC±3% or 3.3VDC±10% or 5VDC±10%, 0.1uF capacitor from VCC1 to GND1, VCC2 = 15VDC±10%, 1uF capacitor from VCC2 to VEE2, CLOAD =1nF. TA = -40°C to 125°C (Unless otherwise noted).

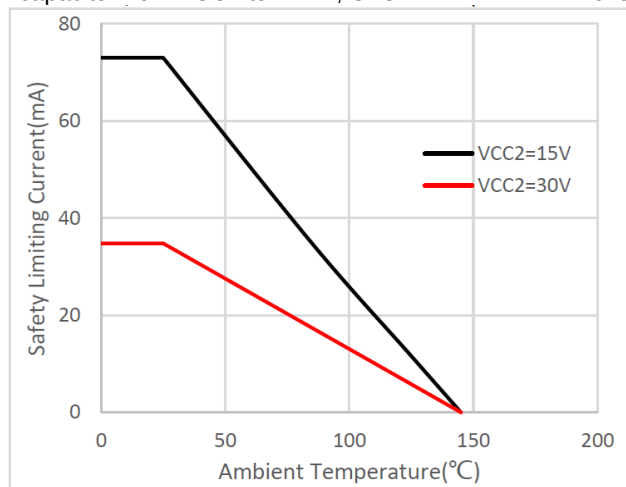


Figure 1. Thermal Derating Curve for Limiting Current with Ambient Temperature per VDE (D)

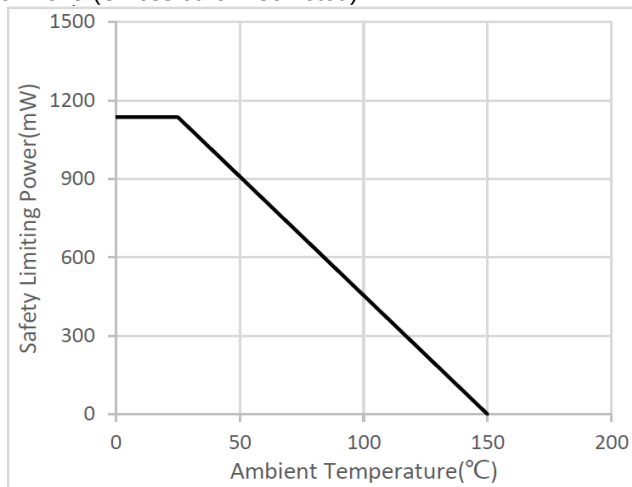


Figure 2. Thermal Derating Curve for Limiting Power with Ambient Temperature per VDE (D)

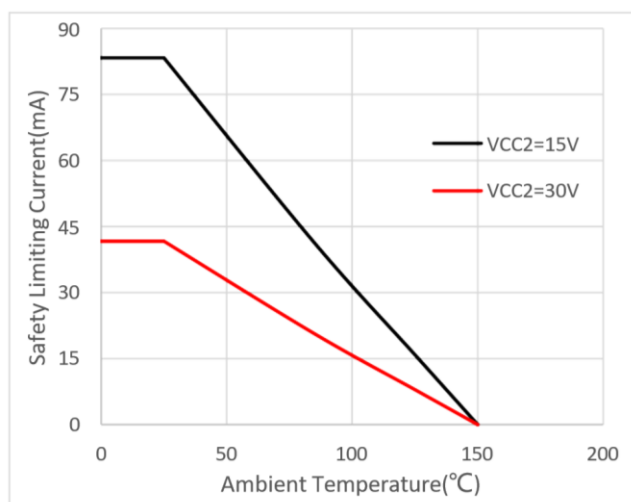


Figure 3. Thermal Derating Curve for Limiting Current with Ambient Temperature per VDE (DW)

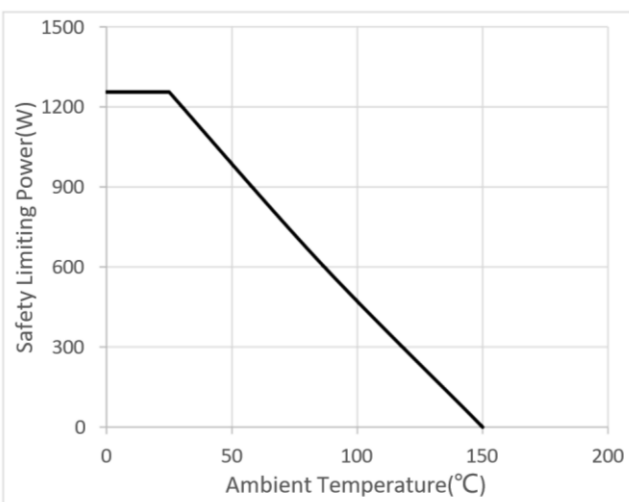


Figure 4. Thermal Derating Curve for Limiting Power with Ambient Temperature per VDE (DW)

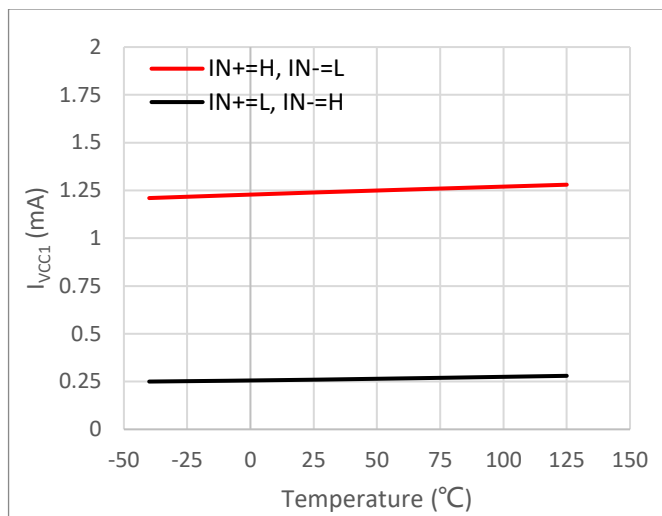


Figure 5. I_{VCC1} Supply Current vs Temperature

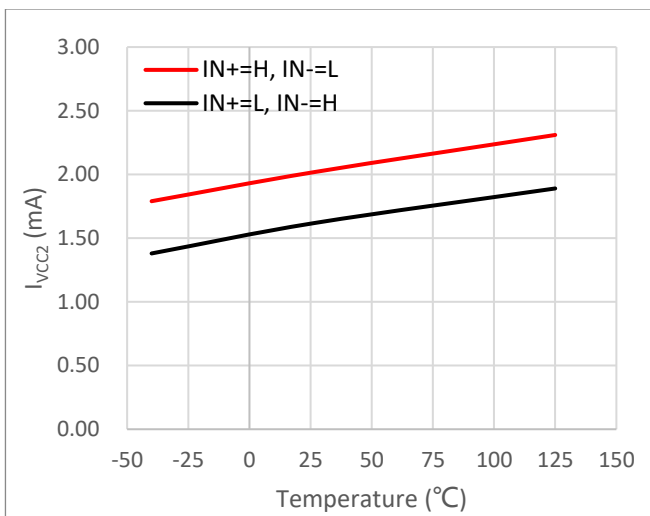


Figure 6. I_{VCC2} Supply Current vs Temperature

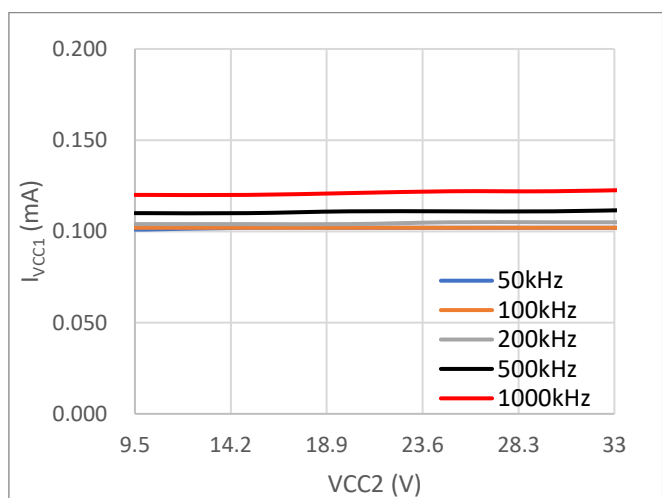


Figure 7. I_{VCC1} Supply Current vs Input Frequency

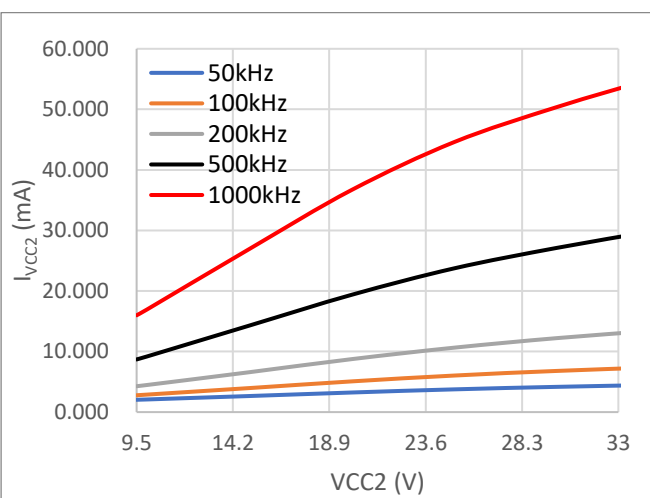


Figure 8. I_{VCC2} Supply Current vs Input Frequency

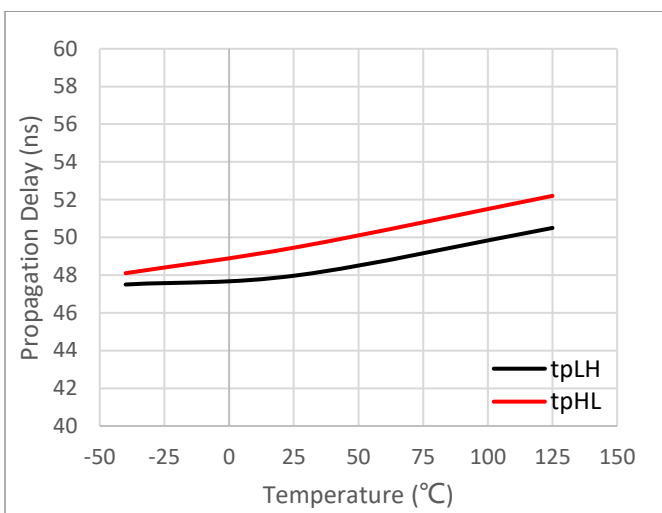


Figure 9. Propagation Delay vs Temperature

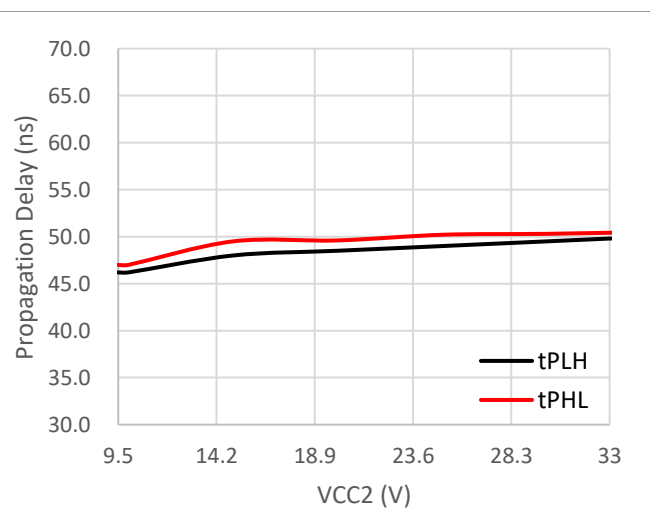


Figure 10. Propagation Delay vs VCC2

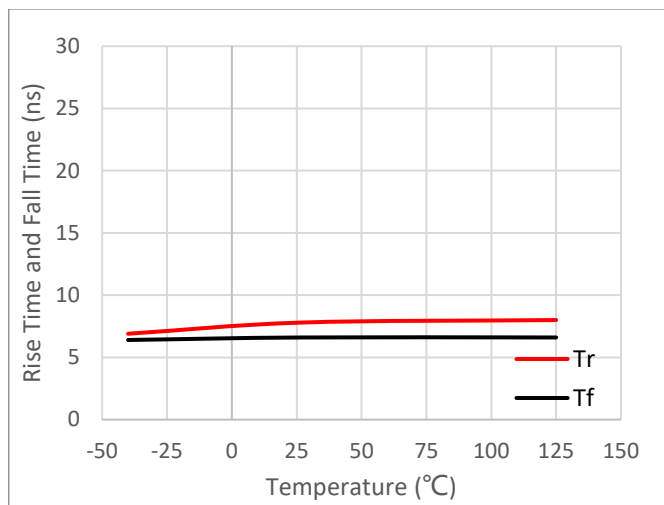


Figure 11. Rise Time and Fall Time vs Temperature

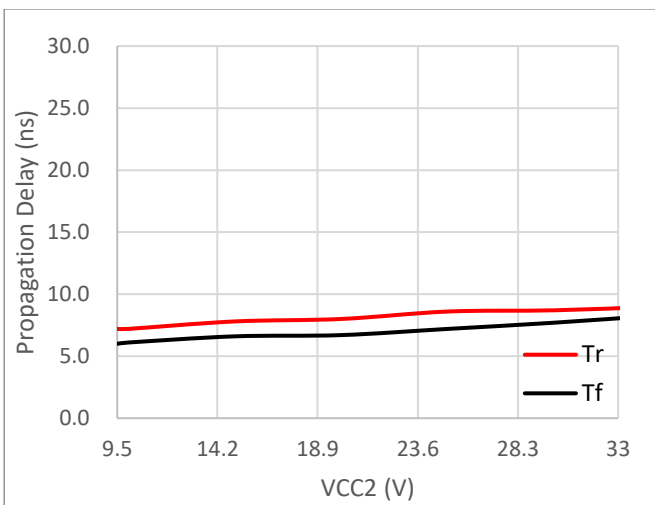


Figure 12. Rise Time and Fall Time vs VCC2

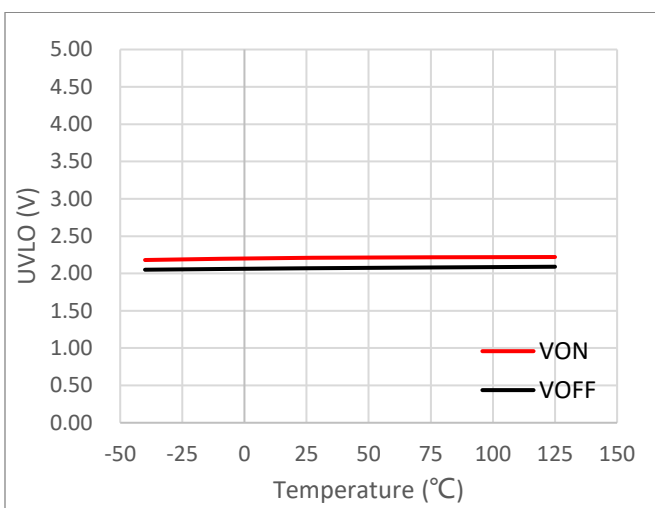


Figure 13. UVLO of VCC1 vs Temperature

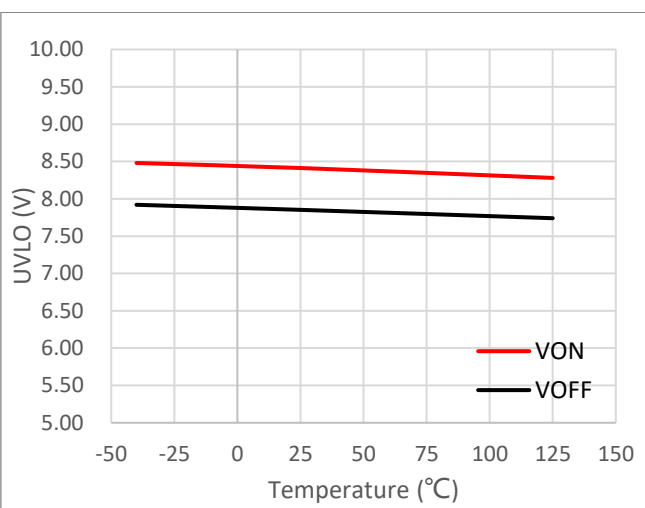


Figure 14. UVLO of VCC2 vs Temperature (IVCO1A01)

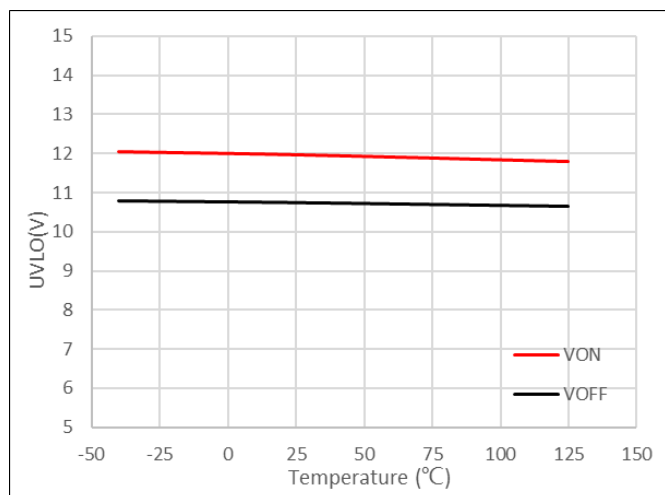


Figure 15. UVLO of VCC2 vs Temperature (IVCO1A02)

7. Detail Descriptions

IVCO1A01/2 driver is single-channel isolated gate driver with 3.75kVrms (D) and 5kVrms (DW) insulation voltage. IVCO1A01 features split outputs which make pull-up and pull-down capabilities independently adjustable. IVCO1A02 features active miller clamp.

7.1 Input Signals

IN+ and IN- are non-inverting and inverting logic gate driver inputs. The pins have a weak pulldown or pullup. When left floating, outputs are pulled to VEE2. The input is a TTL and CMOS logic level with maximum 7V input tolerance.

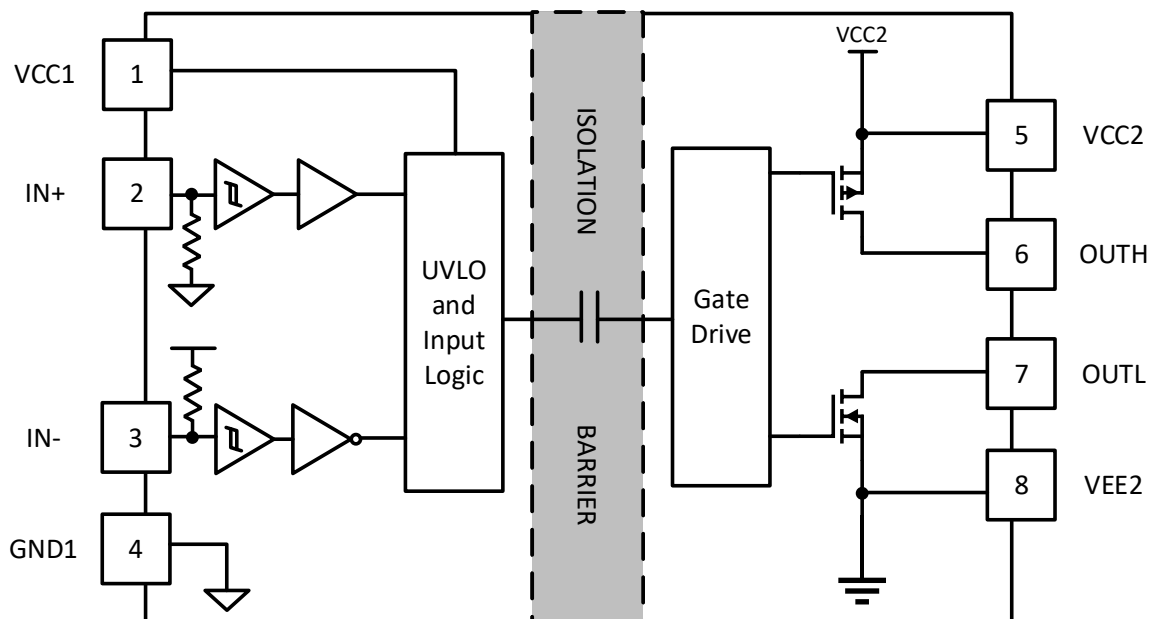


Figure 16. IVCO1A01 Function Block Diagram

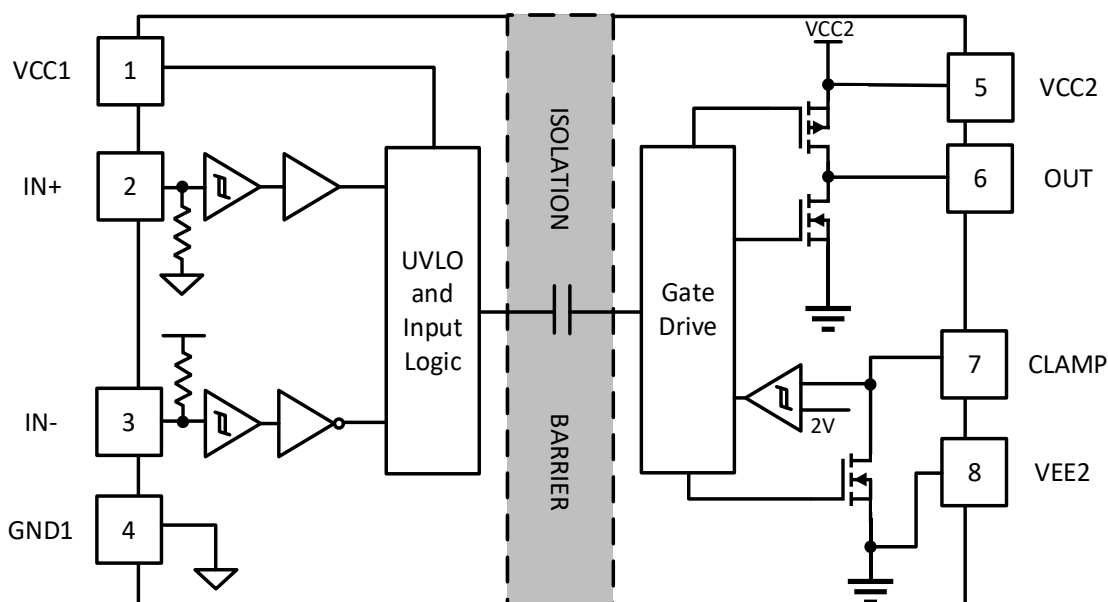


Figure 17. IVCO1A02 Function Block Diagram

7.2 Output Signals

OUTH and OUTL are split outputs. OUTH consists of a hybrid pullup and OUTL consists of an N-channel MOSFET for pulldown. Each output stage in IVCO1A01/2 can supply 8.5A peak source and 10A peak sink current pulses. The output voltage swings between VCC2 and VEE2 providing rail-to-rail operation. The presence of the MOSFET body diodes also offers voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

7.3 VCC and Under Voltage Protection

IVCO1A01/2 maximum VCC1 voltage rating is 7V. The VCC1 internal under voltage lockout (UVLO) protection threshold voltage is 2.2V typical, which enables the input stage working with 2.5V, 3.3V or 5V supply voltages. When VCC1 level is below UVLO (VCC1) threshold, this device holds the output LOW, regardless of the status of the inputs.

IVCO1A01/2 maximum VCC2 voltage rating is 36V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The output stage has VCC2 internal under voltage lockout (UVLO) protection feature. When VCC2 level is below UVLO (VCC2) threshold, this circuit holds the output LOW, regardless of the status of the inputs.

7.4 Isolation and CMTI

IVCO1A01/2 provides insulation withstand voltage 3.75kVrms (D) and 5kVrms (DW) with SOIC-8 narrow body package. This device is designed with capacitive isolation technique. The common-mode transient immunity (CMTI) 100V/ns ensures error-free operation when high dv/dt is present.

7.5 CMTI Measurement

Common mode transient immunity (CMTI), which can be distinguished between static and dynamic CMTI, is defined as the maximum tolerable rate of rise and fall of the common mode voltage applied between two isolated circuits. The measurement principle of the CMTI test is shown in figure 17.

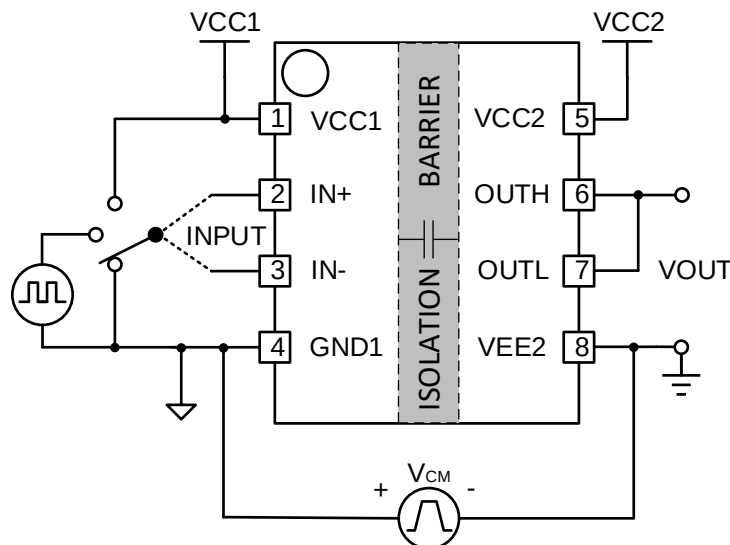


Figure 18. Common-mode transient immunity (CMTI) measurement

8. Application Implementation

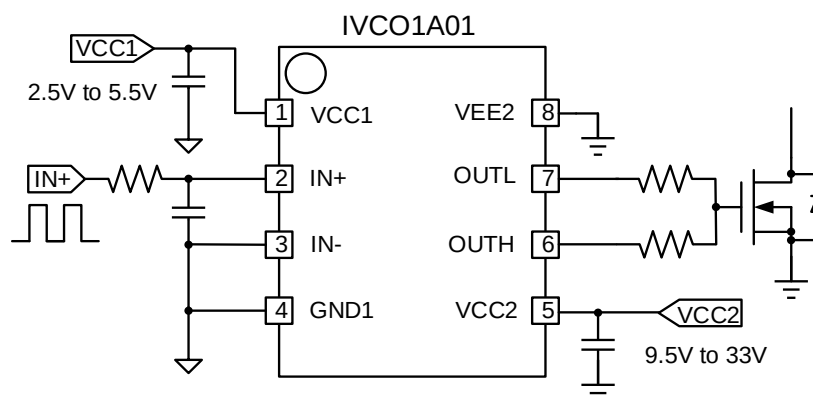


Figure 19. Typical application circuit with IN+ input (IVCO1A01)

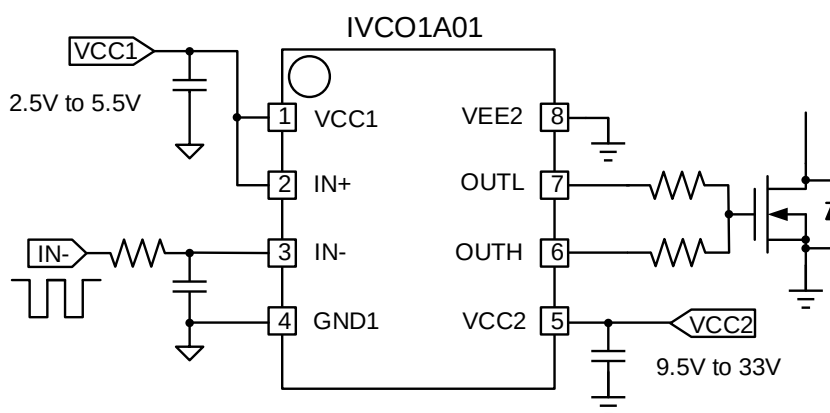


Figure 20. Typical application circuit with IN- input (IVCO1A01)

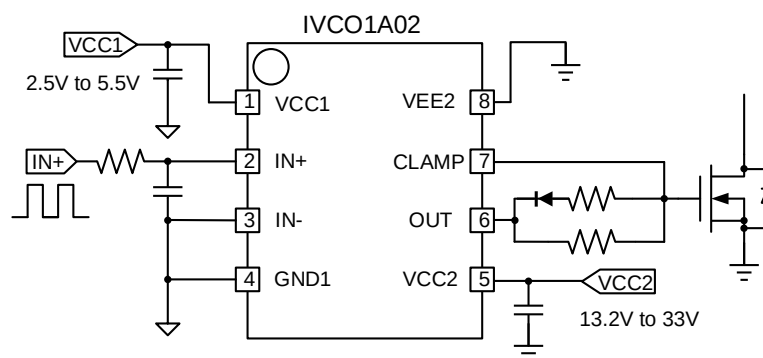


Figure 21. Typical application circuit with IN+ input (IVCO1A02)

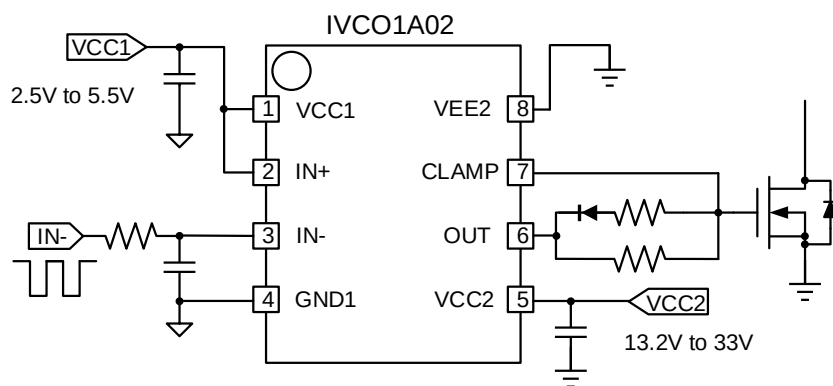


Figure 22. Typical application circuit with IN- input (IVCO1A02)

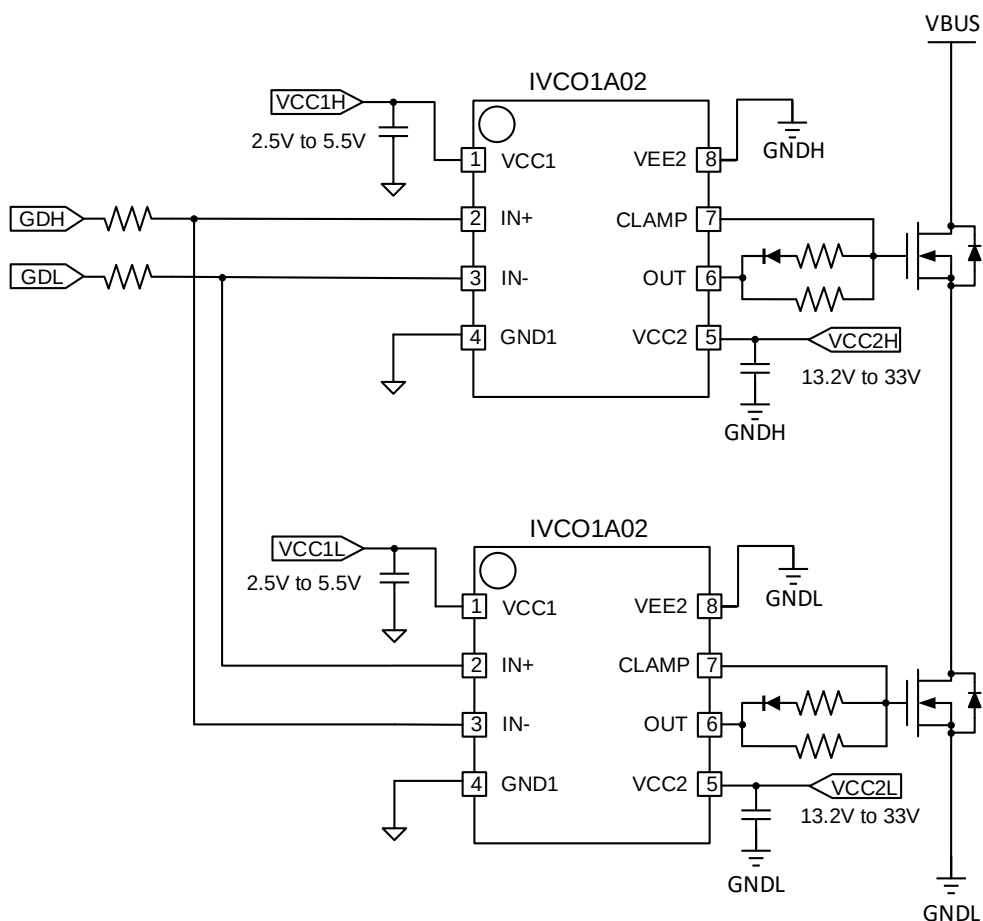


Figure 23. Typical half bridge application circuit

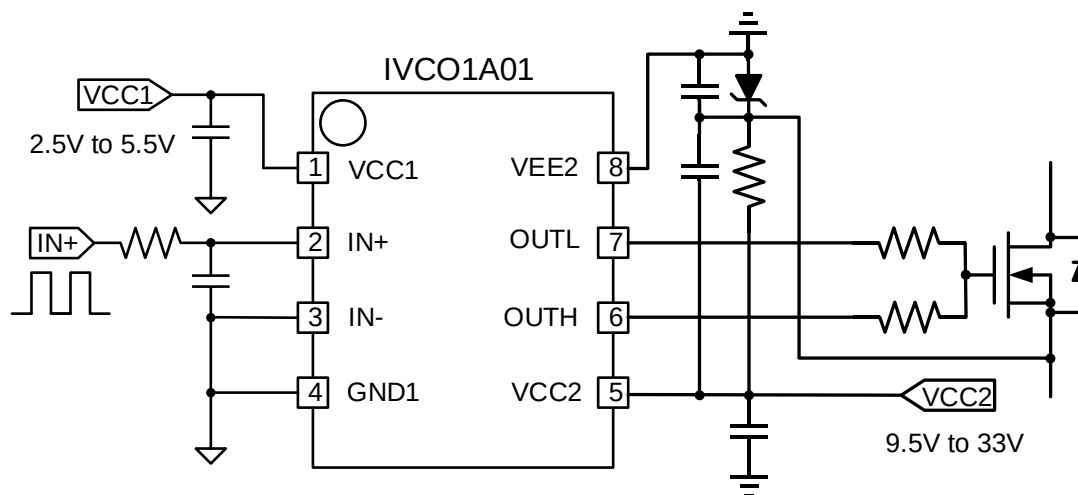


Figure 24. Typical negative bias with Zener diode (IVCO1A01)

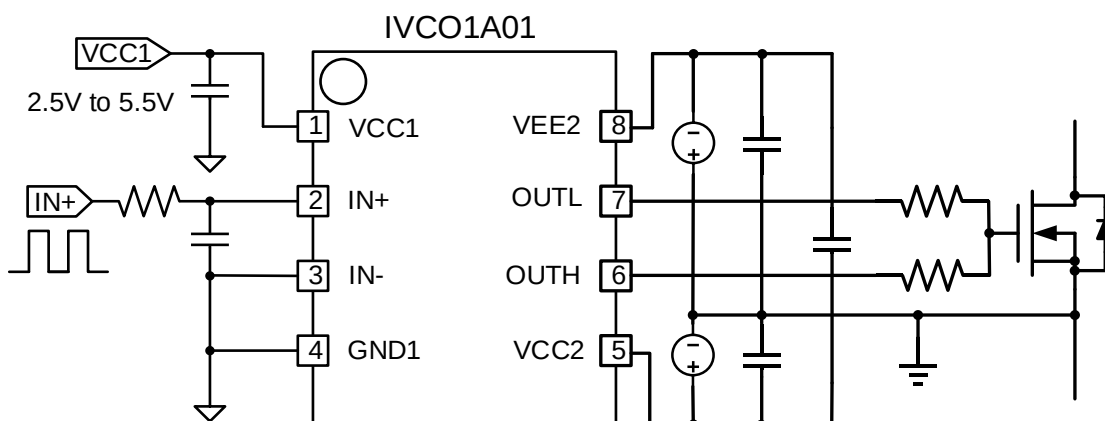


Figure 25. Typical negative bias with two isolated power supplies (IVCO1A01)

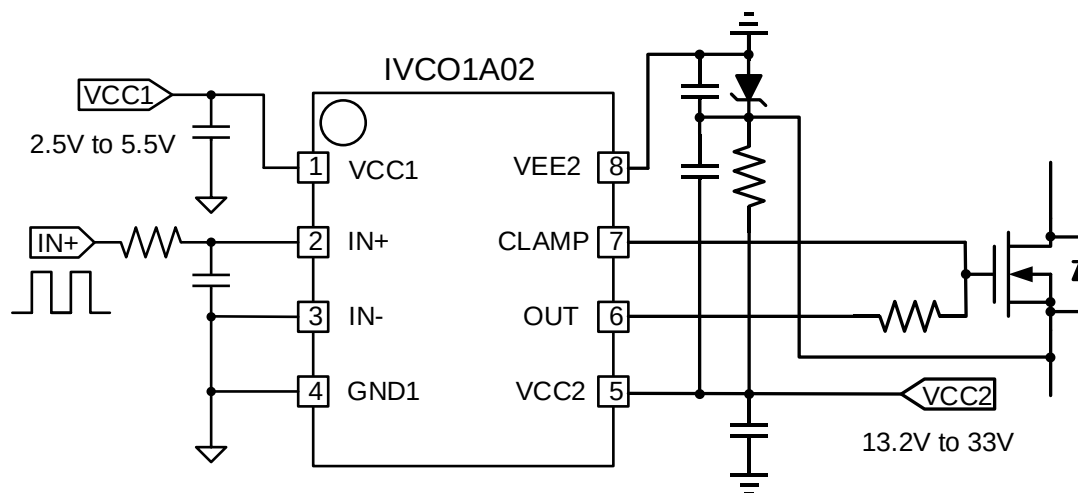


Figure 26. Typical negative bias with Zener diode (IVCO1A02)

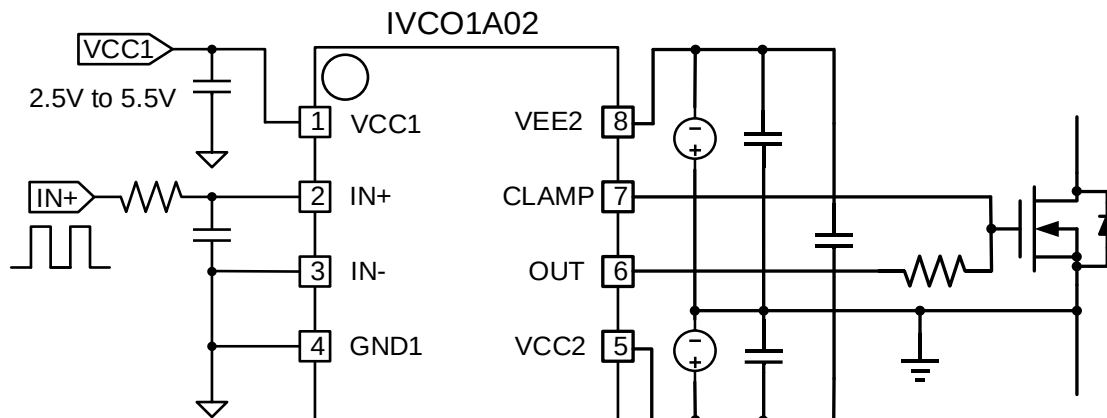


Figure 27. Typical negative bias with two isolated power supplies (IVCO1A02)

9. Layout

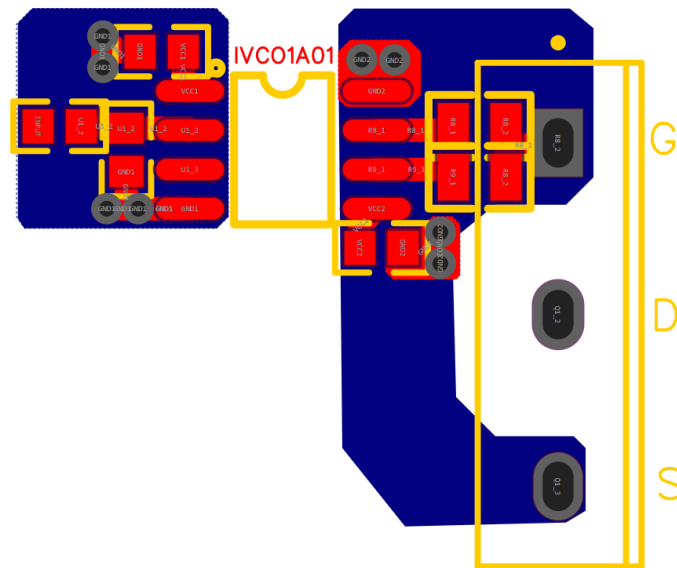


Figure 28. Layout Example for IVCO1A01DR

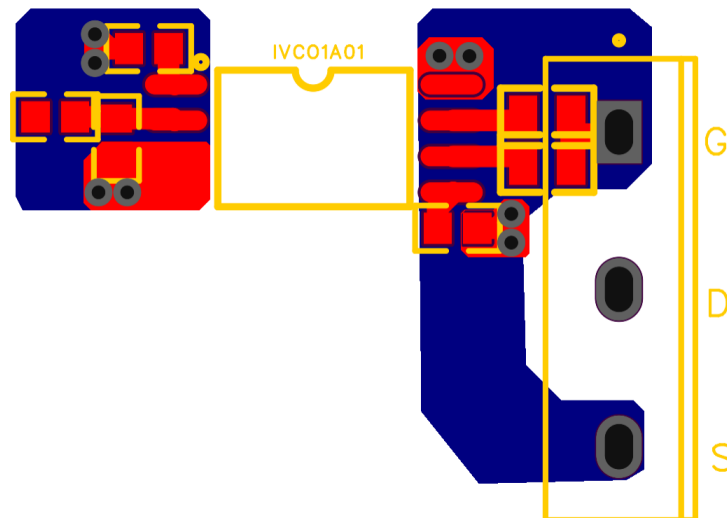
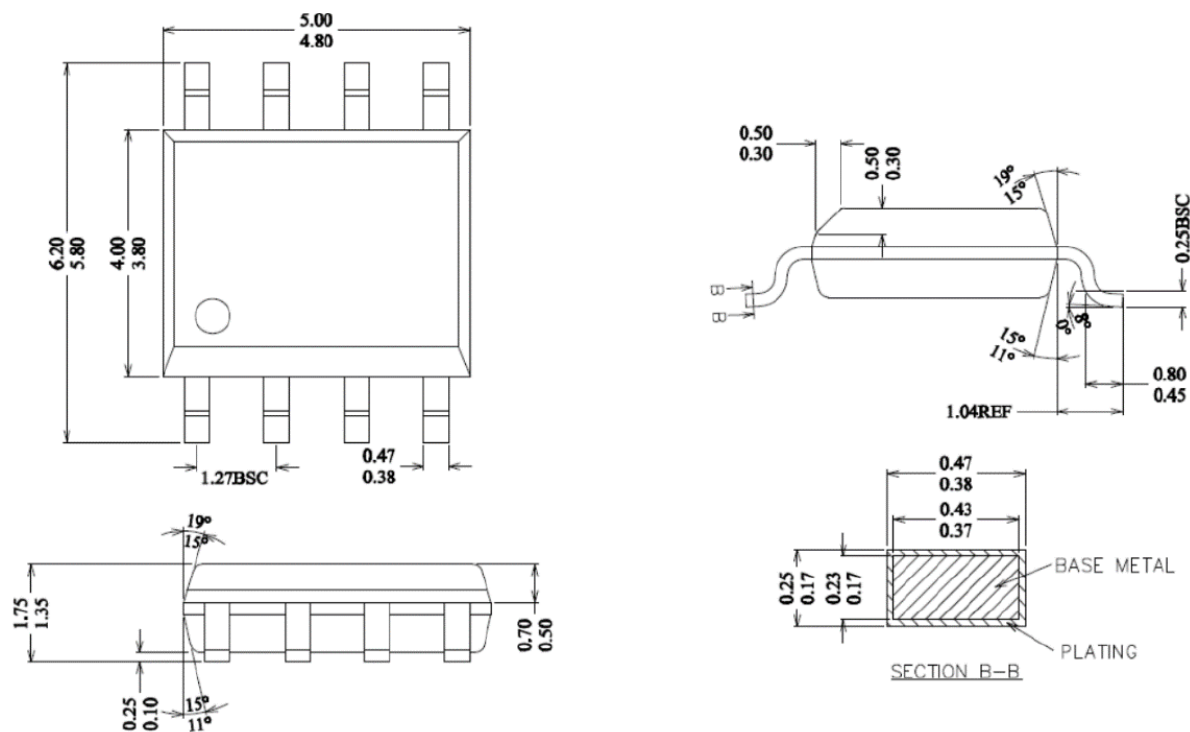


Figure 29. Layout Example for IVCO1A01DWR

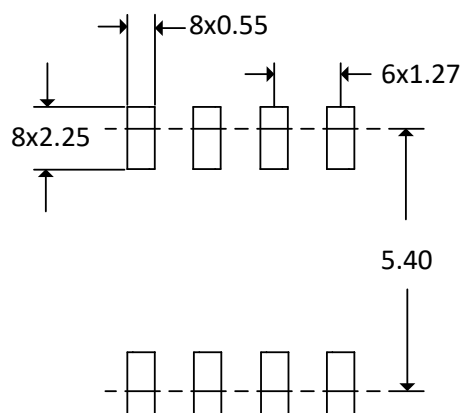
10. Package Information

8-Lead Narrow Body SOIC [D]



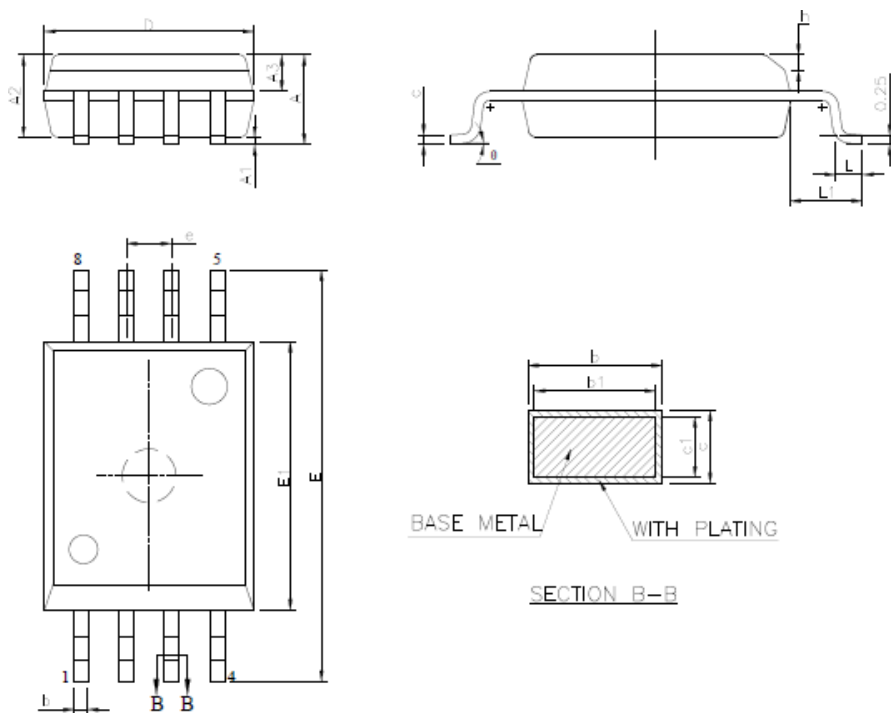
NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

SOIC-8 Package Dimensions (mm)



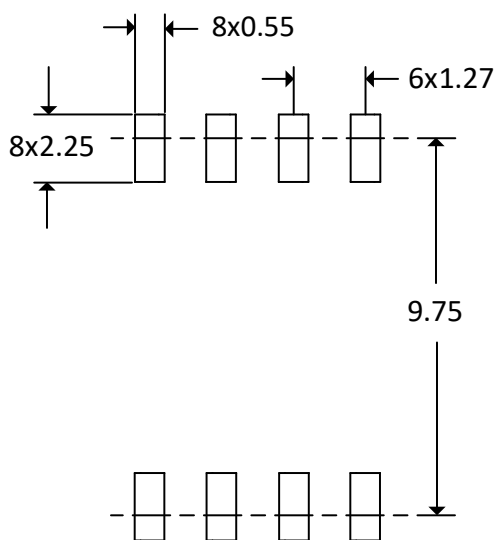
SOIC-8 Recommended Soldering Dimensions (mm)

8-Lead Wide Body SOIC [DW]



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	1.00
L1	2.00REF		
ø	0	-	8°

SOIC(W)-8 Package Dimensions (mm)



SOIC(W)-8 Recommended Soldering Dimensions (mm)

单击下面可查看定价，库存，交付和生命周期等信息

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