GENERAL DESCRIPTION

OB2276A is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2276A.

OB2276A offers complete protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), Brownout protection, VDD over voltage protection (OVP), over temperature protection (OTP), output over voltage protection and VDD under voltage lockout (UVLO). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 22KHZ is minimized in the design and audio noise is eliminated during operation.

OB2276A is offered in SOP8 package.

FEATURES

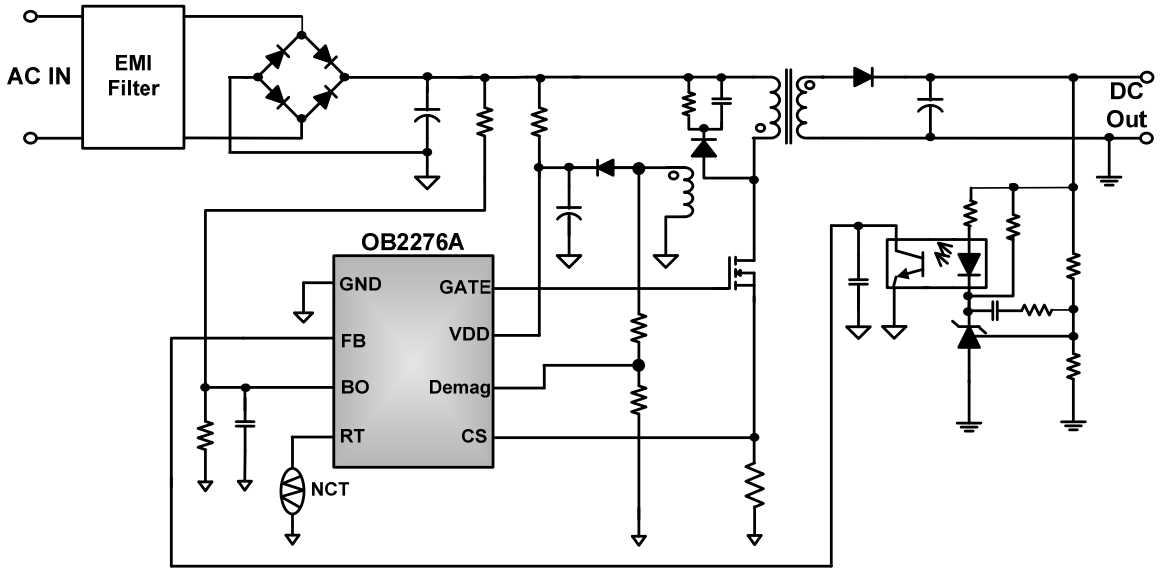
- Power on Soft Start Reducing MOSFET Vds Stress
- Frequency shuffling for EMI
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Fixed 65KHZ Switching Frequency
- Comprehensive Protection Coverage
  - o VDD Under Voltage Lockout with Hysteresis (UVLO)
  - o Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
  - o Overload Protection (OLP) with auto-recovery
  - o Brownout Protection with auto-recovery
  - o VDD OVP with auto-recovery
  - o Over Temperature Protection with auto-recovery
  - o Output Over Voltage Protection with auto-recovery

APPLICATIONS

Offline AC/DC flyback converter for

- Battery Charger
- Power Adapter
- Set-Top Box Power Supplies
- Open-frame SMPS

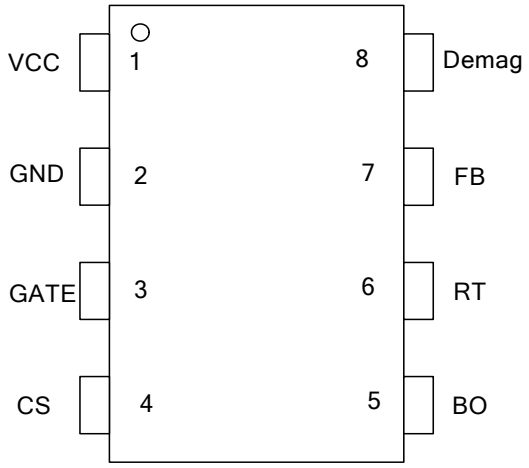
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2276A is offered in SOP8 package, shown as below.



Ordering Information

Part Number	Description
OB2276ACP	SOP8, Pb-free in Tube
OB2276ACPA	SOP8, Pb-free in T&R

Package Dissipation Rating

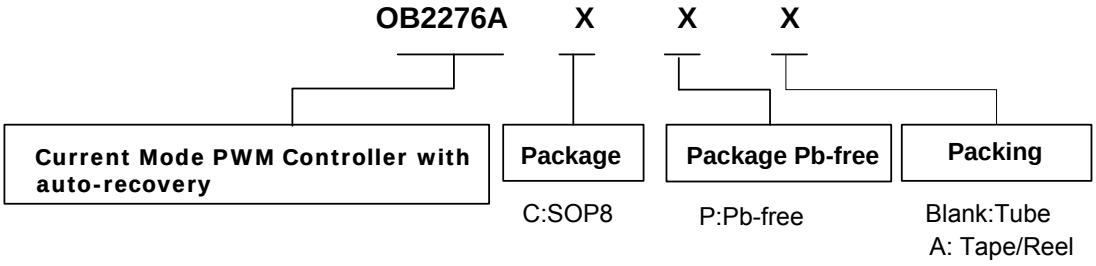
Package	RθJA(℃/W)
SOP8	150

Absolute Maximum Ratings

Parameter	Value
VDD DC Supply Voltage	VOVP-1V
VDD Zener Clamp Voltage[Note]	VDD_Clamp+0.1V
VDD DC Clamp Current	10 mA
FB Input Voltage	-0.3 to 7V
Sense Input Voltage	-0.3 to 7V
BO Input Voltage	-0.3 to 7V
RT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: VDD_Clamp has a nominal value of 34V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
C:SOP8 Package
P:Pb-free Package
A:Character Code
S:Internal Code(Optional)

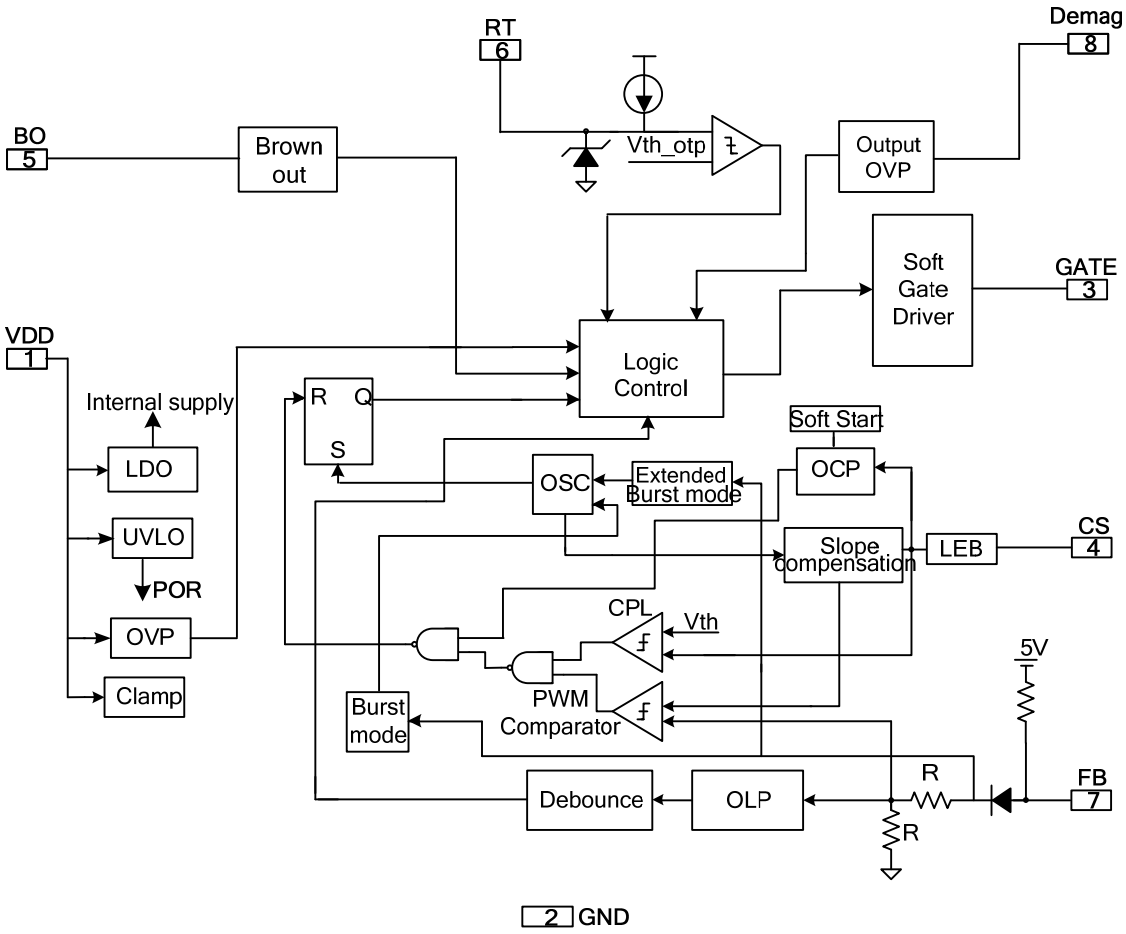
TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
VCC	P	Power Supply
GND	P	Ground
Gate	O	Totem-pole gate driver output for power Mosfet
CS	I	Current sense input
BO	I	Line voltage detection pin. Depends on voltage at this pin, Brownout is triggered or not.
RT	I	Connected through a NTC resistor to ground for over temperature control.
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
Demag	I	Output detection pin through winding of transformer for output over voltage protection

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min/Max	Unit
VDD	VDD Supply Voltage	12 to 27	V
T_A	Operating Ambient Temperature	-20 to 85	℃

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

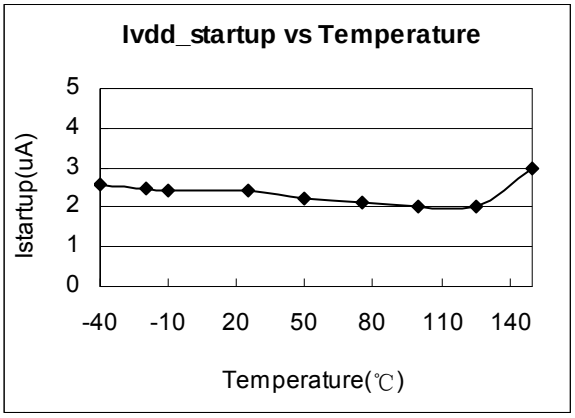
(T_A = 25℃, VDD=18V, unless otherwise noted)

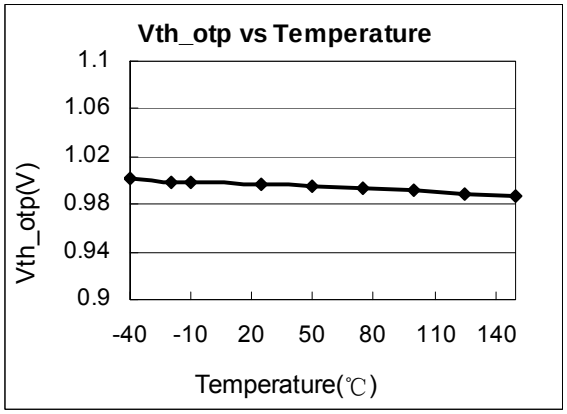
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
Istartup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		3	20	uA
I_VDD_Operation	Operation Current	VDD=18V,V_{FB}=3V, CS=0V,Cgate=1nF		1.8	2.5	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		8	9	10	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		19	20	21	V
Vpull-up	Pull-up PMOS active			13		V
OVP(ON)	Over Voltage Protection Voltage	CS=0V,FB=3V Ramp up VDD until gate clock is off	28.5	30	31.5	V
Vdd_clamp		Ivdd=10mA	32	34	36	V
Feedback Input Section(FB Pin)						
V_{FB} Open	V_{FB} Open Loop Voltage		3.9	4.2		V
Avcs	PWM input gain Δ VFB/ Δ VCS			2		V/V
Maximum duty cycle	Max duty cycle @ VDD=18V,VFB=3V,VCS=0V		75	80	85	%
Vref_green	The threshold enter green mode			1.65		V
Vref_burst_H	The threshold exit burst mode			1.25		V
Vref_burst_L	The threshold enter burst mode			1.15		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		0.2		mA
V_{TH}_PL	Power Limiting FB Threshold Voltage			3.7		V
T_D_PL	Power limiting Debounce Time		80	88	96	ms
Z_{FB}_IN	Input Impedance			16		kΩ
Current Sense Input(CS Pin)						
SST	Soft start time			4		ms
T_blanking	Leading edge blanking time			220		ns
Z_{SENSE}_IN	Input Impedance			40		kΩ
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the Gate driver output starts to turn off		100		ns
V_{TH}_OC	Internal Current Limiting Threshold Voltage with zero duty cycle		0.65	0.7	0.75	V
Vocp_clamping	CS voltage clamper			0.9		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency	VDD=18V, FB=3V, CS=0V	62	65	68	kHz
△f_OSC	Frequency jittering			+/-4		%
F_shuffling	Shuffling frequency			50		Hz
△f_Temp	Frequency Temperature Stability			1		%

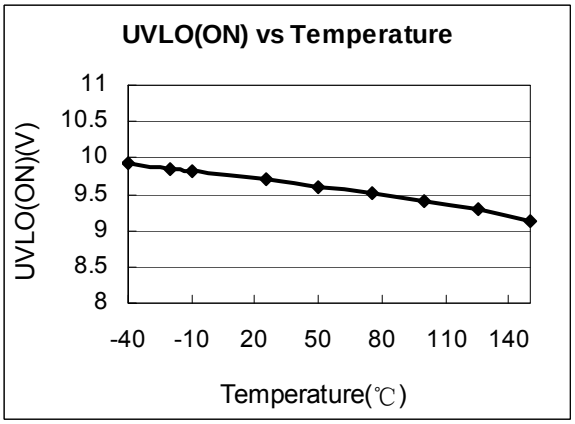
△f_VDD	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			22		KHZ
Brownout						
VBO_Enter	Enter Brownout		0.75	0.8	0.85	V
VBO_Exit	Exit Brownout		1	1.05	1.1	V
OTP						
IRT	Output current of RT pin		95	100	105	uA
VOTP	Threshold voltage for OTP		0.95	1	1.05	V
Td_OTP	OTP debounce time		5	6	7	Cycle
VRT_FL	Float voltage at RT pin			2.5		V
Output OVP						
Vth_Output_OVP	Output OVP threshold voltage		3.6	3.75	3.9	V
Td_Output_OVP	Output OVP debounce time		5	6	7	Cycle
Gate driver						
VOL	Output low level @ VDD=18V, Io=5mA				1	V
VOH	Output high level @ VDD=18V, Io=20mA		6			V
V_clamping	Output clamp voltage			12		V
T_r	Output rising time 1V ~ 12V @ CL=1000pF			175		nS
T_f	Output falling time 12V ~ 1V @ CL=1000pF			85		nS

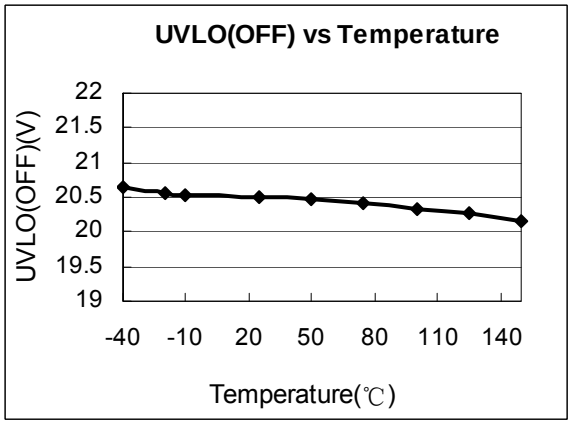
CHARACTERIZATION PLOTS

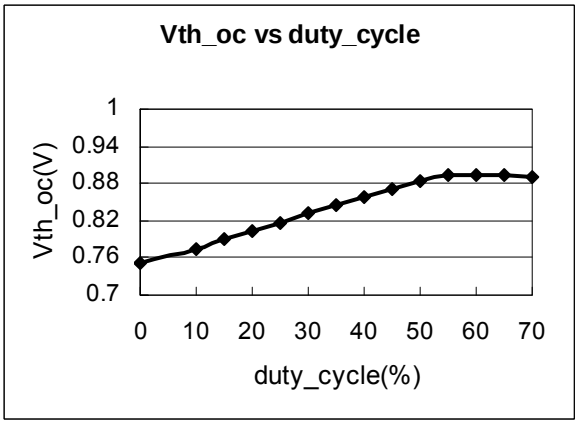
VDD = 18V, TA = 25℃ condition applies if not otherwise noted.

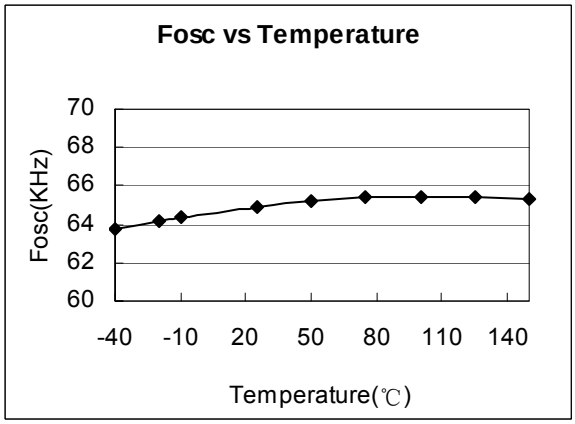












FUNCTION DESCRIPTION

OB2276A is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of OB2276A is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

- **Operating Current**

The Operating current of OB2276A is low at 1.8mA(typical). Good efficiency is achieved with OB2276A low operating current together with the 'Extended burst mode' control features.

- **Soft Start**

OB2276A features an internal 4ms(typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

- **Frequency shuffling for EMI improvement**

The frequency Shuffling (switching frequency modulation) is implemented in OB2276A. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

- **Extended Burst Mode Operation**

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.
The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.
The switching frequency control also eliminates the audio noise at any loading conditions.

- **Oscillator Operation**

The switching frequency is internally fixed at 65kHz(typical). No external frequency setting components are required for PCB design simplification.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2276A current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Driver**

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak gate driver strength results in higher conduction and switching loss of MOSFET while too strong gate drive strength results the compromise of EMI.
A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

- **Output Over Voltage Protection**

Refer to Fig.1. In phase of demagnetization of transformer, the output voltage can reflect at Aux winding via coupling.

$$V_{Aux} = (V_{OUT} + V_{D1}) \frac{N_{Aux}}{N_{Sec}}$$

This information can be detected by the resistor divider R3 and R4 at Demag pin and is sampled by chip to implement Output over voltage protection.

$$V_{Demag} = (V_{OUT} + V_{D1}) \frac{N_{Aux}}{N_{Sec}} \frac{R4}{R3+R4}$$

If V_{OUT} ramp high, V_{Demag} will ramp high too. When V_{OUT} ramp to predetermined voltage threshold of output OVP, $V_{Deamg} > Vth\_ref$ happen and system enter auto-recovery shut down mode after 6 cycle debounce time to avoid mis-trigger.

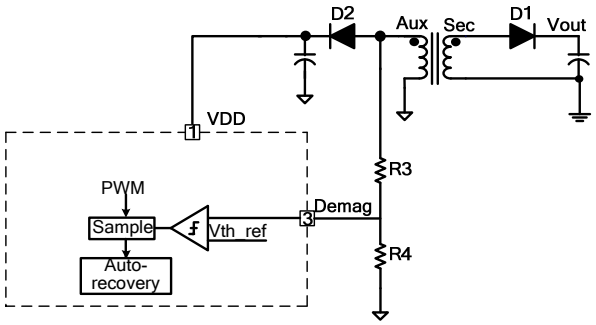


Fig.1 Output OVP implementation scheme

- **Brownout**

To protect the SMPS under low line voltage condition, Brownout protection is implemented in OB2276A. Refer to Fig.2.The line voltage is monitored with resistor ratio from buck capacitor to ground and is averaged by the RC filter (R2 and C1) at BO pin. This protection is active or not depends on voltage level on BO pin.

$$V_{BUCK\_BOP\_Enter} = \frac{0.8V * (R1+R2)}{R2}$$

When the BO voltage level falls blow 0.8V (typical)， the brownout protection is triggered and controller stops pulsing until this voltage goes back to 1.05V(typical).

$$V_{BUCK\_BOP\_Exit} = \frac{1.05V * (R1+R2)}{R2}$$

By adjusting the resistor ratio, the window between brownout enter voltage and exit voltage can be programmed.

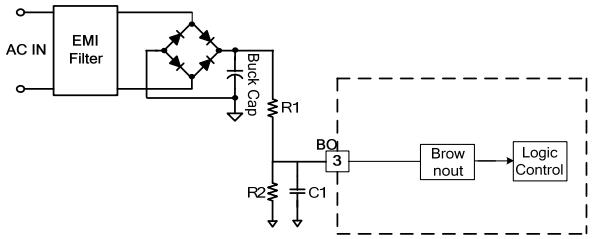


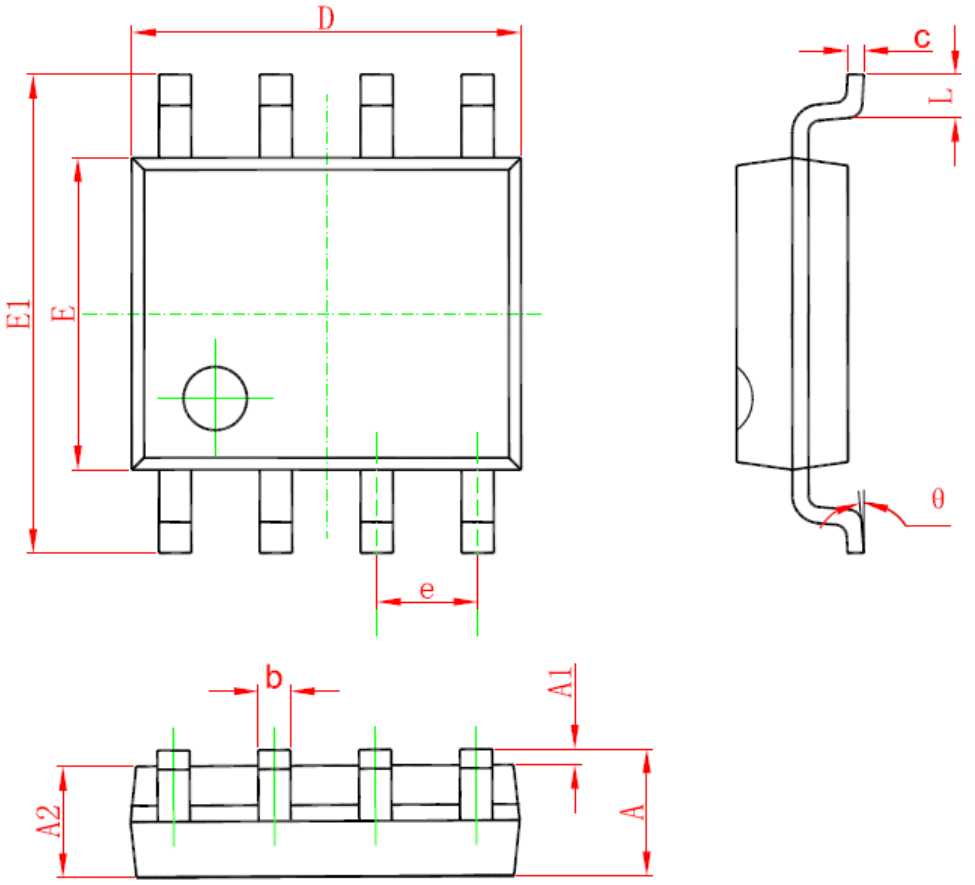
Fig.2 Diagram of BOP

- **Protection Controls**

Besides Brownout Protection and Output OVP, OB2276A also provides other protection features with auto-recovery including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) with auto-recovery, Under Voltage Lockout on VDD (UVLO), VDD over voltage protection (OVP), over temperature protection (OTP). With On-Bright Proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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